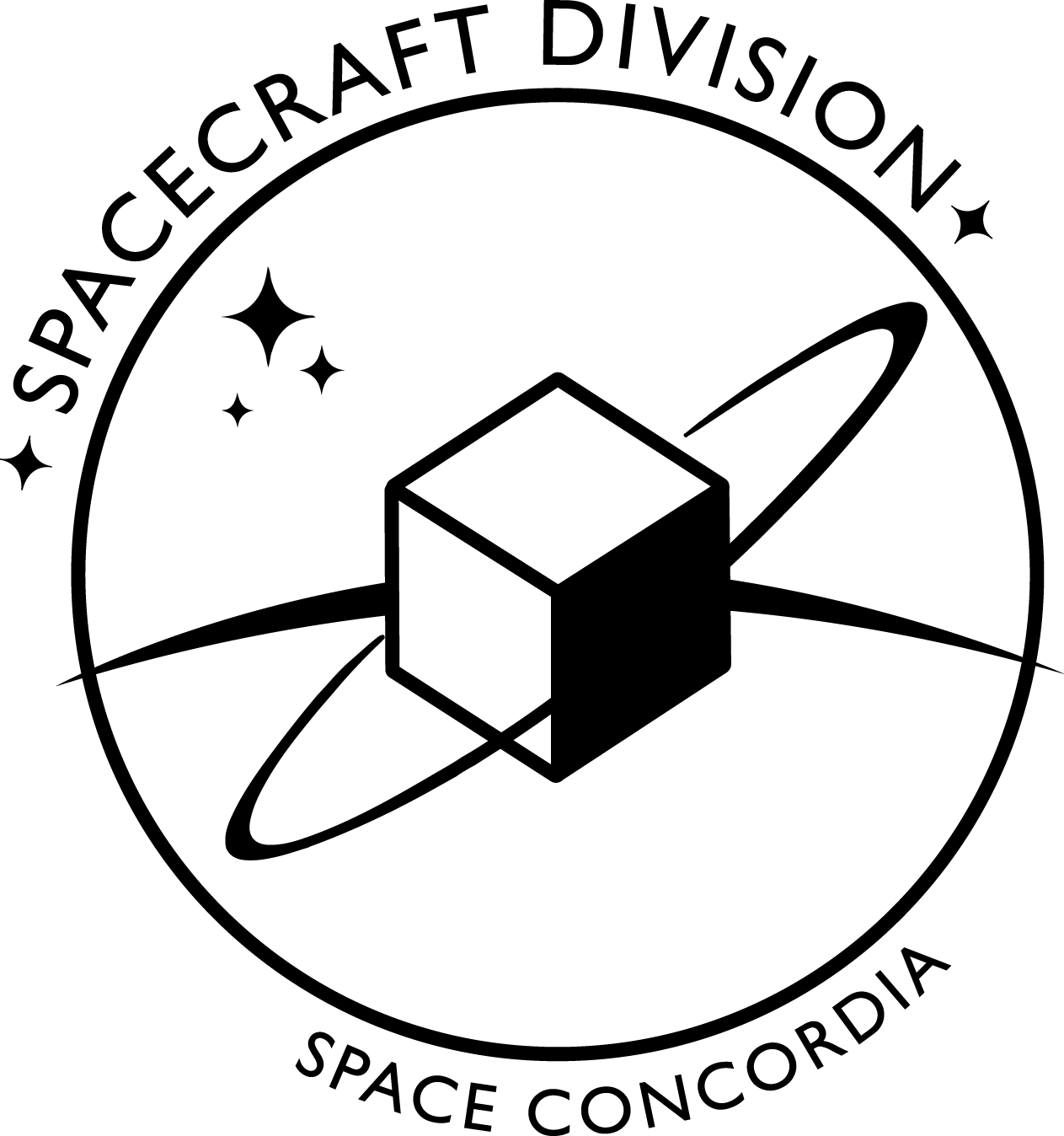
SCSD-LP-EPS-001-A

Power



Prepared by

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Project Manager

Jan 24, 2023

# **Revision History**

| **Date** | **Revision** | **Changes** |
| --- | --- | --- |
| 06-May-2023 | A | Initial Release |

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**Abbreviations and Definitions**

| **Terminology** | **Definition** |
| --- | --- |
| ADC | Analog to Digital Converter |
| ADCS | Attitude Determination and Control System |
| CAN | Controller Area Network |
| CDH | Command and Data Handling |
| CM | Common Mode |
| CSA | Canadian Space Agency |
| DM | Differential Mode |
| DNP | Do Not Place |
| ESD | Electrostatic Discharge |
| GPIO | General Purpose Input/Output |
| LED | Light Emitting Diode |
| LVDS | Low-Voltage Differential Signaling |
| MCU | Micro Controller Unit |
| PDS | Power Distribution System |
| RTC | Real Time Clock |
| SC-FREYR | Fermentation R- Extraterrestrial Yeast R- |
| SPEAR-M7 | Flight computer of SC-ODIN |
| SPI | Serial Peripheral Interface |
| TVS | Transient voltage suppressor |
| UART | Universal Asynchronous Receiver-Transmitter |
| UART | Universal Synchronous and Asynchronous Receiver-Transmitter |
| USB | Universal Serial Bus |

# **Introduction**

Power terminology, component selection, routing and layout are key to functional design. It is the first part of any electronics design and needs to be carefully done to ensure maximum efficiency, performance and low noise power delivery. This document also introduces crucial principles such as decoupling, copper planes, layer stackup, grounding methodologies and includes a few important guides in the Appendixes.

# **Power**

## Power Inputs

## 

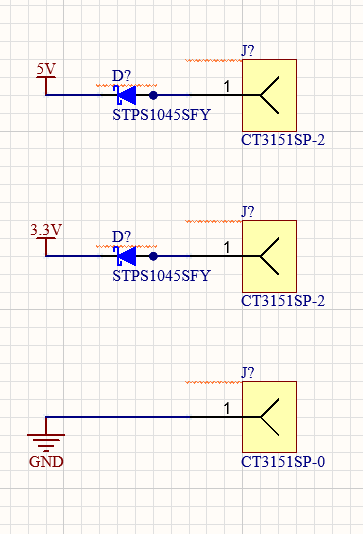
Power inputs refer to power sources in electronics design. These are typically batteries, solar panels or simply external voltage sources. The way these inputs are dealt with is the first step to any electronics design and if done improperly, could severely damage the rest of the design. This section will mainly look at solar panels and external voltage sources since batteries are much more complicated and fall under strict regulations for ISS launches. For in depth information on handling batteries, read the learning package on battery protection circuitry (reference [7]).

To start with the basics, external voltage sources are some of the easiest power sources to implement to a design. A wide variety of voltage sources can be used: bench power supplies, wall DC adapters or even wall socket connectors. For the purpose of spacecraft electronics, mainly the bench power supply and wall adapter DC supplies are used given the simplicity and relatively lower risk involved with them.

Bench Power Supply

These supplies are some of the most used lab equipment, coming in at a close second to the multimeter. They are relatively simple and safe to use, but they can do a lot of damage to circuit boards if handled improperly. Most university classes use modified power supplies that are already set to fit specific experiments and for this reason, Appendix A explains in detail how to set a bench power supply.

In terms of schematic implementation, all that is required is the proper connector. The chosen part will highly depend on the specific bench power supply available, but in general, banana jacks are the easiest and most commonly used for power supplies. On Space Concordia’s library (as of 26/04/2023), they can be found under the names “CT3151SP-0”, “CT3151SP-2” and “CT3151SP-5” with “-0” is a red banana jack header, “-2”is a black header and “-5” is a generalized footprint. It only has one connection since banana jacks are basically a single metal contact. The connector pins can then be connected to a ground, a power object or a specific net. In most cases, please use a power object when using the connectors as power sources. Power objects refer to the red symbols like the ground symbol, bar style symbol, etc (can be placed from Place > Power Port). Figure 1 shows three connectors used to provide 5V and 3.3V to a board. Note the presence of Schottky diodes: they are in place because the board being powered on also has another 3.3 and 5 volt source, which could back power the supply and damage the internals. If the design being implemented solely relies on the banana jacks to provide power, the diodes are not needed.



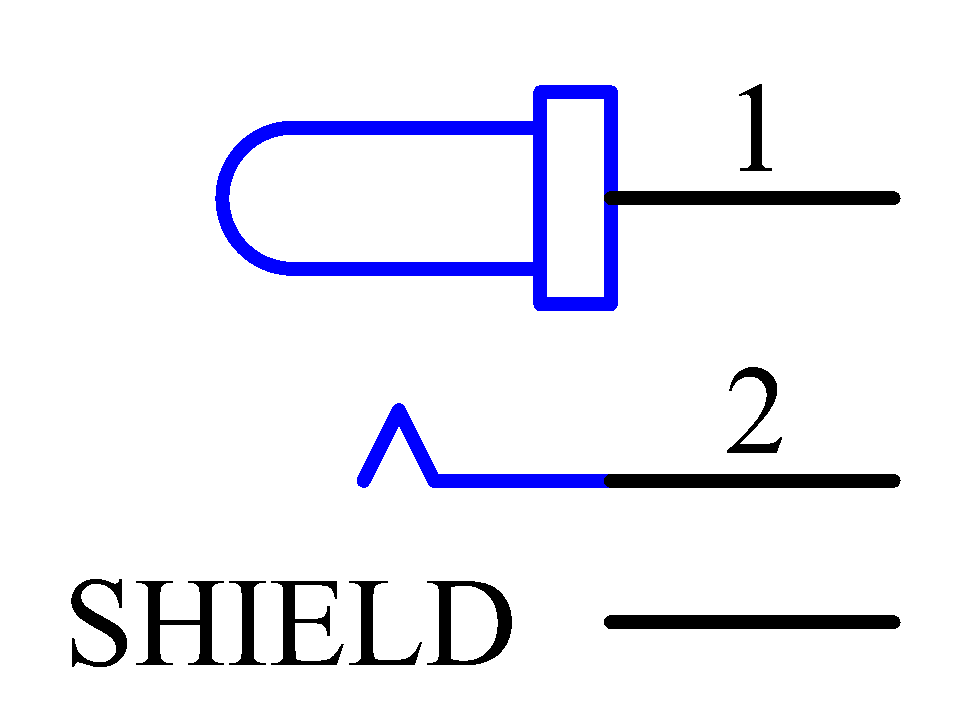
**Figure 1: Schematic Diagram of Banana Jacks**

DC Wall Adapter

This type of power input is not very common in Spacecraft Division’s electronics because bench power supplies are easily accessible at the lab and offer more versatility when testing the electronic systems. With that being said, specific design might make use of a simple DC wall adapter input as its power source when dealing with designs that are meant to move around, like ground support equipment. Through the course of SC-ODIN, only one design made use of a DC wall adapter jack: the umbilical board. This board is meant to be the interface between any computer and the satellite when fully assembled. It is meant to be brought to CSA, MDA and other test facilities towards the end of the project and because of that, it needs to be able to be powered practically anywhere. DC wall adapters are great for that since every test facility will have at least a wall outlet, while some might not have a bench power supply.

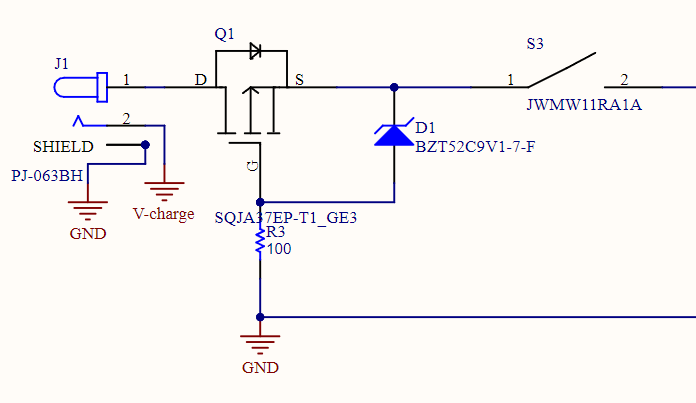
Jacks come in a wide variety of connector types but the most commonly used are barrel connectors. They are very easy to use and compatible with virtually any DC wall adapter with the same mating diameter. In terms of schematic implementation, just like the banana jack, it is fairly straightforward. The main thing that will change is the voltage provided to the connector, which is determined by the specific wall adapter chosen. Make sure to design around the typical voltage inputs of DC wall adapters, usually 5, 12 or 24V. This means making sure the components directly connected to the power net, typically power converters, are able to take a wide range of voltages as input.

The schematic diagram of a typical DC power jack can be seen in figure 2. It is important to note that there are three terminals to this connector: terminal one is the positive voltage input terminal and will be connected to 5, 12 or 24V. Terminal 2 is the ground terminal and the SHIELD pin is to be connected to CHASSIS in most cases (read the section on CHASSIS grounding to understand why).



**Figure 2: DC Power Jack Symbol**

The last thing to keep in mind when designing around a DC power jack is reverse polarity protection. Although barrel connectors are difficult to connect “the opposite way”, some manufacturers might use a different standard then most and could potentially damage your electronics. To make the design “dummy proof”, a simple reverse polarity protection circuit is added after a barrel connector. A designer’s first instinct might be to simply put a schottky diode in line with the barrel jack connector, which would effectively prevent the circuit from being reverse powered. Unfortunately, this method is generally inefficient since the diode will drop some voltage and dissipate power. This can be avoided by implementing the protection circuit shown in figure 3.



**Figure 3: Common Reverse Protection Circuit**

Instead of using a schottky diode to prevent reverse polarity, a PMOS is used in a configuration that dissipates negligible power during normal operation but prevents reverse polarity completely in case of a manufacturer or user error. A video containing more visual information as well as an article regarding this protection can be found in references [8] and [9], but in a nutshell, the PMOS will be biased through the zener diode during normal operation but will block reverse polarity since the threshold voltage will not be met. The resistor is simply to limit the current during normal operation and the switch is a design specific element that can be ignored.

## Power Converters

Power converters are some of the most basic building blocks of every circuit. Without proper converter design, a design cannot be trusted to work properly. Improper converter design can damage devices, not supply enough power and/or introduce significant amounts of noise in the system. This section will look at very basic power converters and how to implement them, and will glance over more complicated designs.

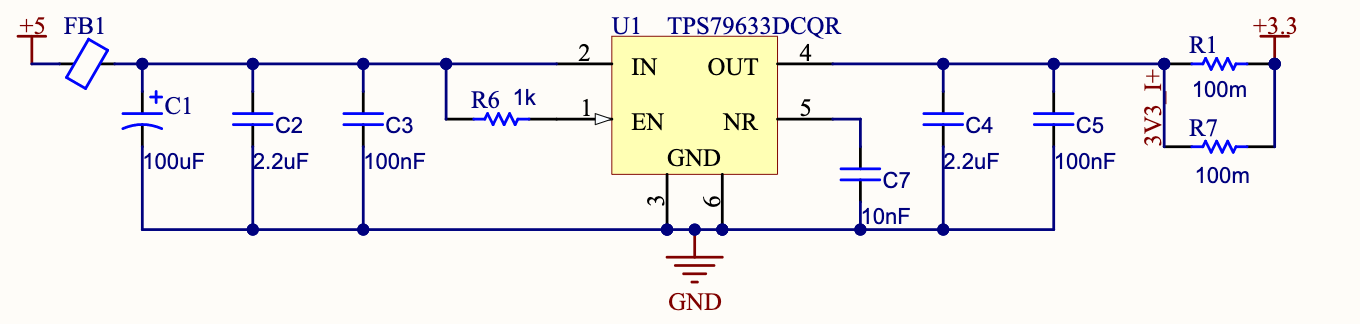
Types of converters

The main use for them is to step down or step up a general input voltage to a voltage required by other components in the design. There are two main types of voltage converters: linear converters and switching converters, also commonly referred as buck converters. Linear converters are fairly simple in the way they work: they take a certain voltage range as input and output a constant voltage with a limited current output. The extra power is all dissipated as heat. This is one of the main disadvantages of linear converters: they are not very efficient and generate a lot of heat, which is not great for space design. They are also only available as step-down DC/DC conversion, which means they cannot increase the voltage of the line, only reduce it. On the other hand, they are really easy to implement and produce a very low amount of noise given the simple transfer operation. Switching converters are much more complicated and utilize inductors and capacitors being switched on and off constantly to produce the required voltage. The advantage of this switching is that virtually no power is wasted and dissipated. Buck converters can reach 90% efficiency, which is a really good property for space applications. The downside of this type of converter is that they are more complex, expensive and induce a lot more noise because of the switching. More in depth information about how DC/DC converters actually work can be found in reference [1].

The typical design procedure for these converters is to select the IC based on the required characteristics of the system, look at the datasheet and extract the relevant information for the specific implementation. Some main characteristics that should be taken into account are voltage input/output conversion, ripple voltage, current limit, quiescent current and power dissipation of the converter. Examples of both a linear and a switching converter will be shown in this section, as well as the reason behind the IC selection and the design implementation.

Linear converter exemple

A great example of a linear converter is the TPS79633DCQR. It is a 3.3V fixed output with a current limit of 1A and it can take a voltage input between 0 and 6V. This is a particularly relevant converter for building dev boards that use USB as a power input and require 3.3V for most devices. The data sheet for this particular IC can be found in reference[. The reason behind the choice of this particular IC is its simple implementation, ultralow-noise output and low dropout voltage. Its stability makes it a perfect choice for MCU design. Figure 4 shows an implementation of this IC for an MCU breakout board.



**Figure 4: Implementation of the TPS79633DCQR**

Most linear converters will have similar configurations: an IN and OUT pin for voltage input and output, an enable line, ground connections, some will have a bypass capacitor line (NR in this case) and some will have a SET pin, which requires extra circuitry to select the output voltage (often times a simple resistor circuit). In the case of the TPS79633DCQR, the output voltage is set by the numbers after the TPS796 part number, so a TPS79630 has a 3V output, and so on for different part numbers.

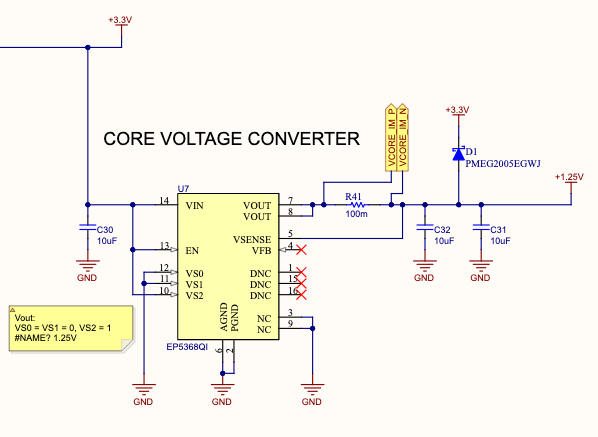
A few things to notice on figure 4 which are critical to most designs: a lot of decoupling capacitors are added on both sides of the converter. The datasheet only specifies one capacitor per pin, but adding 100nF capacitors on both sides is always good practice. It is also recommended to add a bulk capacitor, in this case the 100uF, at the input of the converter. This ensures that the line will stay stable, and that most of the AC noise introduced to the line will be shunted out. As a reminder of the basic principles, decoupling capacitors have two main benefits: in an AC, a capacitor is equivalent to a short circuit, which means most of the AC noise will go directly through the capacitor to ground. Smaller capacitors deal with higher frequency noise and vice-versa for bigger capacitors. The second benefit is that because of their slow charge and discharge rates, they prevent big voltage spikes and drops to affect the line significantly.

The ferrite bead FB1 provides additional filtering which is not required, but good practice to implement. Lastly, unlike specified by the datasheet, a 1K ohm resistor is added in front of the enable pin to ensure that the pin will not be destroyed in case of a high transient. The 100m ohm resistors are only for current sensing purposes, and can be ignored unless current sensing is required by the design.

One last parameter to be considered when designing around linear converters is the drop-out voltage. It is a particularly important parameter to consider during part selection when designing for low voltage drop conversion. Drop-out voltage is the minimum voltage drop that the converter is capable of producing between its input and output. To illustrate this, let's use an example: a chip in a design requires a 3V power source, but the only other voltage level available from the system is a 3.3V power line. To step the voltage down, the use of a linear converter is a convenient choice considering it won’t need to reduce the voltage by much and thus, dissipating only a low amount of power. The only issue is that the chosen converter needs to have a dropout voltage of at most 300 mV (3.3V - 3V), which is difficult to find in regular converters. Fortunately, there exists a specific type of converter that is made to have a low drop-out voltage: LDOs (low drop-out).

Switching converter example

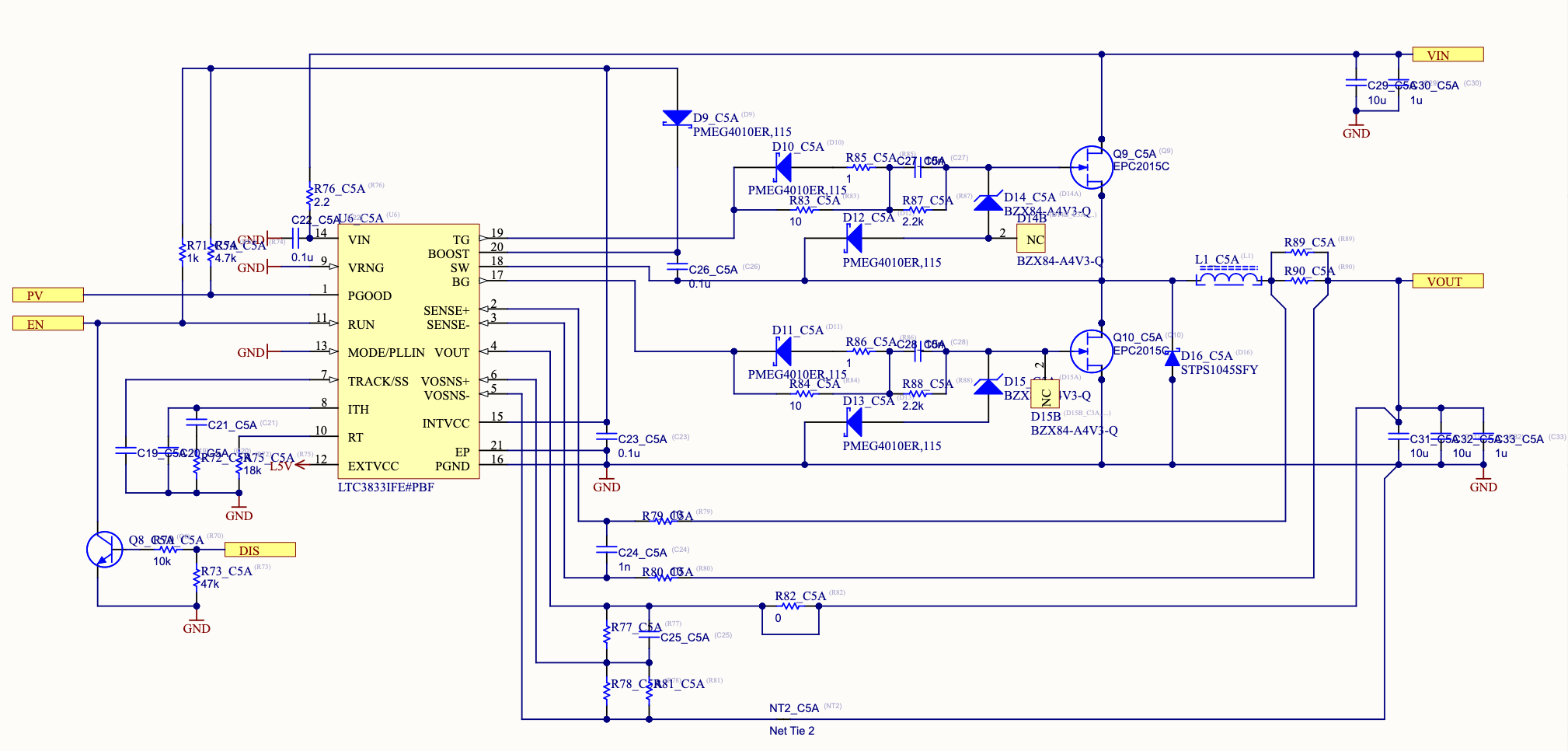
The first example that will be looked at is a fully integrated and simple switching converter, the EP5368QI. It features a fully integrated inductor, selectable voltage output, low ripple voltage and up to 94% efficiency (80% for 3.3 to 1.25 conversion), which is impossible to match in a linear converter. It also integrates its own PWM driver and MOSFET switching circuit, meaning the only thing to add to the chip are external decoupling capacitors. All of its features packed in an easy to implement chip makes it a perfect choice for MCU power supplies, as discussed in reference [3]. Figure 5 shows its full implementation of the SPEAR-M7.



**Figure 5: Implementation of the EP5368QI**

As seen in previous designs, the 100m resistor is implemented for current sensing purposes. C30, C31 and C32 are the decoupling capacitors and D1 is a schottky diode which will protect the 1.25V line from inductive voltage spikes. The VSENSE pin is used by the converter to continuously sense the voltage output and adjust it to match the desired voltage and precision. Lastly, VS0, VS1 and VS2 are used to program the voltage output of the converter.

The second example that will be looked at is very complex, and this document will not go in depth on it. For more detail on the specific implementation of this chip, reach out to [Joshua Zhang](mailto:joshua.zhang@spaceconcordia.ca) as he is the designer of the converter. The chip in question is the LTC3833, which is a high accuracy, fast transient response, adjustable switching converter with integrated protections. Figure 6 shows the implementation of the LTC3833 on SC-ODIN’s PDS.



**Figure 6: LTC3833 implementation on the SC-ODIN PDS**

Unlike the EP5368QI, it does not have an integrated inductor nor does it have the integrated MOSFET switches. These need to be selected and implemented externally. With that said, the converter generates its own switching signal and the frequency of this switching can be manually adjusted through the RT pin. The value of VOUT is selected from a resistor network connected to VOSNS+ and VOSNS- (different resistance values will yield different output voltages). TG and BG stand for Top Gate and Bottom Gate, and they drive the gates of the two MOSFETS. SENSE+ and SENSE- are current sensing pins that can detect overcurrent events and shutdown the converter if necessary. Since this converter is implemented in a design that will be in a space environment, it is highly recommended to connect EXTVCC to a 5V linear converter. This disables the LTC3833’s internal LDO and prevents the device from dissipating too much heat. RUN is the enable of the chip, and the designer opted to add an additional DIS (disable) signal for redundancy purposes. Lastly, VOUT is the converter output.

It is important to understand that the only way to design complicated converters like this one is to carefully read the chip’s datasheet, understand the functionality of each individual pin and follow application examples provided by the datasheet. It would be highly recommended for any reader of this document to go to this [datasheet](https://www.analog.com/media/en/technical-documentation/data-sheets/3833f.pdf) and try to understand the designers choice for components and values. Additionally, recommendations for the layout are also often included in the datasheet to ensure proper operation of the chip.

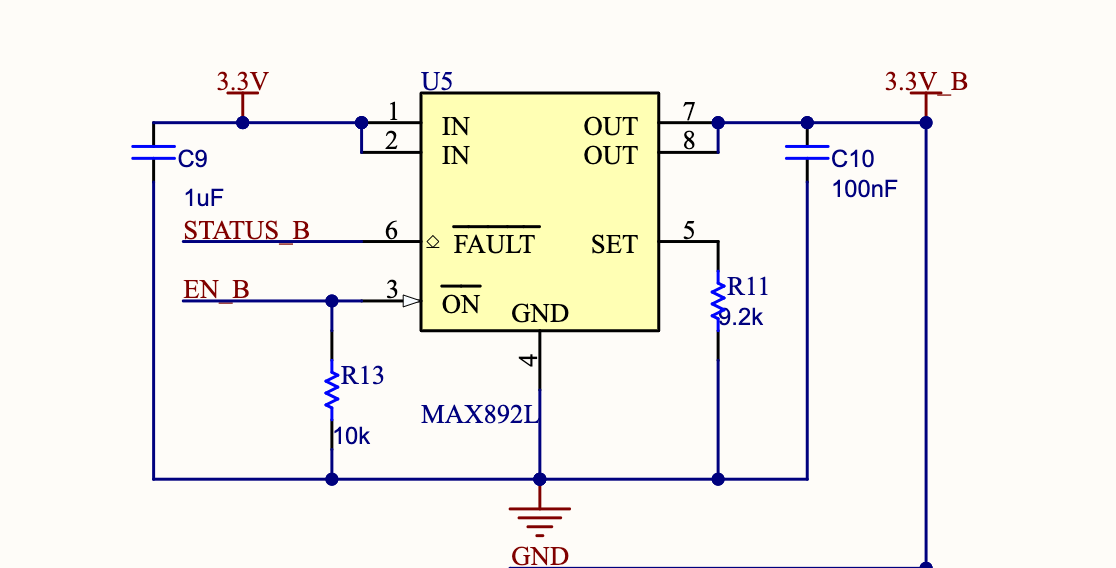
Design note: although GAN FETS (EPC2015C) have great properties that pair well with the LTC3833, Space Concordia’s soldering capability is too limited for this kind of component, and cause more damage to the board than benefit from its properties. Different power mosfets should be selected for future design.

## Power Switches

Power switches are an essential component in space design since they offer redundant protections like overcurrent protection, precise current limiting and allow parts of the system to be completely disabled when they are not required for a specific mode of operation. This allows for better control over power consumption of the system and even monitoring of the functionality of each part of the system given that the chosen component has that feature. They can either be put at the input of an entire board, or in front of a particular block of components. There are two main types of power switches: fully integrated or power MOSFETS. The fully integrated power switches refer to ICs which fully integrate the switching and protection of a line. They are simple to implement and offer a lot of useful features. With that said, they are not recommended for high current designs since they tend to have high on resistance and can dissipate a lot of unwanted heat. They also tend to be limited to lower currents than required by some designs. The power MOSFET switches are less commonly used in Spacecraft’s design but required for high power applications. They are more versatile and adjustable than fully integrated solutions, but are also more complex to implement since all the biasing and power calculations need to be done by the designer. This section will show an example of both options.

Fully integrated power switches

A commonly used power switch in SC-ODIN and by other space agencies is the MAX891 and MAX892. They are P-channel switches with current limit, overcurrent protection and thermal shutdown. The polarity of the channel makes it a highside switch, which is very easy to implement. The 891 and 892 variants offer 500 mA and 250 mA upper current limit respectively. This limit can be programmed lower to fit the design requirements. Figure 7 shows an implementation of the MAX892 used to switch on or off one of the redundant SPEAR-M7s on the CDH board of SC-ODIN.



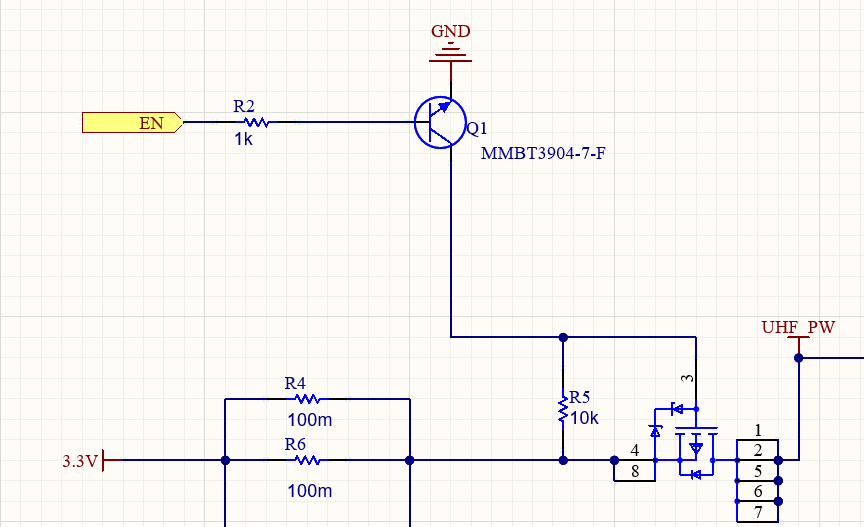
**Figure 7: MAX892L implementation on the CDH board**

The implementation of integrated power switches is generally very simple as can be seen in figure 7. A voltage is fed to the IN pins, and the same voltage will be outputted on the two OUT pins. It is important to name the output voltage of the converter with a different net name to differentiate which line is limited. The SET pin is connected to a resistor to ground, and the value of this resistor will dictate the current limit of the output. The datasheet will provide the equation to set the current limit. The ON function is the active low enable pin, and if an external source drives it high, the switch will turn off the output voltage of the device. In this particular implementation, the ON pin is connected to the main flight computer, which enables it to shutdown or power cycle the redundant flight computer if necessary. The FAULT pin is also connected to the main computer, since this open drain pin will be driven to ground if the current limit is reached or if the thermal shutdown is triggered. This basically acts as a status flag and will let the main computer know if the redundant computer’s power source encounters any fault. It is important to remember that since the FAULT pin is an open drain by default, a pullup resistor is required to keep the line high until the switch drives it low.

Power MOSFET switches

This section will look at two different uses of power MOSFET switches and will explain some of the criterias for part selection as well as the design choices behind their implementation. Both designs were used in SC-ODIN for high power purposes: battery isolation and high current switching.

First, this section will look at the high current switching application. It was used on the UHF transceiver daughter board to turn on and off all devices on the board, including the transceiver. At maximum power, the transceiver draws 1.2 A at 3.3 volts, which means most integrated switches will not fit this application as they would dissipate too much heat. The proper way to implement a switch is to use a single power MOSFET and add a control element at the gate such that the biasing of the MOSFET can be controlled by an MCU I/O. There are multiple ways to implement this, but one of the easiest ways can be seen in figure 8.



**Figure 8: Power MOSFET switch for the UHF transceiver**

Before going in depth with the specific power MOSFET choice, it is important to understand the basic implementation of this switch. The goal of this switch is to enable or disable the power input of the transceiver, so it needs to be a highside switch as opposed to a low side switch which connects or disconnects the ground. In electronics, PMOS are always used for high side switching while NMOS are used for low side switching (see reference [4] for explanation). To bias this PMOS, a resistor needs to be added in between the drain and gate of the transistor. This makes it so it does not conduct without other biasing circuitry. To add the controlling element, another transistor will be used. Using a BJT NPN transistor, connecting the collector to the gate of the PMOS and the emitter to ground transforms the base of the NPN into a simple logic controller. Applying a high on the base Q1 will turn it on, grounding the gate of the PMOS and creating the required Vgs threshold voltage. On the contrary, grounding the base of Q1 will prevent it from conducting, keeping Vgs below the threshold voltage. The last element to add is a 10K resistor in line with the base of Q1 to ensure no damage is done when connecting an MCU pin directly to it. Much like the integrated switch implementation, it is crucial to name the net of the output of the switch, in this case the PMOS’s source, something different than the overall board's power.

The most critical part of a power MOSFET switch design is the component choice for the MOSFET. When designing for high power applications, especially in space applications, dissipated power is of the utmost importance. Unfortunately, ideal transistors are only in textbooks. They will never have zero resistance across the drain and the source, which means that they will dissipate heat based on the ON resistance of the transistor, called . For this application, the lower the on resistance is, the less power will be dissipated following this simple power equation:

There is another factor to consider when choosing the power MOSFET for our switching circuit: thermal resistances from the junction. This parameter, named , quantifies how much temperature change occurs per watt dissipated. Once again, the lowest possible value is best. With these two parameters in mind, the calculations to perform to qualify a transistor for the design go as follow:

Important to note that for space applications, the ambient temperature used is 60C. This means that for a system design to withstand 125C, the maximum allowable temperature rise is 65C. Ideally, the chosen power MOSFET would stay far below this temperature at maximum usage. Here is an example of the calculation used to choose the UHF transceiver’s switching MOSFET seen in figure 5 (values taken from the [datasheet](https://www.mouser.ca/datasheet/2/916/BUK4D38-20P-1880069.pdf) of the MOSFET).

A temperature of 64.15 Celsius is well below the upper limit and therefore qualifies for use. All the maximum provided values were used to ensure a worst case scenario analysis.

## 

## Power Planes

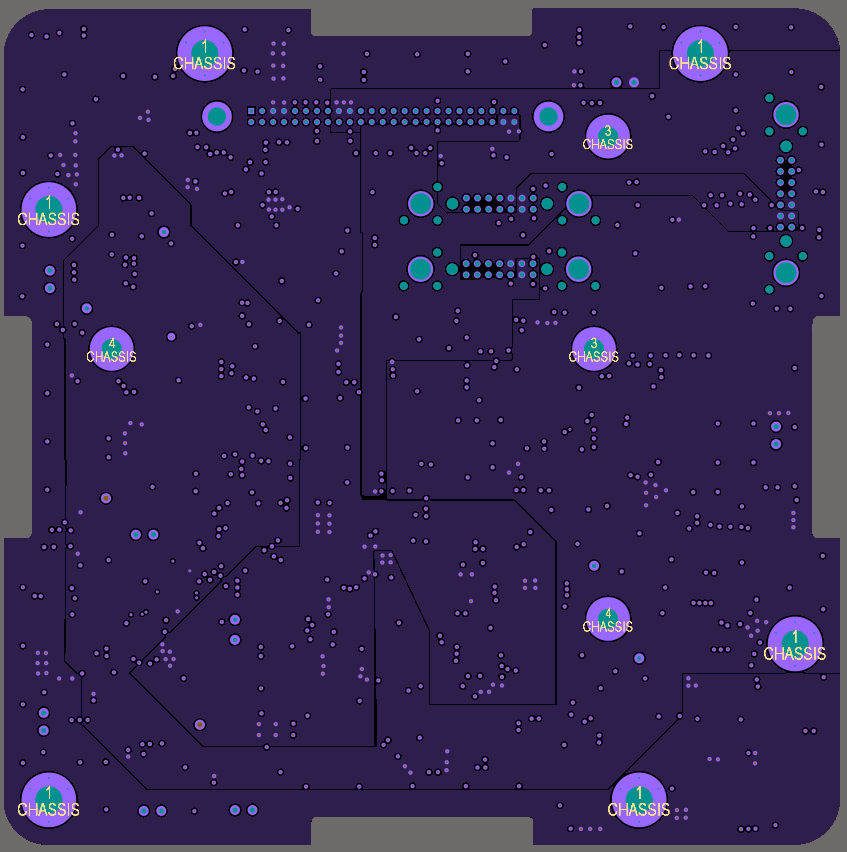
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Note: before adding power planes or ground planes to your PCB, make sure to read the next two sections as well as the Layer Stackup section.

Power planes are an essential part of PCB design. It is one of the main ways designers use to simplify routing and improve thermal properties of a PCB. It comes with a specific set of challenges and fair share of complexity, but most designs will require the use of power planes. This document will help decide whether or not they are necessary for a design, to what extent they should be used and will then go over the different rules and features surrounding power planes.

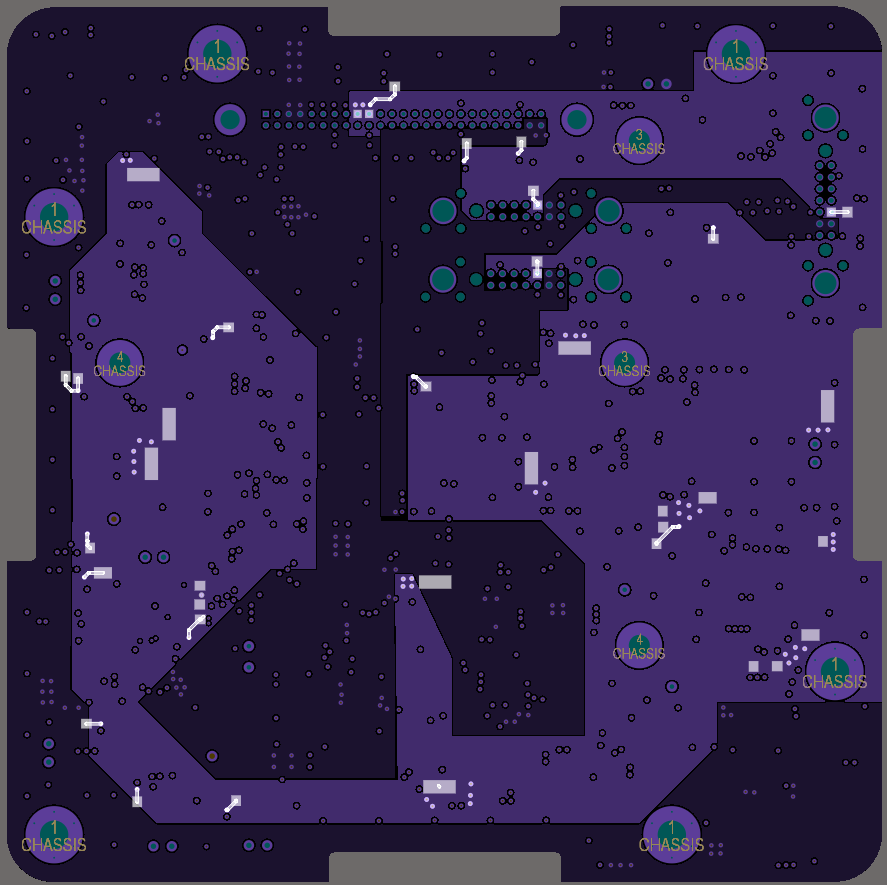
First, it’s important to understand what exactly power planes are. When designing PCBs that have more than 2 layers, it is very common to have specific layers reserved for power. Having a full layer only for power allows the designer to make big polygon pours (Appendix B explains how to create polygons), which help a lot with routing, improve current capacity between connections and improve overall thermal dissipation of the board. More surface area means less current density and lower temperature rise on specific spots. Figure 9 shows an example of power planes being used on the ADCS board of SC-ODIN.

v



**Figure 9: Internal Layer 4 of 6 on the ADCS Board**

The contrast is a bit difficult to see, but the entire layer is divided into specific polygons which all have a power net. One is dedicated to 3.3V, another one to 5V and the last one to VBATT. The main advantage of this is that every single component using these nets do not require long traces anymore, simply a small trace and a via that connects to the plane. To demonstrate this, figure 10 shows the same board with the 3.3V plane highlighted. The white boxes are components directly connected to the plane. The power plane connects them all in a much simpler way than trace can.



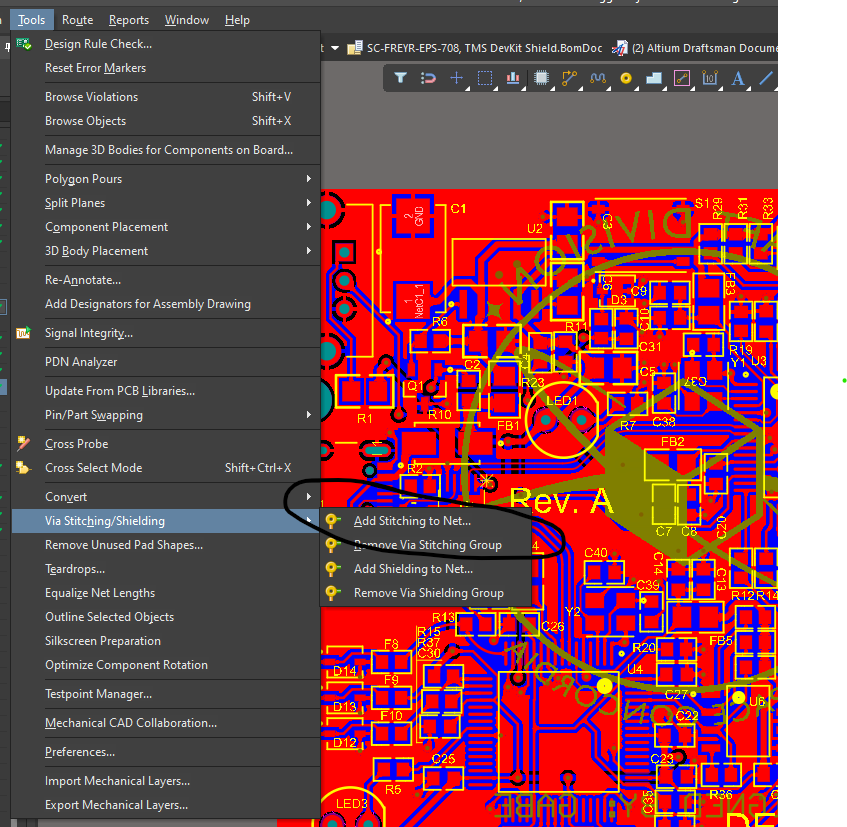
**Figure 10: Highlighted 3.3V Net on the ADCS Board**

The question then becomes: why not use them in every design? The main driving factors to this decision are complexity and cost. Every added layer to a PCB results in increased cost and manufacturing lead time, which obviously needs to be kept to a minimum. With that said, as a design’s complexity increases, the required layers will increase as it becomes impossible to route everything without a certain amount of layers. Finding the balance is always crucial and very difficult as a beginner designer, but eventually it will come naturally. Before committing to adding extra layers to a board, it is highly recommended to get a second opinion on it, ideally from your lead or someone more experienced.

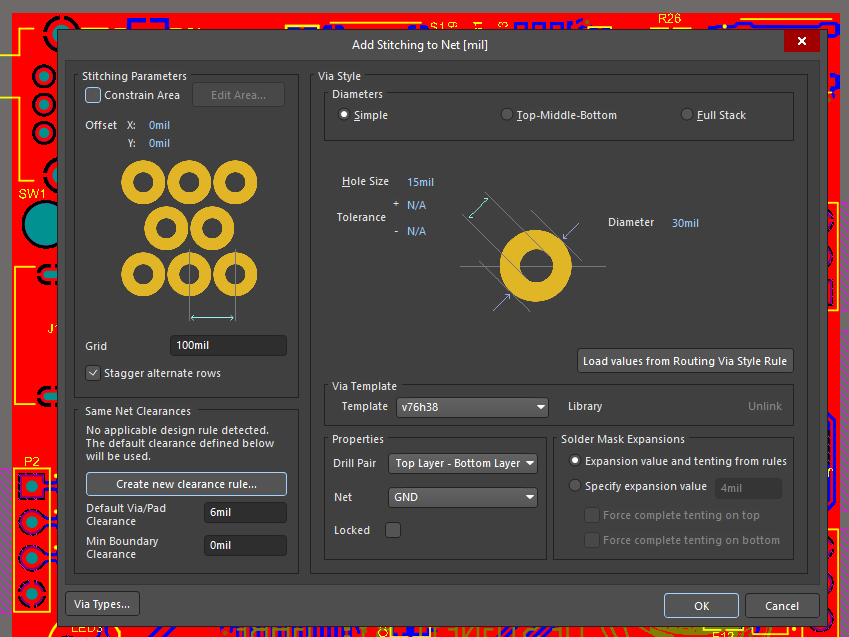
## Ground Planes

Ground planes are another very useful tool available for designers to help with routing, power distribution and improve the thermal properties of a PCB. Although very similar to power planes, these ground planes come with some added complexity and considerations. First, just like power planes, ground planes refer to entire layers of a board being dedicated to the ground net in a design. Compared to power planes, ground planes do not need to be split in different planes since they are only on ground (there are some exceptions to this but it is outside of the scope of this section). This means that they are extremely easy to implement: add a layer, make a polygon from the board outline on the new layer and assign it the GND net (again, refer to Appendix B on how to create the polygon). From this point, every ground pad in the design can be routed to a via, which will essentially connect all grounds together.

One particularity of ground planes is that they require stitching once a design is done. Stitching means exactly what it sounds like: connect all the ground planes together using a LOT of vias. Fortunately, this process does not have to be done manually; Altium has a feature to automatically do it. Figure 11 shows where the tool is located (Tools > Via Stitching/Shielding > Add Stitching to Net…). It is important to note that the ground polygon pours need to all be repoured before using this tool. It also needs to be cleared of any polygons on internal layers (meaning that it will not stitch if you have a power layer in between the ground polygons). If there are power layers in between, simply shelve them and repour once the stitching is done.



**Figure 11: Via Stitching tools**



**Figure 12: Via Stitching Menu**

This menu will then pop up. There are a lot of different settings in this menu, but most of the default stuff can be left as is. The main things to adjust are the grid, the net and the via size. The grid basically tells the tool how far you want your vias to be apart. Depending on the density of the board, this grid can be adjusted (high density = smaller grid, vice-versa). The via size should be the rule’s preferred via size and the net should obviously be GND. This tool can be tricky to use sometimes, and if ever the tool says it cannot stitch a net, there's a few things that can be done to debug this. First, try shelving and repouring all polygon pours. Second, reduce your grid as it might be an issue with the grid versus board density. Lastly, make sure you have multiple polygons to stitch and that they aren’t shelved.

Last thing that needs to be considered with ground planes is the use of ground polygons on the top and bottom layer. It is virtually required in every single design for a lot of reasons. First, it helps with routing density since most ground pads will be connected with this polygon. Second, it is required to properly impedance match differential traces (see reference [10], Appendix B). Third, it improves the board’s plane decoupling, as will be explained in the next section. Lastly, it helps balance the copper distribution on PCBs by virtually equalizing the presence of copper on all sides of a board.

## Layer Stackup

Layer stackup is not an aspect that is purely related to power, but it does have a significant impact on the design methodology and thus, it will be quickly looked over in this section. As mentioned in the previous, the principle of power plane decoupling will be explained.

When looking at the side section of a PCB, it can be seen that the board is sectioned in different layers of material. Three main types of material are always present: prepreg, core and copper or layer. Both the cores and prepreg layers are specific dielectric materials that are used to separate the different layers of a design. The copper planes are where signals, power or ground will be routed. Now for those of us who took ELEC 251 or equivalent classes, this combination of copper, dielectric and copper again sounds a lot like a component we commonly use in electronics design: a capacitor. Especially when looking at power and ground planes, having these layers of dielectric surrounded with copper plates at different potential is the exact definition of capacitor, except it’s the size of your entire board. This obviously brings some considerations to the table when designing around these planes. Without going in depth into the physics of it, how far apart the planes are, how they are sequenced and interconnected will all affect a board’s planar impedance. In a nutshell, layers need to be sequenced properly to adequately decouple a design’s plane. This aspect becomes more and more critical as the frequency of the signals on the board increases, but it is an important thing to incorporate in all designs to reduce noise and cross coupling.

There are a few easy rules to follow in order to properly sequence power, ground and signal planes. First, as much as possible, a ground plane should be placed between any adjacent power or signal planes. This means having a ground plane between two power planes, two signal planes or a power plane and a signal plane. The only exception to this rule are the two most inner layers: these are often left adjacent and simply spaced according to the type of layer it is. Top and bottom should always remain signal layers. Before diving into layer spacing, below are some examples of classic layer stackups.

4 Layers:

* Top Signal
* Power
* Ground
* Bottom Signal

6 Layers:

* Top Signal
* Ground
* Signal
* Signal
* Power
* Signal

6 Layers (Better alternative):

* Top Signal
* Ground
* Power
* Signal
* Ground
* Bottom Signal

8 Layers:

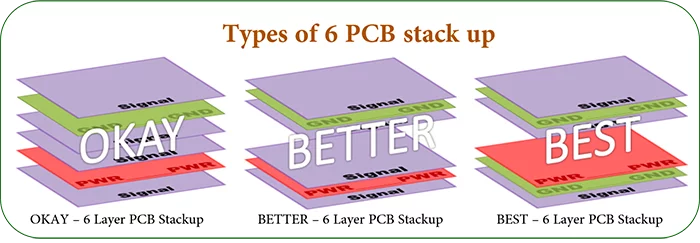
* Top Signal
* Ground
* Signal
* Power
* Ground
* Signal
* Ground
* Bottom Signal

8 Layers (Better alternative):

* Top Signal
* Ground
* Signal
* Ground
* Ground
* Signal
* Ground
* Bottom Signal

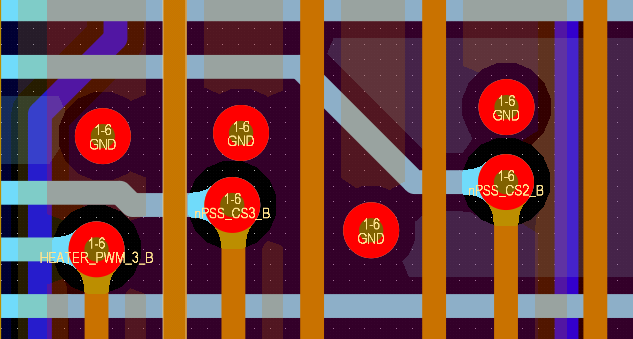
These examples all follow the aforementioned design terminology of separating all layers with ground planes, as much as possible. The two stackup marked “better alternative” are ideal cases for stackups, but are also often difficult to work with as the routing estate is reduced compared to the other cases.

Another important topic when looking at the layer stackup is how planes are distanced from each other. A general rule of thumb is simply as followed: power and signal planes should be kept as close as possible to a ground plane, and as far as possible from each other when they are not separated by a ground plane. Figure 13 is a great visualization of this principle.



**Figure 13: 6 Layer Stackup**

The last important aspect of the layer stackup is how it will affect the use of vias in a design. In a two or four layer board, no particular attention is given to the use of vias. For six layers or more though, an extra consideration needs to be included in the design: since more than one ground plane is present, signals going for example from top layer to inner layer 4 will have different reference planes. By this, it is meant that the closest ground plane is not the same. This could have very bad effects if not treated properly, as the return path for a signal crossing multiple layers will now become much bigger and maybe create loops, inducing a lot of noise into the system or even completely altering the signal itself. Fortunately, there are two main techniques that can be used to mitigate this effect: ground stitching and vias follower. Ground stitching was explained earlier in this document, while via follower is quite simple: everytime a via is used which carries a signal across multiple ground layers, a ground via should be placed right next to it. This ensures that the signal has a short return path no matter how many ground layers it crosses. Figure 14 shows this principle implemented on a 6 layer PCB.



**Figure 14: SC-ODIN’s CDH Board Utilizing Via Follower**

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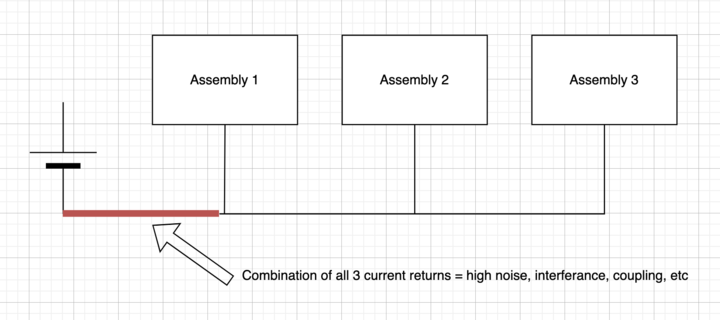
## Star Grounding

For this section and the next one, more detailed information can be found in reference [5].

Star grounding is a relatively simple but important concept to implement in designs that require low noise. This is particularly relevant to MCU, RF and analog designs which also require a generally “quieter” ground. Star grounding can be applied at a system level and at a board level. It is good practice to implement it in both, but generally the most important one is the system level. This will be the first aspect that will be looked at in this section.

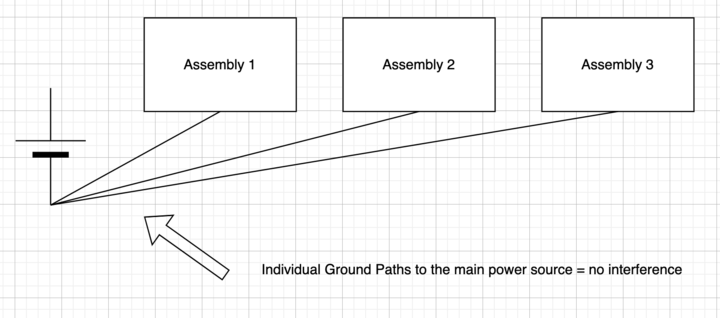
System Level Star Grounding

Although a bit counterintuitive when compared to the theoretical knowledge learned in classes, the ground of a circuit does carry current and therefore, can be a source of noise. In a simple circuit, the ground is usually a one to one connection with components or parts of the circuit, but in more complex systems, issues can arise from mishandling the ground connection. If the grounds of multiple boards are merged together at a single point, they can start interfering with each other, causing slight voltage differences on the ground segment and even inject noise into another system. This can be seen in figure 15.



**Figure 15: Typical Multipoint Ground Illustration**

A better practice to avoid this unwanted effect is to connect each system’s ground to the main ground through an isolated path. This means having a dedicated return path per board in the system. This greatly reduces the generated noise since currents cannot interfere with one another anymore. This is illustrated in figure 16. This type of grounding can be achieved by either creating different ground nets in a system and sorting them to the main ground directly at the power source or by simply keeping track of the board’s return path and manually separating them.



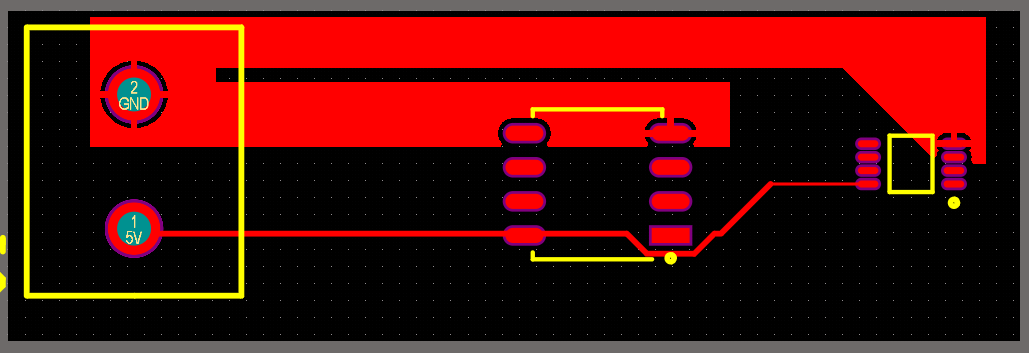
**Figure 16: Star Grounding Illustration**

Although it is good to understand the concept, most designers will not need to keep this in mind constantly when designing boards within a system since only the overall system designer or interface board designer will need to consider this aspect. With that said, it is still a good concept to be aware of, especially since it can be implemented virtually anywhere.

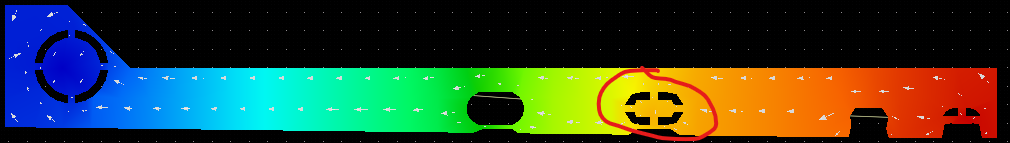
Board Level Star Grounding

Board level star grounding is a recommended practice to keep the noise level low and reduce interference between the different grounds, but it is also difficult to implement given the sheer amount of grounds to potentially isolate. This is only necessary when designing for sensitive analog circuits, RF electronics design and in some rare cases, MCU design. It also typically takes much more space on a board given that typical ground planes can’t be used, causing routing density to increase. This is why star grounding is not something that is usually implemented, but in specific designs it might be a requirement either set by the selected chip or the overall system designer.

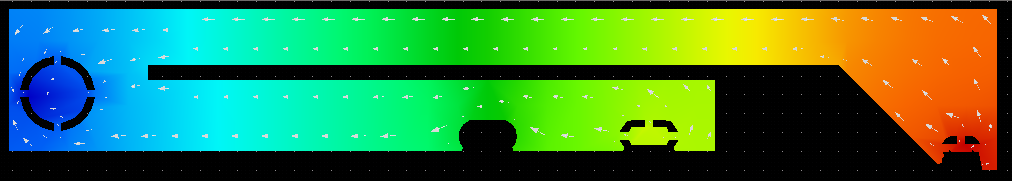
Without going in depth, board level star grounding can be simply achieved by routing the ground pins of different ICs directly to the source of a board instead of all together. To better illustrate this, a simple circuit board with one voltage source and two components was created and analyzed using the PDN analyzer tool. Figure 17 shows the analyzed design, figure 18 shows the analysis result with both ground connected, while figure 19 shows it with start grounding implemented.



**Figure 17: Analyzed Design**



**Figure 18: Voltage Gradient Without Star Grounding**



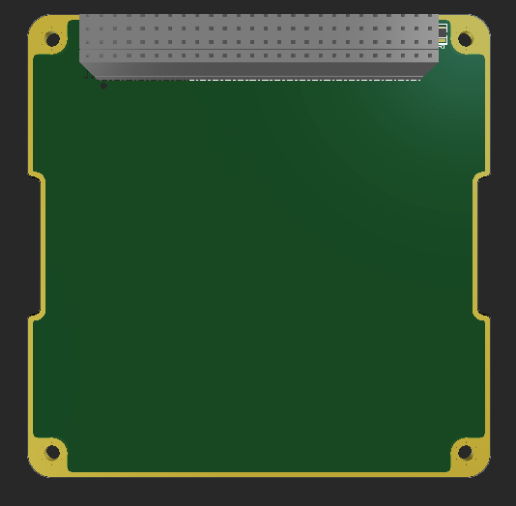
**Figure 19: Voltage Gradient With Star Grounding**

The color gradient represents the voltage distribution across the ground polygon, with red being the highest voltage and blue being the lowest. The point of interest in the last two images is the ground pad of the middle component (circled in red in figure 18). It can be seen between both simulations that with the same amount of current drawn from both components, the middle component’s ground voltage is much higher without star grounding, which can be a problem for very noise sensitive components. The simulation also shows the first component’s current going through the ground of the first components (the small white arrows). This is why simply separating the grounds and merging them at the board’s source can be beneficial. With that said, this is a great example of how space can get affected: the second configuration takes much more space than the first one. It is the designers responsibility to decide between both options depending on the requirements of the board.

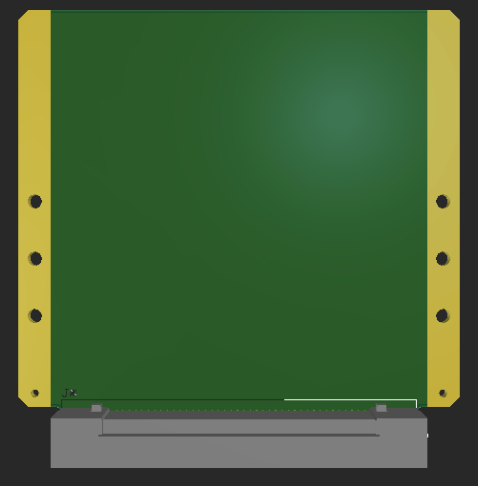
## Chassis Grounding

CHASSIS Ground, commonly referred to as CHASSIS, is a type of ground that is present in large electrical systems which are implemented within a conductive metallic structure. A satellite’s structure fits that criteria and therefore, proper ground methodology should be implemented on all PCBs that will be in the satellite. Ideally, the structure should remain at the same potential as the system’s ground and to achieve this, it needs to be electrically bonded to the system’s regular ground. First, it is important to know how to properly bond the structure to a CHASSIS net on a PCB before being able to connect it to the system’s ground. Electrical bonding refers to the action of reliably connecting two surfaces electrically to ensure they are at the same electric potential.

Typically, flight PCBs have a very distinct exposed copper area around the edge of the board. Two different implementations of these borders can be seen on figure 20 and figure 21. These areas are what provide the electrical bonding of the PCB to the chassis.



**Figure 20: CHASSIS Bonding for SC-ODIN PCBs (gold border)**

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**Figure 21: CHASSIS Bonding for SC-FREYR PCBs (gold border)**

These exposed copper areas are present by default when creating a SC-ODIN or SC-FREYR PCB. A detailed guide on how to create these exposed copper areas can be found in Appendix C of this document if specific bonding needs to be performed. For SC-ODIN PCBs, the exposed copper area around the four mounting holes provides a bond to the overall structure since metallic standoffs are attached on these holes. The trace which goes around the board ensures that all standoffs are connected and at the same electric potential. In the case of SC-FREYR PCBs, the exposed copper is directly connected to metal wedge-locks, which provide the mechanical support for the board as well as the electrical bonding to the overall structure. The wedge-locks are simply laid directly on the exposed copper and screwed in through the designated holes. It is important to ensure that these exposed copper pads have the net “CHASSIS” in the PCB file. This will ensure that the structure is properly connected to the main electrical ground.

Now that the bonding is achieved, it is very tempting to simply connect CHASSIS and GND directly together. This would ensure that the structure is always maintained to the exact same electric potential as the system. This is unfortunately not the proper way to connect them. Although it is important to keep the structure and ground at equal potential, shorting them together will make it so all the energy and noise captured by the structure of the satellite will be directly fed into the system’s ground. This is obviously not ideal, which means we need to find another way to achieve this. The solution is quite simple: add a filter in between CHASSIS and GND with high DC resistances and bypass capacitors for noise immunity. The filter or separation can be seen in figure 22. Another advantage of this separation is that it isolates the main power system from a short between CHASSIS and any power net. The 1M Ohm resistances make it so if a short occurred, not significant current would flow.

## 

## 

**Figure 22: CHASSIS Ground Separation**

# **Appendix A: Bench Power Supply User Manual**

Bench Power Supplies are extremely important equipment for electrical design and need to be used properly to ensure no damage or injuries ensue from its use. This Appendix quickly outlines how to set a dual channel power supply. The same principles will apply to single channel supplies. Before considering connecting a power supply to any circuit, the resistance between the power rails and ground should be verified to ensure no obvious short circuit is present. This can literally be done by plugging a multimeter from the power rail to ground and verifying there is no short circuit. This does not guarantee that no short is present completely since one could be after an active component, but it still reduces the chance of one being present.

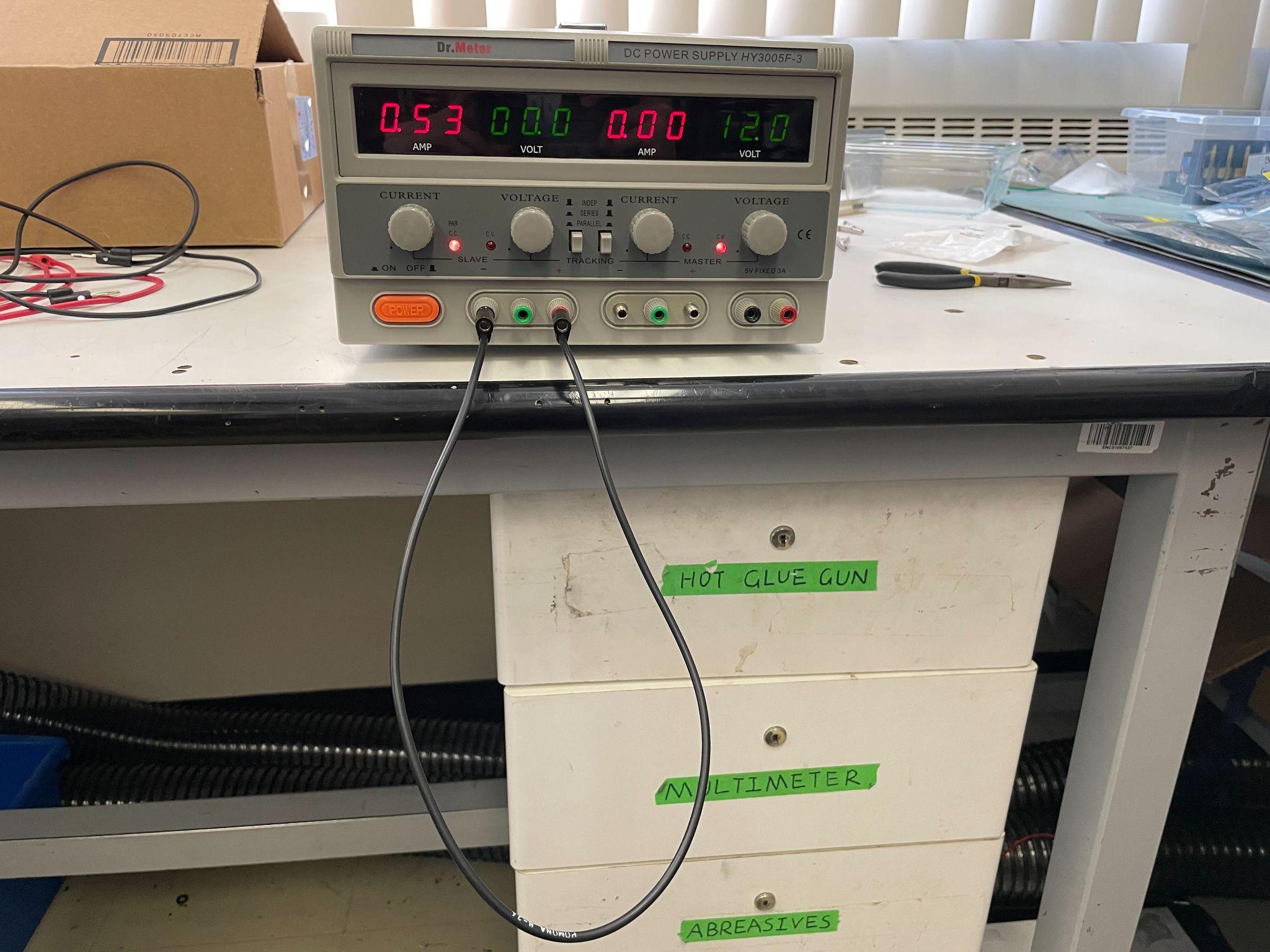
The first step is to take the power supply off its shelf and place it somewhere with enough space around it. Most importantly, keep the front of the power supply free from any obstructions.



Connect the power cable to the back of the supply and turn it on.



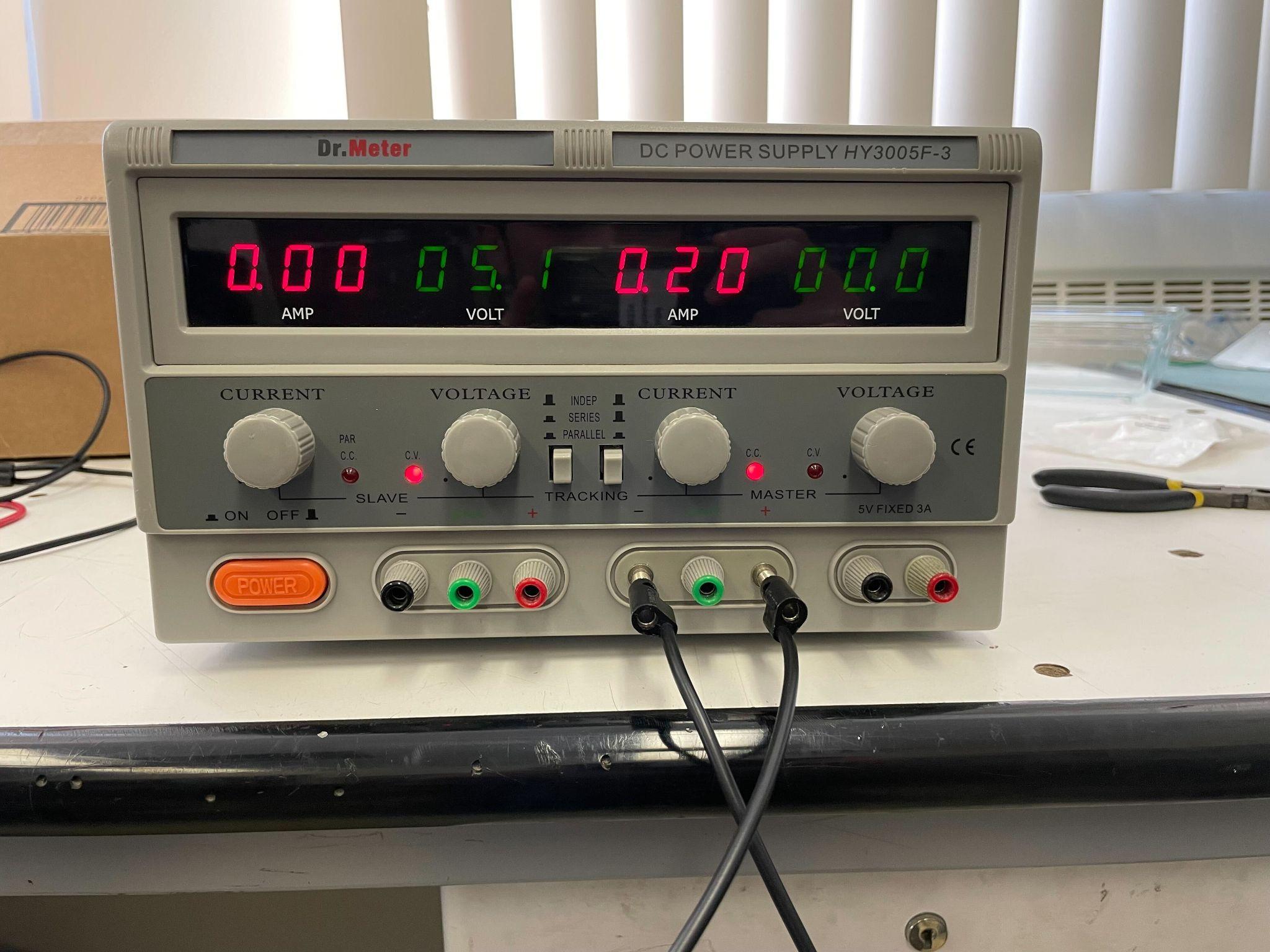
Using the voltage knob(s),set the needed voltage(s). **It is important to set the voltage before connecting anything to the power supply.** Once the desired voltage(s) have been set, the next step will be to set the current limit of the power supply. If this step is not done and the supply is connected to a circuit where a short is present, the power supply could deliver an extremely high current to the circuit and permanently damage components and even PCBs. To set the current limit, connect the positive and negative terminals together using a banana plug.



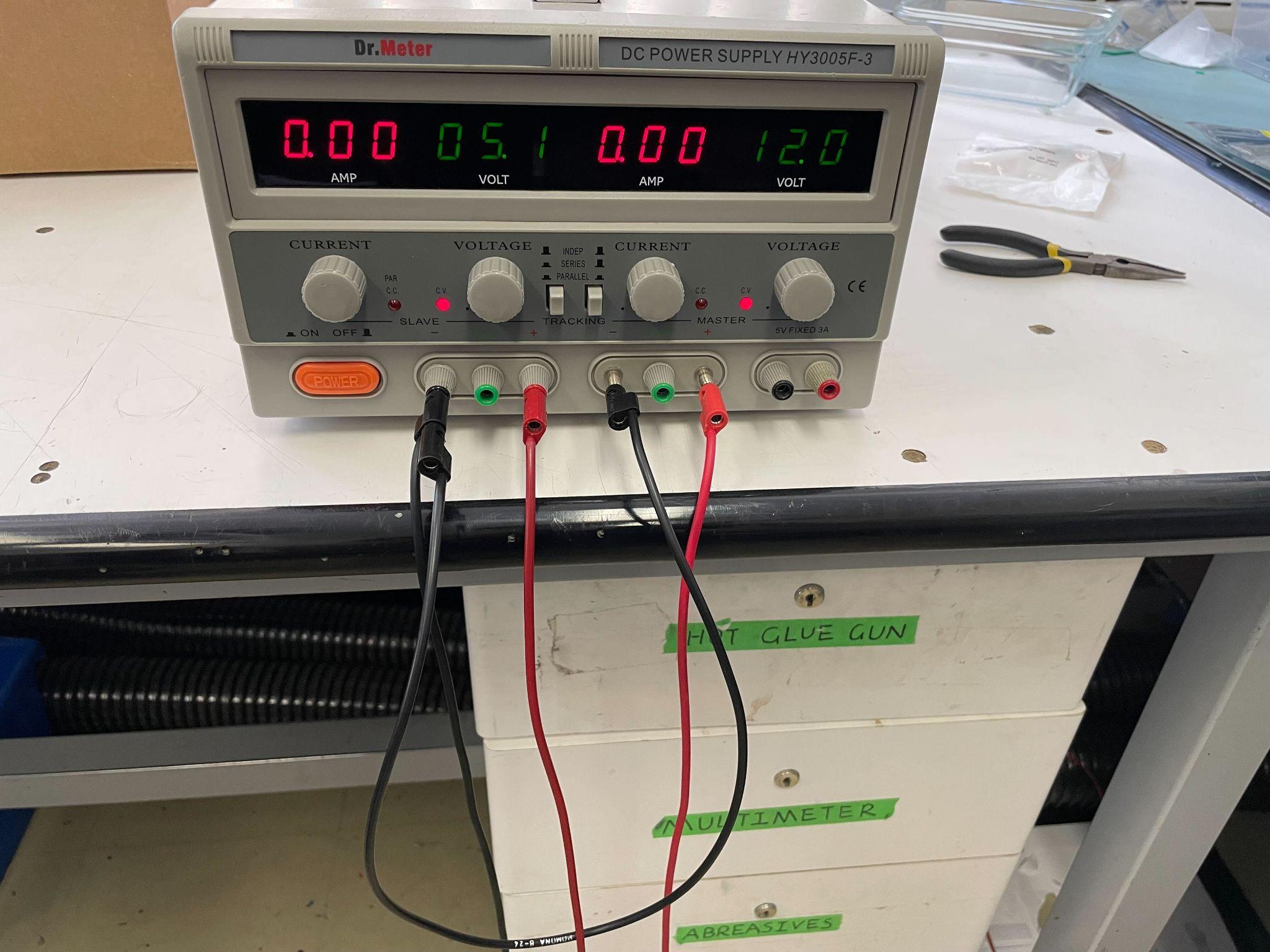
Then, using the current knob, the current limit of the supply can be set. In the above picture, the current limit was set to 0.53 amps, which is 530 mA. The value of the limit you should set is entirely dependent on the circuit under test. A typical value is just above the rated current consumption of a design. If unknown, it is highly recommended to set the current limit to a low value, power the circuit and if more current is needed, adjust at this point.

There are easy signs to recognize a dead short versus a lack of supply current: if a circuit is powered on and the voltage displayed by the source goes to 0, and the current is maxed to the limit, this indicates that there is a short circuit present. If the voltage only slightly drops when the current limit is reached, it typically means that the limit is too low. It can be manually increased while the circuit is powered on, and if the voltage reaches the set voltage when the current limit is increased, it means that the limit was indeed a bit too low.

If you intend on using both channels of the power supply, the second channel’s current limit should also be set.



Once the current limit is set, **and before connecting the supply to the circuit**, the two grounds should be shorted together using another banana cable. This will allow the two channels to have a common ground. The final setup should look something like this.

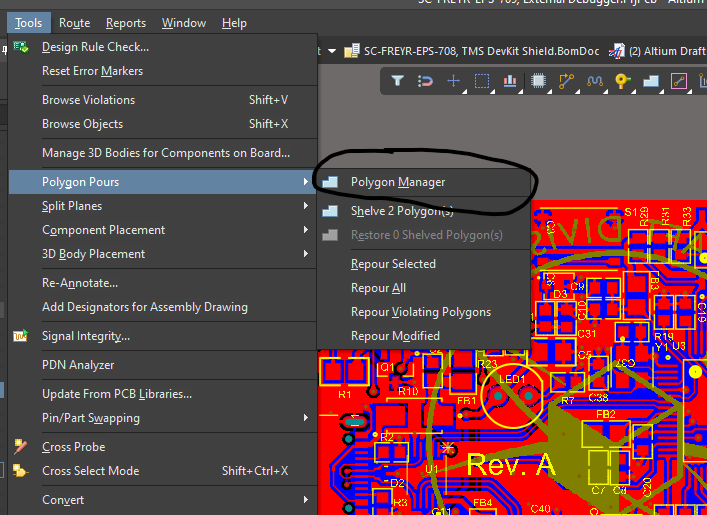


The last two jacks on the right side of the front panels can be used to supply a 5V rail with up to 3A of current. **Keep in mind that this supply is not current limited** and should only be connected to a circuit which was verified before.

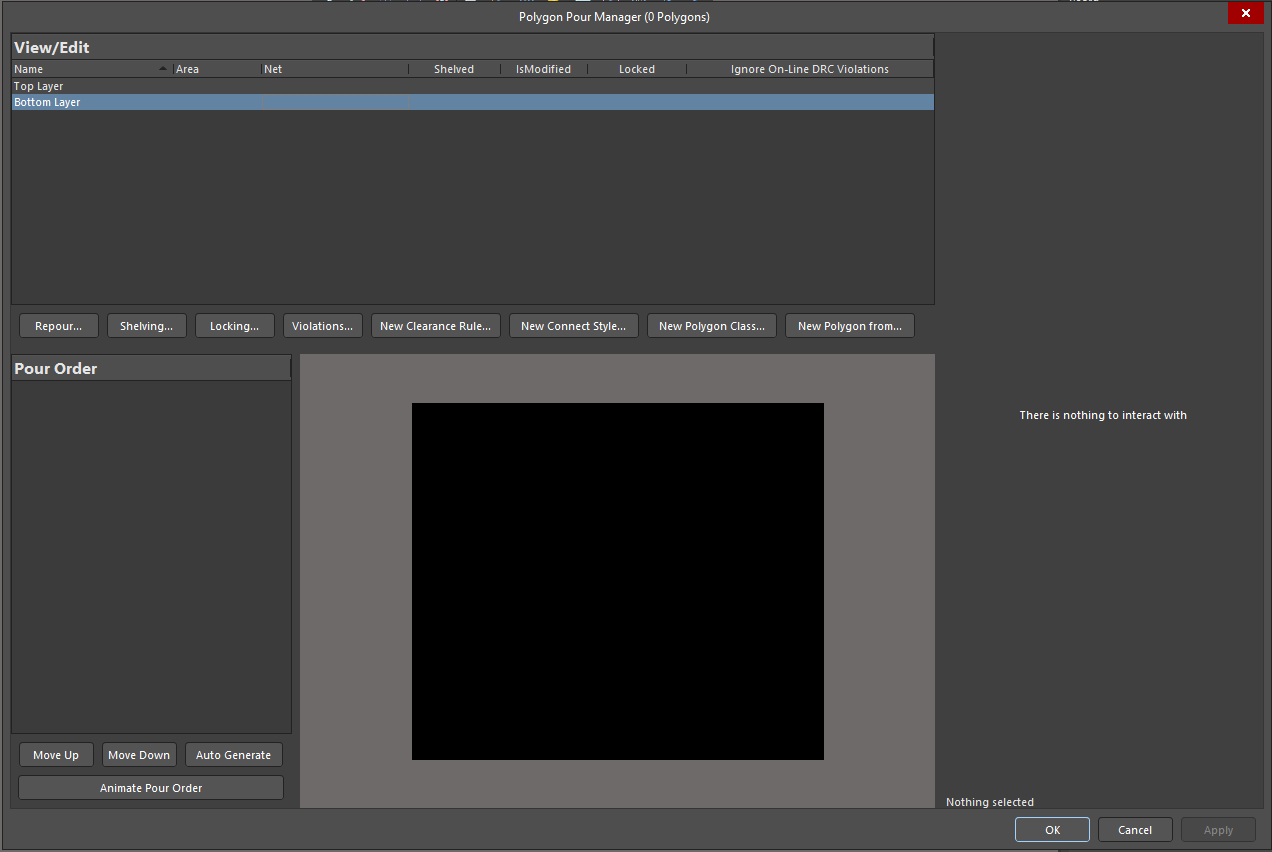
# **Appendix B: Polygon Creation**

This Appendix will do an overview of how different types of polygon pours are created, assigned and organized together. If anything specific is not mentioned here, more information can be found in reference [11].

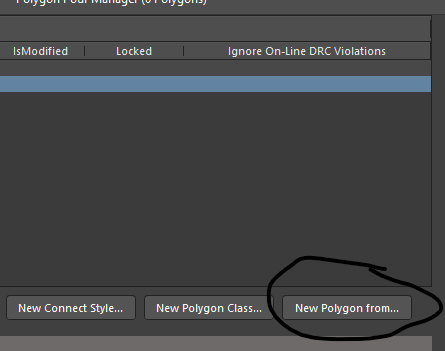
One of the most used polygon pour objects is the board sized polygon pour. This is not only useful to create power and ground planes, but also to fill signal layers with ground polygons for impedance matching and overall plane decoupling. Creating this type of polygon is very straightforward: open the polygon manager in Tools > Polygon Pours > Polygon Manager.



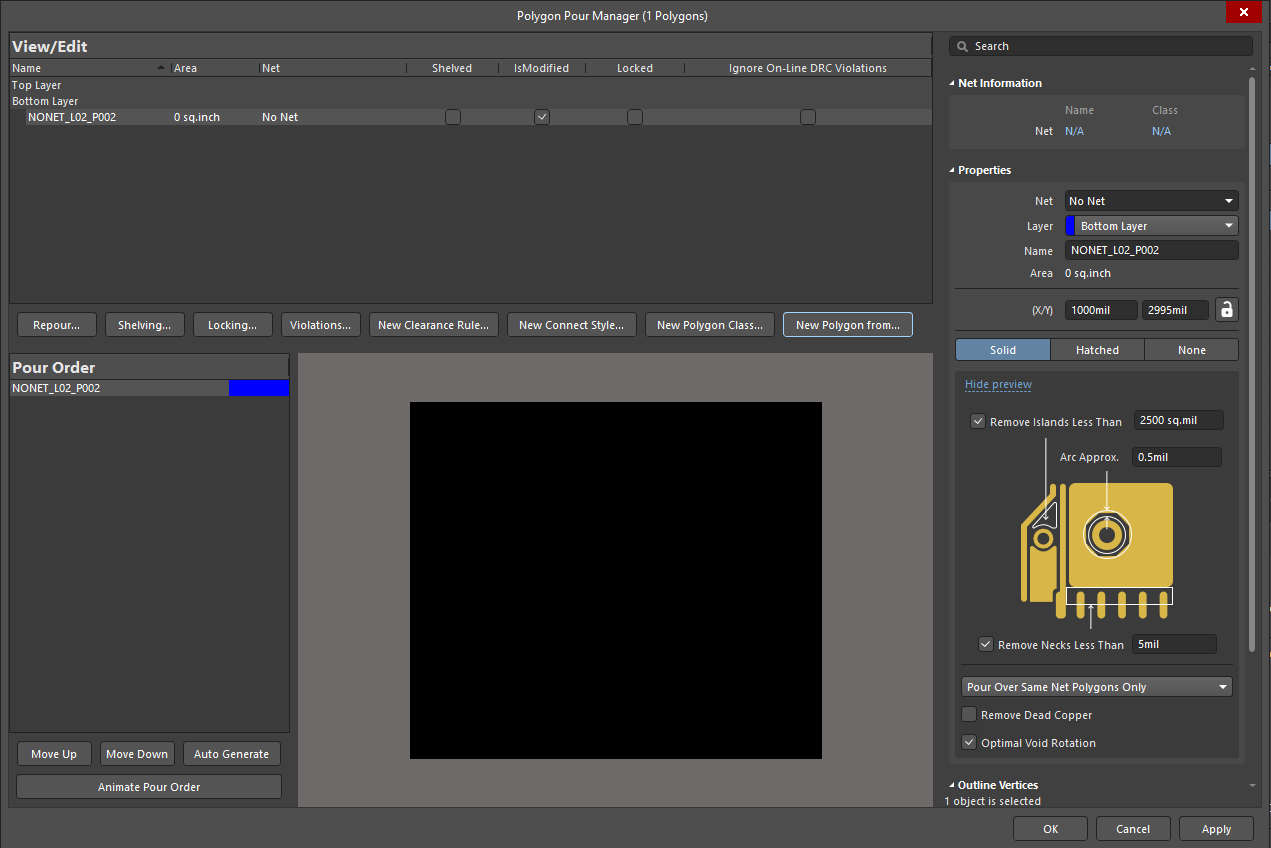
The following menu will open. All previously created polygons will also appear in this menu.



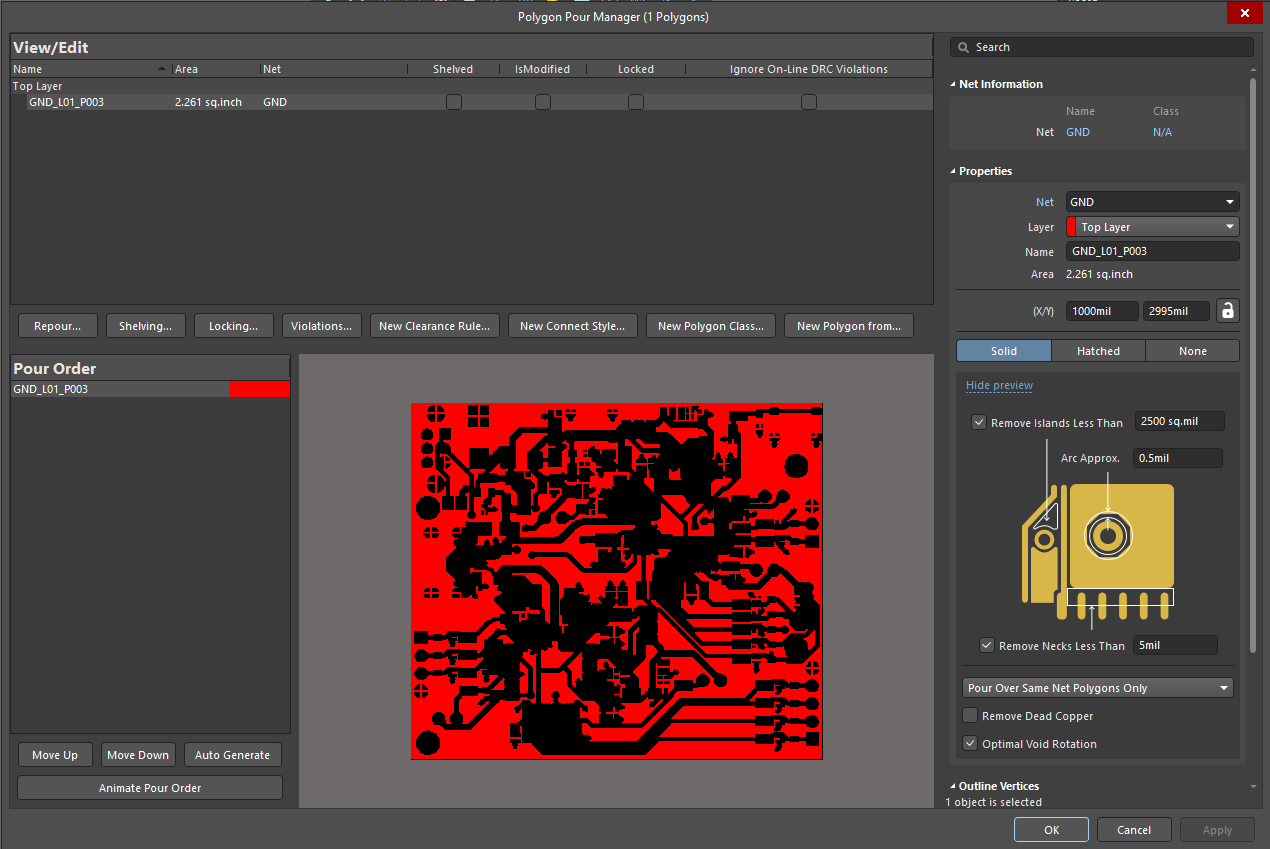
To create a polygon with the shape of the board, simply click on New Polygon from… and select board outline.



The polygon will then appear in the menu. The next step is to assign it the specific layer and net wanted. For via stitching, make sure to assign both the top and bottom layers to ground. On the right side, a few other options appear as to how the polygon will be poured, what to remove and what to keep, etc.



Once the layer and net is set, select Apply on the bottom right of the menu. Click Yes in the popup menu and the polygon will be poured.

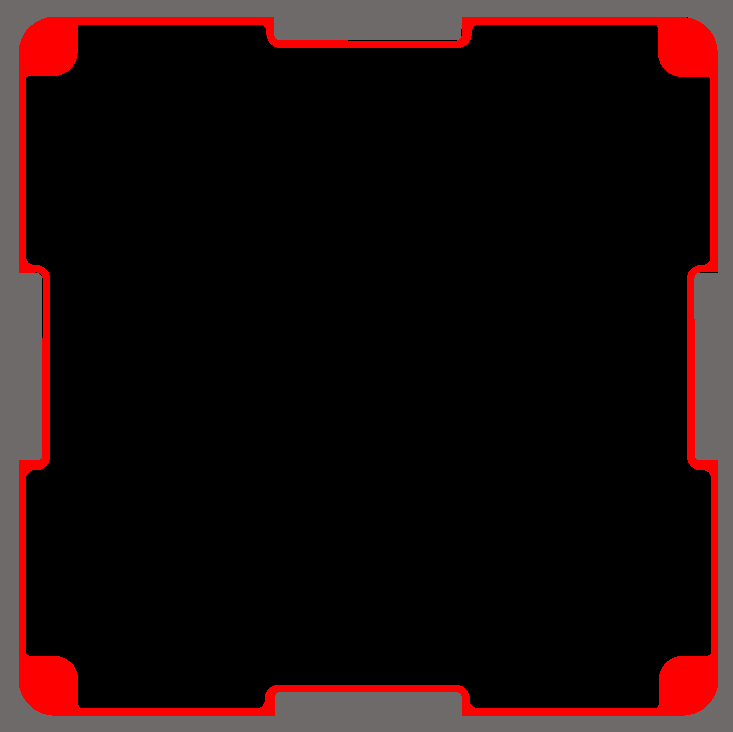


As can be seen in the above image, the polygon will pour over the entirety of the board while avoiding other nets.

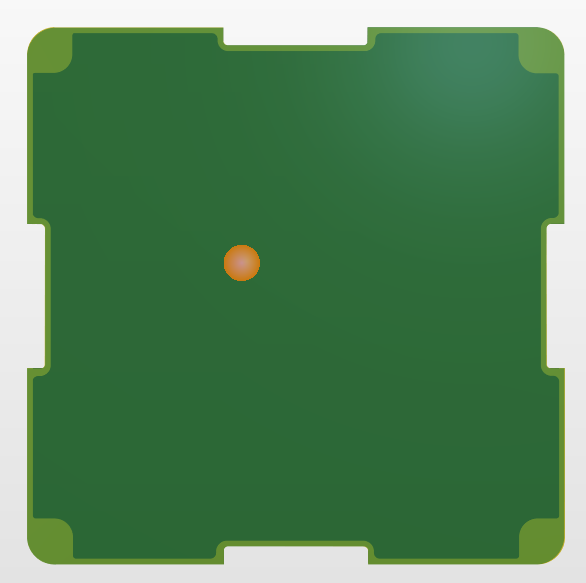
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# **Appendix C: Exposed Chassis**

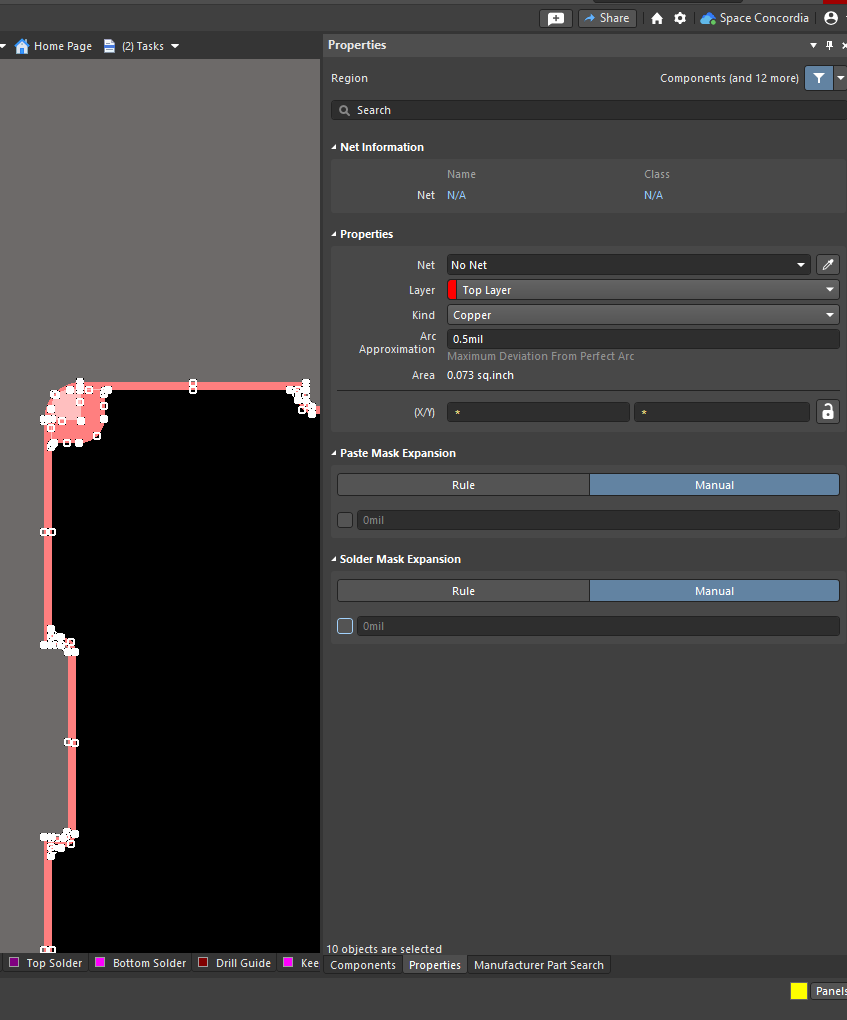
Exposed Chassis is not anything complicated in of itself, but it might not be very intuitive at first and this is why this Appendix will quickly look over how to expose a chassis properly. There are two main ways to achieve this once the poly region is defined for the chassis. Let’s use the SC-ODIN chassis as an example.



If left as is, the chassis will look something like this:



This is because the solder mask is still present over the copper. To properly expose the copper, one thing that can be done is to select the entirety of the chassis region (click on one of them and hit tab) and open the properties tab. At the bottom, a section called “Solder Mask Expansion” is present. By default, it will be set to Rule. To override this, simply click on manual and then check the box on the left. Set the number to 0 mils if not already done, and this will expose the copper of the region.



Unfortunately, this option is not available for polygon pours, only for polygon regions. If a design requires a polygon pour to be exposed, the second method will need to be used. The second method is also quite simple: once the polygon pour is drawn, copy and paste it right on top of itself, select the newly copied polygon and assign it the layer: Top Solder or Bottom Solder. These two layers, being negative fill, will effectively tell Altium where to remove the solder mask from the board. By placing an exact copy of a polygon on top of the actual polygon and assigning it one of these layers will remove all solder masks on top of the polygon.

# 

