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Modeling and Analysis of Positive Output Luo Converter in Voltage Control Mode

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ABSTRACT

This paper presents the modeling, controller design, and stability analysis for positive output LUO converter (POLC) in voltage control mode. The POLC uses elementary voltage lift technique to regulate the output voltage from a variable input voltage. In modeling of POLC, the transfer functions for control input to output and disturbance input to output are derived using linearized state-space averaging technique. The developed transfer function of POLC is analyzed for various duty cycles and circuit parameters. To improve the dynamic performance of POLC, the integral lead controller and the integral lag-lead controller are designed. This paper also presents the maximum time delay computation of POLC without losing small signal stability. Rekasius's substitution was used to analyze the stability with time delay. The performance of both the controllers was analyzed for various input voltages, reference voltages, and loads in MATLAB Simulink environment. The integral lag-lead controller provided an improved transient response and better stability. To validate the performance of the controllers, prototype experimental setup was implemented. The performance of the integral lag-lead controller was better despite the time delay caused by feedback element.

Keywords: Integral lag-lead controller, positive output LUO converter, Rekasius's substitution, stability, state space averaging techniques, time delay

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Introduction

Renewable energy sources such as solar PV, wind energy, and fuel cell, and so forth, are extensively used for generation of electrical power due to the depletion of fossil fuels, global warming, and the effects of greenhouse gas emissions. The output voltage from most renewable sources is in the form of direct current (DC) [1-4]. Hence, DC-DC converters are employed to interface source and load. The basic topologies of DC-DC converters such as buck, boost, and buck-boost converters have been proposed to regulate the output voltage of the system under consideration. The effects of parasitic elements in fundamental converters restrict the output voltage and conversion efficiency [5-9]. The recently developed converters such as Luo converters are widely used for the control and conversion of power [10, 11]. One of the most efficient converters among Luo converters is the positive output Luo converter (POLC), which provides large conversion ratio, high power density, high efficiency, positive output voltage, and low ripple content [12-14]. To design a controller for DC-DC converter, proper mathematical model of the converter and its response are required [15, 16]. The mathematical model of the converter completely describes the behaviour of the system due to disturbances and variations in control signals. Many control algorithms and mathematical models of DC-DC converters using Laplace transform and Z transform have been proposed in the previous literature [17, 18]. Generally, DC-DC converters have power semiconductor switches and diodes, which are nonlinear in nature. The dynamic model of the power electronic converters can be described using state-space modeling. State-space averaging and small-signal linearization technique provides an effective solution for the application of control techniques to DC-DC converters [19, 20]. The state-space modeling, design, and analysis of controllers are simple for the basic power converters topologies. However, recent converters require complex mathematical models [21-24]. Time delays have become an issue in the dynamic analysis of the POLC while measuremeing the output voltage for feedback. The maximum time delay is the minimum time required for the converter to operate in a stable

region. The estimation of time delay has been introduced in the literature [25227], but the algorithm is considerably complex.

In this paper, the linearized small signal state-space averaging model and transfer functions of POLC are derived. Using transfer functions, the open loop stability of the converter is analyzed using step response and root locus plots. This paper also describes the computation of maximum time delay of the converter without losing the small signal stability using Rekasius's substitution theorem and Routh stability criterion. The characteristic equation of dynamic system with transcendental term cannot be solved by analytical method. Rekasius's substitution converts the characteristic equation of the converter with transcendental term into polynomial equation. The maximum time delay and the roots at which crossing the imaginary axis is computed using the Routh Hurwitz criterion. The integral lead and lag-lead controllers have been designed for POLC, and their dynamic performance is analyzed for sudden changes in input voltage, reference voltage, and load. The prototype model has been developed to validate the simulation results.

This paper is organized as follows: In continuation to this introduction, Section II presents the design and working of the converter along with the details of formation of state-space equations, state-space averaging, small-signal linearization, and transfer function formulation. In Section III, the performance of the converter is analyzed using time response plots in open-loop modes. This section also emphasizes on the design of controllers, time delay computation, and stability analysis of POLC. Section IV presents the hardware implementation of the converter. Section V discusses the conclusion of the proposed work.

Mathematical Modeling of POLC

The structure of POLC is shown in Figure 1. POLC configuration allows only unidirectional power flow, that is, from source to load. The converter output can be regulated based on the control signal and perturbations in input voltage and circuit parameters. The MOSFET is used as a power switch, which operates either in conduction mode or in blocking mode. A time-dependent switching variable 'd' is used to describe the switching states. When d = 1, the switch is in ON state; when d = 0, the switch is in OFF state.

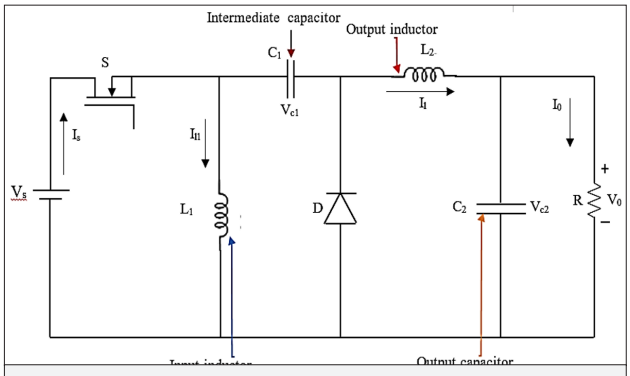

Figure 1. Configuration of POLC

The following assumptions are considered for the analysis: The switches are in ideal condition, and conduction of the converter is in continuous mode; the initial voltage across the capacitor is zero. The variables V_s and V_o are the input and output voltages of the converter, respectively.

In general, the state-space representation of the converter is given by

$$\dot{x} = A_i x + B_i u$$
$$y = C_i x$$

where state vector $x = [i_{l1}\ i_{l2}\ v_{c1}\ v_{c2}]^T$.

A_i-State-space matrix: i = 1 when switch S is ON and i = 0 when switch S is OFF. B_i-Input matrix and C_i- Output matrix. $v_0 = v_{c2} =$ [0001]. There are two inputs (disturbance input and control input), namely $u = [V_s\ d]^T$.

When the switch S is ON, the diode D is reverse biased and the corresponding state equations are

$$v_s = L_1 \frac{di_{l1}}{dt} \quad (1)$$

$$v_s - v_{c1} - v_{c2} = L_2 \frac{di_{l2}}{dt} \quad (2)$$

$$C_1 \frac{dv_{c1}}{dt} = i_{L2} \quad (3)$$

$$C_2 \frac{dv_{c2}}{dt} = i_{L2} - \frac{v_0}{R} \quad (4)$$

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ \frac{1}{L_2} & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, C_1 = [0\ 0\ 0\ 1]$$

When the switch S is OFF, the diode D will conduct and the corresponding state equations are

$$v_{c1} = -L_1 \frac{di_{l1}}{dt} \quad (5)$$

$$v_{c2} = -L_2 \frac{di_{l2}}{dt} \quad (6)$$

$$C_1 \frac{dv_{c1}}{dt} = i_{L1} \quad (7)$$

$$A_0 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & 0 \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}, \quad B_0 = [0], C_0 = [0\ 0\ 0\ 1] \quad (8)$$

To achieve the final state-space equations of POLC, averaging of state-space matrices A, B, and C are given by

$$A = A_1 d + A_0(1-d) \quad (9)$$

$$B = B_1 d + B_0(1-d) \quad (10)$$

$$C = C_1 d + C_0(1-d) \quad (11)$$

Using equations (1)–(11), the final state-space equations obtained are

$$L_1 \frac{di_{l1}}{dt} = (d-1)v_{C1} + dv_s \quad (12)$$

$$L_2 \frac{di_{l2}}{dt} = dv_{C1} - v_{C2} + dv_s \quad (13)$$

$$C_1 \frac{dv_{c1}}{dt} = (1-d)i_{l1} - di_{l2} \quad (14)$$

$$C_2 \frac{dv_{c2}}{dt} = i_{l2} - \frac{v_0}{R} \quad (15)$$

$$A = \begin{bmatrix} 0 & 0 & \frac{d-1}{L_1} & 0 \\ 0 & 0 & \frac{d}{L_2} & \frac{-1}{L_2} \\ \frac{(1-d)}{C_1} & \frac{-d}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}, B = \begin{bmatrix} \frac{d}{L_1} & 0 \\ \frac{d}{L_2} & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, C = [0\ 0\ 0\ 1]$$

Small signal linearization of state equations

The time-varying state equations (12) to (15) can be linearized using small-signal perturbation technique. The duty cycle and input voltage are represented by the addition of DC quantities and superimposed small alternating current (AC) signal variations.

By adding variations in the duty cycle and input voltage, the modified duty cycle and input voltage are given as,

$$d = D + \hat{d},\ v_s = V_s + \hat{v_s}\ \&\ 1 - d = 1 - D - \hat{d}$$

which causes changes in the state and output of the converter. Hence, variations in the inductor voltage, capacitor current, and output voltage are

$$\frac{di_l}{dt} = \frac{d(I_l + \hat{\imath}_l)}{dt} \quad (16)$$

$$\frac{dv_c}{dt} = \frac{d(V_c + \hat{v}_c)}{dt} \quad (17)$$

$$v_0 = V_0 + \hat{v}_0 \quad (18)$$

Substituting the variations in equation (12) to (15), the state-space equations become

$$L_1 \frac{d(I_{l1} + \widehat{\imath_{l1}})}{dt} = -(1 - D - \hat{d})(V_{C1} + \widehat{v_{c1}}) + (D + \hat{d})(V_s + \hat{v_s}) \quad (19)$$

$$L_2 \frac{d(I_{l2} + \widehat{\imath_{l2}})}{dt} = -(D + \hat{d})(V_{C1} + \widehat{v_{c1}}) - (V_{c2} + \widehat{v_{c2}}) + (D + \hat{d})(V_s + \hat{v_s}) \quad (20)$$

$$C_1 \frac{d(V_{c1} + \widehat{v_{c1}})}{dt} = (1 - D - \hat{d})(i_{l1} + \widehat{\imath_{l1}}) + (D + \hat{d})(i_{l2} + \widehat{\imath_{l2}}) \quad (21)$$

$$C_2 \frac{d(V_{c2} + \widehat{v_{c2}})}{dt} = i_{l2} + \widehat{\imath_{l2}} - \frac{(V_0 + \widehat{v_0})}{R} \quad (22)$$

The above equations are simplified based on the derivative of a constant term and the product of two AC terms. The product of two AC terms gives second-order nonlinear terms and are assigned to zero. The product of an AC term and a DC term is a DC quantity, and therefore, it is linear. The linearized and simplified state equation is of the form

$$\dot{\widehat{x(t)}} = \tilde{A}\widehat{x(t)} + \widetilde{B_1}\,\hat{v_s} + \widetilde{B_C}\hat{d}$$

and is given as

$$\begin{bmatrix} \frac{d\widehat{i_{l1}}}{dt} \\ \frac{d\widehat{i_{l2}}}{dt} \\ \frac{d\widehat{v_{c1}}}{dt} \\ \frac{d\widehat{v_{c2}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-D)}{L_1} & 0 \\ 0 & 0 & \frac{D}{L_2} & \frac{-1}{L_2} \\ \frac{1-D}{C_1} & \frac{-D}{C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix} \begin{bmatrix} \widehat{i_{l1}} \\ \widehat{i_{l2}} \\ \widehat{v_{c1}} \\ \widehat{v_{c2}} \end{bmatrix} + \begin{bmatrix} \frac{D}{L_1} \\ \frac{D}{L_2} \\ 0 \\ 0 \end{bmatrix} \hat{v_s} + \begin{bmatrix} \frac{V_s}{L_1(1-D)} \\ \frac{V_s}{L_2(1-D)} \\ \frac{-DV_s}{RC_1(1-D)^2} \\ 0 \end{bmatrix} \hat{d} \quad (23)$$

$$\widehat{v_0} = \tilde{C}\widehat{x(t)} \quad (24)$$

Transfer functions

To derive continuous current mode transfer functions, Signal flow graph was drawn using the linearized small signal equations from (19)–(22), as shown in Figure 2. The four state variables are nodes of the graph. Inputs of the signal flow are and control input . The nodes are connected by branch gains as in equations (19)–(22). The transfer functions between input signals and output signal were obtained using Mason's gain formula and are listed in Table 1.

Performance Analysis

For the analysis of converter in voltage control mode, two inputs namely, disturbance input voltage - and the control input were considered. The POLC was modeled and simulated in Simulink MATLAB environment and their corresponding results are presented with and without controllers.

The specifications of POLC are listed in Table 2 and are considered for the analysis.

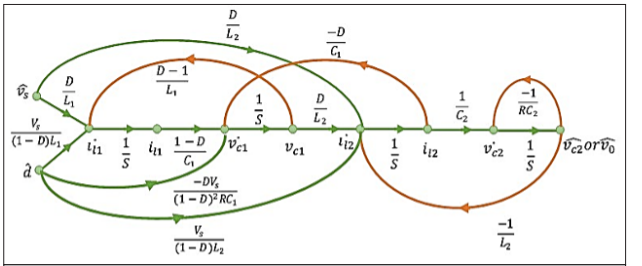

Figure 2. Signal flow graph of POLC

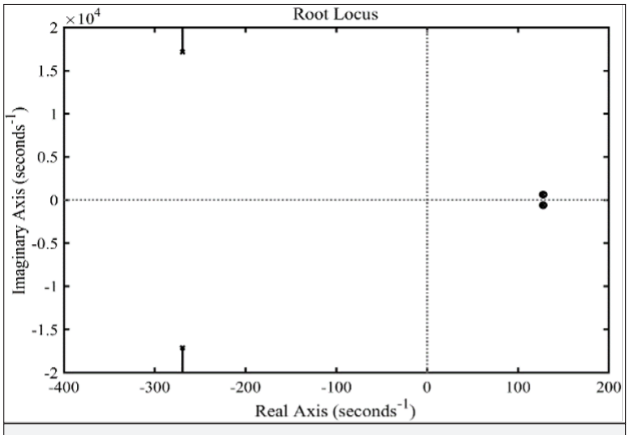

Figure 3. Root locus plot of output to control input transfer function for D = 0.6

Table 1. Transfer functions of POLC $\frac{\hat{v}_0(S)}{\hat{d}(S)}$

Transfer functions of output voltage to control input

No. of forward paths K = 3

(i) $P_1 = \frac{V_s D}{L_1L_2C_1C_2}\frac{1}{S^4}$ $\quad \Delta_1 = 1$

(ii) $P_2 = \frac{-D^2V_s}{L_2C_2RC_1(1-D)^2}\frac{1}{S^3}$ $\quad \Delta_2 = 1$

(iii) $P_3 = \frac{V_s}{(1-D)L_2C_2}\frac{1}{S^2}$ $\quad \Delta_3 = 1 + \frac{(1-D)^2}{L_1C_1}\frac{1}{S^2}$

Loop gains:

$$L_1 = -\frac{(1-D)^2}{L_1C_1}\frac{1}{S^2};\ L_2 = -\frac{1}{L_2C_2}\frac{1}{S^2};\ L_3 = -\frac{D^2}{L_2C_1}\frac{1}{S^2}\ L_4 = -\frac{1}{SRC_2}$$

Non touching loop gains:

$$G_{od} = \frac{\hat{v}_0(S)}{\hat{d}(S)} = \frac{\frac{V_s}{(1-D)L_2C_2}S^2 - \frac{D^2V_s}{L_2C_2RC_1(1-D)^2}S + \frac{V_s}{L_1L_2C_1C_2}}{S^4 + \frac{S^3}{RC_2} + S^2\left(\frac{D^2}{L_2C_1} + \frac{1}{L_2C_2} + \frac{(1-D)^2}{L_1C_1}\right) + S\left(\frac{D^2}{RL_2C_1C_2} + \frac{(1-D)^2}{RL_1C_1C_2}\right) + \frac{(1-D)^2}{L_1C_1L_2C_2}} \quad (25)$$

Transfer function of output voltage to disturbance input voltage $\frac{\hat{v}_0(S)}{\hat{v}_s(S)}$

No. of forward paths K = 2

(i) $P_1 = \frac{(1-D)D^2}{L_1L_2C_1C_2}\frac{1}{S^4}$ $\quad \Delta_1 = 1$

(ii) $P_2 = \frac{D}{L_2C_2}\frac{1}{S^2}$ $\quad \Delta_2 = 1 + \frac{(1-D)^2}{L_1C_1}\cdot\frac{1}{S^2}$

Loop gains:

$$L_1 = -\frac{(1-D)^2}{L_1C_1}\frac{1}{S^2};\ L_2 = -\frac{1}{L_2C_2}\frac{1}{S^2};\ L_3 = -\frac{D^2}{L_2C_1}\frac{1}{S^2}\ L_4 = -\frac{1}{SRC_2}$$

Non touching loop gains:

$$L_3L_4 = \frac{D^2}{RL_2C_1C_2}\frac{1}{S^3};\ L_1L_4 = \frac{(1-D)^2}{RL_1C_1C_2}\frac{1}{S^3};\ L_1L_2 = \frac{(1-D)^2}{L_1C_1L_2C_2}\frac{1}{S^4}$$

$$G_{os} = \frac{\hat{v}_0(S)}{\hat{v}_s(S)} = \frac{\frac{D}{L_2C_2}S^2 + \frac{D(1-D)}{L_1L_2C_1C_2}}{S^4 + \frac{S^3}{RC_2} + S^2\left(\frac{D^2}{L_2C_1} + \frac{1}{L_2C_2} + \frac{(1-D)^2}{L_1C_1}\right) + S\left(\frac{D^2}{RL_2C_1C_2} + \frac{(1-D)^2}{RL_1C_1C_2}\right) + \frac{(1-D)^2}{L_1C_1L_2C_2}} \quad (26)$$

Table 2. Parameters of POLC

Parameter	Value
Inductors: L_1, L_2	36.04 mH
Capacitors: C_1, C_2	21.40, 30.4 µF
Load Resistance: R	135.2 Ω
Power	600 W
Input Voltage - V_s	90–150 V
Output Voltage - V_0	260 V

Output to control input transfer function $\frac{\hat{v}_0(S)}{\hat{d}(S)}$

The transfer function of the converter was developed using the values provided in Table 2 and equation (25) for duty ratio of D = 0.6 and is given by

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{2.923*10^9S^2 - 7.471*10^{10}S + 1.139*10^{14}}{S^4 + 284S^3 + 2.937*10^9S^2 - 7.457*10^{10}S + 1.14*10^{14}} \quad (27)$$

The root locus plot of the above transfer function is shown in Figure 3. Two complex poles lie on left half of s-Plane, and two complex poles and two complex zeros lie on the right half of s-Plane. The step response plot is shown in Figure 4. The output of the system continuously increased with time. Hence, the system was concluded to be unstable.

When the load resistance value R was changed from 135.2 W to 1000 W, the corresponding transfer function became

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{2.923 * 10^9S^2 - 7.471 * 10^{10}S + 1.139 * 10^{14}}{S^4 + 28.4S^3 + 2.937 * 10^7S^2 - 7.457 * 10^9S + 1.14 * 10^{14}}$$

The transfer function has four complex poles and two complex zeros and is shown in Figure 5. Two complex poles lie on the left-hand side (LHS) and another two poles lie on the right-hand side (RHS). The complex zeros also lie on the RHS. The two complex poles and zeros moved slightly on the LHS but never crossed the origin. Hence, the system was completely unstable, and the corresponding step response is given in Figure 6. When the load resistance value is increased, the complex poles moves towards the imaginary axis. This makes the system less stable.

When the capacitor value C_2 was changed to 360 µF from 30.4 µF and on time of the MOSFET was changed to D = 0.3, the transfer function became

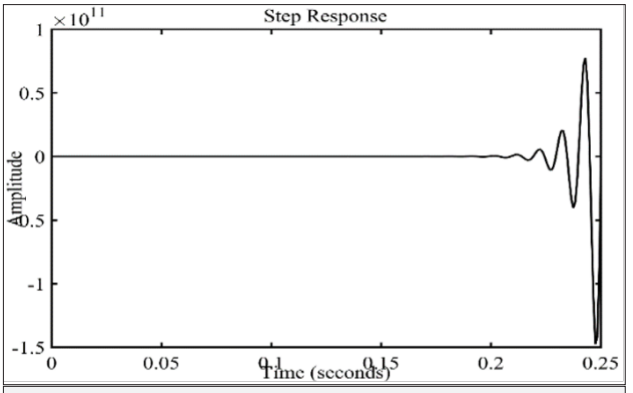

Figure 4. Step response of output to control input transfer function for D = 0.6

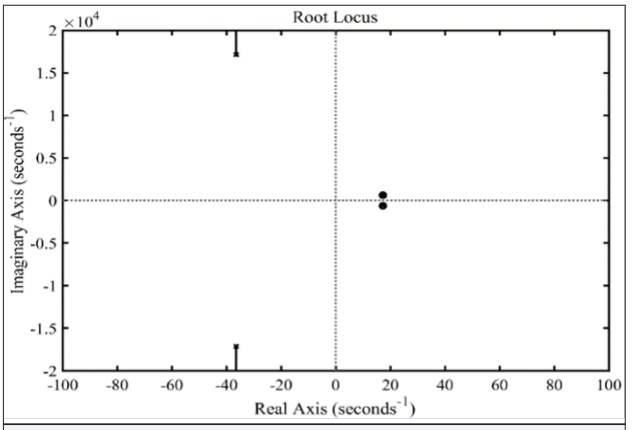

Figure 5. Root locus plot of output to control input transfer function for D = 0.6 and R =1000 Ω

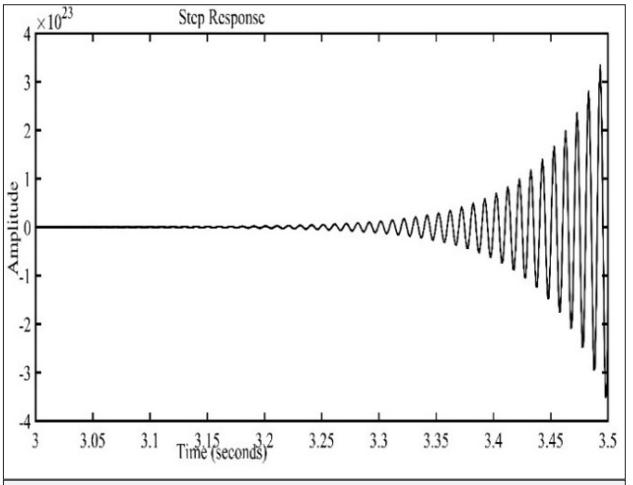

Figure 6. Step response of output to control input transfer function for D = 0.6 and R = 1000 Ω

$$\frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{2.923 * 10^9 S^2 - 7.471 * 10^{10} S + 1.139 * 10^{14}}{S^4 + 28.4S^3 + 2.937 * 10^7 S^2 - 7.457 * 10^9 S + 1.14 * 10^{14}}$$

The transfer function had two complex poles and two zeros. Two poles and zeros lie on the RHS plane, as shown in Figure 7.

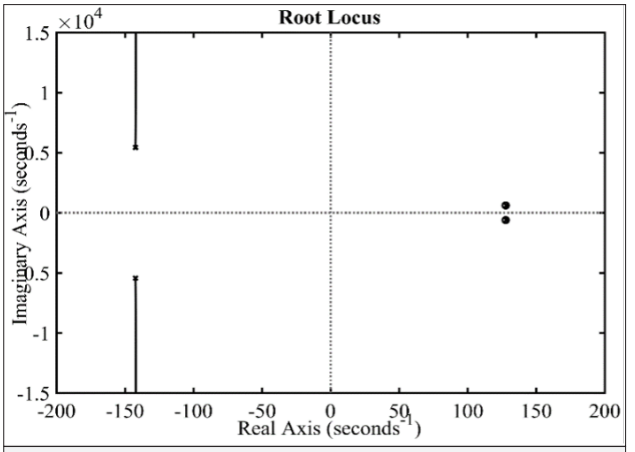

Figure 7. Root locus plot of output to control input transfer function for D = 0.3 and C_2 = 360 μF

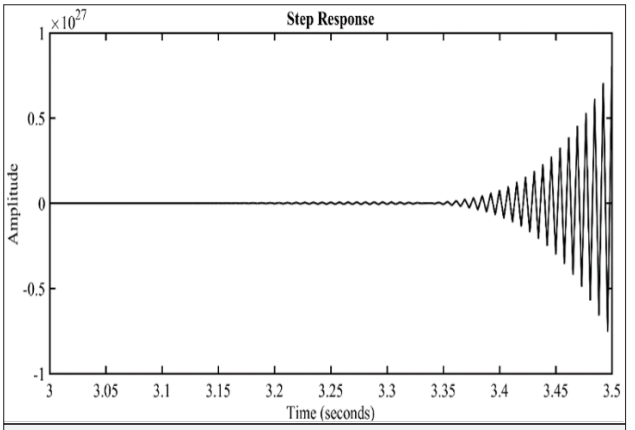

Figure 8. Step response plot of output to control input transfer function for D = 0.3 and C_2 = 360 μf

This indicates that the system is unstable. The system response is shown in Figure 8.

Output to disturbance input transfer function $\frac{\hat{v}_0(S)}{\hat{v}_s(S)}$

For $L_1 = L_2$ = 36.04 mH, C_1 = 29.04 μF, C_2 = 260 μF and D = 0.6, the input to output transfer function using equation (26) is given by

$$\frac{\hat{v}_0(s)}{\hat{v}_s(s)} = \frac{5.845 * 10^4 S^2 + 2.278 * 10^{10}}{S^4 + 28.4S^3 + 6.624 * 10^5 S^2 + 1.439 * 10^7 S + 3.796 * 10^{10}}$$

This transfer function has four poles and two zeros. The four poles lie on the LHS plane, and the zeros lie on the imaginary axis. The corresponding root locus and step response are shown in Figure 9 and Figure 10, respectively. The step response of the system seems to be stable, but it has ripples and there is a steady state error.

From the above analysis, it can be inferred that the system is unstable due to the presence of RHS plane zeros and poles of the system even when the duty cycle or the circuit parameters are changed. To improve the stability and transient behaviour of the system, integral lead controller was considered.

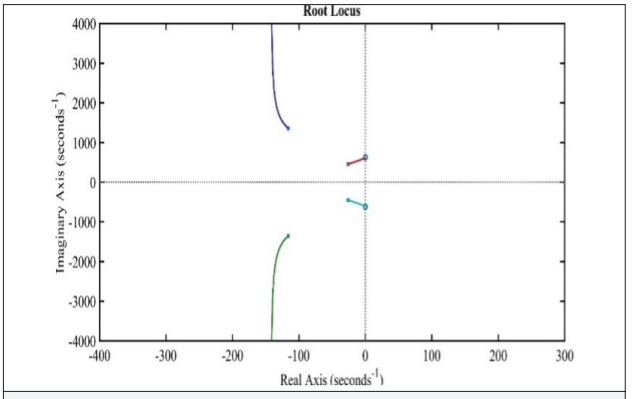

Figure 9. Root locus plot of output to disturbance input transfer function for D = 0.6

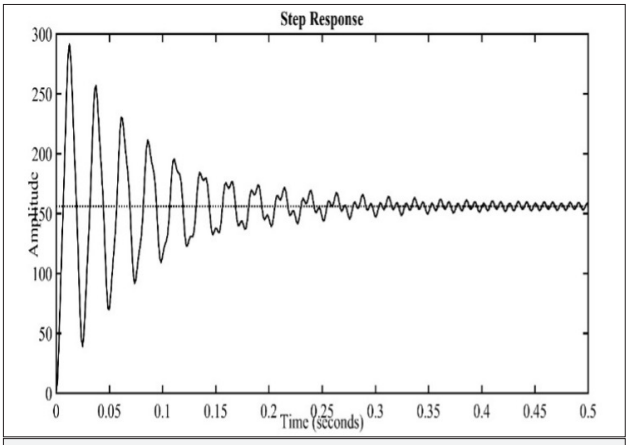

Figure 10. Step response plot of output to disturbance input transfer function for D = 0.6

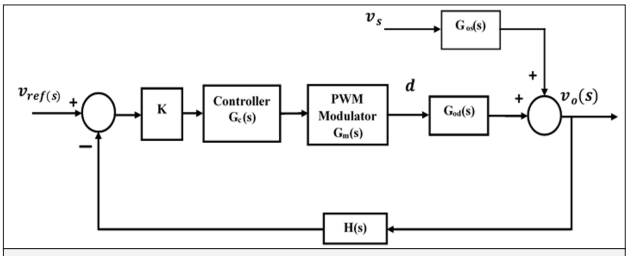

Figure 11. Block diagram: Closed loop control

Closed loop analysis of the converter

The main objective of the closed loop system is to design a suitable controller to make the system more stable and to maintain the desired output voltage when perturbations are introduced in the input voltage from 90 to 130 V.

The open-loop transfer function with integral lead controller for D = 0.6 is given as

$$G(S) = \frac{2.63 * 10^8 S^3 + 5.565 * 10^{10} S^2 + 7.108 * 10^{13} S + 4.789 * 10^{16}}{S^6 + 7444 S^5 + 3.515 * 10^6 S^4 + 1.075 * 10^{10} S^3 + 1.182 * 10^{12} S^2 + 2.087 * 10^{15} S}$$

The open-loop transfer function with integral lead lag controller for D = 0.6 is given as

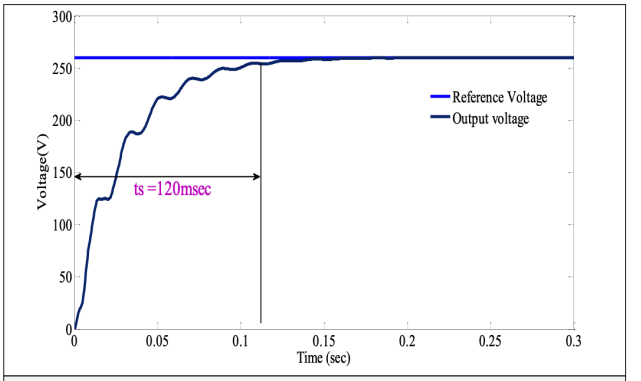

Figure 12. Step response of the system with integral lead controller

$$G(S) = \frac{2.057 * 10^7 S^4 + 4.597 * 10^{10} S^3 + 2.422 * 10^{13} S^2 + 1.247 * 10^{16} S + 1.142 * 10^{19}}{S^7 + 7584 S^6 + 4.557 * 10^6 S^5 + 1.124 * 10^{10} S^4 + 2.682 * 10^{12} S^3 + 1.253 * 10^{15} S^2 + 2.522 * 10^{17} S}$$

The controller is designed to meet the time domain specifications such as damping factor of 0.7, settling time of 60 ms, and an overshoot of 6%. The block diagram of the closed-loop voltage-controlled converter is shown in Figure 11.

The AC component of the output voltage of the converter is given as

$$v_0(s) = \frac{KG_c(s)G_m(s)G_{od}(s)}{1 + KG_c(s)G_m(s)G_{od}(s)H(s)} v_{ref}(s) + \frac{KG_{os}(s)}{1 + KG_c(s)G_m(s)G_{od}(s)H(s)} v_s(s)$$

where

$G_C(S)$ - Transfer function of the controller

$G_m(S)$ - Modulator gain = 0.125

$H(S)$ - Feedback gain = 26

While analyzing the performance of the controller, the change in disturbance input was assumed to zero.

Integral lead controller design

To reduce the DC gain and increase the margin of stability, the integral lead controller is required to achieve high gain at low frequencies. The pole at origin provided a phase lag of 90° at all frequencies. The lead controller was designed to compensate the phase lag and to increase the speed of response. At low frequency f < 476 rad/s and at high frequency f > 7143 rad/s, the phase angle was approximately -90°. The maximum phase angle contributed by the lead controller was 60° at 1843 rad/s, which is a geometric mean of pole and zero frequencies.

The transfer function of the controller was

$$G_c(s) = \frac{0.068(1 + 0.0021s)}{s\,(1 + 0.00014s)}$$

The open-loop transfer function of the system was

$$G(s) = G_c(s) * G_m(s) * G_{od}(s) * H(s)$$

The step response of the closed system for duty ratio of D = 0.6 is shown in Figure 12.

The controller provides the settling time of 120 ms, and there are oscillations in the transient response. After that, it follows the reference value. The step response indicates that the system is stable, but the high value of settling indicates that the system response is sluggish.

Integral lag-lead controller design

To improve the speed of response and relative stability of the converter, an integral lag-lead controller is proposed. The controller provides high gain and phase lag of -90° at low frequencies. The gain of the controller is 0.1. There is no intersection between the responses of the controller. The two zeros are placed at f_{z1}=0.892 KHz and f_{z2}=8 KHz. The poles are located at f_{p1}=7.142 KHz and f_{p2}=0.14 KHz. To get a faster response, the value of f_{z2} is set high and is nearly 10 times of the value of f_{z1}. The pole at the origin and the other two poles minimize the steady state error to zero and improve the speed of response.

The transfer function of the integral lag-lead controller is

$$G_c(s) = \frac{0.1(1 + 0.001121s)(1 + 0.000125s)}{s\,(1 + 0.00014s)(1 + 0.00714s)}$$

The step response plot for the closed loop system with integral lag-lead controller is shown in Figure 13. The integral lag-lead controller provides settling time of 65 ms with negligible overshoot for duty ratio of D = 0.6. The reduced value of settling time indicates that the speed of response of the system is improved.

Time delay analysis

This section presents the time delay analysis of POLC where the time delay element is introduced in the feedback. If all the roots of the characteristic equation lie on the LHS of the complex S-plane, the delayed linear system is asymptotically stable. However, the characteristic has many roots that result in high computation burden.

To compute the delay margin and analyze the stability of the system, it is necessary to obtain its characteristic equation with integral lag-lead controller. The characteristic equation is of the form

$$1 + KG_c(s)G_m(s)G_{od}(s)H(s)e^{-s\tau} = 0 \text{ or}$$
$$\Delta(s,\tau) = A(S) + B(S)e^{-s\tau} = 0 \quad (27)$$

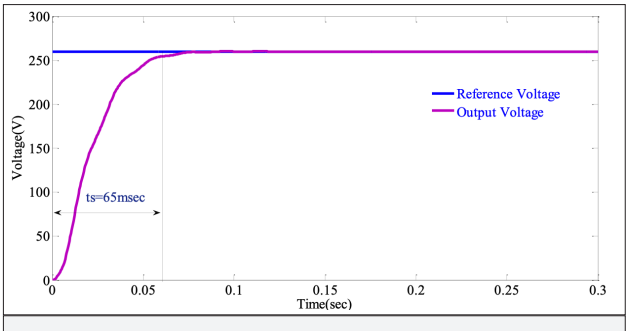

Figure 13. Step response of the system with integral lag-lead controller

where τ-Time delay. A(S) and B(S) are the polynomials of the characteristic equation having coefficients in terms of S and parameters of POLC.

$$A(S) = a_7S^7 + a_6S^6 + a_5S^5 + a_4S^4 + a_3S^3 + a_2S^2 + a_1S + a_0$$
$$B(S) = b_4S^4 + b_3S^3 + b_2S^2 + b_1S + b_0$$

Coefficents of the polynomial depends on the converter parameters, controller gain, and delay.

The main objective is to study the location of roots of the characteristic equation using Rikasius's substitution [26]. The Rikasius's substitution converts the transcedental equation into polynomial equation. The Rikasius's substitution is $e^{-s\tau} = \frac{1-ST}{1+ST}$. τ€ R, T€ R, which is defined for the imaginary axis S= j ω, ω € R, the roots are on the imaginary axis.

This exact transformation holds if and only if

$$\tau = \frac{2}{\omega}(tan^{-1}(\omega\tau) + k\frac{\pi}{2}$$

where k = 0,1,2,…

By substituting. $e^{-s\tau}$ value in equation (27), we obtain

$$\Delta(s,\tau) = A(S) + B(S)(\frac{1-ST}{1+ST}) = 0$$
$$\Delta(s,\tau) = A(S)(1+ST) + B(S)(1-ST) = 0 \quad (28)$$

The equation is of the form

$$\Delta(s,\tau) = p_8S^8 + p_7S^7 + p_6S^6 + p_5S^5 + p_4S^4 + p_3S^3 + p_2S^2 + p_1S + p_0 = 0$$

where

$p_8 = T, p_7 = 1 + 7584T,$
$p_6 = 7584 + 4.557 * 10\text{^}6T$
$p_5 = 4.557 * 10^6 + 1.122 * 10\text{^}10T$
$p_4 = 1.126 * 10\text{^}10 + 2.641 * 10\text{^}12T$
$p_3 = 2.733 * 10\text{^}12 + 1.25 * 10\text{^}15T$
$p_2 = 1.255 * 10\text{^}15 + 1.3973 * 10\text{^}17T$
$p_1 = 1.65 * 10^{17} - 1.241 * 10\text{^}19T$
$p_0 = 1.241 * 10\text{^}19$

After Rekasius's substitution, the characteristic changes into eighth-order polynomial.

Now, the Routh stability criterion can be used to find the roots of the equation. The maximum time delay is computed from the Routh table as T_{max}= 8.7472 ms.

The crossing frequency of imaginary axis is found by equating S^2 row of Routh array to zero, i.e., 2.308*10^15 S^2 + 1.142 * 10^{19}=0, solving ±jω=±j70 rad/s. The time delay is in the order of ms, as the proposed system does not have any communication network. The time delay occurs only due to the measurement.

When the time delay exceeds 8.7472 ms, the system is unstable, that is, it loses its small signal stability. The theorectical time delay calculation is verified using time response plots.

Figure 14a shows the pole zero plot of the characteristic equation with time delay τ = 8.8 ms. All the roots of the characteristic equation lie on the LHS of the complex S-plane, and the

corresponding step response is shown in Figure 15a. The response attains the steady-state value without error. However, when delay t is added, the transient response increases linearly rather than exponentially. The time delay component modifies the nature of transient response of the system. Overshoot increases as the time delay increases. When the delay is less than the critical value, $t = t_{max} = 8.7472$ ms, the system is stable.

Figure 14b shows the pole zero plot of the characteristic equation with time delay $\tau = \tau_{max} = 8.7472$ ms. The complex conjugate pair of roots located on the imaginary axis of the complex S plane. Hence, the system is mariginally stable.

If the delay ($\tau = 9$ ms) exceeds the maximum limit slightly, the system no longer remains stable. The complex conjugate pair of roots moving on to the RHS of the complex S-plane is shown in Figure 14c and d. For $\tau = 9$ ms, magnitude of step response increases abruptly and is shown in Figure 15b. Hence, the system is unstable.

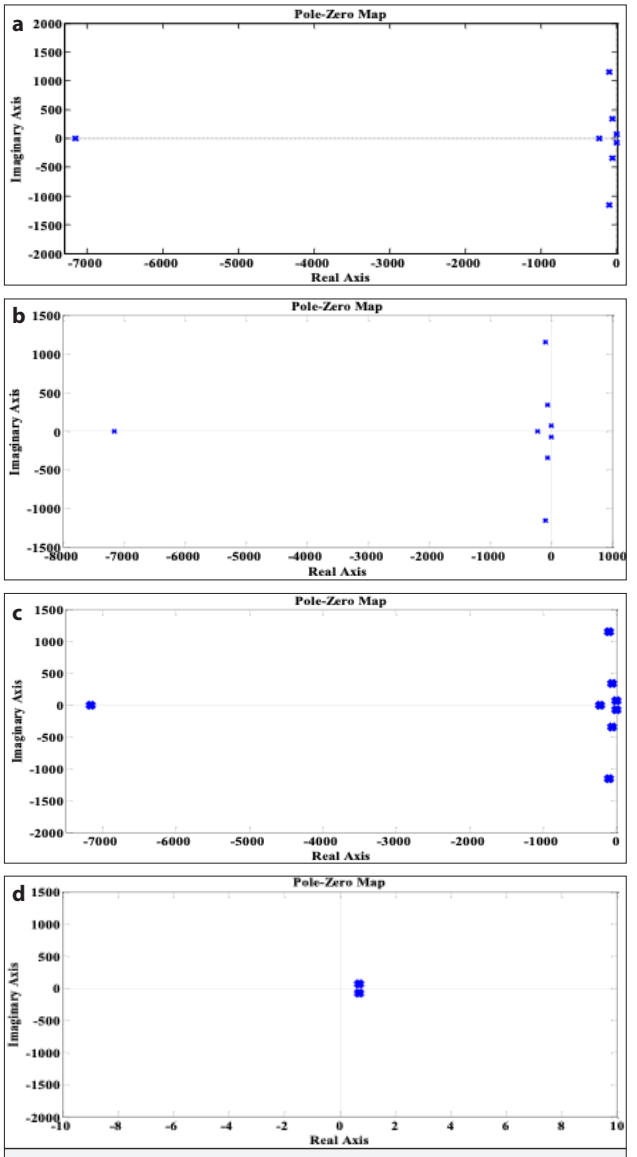

Figure 14. a-d. Pole-zero plot of the converter. (a) time delay = 8 ms (b) time delay = 8.747208 ms (c) time delay = 9 ms (d) expanded view of (c) near origin

Steady-state performance

Sudden change in input voltage

The steady-state performance is analyzed for varying input voltage with integral lead and lag-lead controller, as shown in Figure 16. The figure is plotted for output voltage and load current as a function of time. The output voltage is 260 V for the input voltage of 110 V, and the duty ratio evaluated by the controller is 0.71. The load current obtained is 1.9 A. At time t = 1 s, the input voltage is increased to 120 V, the output voltage is maintained as the reference value of 260 V. At t = 1.6 s, the input voltage is changed from 120 V to 110 V, and the corresponding output is 260 V. The output voltage and load current with integral lead controller is more oscillatory than the integral lag-lead controller. For perturbation in input, the output voltage takes 160 ms to settle at its steady state for integral lead controller, whereas the settling time is 60 ms for integral lag-lead controller. The overshoot of 60/260 = 23% and 17/260 = 6.61% are observed for integral lead and integral lag-lead controller, respectively. The steady state error is negligible in both cases.

Sudden change in reference voltage

The steady state performance is analyzed for varying reference voltage, as shown in Figure 17. At time t = 1 s, the reference voltage is increased to 260 V from 240 V for the constant input voltage of 120 V. The converter output voltage tracks the reference voltage with negligible overshoot and steady-state error. The duty ratio varies from 0.667 to 0.686. The load current varies from 2.39 A to 2.61 A. At time t = 1.6 s, the reference voltage is changed from 260 V to 240 V, and the converter fol-

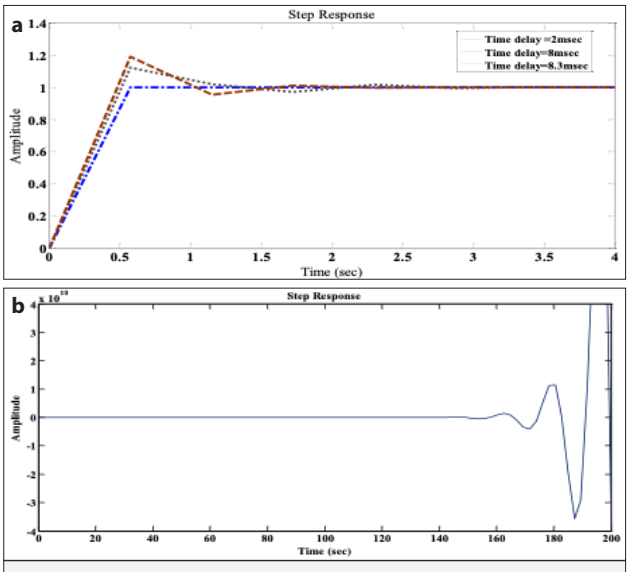

Figure 15. a, b. Step response of the converter with time delay (a) time delay = 2 ms, 8 ms, and 8.3 ms (b) time delay = 8.8 ms

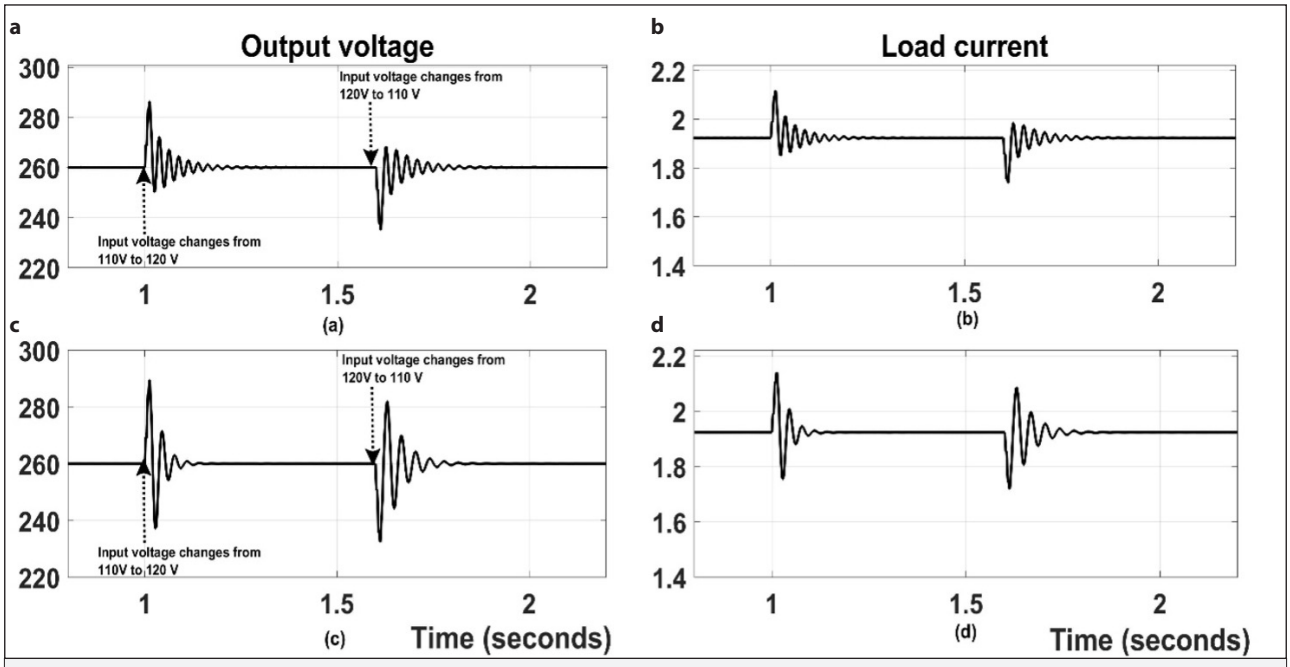

Figure 16. a-d. Simulated response of sudden change in input voltage -POLC (a), (b)-output voltage and load current - integral lead controller (c), (d) output voltage and load current - integral lag-lead controller

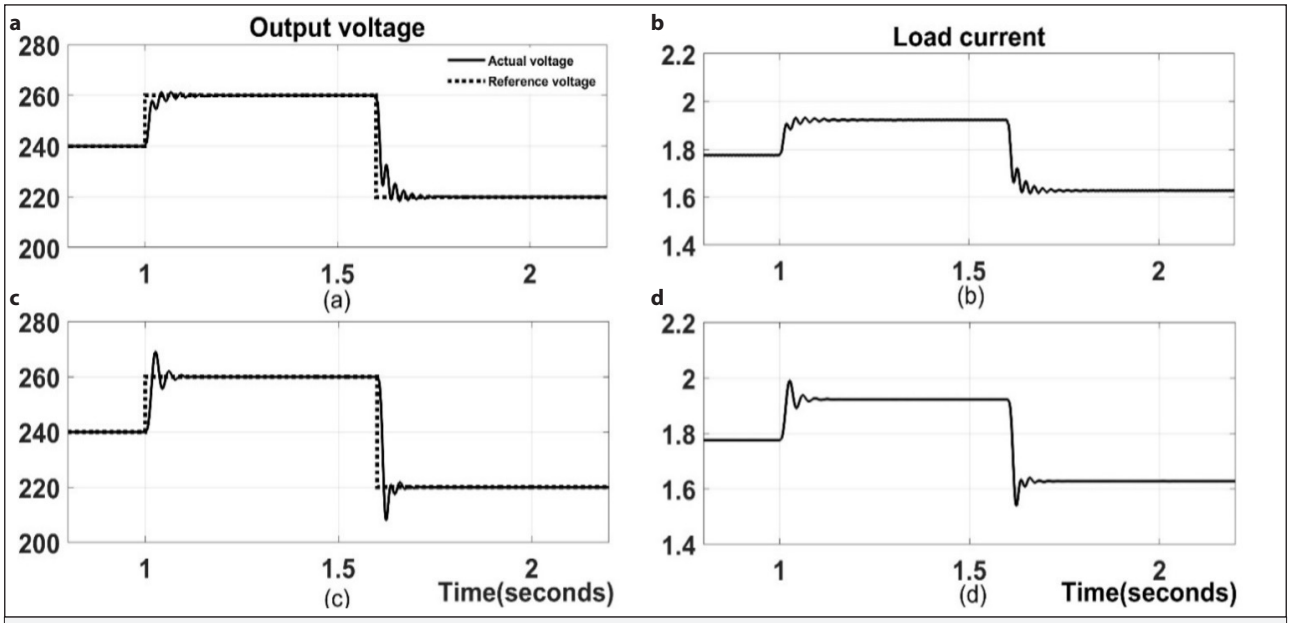

Figure 17. a-d. Sudden change in reference voltage -(a), (b) output voltage and load current - integral lead controller (c), (d) output voltage and load current - integral lag-lead controller

lows the reference value. After perturbation in reference, the voltage and load current response of integral lead controller is overdamped and it takes 160 ms to settle at its reference value. The voltage and load current response with integral lag-lead controller is underdamped and it takes 50 ms to settle at its reference value. On comparing the responses, the response of POLC with the integral lag-lead controller is faster than that with the integral lead controller.

Sudden change in load resistance

The performance of the converter is analyzed for varying load resistance by keeping the reference voltage as 260 V and the input voltage as 120 V, as shown in Figure 18. Initially, the load resistance value is 135.2 Ω.

At time t = 1 s, the load resistance value is changed to 104 Ω, and at time t = 1.6 s, the load resistance is changed to 135.2 Ω

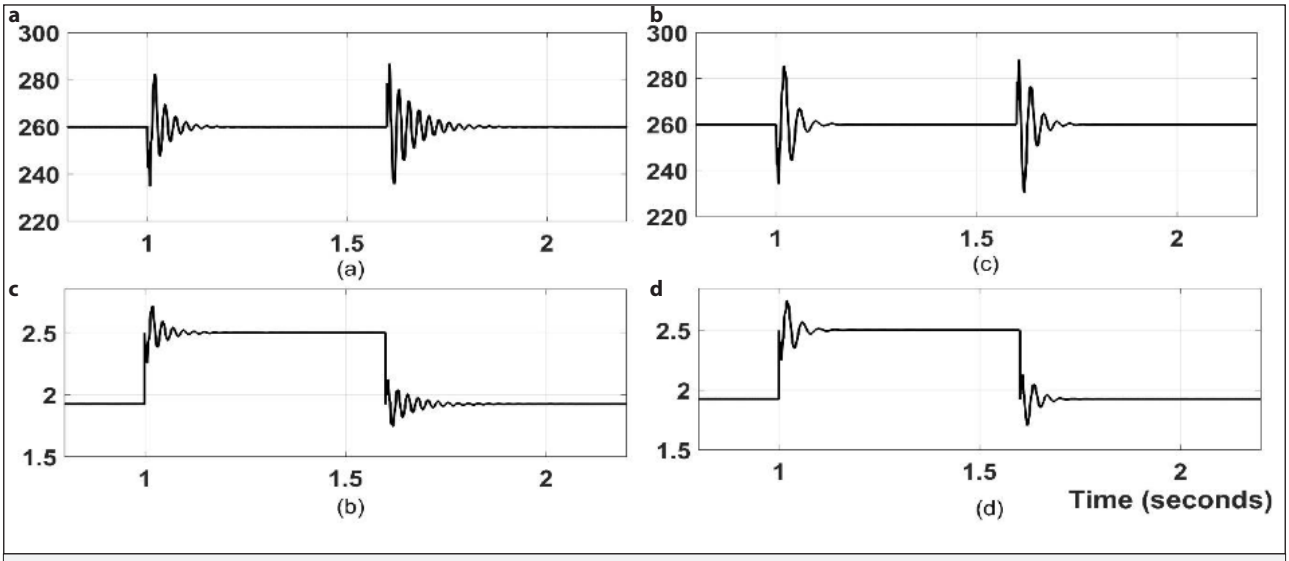

Figure 18. a-d. Simulated response of sudden change in load resistance -(a), (b) – output voltage and load current - integral lead controller (c),(d) output voltage and load current - integral lag-lead controller

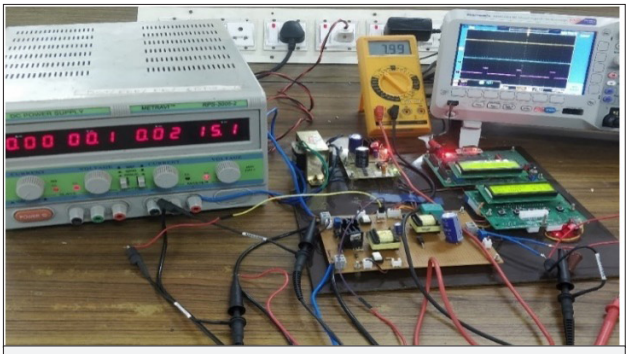

Figure 19. Experimental setup

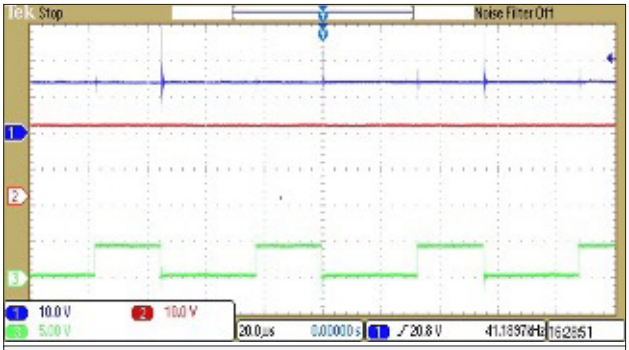

Figure 20. Open loop mode
(x axis: time (20 µs/div), y axis: Channel 1-Input voltage (10 V/div); Channel 2-output voltage (10 V/div); Channel 3-Control pulse 5 V/div)

Table 3. Performance comparison

Parameter	Integral lead controller	Integral lag-lead controller
% Overshoot	24	6.61
Settling time	160 ms	60 ms

again. While reducing the resistance, the load current increases to 2.5 A and the overshoot is observed as 22/260 = 8.46% with negligible steady-state error for both controller design. When the load resistance is increased, the output voltage and load current responses take 220 ms to settle at its reference value for integral lead controller, whereas the settling time of integral lag-lead controller is 120 ms.

On comparing the performances of two controllers, the integral lag-lead controller gives better transient as well as steady-state performance (Table 3). The settling of the output voltage is 600 s to reach its steady-state value of 260 V using the MPPT algorithm is reported in [1].

Experimental Results

A prototype model of POLC was constructed to validate the simulation results. The photograph of the experimental setup is shown in Figure 19.

The power switches were implemented by MOSFET-IRF540, which is driven by gate driver IC-TLP250. The switching frequency is set to 20 KHz. The control algorithm was implemented using dsPIC, and the gate pulses for power switch were produced based on the difference between the reference voltage and actual voltage.

The input voltage could vary from 12 V to 30 V, and the maximum load current (R_L = 135.5 W) was chosen for the controller design. To validate the simulation results, the prototype was implemented. The POLC was tested under open loop mode for the fixed input voltage of 15 V with varying duty ratio. The corresponding output voltage waveforms are shown in Figure 20.

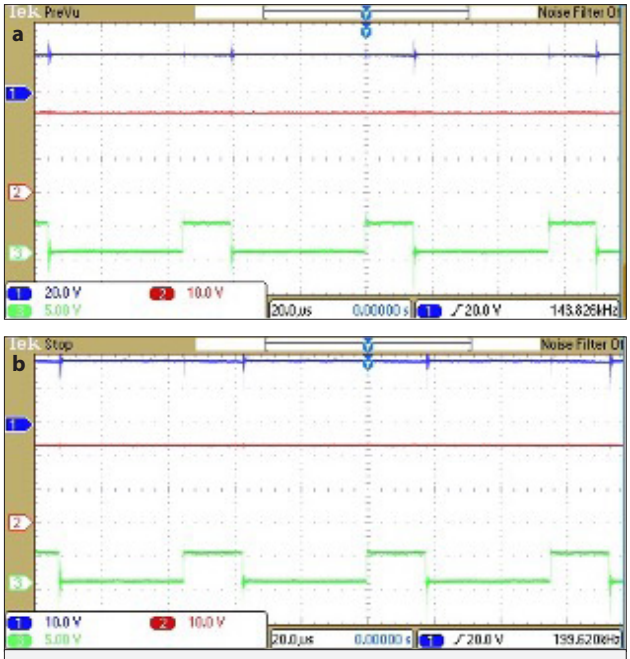

Figure 21. a, b. Closed loop mode (a) duty ratio > 0.5 (b) duty ratio < 0.5
(x axis: time (20 µs/div), y axis: Channel 1-Input voltage (10 V/div) ; Channel 2-output voltage (10 V/div); Channel 3-Control pulse 5 V/div)

The output voltage changed with change in input voltage without controller. By incorporating the controller, the output voltage was maintained as constant at 24 V for variation in input voltage, as shown in Figure 21.

Conclusion

The modeling and analysis of voltage-controlled POLC with closed loop control is presented for different circuit parameters. The transfer functions of the converter are derived in detail (24, 25) using linearized state-space averaging technique. The integral lead controller and lag-lead controller are designed. Time delay analysis is carried out for the proposed controller using Rekasius's substitution and Routh stability criterion. The time delay value is in the order of milliseconds, as the delay is due to the measuring device. The integral lag-lead controller offers good closed loop system dynamics even when perturbations are present in input voltage and load when compared with the integral lead controller (Table 3). Furthermore, a prototype model is developed, and its results are incorporated.

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