Project 14: Capacitive Coupling in 2D Field-Effect Transistors

MNIS – Introduction to Finite Element Modeling

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1 Introduction and Motivation

1.1 Field-Effect Transistors and 2D Materials

The evolution of modern electronics has been driven by the continuous miniaturization of the silicon-based Field-Effect Transistor (FET). However, as device dimensions approach the atomic scale, traditional bulk materials face physical limitations, including short-channel effects and heat dissipation issues. This has spurred intense research into two-dimensional (2D) materials, a new class of crystals that are atomically thin. The most prominent example is graphene, a single layer of carbon atoms arranged in a hexagonal lattice. Due to its exceptional carrier mobility and mechanical strength, graphene is considered a prime candidate for next-generation nano-electronic devices, particularly in the form of Graphene Field-Effect Transistors (GFETs).

In a typical back-gated GFET configuration, the graphene sheet acts as the conductive channel. It rests on a dielectric substrate (commonly silicon dioxide, SiO_2), which covers a conductive bottom gate (typically doped silicon). The current flowing between the source and drain electrodes is modulated by the potential applied to the bottom gate.

Conventionally, the electrostatic coupling in such devices is modeled using the parallel-plate capacitor approximation. In this simplified view, the gate capacitance (C_g) is strictly determined by the thickness (d) and the dielectric constant (ϵ) of the gate oxide separating the channel from the gate:

$$C_{plate} = \frac{\epsilon_0 \epsilon_r A}{d} \tag{1}$$

where A is the area of the channel. This approximation assumes that electric field lines are confined entirely within the dielectric layer between the plates.

1.2 The Role of the Top Dielectric Environment

While the parallel-plate model is sufficient for macroscopic devices, it often fails to capture the complexity of nanoscale 2D devices. Graphene's atomically thin nature means it is extremely sensitive to its surrounding environment.

It has been experimentally observed that placing dielectric materials on top of the graphene channel significantly alters the transport properties of the device. Specifically, GFETs exposed to high-κ top dielectrics exhibit a dramatic increase in drain current and transconductance.

For some time, the prevailing hypothesis in the scientific community was that this performance boost was caused by *dielectric screening*. The theory suggested that the high dielectric constant of the top medium screens the Coulomb potential of charged impurities trapped at the graphene-substrate interface. By reducing the scattering of charge carriers, the carrier mobility (μ) would increase, thereby increasing the current, as described by the fundamental FET equation in the linear regime:

$$I_{ds} \approx \frac{W}{L} \mu C_g (V_g - V_{Dirac}) V_{ds} \tag{2}$$

However, recent studies have challenged this mobility-centric explanation, proposing that the geometry of the electric fields plays a much larger role than previously anticipated.

1.3 Motivation

The motivation for this project is heavily drawn from the work of Xia *et al.*, published in *Nano Letters* (2010), titled "Effect of Top Dielectric Medium on Gate Capacitance of Graphene Field Effect Transistors" [1].

In this paper, the authors investigated the transport properties of back-gated graphene FETs when exposed to different top dielectric media, specifically focusing on water droplets. They observed that the gate efficiency increased by up to two orders of magnitude in the presence of a top dielectric. Crucially, through Hall effect measurements, they were able to decouple the carrier concentration (n) from the mobility (μ).

Their findings contradicted the dielectric screening hypothesis. The experimental data showed that the carrier mobility of the graphene did not change significantly when the top dielectric was added. Instead, the massive increase in current was attributed to a dramatic enhancement of the back-gate capacitance (C_g).

Xia *et al.* argued that the parallel-plate capacitor model is invalid for open-top GFET structures. Because graphene is a "surface-only" material, the electric field lines from the back gate are not confined to the SiO_2 layer. Instead, fringe fields extend out from the gate, loop through the top dielectric medium, and terminate on the graphene channel. When a high-κ material (like water) is placed on top, it facilitates these fringe fields, effectively increasing the total capacitive coupling between the back gate and the channel, even though the physical geometry of the gate oxide has not changed.

2 Project Objectives

The primary objective of this project is to verify the hypothesis presented by Xia *et al.* using Finite Element Modeling (FEM). While the parallel-plate approximation suggests that materials placed *outside* the capacitor plates should not affect the capacitance, electrostatic theory regarding fringe fields suggests otherwise.

In this project, we will build a 3D electrostatic model of a graphene FET to investigate the capacitive coupling. The specific goals are as follows:

1. **Baseline Simulation:** We will construct a simple model of a graphene flake on a SiO_2/Si substrate to calculate the capacitance . This will serve as a benchmark to compare against the theoretical parallel-plate approximation.

2. **Dielectric Influence:** We will introduce various dielectric layers (HfO_2, Al_2O_3, Si_3N_4) on top of the graphene channel. We will quantify how the presence of these top dielectrics alters the capacitance between the graphene and the "bottom" gate. This will allow us to test if the presence of a top dielectric can indeed increase the back-gate capacitance as predicted by Xia *et al.*

3. **Top-Gate and Geometry Effects:** We will further expand the model to include a realistic top-gate electrode geometry, including leads and bonding pads at floating potentials. This step is crucial for understanding how experimental setups and metallic contacts contribute to the total parasitic capacitance of the device.

By performing these simulations, we aim to confirm whether the enhancement of GFET performance in dielectric environments is a result of fringe-field capacitance scaling, rather than an intrinsic improvement in material mobility.

3 Modeling Strategy and Simulation Setup

Geometry and Dimensions

The model consists of a silicon substrate (Ground), a silicon dioxide (SiO_2) dielectric layer, a single-layer graphene flake, and subsequent top-layers.

Table 1: Geometric and Material Parameters

Component	**Material**	**Dimensions ($L \times W \times H$)**	**Permittivity (ϵ_r)**
Substrate (Bottom Gate)	Si modelled as Copper	$50\mu m \times 50\mu m \times 500nm$	conductive (Ground)
Bottom Oxide	SiO_2	$50\mu m \times 50\mu m \times 300nm$	4.2
Graphene Flake	copper(Conductive Layer)	$1\mu m \times 1\mu m \times 6nm^*$	Conductive
Top Dielectric	Al_2O_3 / High-κ	$50\mu m \times 50\mu m \times 30nm$	5.7
Top Gate (Lead)	Copper	$10\mu m \times 1\mu m \times 30nm$	Conductive
Top Gate (Pad)	Copper	$20\mu m \times 20\mu m \times 30nm$	Conductive

* Modeled as a thin 3D block for mesh stability.

Boundary Conditions

- **Ground:** Applied to the entire substrate domain to make bottom gate ($V = 0$).
- **Terminal (Voltage):** Applied to the Graphene domain ($V = 1$V) to measure capacitance via global evaluation.
- **Terminal (Charge):** Applied to the Top Gate ($Q = 0$) to simulate a Floating Potential. This mathematically implements the two necessary physical constraints for an isolated conductor:
  1. **Equipotential Constraint:** The terminal condition enforces a constant electric potential V_{float} across the entire metal domain ($\nabla V = 0$ inside the domain).
  2. **Charge Conservation:** Setting $Q_0 = 0$ enforces Gauss's Law such that the net induced charge on the surface is zero:

$$\oint_{\partial\Omega} \mathbf{D} \cdot \mathbf{n}\, dA = 0 \tag{3}$$

  By satisfying these conditions, the solver automatically determines the unique floating potential V_{float} induced by the capacitive coupling from the graphene channel.
- **Surrounding Environment:** The model was enclosed in a large air sphere to approximate free-space conditions and ensure electrostatic isolation.

Question 1

Calculate the capacitance in the simplest case, with no dielectric or top gate electrode covering graphene.

Ans. $\mathbf{2.3334 \times 10^{-16}\,F}$

Approach

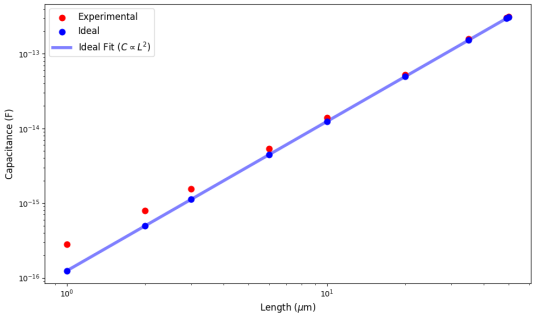
We modeled the GFET using a copper bottom gate ($50\,\mu\text{m} \times 50\,\mu\text{m}$) and a 300 nm SiO_2 substrate. To validate the FEM setup, we first simulated a standard parallel-plate capacitor with a matching $50\,\mu$m top electrode, confirming that the results aligned with the ideal formula ($C = \epsilon A/d$). Next, to characterize fringe effects, we progressively reduced the top electrode area to $1\,\mu\text{m} \times 1\,\mu$m. As the electrode size decreased, the simulated capacitance deviated significantly from the ideal parallel-plate approximation due to the increasing dominance of fringing fields at the edges. Finally, to define the graphene channel, we reduced the top electrode thickness. Because meshing the theoretical graphene thickness of 0.34 nm creates an unmanageable aspect ratio, we approximated the layer as a **6 nm** thick copper film. Since 6 nm $\ll$ 300 nm (the oxide thickness and the bottom gate thickness), this layer effectively behaves as a 2D equipotential surface while ensuring mesh convergence.

Observations

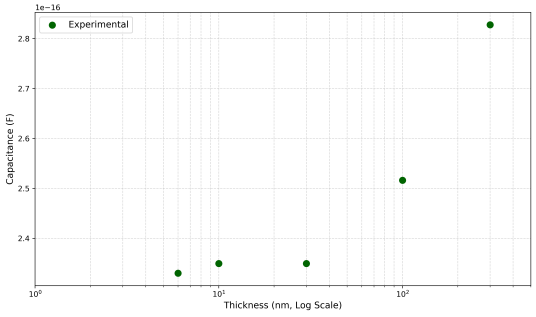
Initially, assuming a symmetric parallel-plate capacitor and introducing a dielectric yields results close to the ideal case. The theoretical capacitances are 7.37×10^{-14} F and 3.096×10^{-13} F, while the simulated values are 7.644×10^{-14} F and 3.12×10^{-13} F.

Fringe Effects

As we decrease the area of the top electrode (graphene), we observe that for $A \gg d^2$, i.e., at $50\,\mu\text{m} \times 50\,\mu$m, the simulated capacitance is close to the ideal value. As the area decreases, fringe effects become more prominent, with the final reading at 2.828×10^{-16} F instead of the ideal 1.24×10^{-16} F, a twofold change. This suggests that fringe effects are significant and the ideal parallel-plate capacitance equation is not reliable at this scale. The plot of capacitance versus length is shown in Figure 1a.



(a) Capacitance versus length of the top electrode

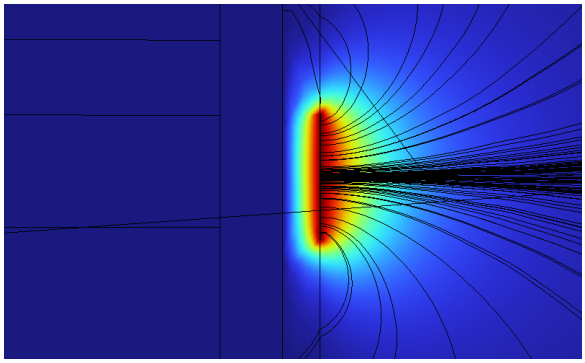


(b) Capacitance versus thickness of Graphene layer

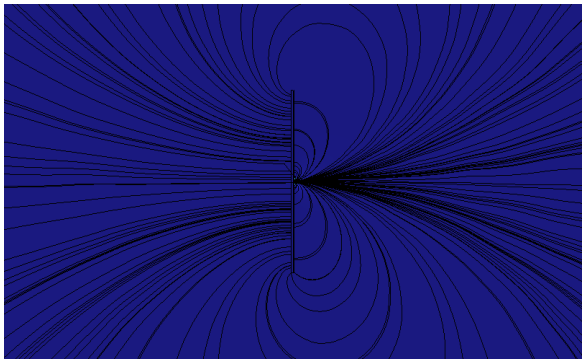
Effect of thickness of Graphene

As the thickness decreases from 300 nm to 0.34 nm, the capacitance should ideally remain constant, since under ideal conditions it is independent of thickness. In practice, we observe variations in capacitance for larger thicknesses, while it stabilizes for smaller thicknesses, as shown in Figure 1b. In practice, we observe below 6 nm, COMSOL produces meshing errors. Since the capacitance plot is stable at 6 nm, we adopt this thickness for the layer in all subsequent simulations.

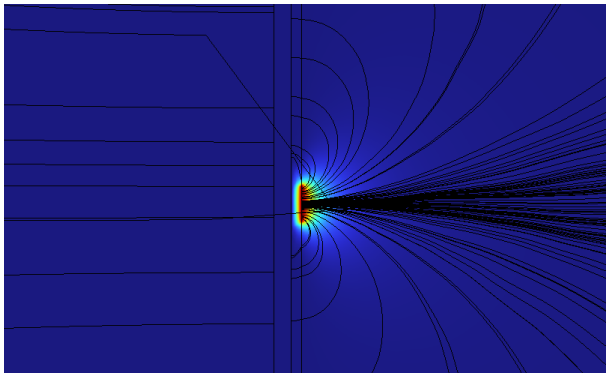
Figures



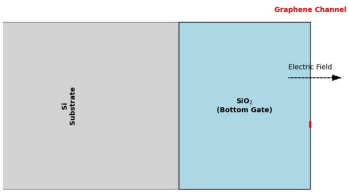
(a) Zoomed-in view showing the thin graphene layer



(b) Visualization of fringe effects around the electrode



(c) Full capacitor setup showing potential concentrated near the graphene



(d) Schematic

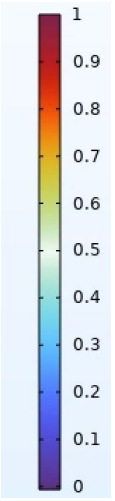


Figure 2: Electric potential distribution of the simple capacitor (Q1).

Conclusion and Learnings

1. Fringe effects become significant in capacitors with small electrode areas.
2. Modeling thin 2D structures in COMSOL is challenging, as small thickness relative to lateral dimensions can lead to meshing difficulties.
3. The measured capacitance is $\mathbf{2.3334 \times 10^{-16}\,F}$, which deviates from the ideal value of $1.15 \times 10^{-16}\,\mathrm{F}$ due to the effects described above.

Question 2

Add a 30nm thick layer of HfO_2, Al_2O_3 or Si_3N_4 on top of the entire model. What is the capacitance between graphene and the bottom gate now?

Ans. $\mathbf{3.3710 \times 10^{-16}\,F}$

Approach

Add a Al_2O_3 block in COMSOL, with dimenesions $50\mu m \times 50\mu m$ and thickness 30nm on top of the Graphene layer. Compare it with no-dielectric case. Change the material (and thus the dielectric constant) and see the change in capacitance.

Observations

The capacitance increases from $2.33 \times 10^{-16}\,\mathrm{F}$ to $3.37 \times 10^{-16}\,\mathrm{F}$ upon adding a 30 nm thick layer of Al_2O_3, demonstrating that introducing a dielectric layer on graphene increases the capacitance. The corresponding ratio is

$$\frac{C_{Al_2O_3}}{C_{\text{air}}} = \frac{3.37 \times 10^{-16}\,\mathrm{F}}{2.33 \times 10^{-16}\,\mathrm{F}} \approx 1.45.$$

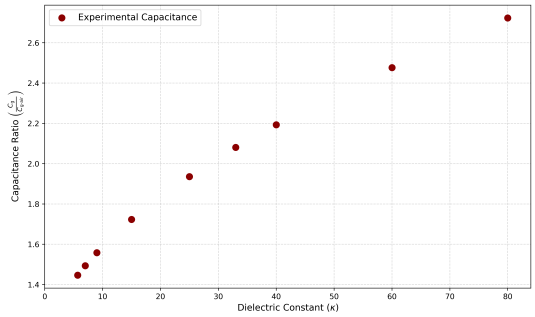
In COMSOL, the default dielectric constant for Al_2O_3 is 5.7. We varied the dielectric constant while keeping other dimensions and properties fixed to study its effect, as shown in Figure 3a. While the trend is consistent, the absolute values are lower compared to Figure (a) on Page 10 of the supplement for the $\frac{C_{\text{g}}}{C_{\text{g-air}}}$ scale, suggesting a missing factor. This discrepancy is likely due to the difference in dielectric thickness.
From Figure (b) on Page 10 of the supplement, two observations can be made:

1. The dielectric thickness affects capacitance and the ratio $\frac{C_{\text{g}}}{C_{\text{g-air}}}$ for lengths greater than $10\,\mu$m.

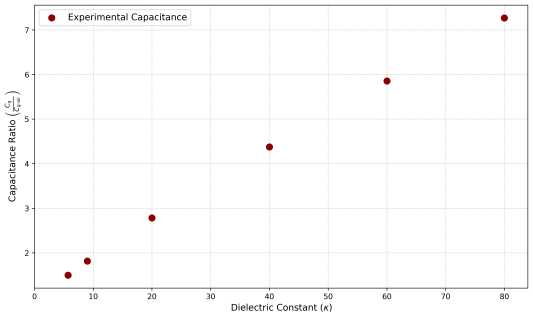
2. The thickness of the dielectric considered in the supplement is of the order of $1\,\mu$m.

3. Thinner dielectric layers result in lower capacitance and a smaller ratio $\frac{C_{\text{g}}}{C_{\text{g-air}}}$.

Since our dielectric layer is only 30 nm thick, much smaller than $1\,\mu$m, the resulting capacitance ratio is correspondingly lower.
When the thickness was increased to $1\,\mu$m, we obtained a capacitance of $16.93 \times 10^{-16}\,\mathrm{F}$ at $\kappa = 80$, corresponding to a ratio of 7.27, which is closer to the value of 8.2 shown in the reference figure. Since the exact dielectric thickness used in the reference was not specified, an exact quantitative match could not be achieved. We also observed that at a thickness of $1\,\mu$m, the dependence of capacitance on the dielectric constant becomes more linear and less parabolic, as shown in Figure 3b.



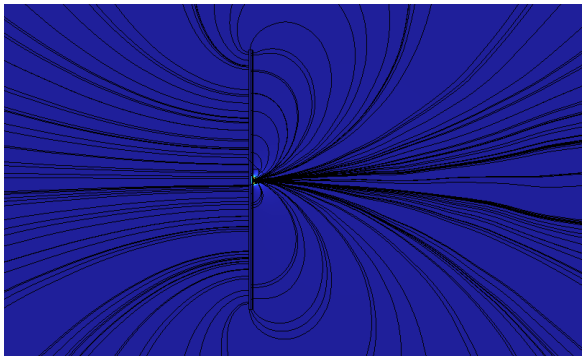
(a) 30 nm thickness



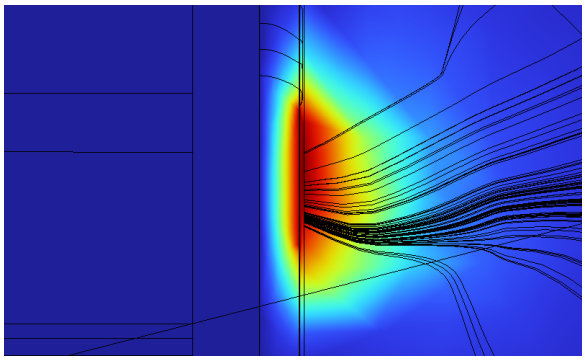
(b) 1 μm thickness

Figure 3: Capacitance ratio $\left(\frac{C_{\text{g}}}{C_{\text{g-air}}}\right)$ as a function of dielectric constant κ. Increasing the dielectric constant results in higher capacitance.

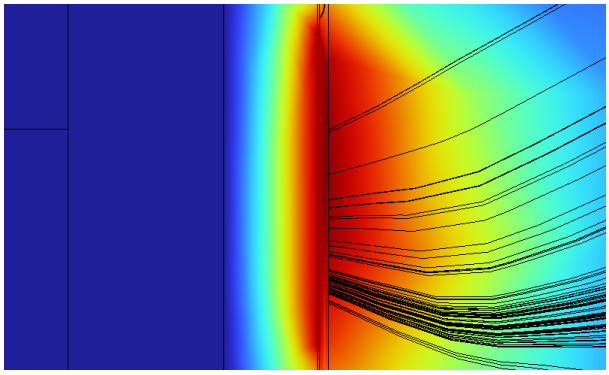
Figures



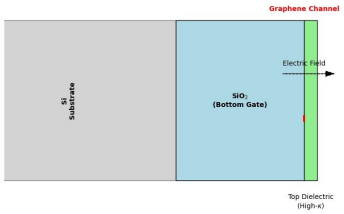
(a) Complete capacitor geometry illustrating the presence of fringe electric fields.



(b) Modification of the electric potential distribution near the graphene electrode due to the dielectric layer.



(c) Magnified view highlighting the electric field distribution within the capacitor structure.



(d) Schematic

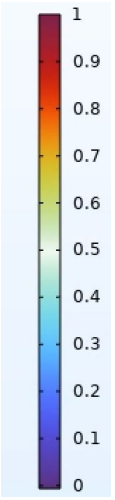


Figure 4: Electric potential distribution of the capacitor incorporating a dielectric layer (Q2).

Conclusion and Learnings

1. Introducing a dielectric layer on Graphene leads to a measurable increase in capacitance.
2. The capacitance increases with the dielectric constant κ. For sufficiently thick dielectric layers, this dependence is approximately linear.

3. For thin dielectric layers (e.g., 30 nm), the dependence of capacitance on κ deviates from linearity and exhibits a slightly parabolic trend.

4. The thickness of the dielectric layer plays a critical role in determining the overall capacitance. Increasing the dielectric thickness results in higher capacitance and a larger ratio $\frac{C_{\text{g}}}{C_{\text{g-air}}}$, particularly for larger lateral dimensions of the capacitor.

Question 3

Add a top-gate electrode on top of the dielectric added in 2. The electrode should cover the entire graphene flake and have an approximate shape like in the figure, part c. The lead part should be cca 1μm wide and 10μm long. The bonding pad should be a square with dimensions of 20μm $\times$ 20μm. Assume that the top gate is at a floating potential. What is the capacitance between graphene and the bottom gate now?

Ans. $\mathbf{2.020 \times 10^{-15}\,F}$

Approach

Two copper blocks were added in COMSOL above the top dielectric, with dimensions of $20\,\mu\text{m} \times 20\,\mu\text{m}$ (pad) and $10\,\mu\text{m} \times 1\,\mu\text{m}$ (lead), each having a thickness of 30 nm. All surfaces of the dielectric were then selected and assigned a floating potential.

Observation

We observe a significant increase in the measured capacitance value, now at $C_{\text{total-experimental}} = 2.020 \times 10^{-15}\,\text{F}$. This value is approximately 8.67 times greater than the previously measured capacitance.

Furthermore, we see in Figure 5c that there is another straight potential gradient, similar to the one observed for the bottom capacitor. This visual evidence suggests the presence of an **additional capacitance** in the measured circuit.

Understanding the Capacitance Increase

To account for this large jump, we must consider all possible capacitance components in the device structure:

1. $C_{\textbf{bottom}}$ **(Oxide Capacitance):** The capacitance between the Graphene and the Grounded Substrate (through 300 nm SiO_2).

2. $C_{\textbf{top}}$ **(Top Dielectric Capacitance):** The capacitance between the Graphene and the Metal Top Gate (through 30 nm High-k dielectric).

3. $C_{\textbf{pad}}$ **(Pad Capacitance):** The stray capacitance from the Metal Top Gate to the Ground.

Equivalent Circuit Model

The Graphene layer is connected to two paths leading to AC ground:

1. Directly down through the bottom oxide (C_{bottom}).

2. Up to the Top Gate (C_{top}), and then from the Top Gate to Ground (C_{pad}).

Thus, C_{top} and C_{pad} are in series, and this combination is in parallel with C_{bottom}.

The total theoretical capacitance C_{total} is given by:

$$C_{\text{total}} = C_{\text{bottom}} + \left(\frac{1}{C_{\text{top}}} + \frac{1}{C_{\text{pad}}} \right)^{-1}$$

Since the Top Gate contact pad is huge ($20 \times 20\,\mu\text{m}$), C_{pad} is relatively large ($C_{\text{pad}} \gg C_{\text{top}}$). This large capacitance effectively anchors the Top Gate to AC ground.

Therefore, the total capacitance can be approximated as:

$$C_{\text{total}} \approx C_{\text{bottom}} + C_{\text{top}}$$

Rough Calculation and Verification

We use the experimental value for C_{bottom} (including fringing) from Q1: $C_{\text{bottom}} = 2.83 \times 10^{-16}\,\text{F}$.

The theoretical value of C_{top} (ideal parallel-plate) is:

$$\begin{aligned} C_{\text{top-ideal}} &= \frac{A\epsilon_r\epsilon_0}{d} \\ &= \frac{(1 \times 10^{-6}\,\text{m})^2 \times 5.7 \times 8.85 \times 10^{-12}\,\text{F/m}}{30 \times 10^{-9}\,\text{m}} \\ &= 1.6815 \times 10^{-15}\,\text{F} \end{aligned}$$

Since C_{top} has ten times less distance for the same area, its fringe effects are negligible compared to C_{bottom}.

The total calculated capacitance is:

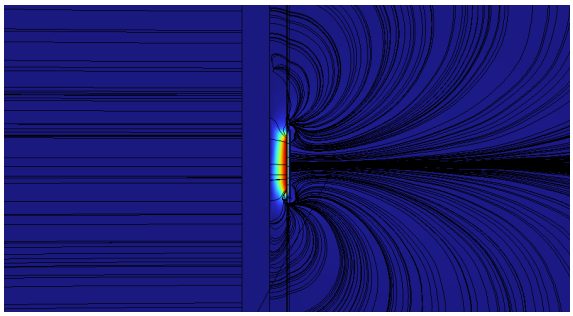
$$\begin{aligned} C_{\text{total-theory}} &\approx C_{\text{bottom}} + C_{\text{top-ideal}} \\ &\approx (2.83 \times 10^{-16}\,\text{F}) + (16.815 \times 10^{-16}\,\text{F}) \\ &\approx 19.645 \times 10^{-16}\,\text{F} \\ &\approx 1.965 \times 10^{-15}\,\text{F} \end{aligned}$$

Comparison to Experimental Data

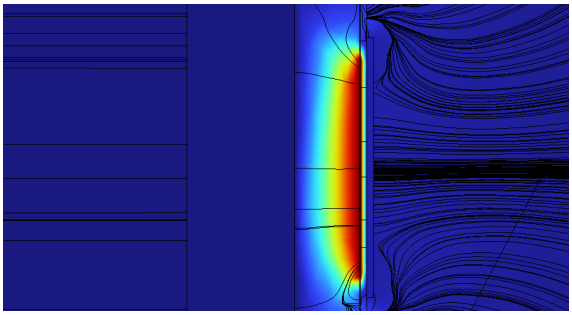
$$\begin{aligned} C_{\text{total-theory}} &= 1.965 \times 10^{-15}\,\text{F} \\ C_{\text{total-experimental}} &= 2.020 \times 10^{-15}\,\text{F} \end{aligned}$$

There is only a 2.7% difference , which is likely due to the neglected fringe effects that slightly increase the capacitance. This confirms the successful measurement of the parallel C_{top}.

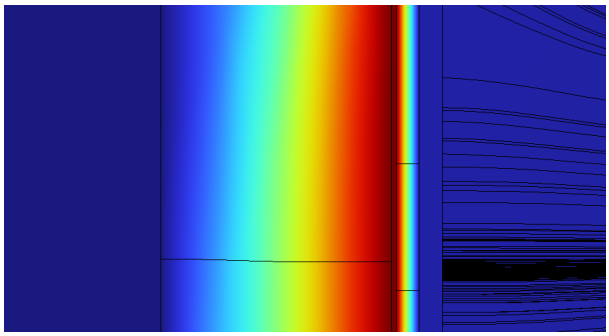
Figures



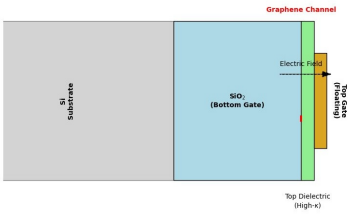
(a) Zoomed-out view with electric field s



(b) Midway zoom



(c) Zoomed-in view shows two straight potential gradients



(d) Schematic

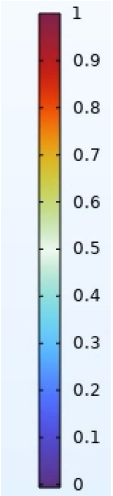


Figure 5: Electric potential distribution of the simple capacitor (Q1).

Conclusion and Learnings

1. **Field Termination:** The conductive Top Gate electrode terminates the upward-directed electric field lines, effectively establishing a second capacitor (C_{top}) in parallel with the bottom oxide.
2. **Parallel Capacitance Dominance:** The total capacitance increased to 2.020×10^{-15} F (8.67× enhancement) due to the dominant top dielectric path. This validates the parallel model $C_{\text{total}} \approx C_{\text{bottom}} + C_{\text{top}}$, where the top gate drives the majority of the coupling.
3. **Physical Confirmation:** The potential gradient exhibits two distinct linear slopes, verifying the formation of parallel top and bottom capacitors ($C_{\text{bottom}} \parallel C_{\text{top}}$) which collectively enhance the total device coupling.
4. **Fringing Fields:** For very thin/short-distance capacitors (C_{top}), the ideal parallel-plate formula is accurate, but for thick/long-distance capacitors (C_{bottom}), fringe effects must be included.

References

[1] J. L. Xia, F. Chen, P. Wiktor, D. K. Ferry, and N. J. Tao, "Effect of Top Dielectric Medium on Gate Capacitance of Graphene Field Effect Transistors: Implications in Mobility Measurements and Sensor Applications," *Nano Letters*, vol. 10, no. 12, pp. 5060–5064, 2010. doi: 10.1021/nl103306a.