MNIS – Introduction to finite element modeling

Project 14: Capacitive coupling in 2D field-effect transistors

Description

Two-dimensional materials are a new class of materials that appear in layers less than 1nm thick. The most well-known example is graphene. 2D materials could be used in a wide variety of applications such as transistors, NEMS, sensors etc. These come most often in the form of field-effect transistors in which the 2D material is used in place of a channel. The channel is capacitively coupled with the bottom-gate (the substrate) via a dielectric film covering the substrate (bottom gate dielectric). In many applications, this capacitive coupling is simply modeled as the one corresponding to a parallel-plate capacitor in which the substrate is one plate and the channel the other one.

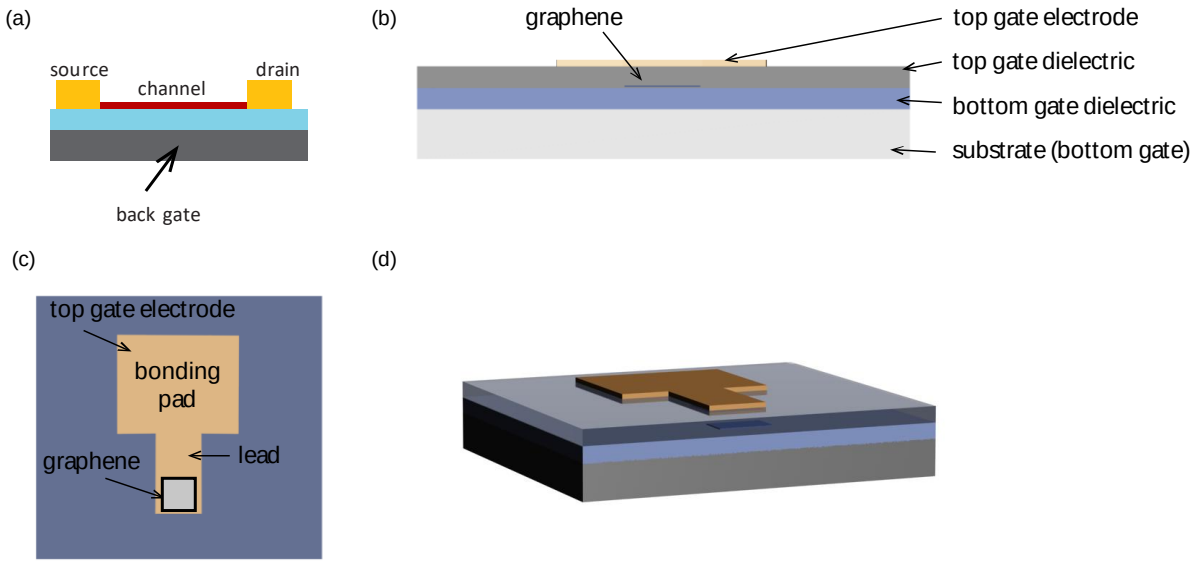


Fig. 1. (a) Simple field-effect transistor geometry with a source, drain, channel and back (bottom) gate. (b) Model to be considered here, with graphene sandwiched between two dielectric layers and covered by a top-gate electrode (side view). (c) Top view of the model. (d) Perspective view of the model.

This approximation is no longer valid when extra materials are placed on top of the channel (see attached paper). Even though these materials are not in the space between the channel and the substrate (bottom gate), their presence can unexpectedly increase the capacitance between the channel and the bottom gate.

Questions

Build a 3D model of a simple capacitor with graphene, modeled as a 0.34 nm thick metal film, 1μm x 1μm in lateral dimensions, sitting on top of a 300nm thick SiO_2 film covering the bottom gate.

1. Calculate the capacitance in the simplest case, with no dielectric or top gate electrode covering graphene
2. Add a 30nm thick layer of HfO_2, Al_2O_3 or Si_3N_4 on top of the entire model. What is the capacitance between graphene and the bottom gate now?
3. Add a top-gate electrode on top of the dielectric added in 2. The electrode should cover the entire graphene flake and have an approximate shape like in the figure, part c. The lead part should be cca 1μm wide and 10μm long. The bonding pad should be a square with dimensions of 20μm x 20μm. Assume that the top gate is at a floating potential. What is the capacitance between graphene and the bottom gate now?

References

1. J.L. Xia, F. Chen, P. Wiktor, D.K. Ferry, and N.J. Tao. Effect of Top Dielectric Medium on Gate Capacitance of Graphene Field Effect Transistors: Implications in Mobility Measurements and Sensor Applications. *Nano Letters* **10**, 5060, 2010. doi: 10.1021/nl103306a

NANO LETTERS

pubs.acs.org/NanoLett

Effect of Top Dielectric Medium on Gate Capacitance of Graphene Field Effect Transistors: Implications in Mobility Measurements and Sensor Applications

J. L. Xia,[†,‡] F. Chen,[†] P. Wiktor,[†] D. K. Ferry,[‡] and N. J. Tao*[,†,‡]

[†]Center for Bioelectronics and Biosensors, Biodesign Institute and [‡]School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ85287

ABSTRACT We have carried out Hall measurement on back-gated graphene field effect transistors (FET) with and without a top dielectric medium. The gate efficiency increases by up to 2 orders of magnitude in the presence of a high κ top dielectric medium, but the mobility does not change significantly. Our measurement further shows that the back-gate capacitance is enhanced dramatically by the top dielectric medium, and the enhancement increases with the size of the top dielectric medium. Our work strongly suggests that the previously reported top dielectric medium-induced charge transport properties of graphene FETs are possibly due to the increase of gate capacitance, rather than enhancement of carrier mobility.

KEYWORDS Graphene, electron transport, dielectric screening, mobility, gate capacitance

Graphene has attracted much attention because of its unique properties for potential high-performance electronics and sensor applications.[1−3] Recent advances have been rapid, for example, graphene field effect transistors (FET) with cutoff frequency up to 100 GHz has been demonstrated,[4] but several issues remain to be addressed before reaching large scale commercial applications.[2] One of the important issues is the large variability in the mobility of graphene FETs. It is believed that charged impurities trapped between graphene and substrate or on the surface of graphene have profound effects on the mobility of graphene, and also on the location and conductivity value of the Dirac Point.[5−8] Many theoretical works have been devoted to determine the relationship between charged impurities and transport properties.[7,9−14] It has been reported that a top dielectric layer can reduce the scattering of carriers by the charged impurities due to screening of the Coulomb potential, and, consequently, significantly increases the graphene mobility.[15] We have also observed large effects of top dielectric media on the current versus gate voltage curves, and attributed the effects to a large enhancement in the mobility.[16,17] However, these conclusions were drawn based on the assumption that the back-gate capacitance is determined by the gate oxide and does not depend on the top dielectric layer. The validity of this assumption was questioned in a footnote by Ponomarenko et al. (ref 18), although no detailed supporting data was provided. Because the back-gate capacitance is critically important for correct interpretation of transport measurements, for understanding the transport mechanism, and for chemical and biosensor applications,[19,20] a systematic study of the effect of top dielectric medium on graphene FET back-gate capacitance is required, which is the goal of the present work.

We performed Hall measurement on graphene FETs in the presence and absence of different top dielectric media. Using a microdroplet method, we were able to determine the back-gate capacitance as a function of the size of the dielectric medium. We observed that adding a top layer dielectric medium dramatically increases the back-gate capacitance, and the increase is proportional to the size, but it has little effect on the mobility of graphene. These findings are further confirmed by numerical modeling of the back-gate capacitance. Our results do not support the assumption of constant back-gate capacitance that led to the conclusion of dielectric enhancement in graphene mobility.[15−17] In addition, our work indicates that one needs to consider both analyte-induced mobility and gate capacitance changes in the chemical and biosensor applications with graphene FETs.[19,20]

We start with a brief clarification of the definition of graphene mobility. Three common methods have been used in literature to extract the mobility of graphene from the transport measurements so far. The first one is to select the linear regime of the transport curve, $\sigma \sim V_g$, and fit it with $\mu = \Delta\sigma/(C_g\Delta V_g)$.[1,5,21,22] This mobility is independent of carrier density, but the selection of linear regime is somewhat arbitrary because the transport curve is nonlinear. The second method is to calculate the mobility with $\mu = \sigma/ne = \sigma/C_g(V_g - V_{dirac})$.[6,18,23,24] In this case, the mobility depends

* To whom correspondence should be addressed.
Received for review: 9/17/2010
Published on Web: 00/00/0000

DOI: 10.1021/nl103306a | *Nano Lett.* **XXXX,** *xxx,* 000–000

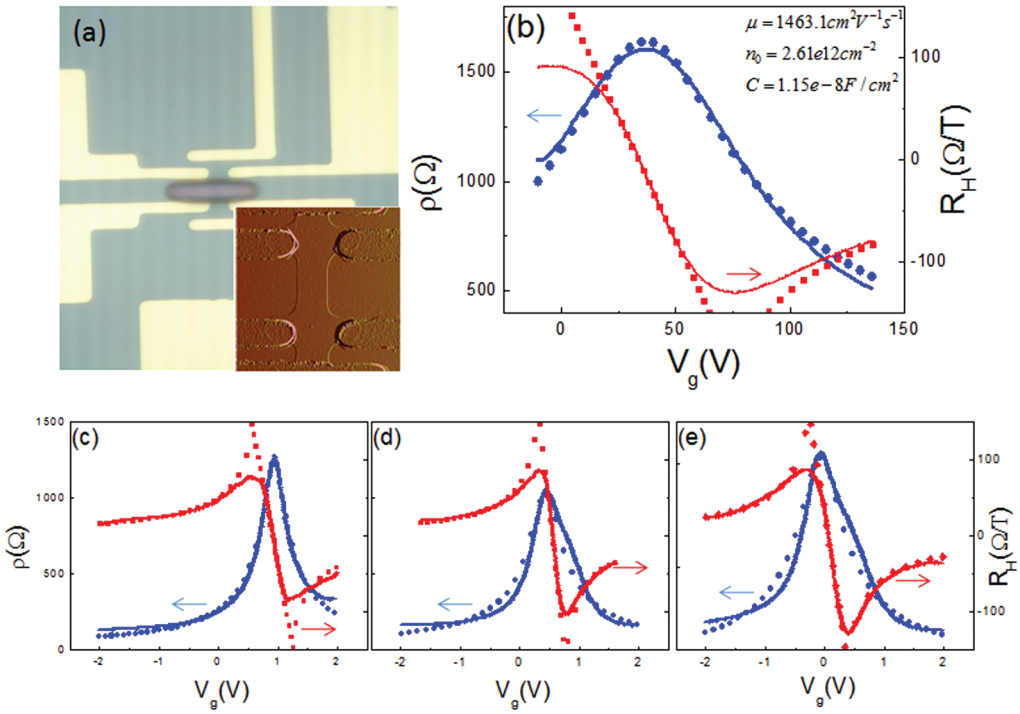


FIGURE 1. Screening effects of top layer dielectric materials on the transport properties of a graphene FET. (a) Optical micrograph of a 6 pin Hall bar graphene FET. The inset is an AFM image of the channel region with channel width of 5 μm. Resistivity (blue curves) and Hall coefficient (red curves) of the graphene FET measured in air (b), 1 mM (c), 100 mM (d), 1 M (e) NaF aqueous solutions, respectively. The symbols are the fittings.

on V_g, or carrier density, because of the nonlinearity of the $\sigma \sim V_g$ curve. Near the Dirac Point (conductivity minimum), σ increases weakly with V_g. This regime has been referred to as the puddle regime, in which the carrier density is not well-defined due to potential fluctuation,[7,25] and the mobility based on the above definition in this regime is meaningless. Moving away from the puddle regime, σ increases rapidly with V_g and the mobility is the highest.[23] Further away from the Dirac Point, it reaches the sublinear regime, where the mobility decreases again due to short-range scattering. The third definition of mobility is based on the following considerations. The total carrier concentration in graphene channel regions is given by $n_{tot} = (n_0^2 + n[V_g]^2)^{1/2}$, so one can obtain the mobility by fitting gate dependent resistance with $R_{tot} = R_{contact} + (L/W)/[(n_0^2 + n[V_g]^2)^{1/2}e\mu]$,[26−28] where n_0 is the carrier density at the conductivity minimum (referred to as residual carrier density[7]), $n[V_g]$ is gated-induced carrier density, R_{tot} and $R_{contact}$ are total resistance and contact resistance, respectively, and L and W are the channel length and width, respectively. Note that the elimination of contact resistance is important to extract meaningful mobility with this approach.[2] In this work, we use the third method to extract graphene FET mobility.

Single layer graphene FETs with Hall bar structure were fabricated using methods described in details elsewhere.[28] Briefly, a graphene piece was prepared on SiO_2 (300 nm)/Si substrate by mechanical exfoliation, and identified by color contrast[29] and Raman spectrum.[30] Cr(5 nm)/Au(80 nm) was used as electrode materials, and all the electrodes were covered by 4.5 μm thick photoresist in order to eliminate leakage current. A narrow window of 4.3 μm wide is opened to expose graphene, as shown in Figure 1a. The inset is an AFM image of the FET channel of 9 μm long and 5 μm wide. Resistivity and Hall coefficient were measured at 0 and 0.5 T at room temperature by applying 1 μA constant current, in air and in 1 mM, 100 mM and 1 M NaF aqueous solutions, respectively (Figure 1b−e). The hall coefficient is fitted by[1]

$$R_H = (n_h\mu_h^2 - n_e\mu_e^2)/e(n_e\mu_e + n_h\mu_h)^2 \quad (1)$$

where n_e and n_h are the carrier densities of electrons and holes, and μ_e and μ_h are the mobilities of electrons and holes, respectively. When one carrier type dominates, $R_H = (1/e)n_{e,h} = 1/C_g(V_g - V_{dirac})$, allowing us to extract the gate capacitance. Also, the resistivity is fitted with the third method[26] mentioned above without including the contact resistance (because of the use of four probe measurement here)

$$\rho = R_{tot}\left(\frac{W}{L}\right) = \frac{1}{\sqrt{n_0^2 + n[V_g]^2}e\mu} \quad (2)$$

DOI: 10.1021/nl103306a | *Nano Lett.* **XXXX,** *xxx,* 000–000

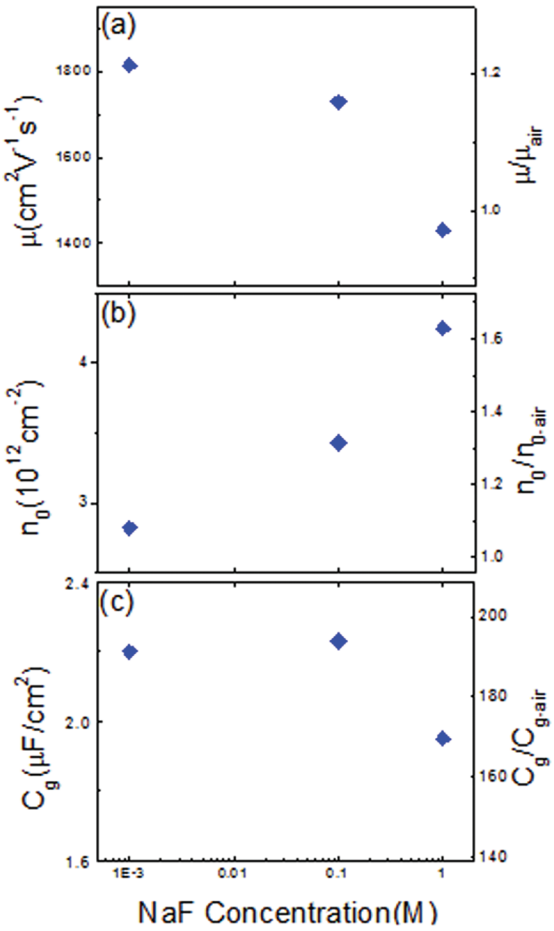


FIGURE 2. Dependence of (a) mobility μ, (b) residual carrier density n_0, and (c) the gate capacitance, C_g of graphene FET on NaF concentration. The data were extracted from the transport and hall measurements (see text for details).

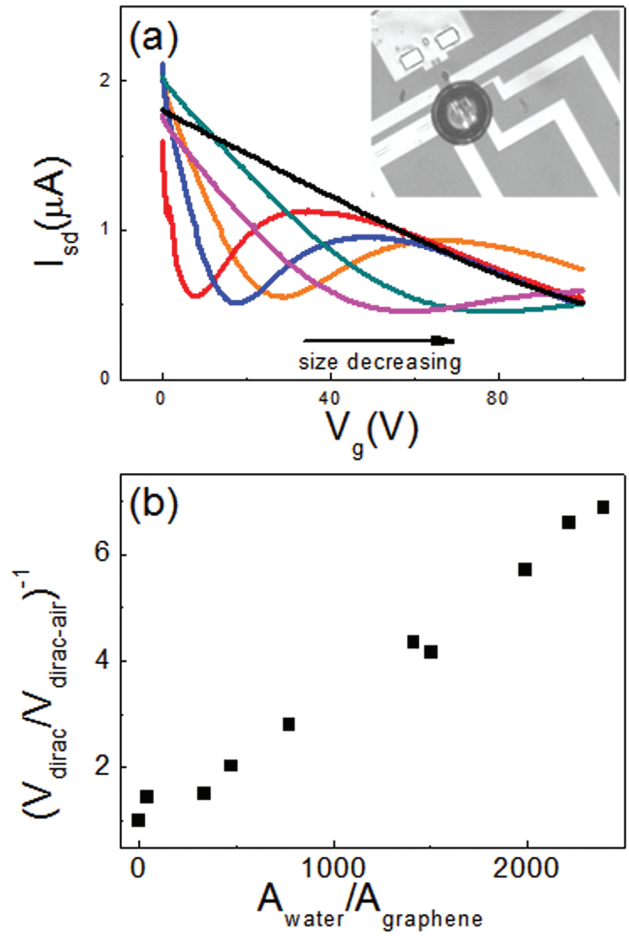


FIGURE 3. Size effect of top dielectric medium. (a) Two-probe transport curves of graphene FET covered by pure water with different sizes with 10 mV source drain bias. The inset is an optical image of measurement configuration. (b) Relative change of Dirac Point as a function of the area ratio of water droplet and graphene channel.

$$n[V_g] = C_g(V_g - V_{dirac})/e \quad (3)$$

μ, n_0, and C_g in each situation were extracted and shown in Figure 2. Exposing the graphene FET to aqueous solutions results in an increase in the mobility by ~20% at 1 mM (Figure 2a). Increasing the ionic concentration leads to a small decrease in the mobility, and this may be attributed to the scattering of carriers by ions adsorbed on graphene. Note this mobility decrease coincides with the increase in the residual carrier density shown in Figure 2b. Adding aqueous solution causes an increase in the gate capacitance by up to 2 orders of magnitude. This capacitance change has a profound effect on the change of transport curves. The gate capacitance does not significantly depend on the ionic concentration (we will return to this later), and it appears to depend on the dielectric constant of the medium.[18] We believe that this top dielectric medium-induced transport characteristic changes in other works[15−17] are also largely due to the gate capacitance.

We have carried out a systematic study of the gate capacitance dependence on the size of the top dielectric medium. To facilitate the study, we used a piezoelectric micropipet that can accurately produce micrometer-scale water droplets on the FET.[31] After placing a droplet on the FET, we controlled the size of the droplet via controlling water evaporation at a desired temperature (e.g., ~1 °C). Figure 3a shows $I_{sd} - V_g$ curves recorded during controlled evaporation (shrinking size) at $V_{SD} = 10$ mV. All the measurements were carried out with the same parameters, including ramping rate and potential windows, to minimize potential-induced effects.[32] When the size of water droplet decreases, the Dirac point shifts toward positive values (Figure 3b). We note that the Dirac point is the potential at which the conductivity is minimum and the gate induced carrier density neutralizes precisely the impurity induced carrier density ($\bar{n}$),[5,7] which is $V_{dirac} = e\bar{n}/C_g$. For different sizes of water droplet, assuming the impurity density does not change, then $\bar{n}$ should not change either. Then the shift in the Dirac point potential must come from the change in the gate capacitance, which increases with the size of water droplet.

DOI: 10.1021/nl103306a | Nano Lett. XXXX, xxx, 000–000

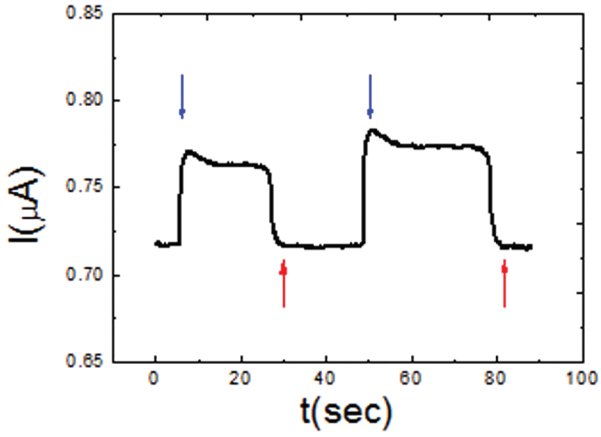


FIGURE 4. Real-time transport current of a graphene FET exposed to a water droplet. Source−drain bias is 10 mV without gate potential. Red and blue arrows indicate water injection and complete evaporation, respectively. Two water droplets of different sizes were studied.

To investigate the cause of this large top dielectric medium-induced change in the gate capacitance, we performed finite element analysis to simulate the gate capacitance of back-gated graphene FET with and without high κmedium. We found that adding water ($\kappa = 80$) induces ~9 times increase in the gate capacitance, which is attributed to the fringe effect (see Supporting Information). However, the experiment found ~200 times enhancement, much larger than the simulation. A possible reason for this discrepancy is that simulation treated graphene as a metal while graphene is a semimetal. A more accurate treatment of graphene requires us to know the dielectric constant of graphene, which is not available. Another possibility is the trapped charges in the substrate or at the water−graphene interface, which also require further studies.

We have also recorded the transport curves of graphene FETs before and after placing a water droplet on top and during the evaporation of the water droplet (Figure 4). Immediately after introducing a water droplet, the source−drain current increases. As the water droplet evaporates, the current decreases, and eventually returns to the original level when the water droplet completely evaporates. The current change depends on the size of the water droplet, which, as we have already shown, is due to gate capacitance change. Vapor sensors based on graphene FETs were demonstrated,[19,20] for water and other molecules detections, and the observed dependence of the transport properties was attributed to charge transfer between graphene and the adsorbed molecules. An alternative explanation is that the adsorbed molecules act as scattering centers to the carriers, which decreases the mobility.[7] The present work shows that adsorbates may also change the transport curve via changing the gate capacitance. This adsorbates induced capacitance change has also been observed in carbon nanotube (CNT),[33] which was attributed to the limited diameter of CNT. For graphene with even thinner thickness, this effect could be more significant.

In conclusion, we have measured gate capacitance and mobility of graphene FET with and without top dielectric medium using Hall measurement. We have found that the gate capacitance can increase by up to 2 orders of magnitude, depending on the size of the top dielectric medium, while the mobility remains nearly constant. We have performed numerical calculations, which support the observation. We have also determined the gate capacitance as a function of the size of the top dielectric medium (water droplet) and observed that the gate capacitance increases with the size. Our work shows that that the previously observed large top dielectric medium effect is large possibly due to the increase in the gate capacitance, rather than enhancement in the graphene mobility. The sensitive dependence of the gate capacitance on the top dielectric medium points to the alternative mechanism of graphene FET-based chemical sensor applications.

Acknowledgment. We thank NSF (CHM-0554786) for support.

Supporting Information Available. Capacitance simulation of back-gated graphene FET and additional figure. This material is available free of charge via the Internet at http://pubs.acs.org.

REFERENCES AND NOTES

(1) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Zhang, Y.; Dubonos, S. V.; Grigorieva, I. V.; Firsov, A. A. *Science* **2004**, *306* (5696), 666–669.
(2) Schwierz, F. *Nat. Nano.* **2010**, *5* (7), 487–496.
(3) Schedin, F.; Geim, A. K.; Morozov, S. V.; Hill, E. W.; Blake, P.; Katsnelson, M. I.; Novoselov, K. S. *Nat. Mater.* **2007**, *6*, 652–655.
(4) Lin, Y.-M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H.-Y.; Grill, A.; Avouris, P. *Science* **2010**, *327* (5966), 662.
(5) Chen, J. H.; Jang, C.; Adam, S.; Fuhrer, M. S.; Williams, E. D.; Ishigami, M. *Nat. Phys.* **2008**, *4*, 377–381.
(6) Tan, Y. W.; Zhang, Y.; Bolotin, K.; Zhao, Y.; Adam, S.; Hwang, E. H.; Das Sarma, S.; Stormer, H. L.; Kim, P. *Phys. Rev. Lett.* **2007**, *99*, 246803.
(7) Adam, S.; Hwang, E. H.; Galitski, V. M.; Das Sarma, S. *Proc. Natl. Acad. Sci. U.S.A.* **2007**, *104*, 18392–18397.
(8) Hwang, E. H.; Adam, S.; Das Sarma, S. *Phys. Rev. Lett.* **2007**, *98*, 186806.
(9) Galitski, V. M.; Adam, S.; Das Sarma, S. *Phys. Rev. B* **2007**, *76*, 245405.
(10) Ando, T. *J. Phys. Soc. Jpn.* **2006**, *75*, No. 074716.
(11) Ghaznavi, M.; Miscaronkovicacute, Z. L.; Goodman, F. O. *Phys. Rev. B* **2010**, *81*, No. 085416.
(12) Fogler, M. M.; Novikov, D. S.; Shklovskii, B. I. *Phys. Rev. B* **2007**, *76*, 233402.
(13) Zhang, L. M.; Fogler, M. M. *Phys. Rev. Lett.* **2008**, *100*, 116804.
(14) Katsnelson, M. I. *Phys. Rev. B* **2006**, *74*, 201401.
(15) Jang, C.; Adam, S.; Chen, J. H.; Williams, D.; Das Sarma, S.; Fuhrer, M. S. *Phys. Rev. Lett.* **2008**, *101*, 146805.
(16) Chen, F.; Xia, J.; Ferry, D. K.; Tao, N. *Nano Lett.* **2009**, *9* (4), 2571–2574.
(17) Chen, F.; Xia, J.; Tao, N. *Nano Lett.* **2009**, *9* (7), 1621–1625.
(18) Ponomarenko, L. A.; Yang, R.; Mohiuddin, T. M.; Katsnelson, M. I.; Novoselov, K. S.; Morozov, S. V.; Zhukov, A. A.; Schedin, F.; Hill, E. W.; Geim, A. K. *Phys. Rev. Lett.* **2009**, *102*, 206603.
(19) Robinson, J. T.; Perkins, F. K.; Snow, E. S.; Wei, Z.; Sheehan, P. E. *Nano Lett.* **2008**, *8* (10), 3137–3140.

DOI: 10.1021/nl103306a | *Nano Lett.* **XXXX,** *xxx,* 000–000

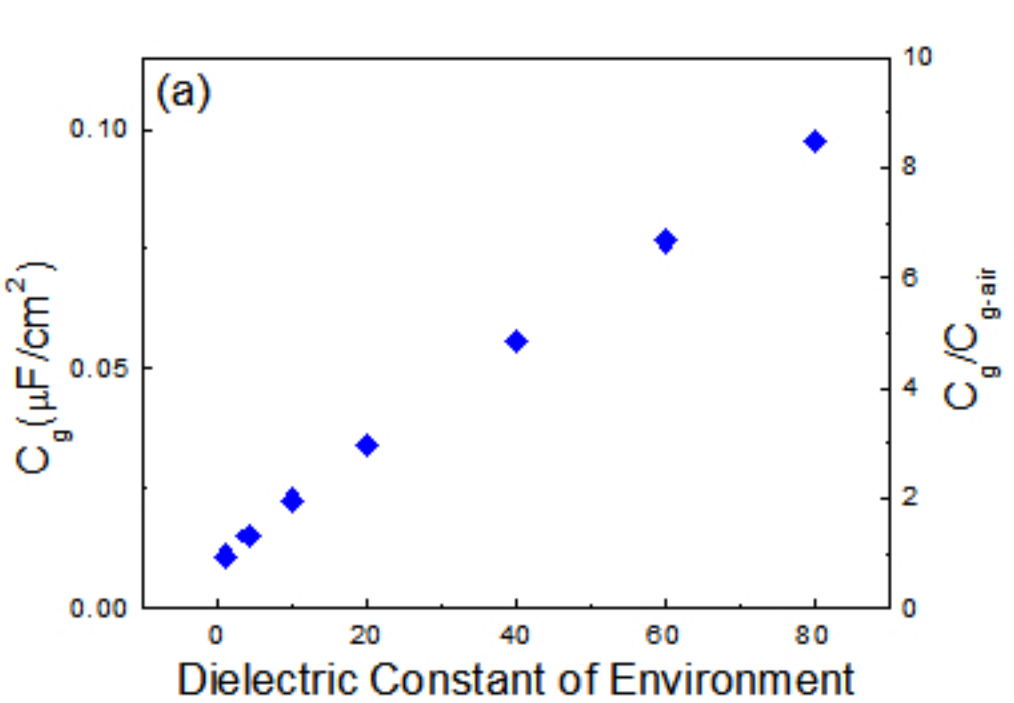
(20) Dan, Y.; Lu, Y.; Kybert, N. J.; Johnson, A. T. *Nano Lett.* **2009**, *9* (4), 1472–1475.
(21) Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. *Nature* **2005**, *438* (7065), 197–200.
(22) Morozov, S. V.; Novoselov, K. S.; Katsnelson, M. I.; Schedin, F.; Elias, D. C.; Jaszczak, J. A.; Geim, A. K. *Phys. Rev. Lett.* **2008**, *100*, No. 016602.
(23) Du, X.; Skachko, I.; Barker, A.; Andrei, E. Y. *Nat. Nanotechnol.* **2008**, *3* (8), 491–495.
(24) Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Klima, M.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. *Solid State Commun.* **2008**, *146* (9−10), 351–355.
(25) Victor, M. G.; Shaffique, A.; Sarma, S. D. *Phys. Rev. B* **2007**, *76*, 245405.
(26) Seyoung, K.; Junghyo, N.; Insun, J.; Davood, S.; Luigi, C.; Zhen, Y.; Emanuel, T.; Sanjay, K. B. *Appl. Phys. Lett.* **2009**, *94*, No. 062107.
(27) Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. *Science* **2009**, *324* (5932), 1312–1314.
(28) Xia, J. L.; Chen, F.; Tedesco, J. L.; Gaskill, D. K.; Myers-Ward, R. L.; Eddy, C. R.; Ferry, D. K.; Tao, N. J. *Appl. Phys. Lett.* **2010**, *96* (16), 162101.
(29) Blake, P.; Hill, E. W.; Neto, A. H. C.; Novoselov, K. S.; Jiang, D.; Yang, R.; Booth, T. J.; Geim, A. K. *Appl. Phys. Lett.* **2007**, *91* (6), No. 063124.
(30) Ferrari, A. C.; Meyer, J. C.; Scardaci, V.; Casiraghi, C.; Lazzeri, M.; Mauri, F.; Piscanec, S.; Jiang, D.; Novoselov, K. S.; Roth, S.; Geim, A. K. *Phys. Rev. Lett.* **2006**, *97*, 187401.
(31) Nagaraj, V. J.; Eaton, S.; Thirstrup, D.; Wiktor, P. *Biochem. Biophys. Res. Commun.* **2005**, *375* (4), 526–530.
(32) Lohmann, T.; von Klitzing, K.; Smet, J. H. *Nano Lett.* **2009**, *9* (5), 1973–1979.
(33) Snow, E. S.; Perkins, F. K.; Houser, E. J.; Badescu, S. C.; Reinecke, T. L. *Science* **2005**, *307* (5717), 1942–1945.

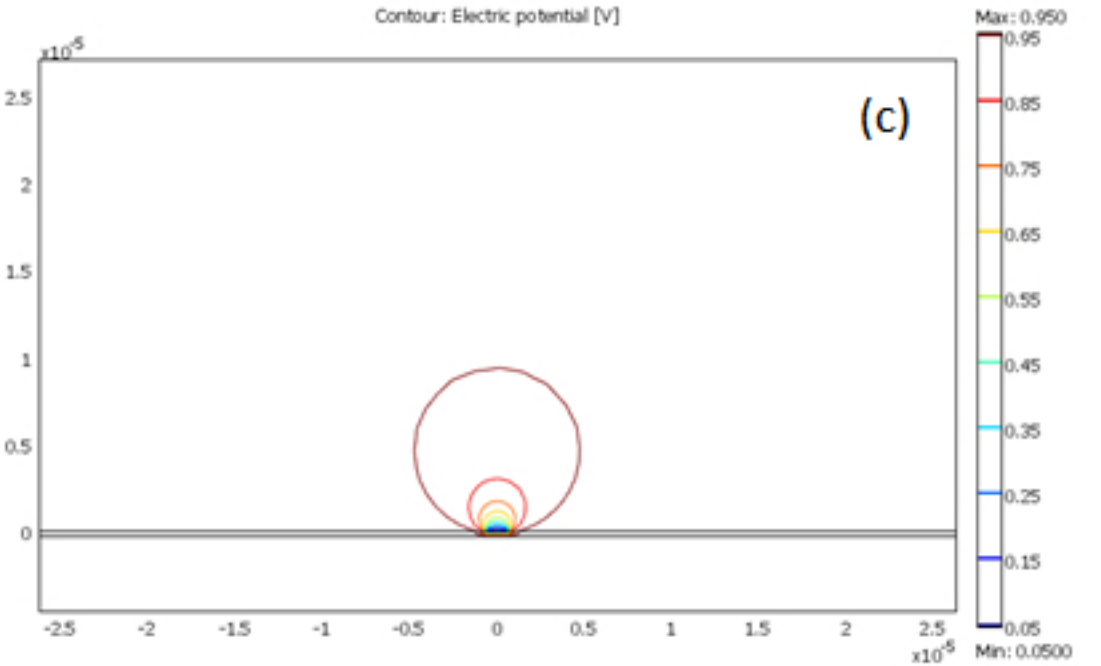
DOI: 10.1021/nl103306a | *Nano Lett.* **XXXX,** *xxx,* 000–000

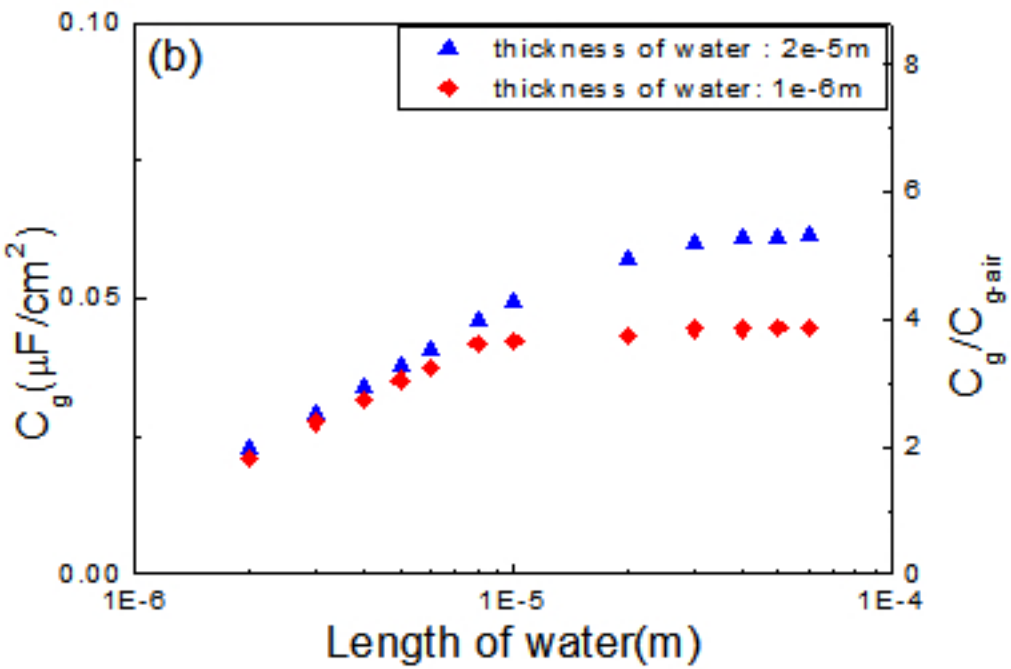
Capacitance Simulation of back gated Graphene FET

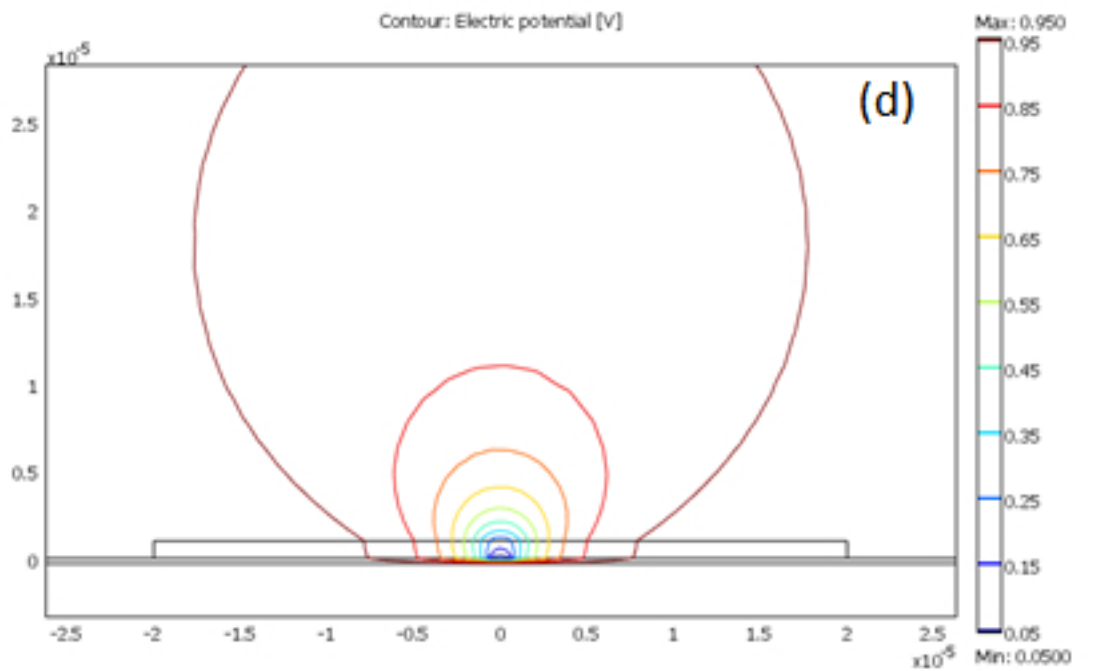
Numerical simulation of gate capacitance using finite element method (FEM) (COMSOL 3.5a AC/DC model) has been carried out. Fig. S1(a) is a 3D simulation, showing the effect of top layer media on the gate capacitance, with different dielectric constant (covering the whole surrounding environment). Note that in the model simulation, the graphene dimensions are 1 μm x 1 μm with thickness of 0.34 nm, and treated as metal. The SiO_2 layer is 300nm with dielectric constant of 3.9 and the top medium has various κ values. The simulation shows that the gate capacitance increases linearly with the dielectric constant of top medium. For $\kappa = 80$ the gate capacitance increases by about 9 times, which is large but smaller than the experimental value (~200 times). This discrepancy could come from the trapped charges in the substrate or at the water-graphene interface due to the electrical field. To illustrate the size effect of water droplet, 2D instead of 3D FEM simulation was carried out due to computational limit. Fig. S1(c) and (d) show the electrostatic field distributions with and without the water droplet. The calculated gate capacitance increases with the size of the water droplet, in agreement with the experimental finding (Fig. S1(b)), it also shows a saturation after certain enhancement.

FIG. S1 Simulations of gate capacitance of graphene FET: (a) 3D simulation of gate capacitance covered by top dielectric media with different dielectric constants. (b) 2D simulation of gate capacitance of a water droplet ($\kappa = 80$) with different sizes. (c) Potential distribution without a water layer. (d) Potential distribution with a water layer($40\mu m \times 6\mu m$). Note that the water layer is simplified as a rectangular shape.


(a)
0.10
0.05
0.00
0
20
40
60
80
10
8
6
4
2
0
C_g (μF/cm^2)
$C_g/C_{g\text{-}air}$
Dielectric Constant of Environment


Contour: Electric potential [V]
(c)
x10^{-5}
2.5
2
1.5
1
0.5
0
-2.5
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2
2.5
x10^{-5}
Max: 0.950
0.95
0.85
0.75
0.65
0.55
0.45
0.35
0.25
0.15
0.05
Min: 0.0500


(b)
thickness of water : 2e-5m
thickness of water: 1e-6m
0.10
0.05
0.00
1E-6
1E-5
1E-4
8
6
4
2
0
C_g (μF/cm^2)
$C_g/C_{g\text{-}air}$
Length of water(m)


Contour: Electric potential [V]
(d)
x10^{-5}
2.5
2
1.5
1
0.5
0
-2.5
-2
-1.5
-1
-0.5
0
0.5
1
1.5
2
2.5
x10^{-5}
Max: 0.950
0.95
0.85
0.75
0.65
0.55
0.45
0.35
0.25
0.15
0.05
Min: 0.0500