Project 14

CAPACITIVE COUPLING IN 2D FIELD-EFFECT TRANSISTORS

EE-536
PHYSICAL MODELS FOR MICRO AND NANOSYSTEMS

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THE PROBLEM & MOTIVATION

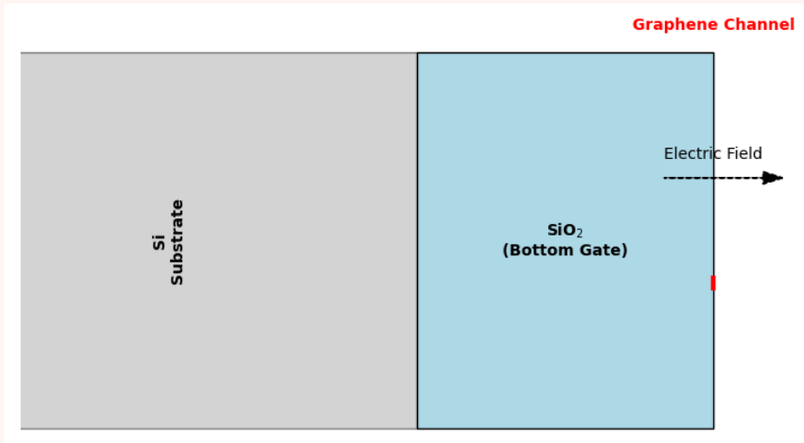
- **Traditional FETs are modeled as simple parallel-plate capacitors**
  - **Assumption:** Electric fields are confined strictly between the plates
- **Graphene is an "open" structure (atomically thin)**
  - **Reality:** Electric fields leak out (Fringe Fields)
- **Researchers found that putting water (or high permittivity dielectrics) on top of Graphene FETs increased current by 100x.**
  - **Hypothesis:** Is it better mobility? Or just higher capacitance?
- **Our Goal:** Use **COMSOL** to prove that capacitance is the driver

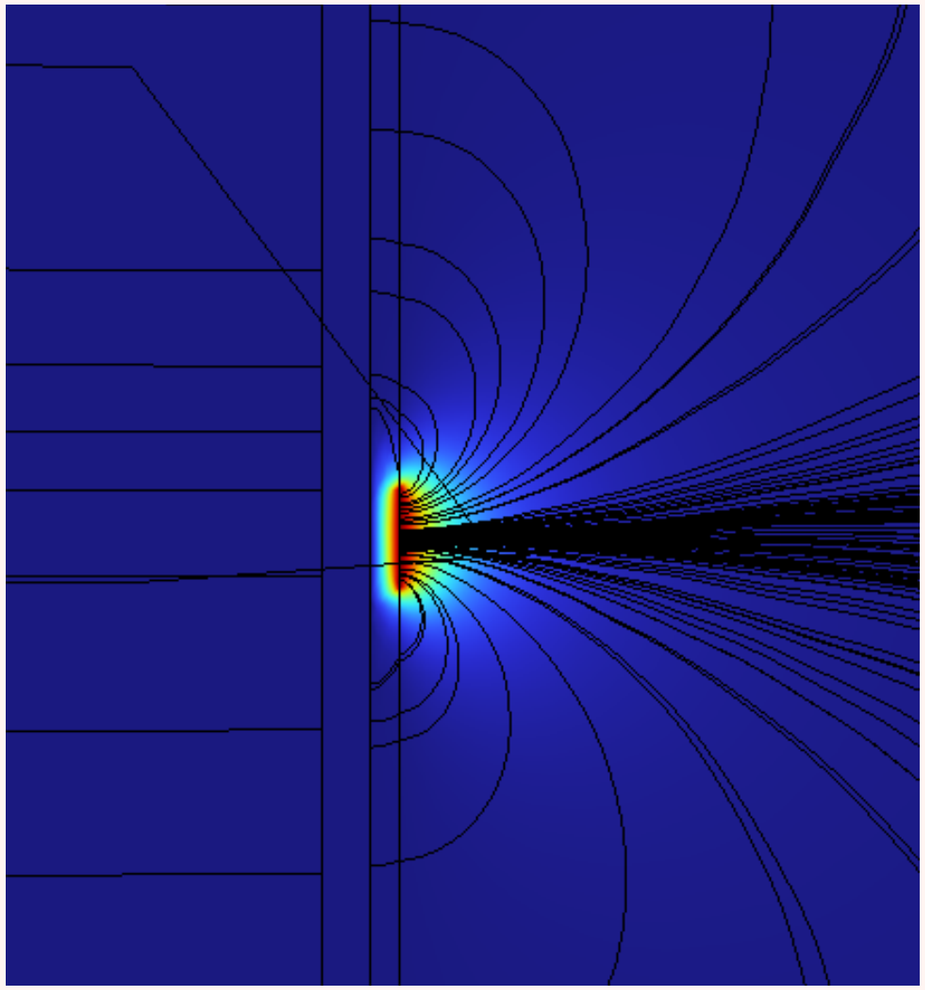
THE SIMULATION CHALLENGE

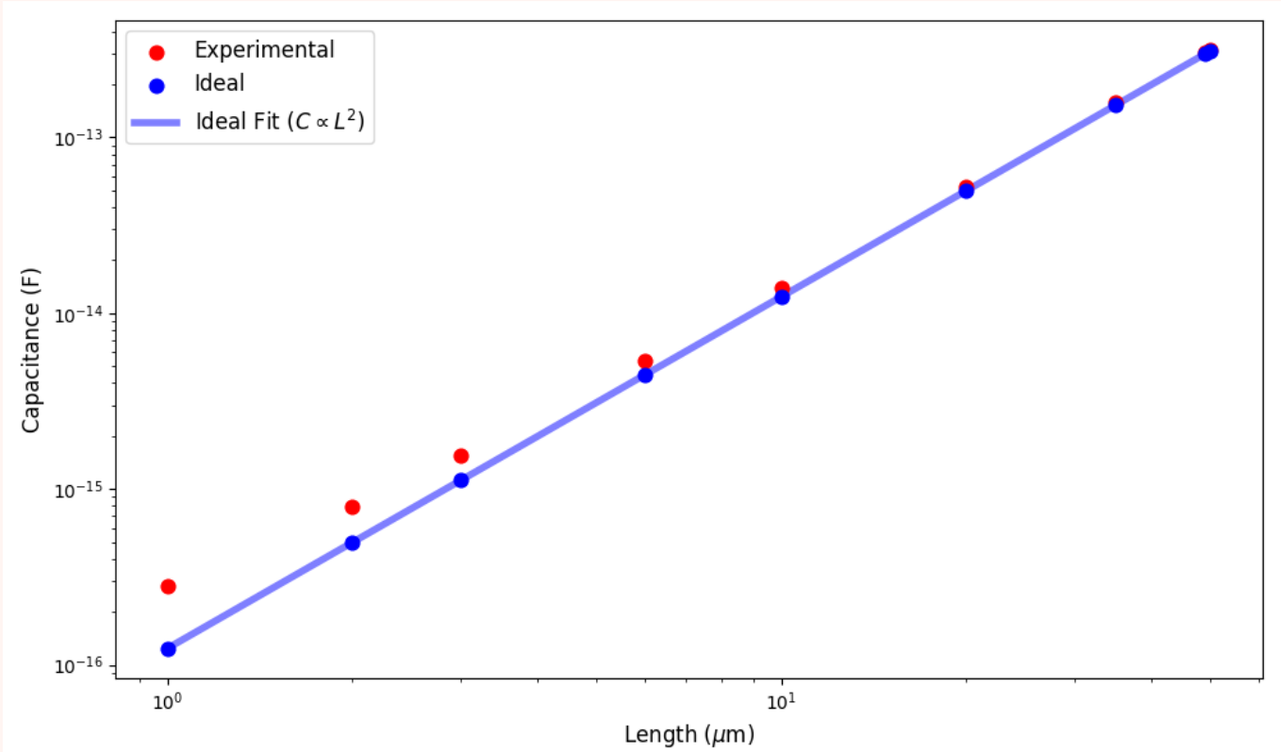
- **The "Aspect Ratio from Hell”:**
  - **Device Width:** 1000 nm
  - **Graphene Thickness:** 0.34nm
  - **Ratio:** approximately 3000:1
- **The Issue:** Standard meshing crashes the computer or creates numerical noise
- **The Engineering Solution:**
  - We approximated Graphene as a 6 nm thick Copper block
  - **Justification**: Since 6nm << 300nm (oxide thickness), the Graphene still acts as a 2D equipotential surface. This allowed for a stable mesh without altering the physics.

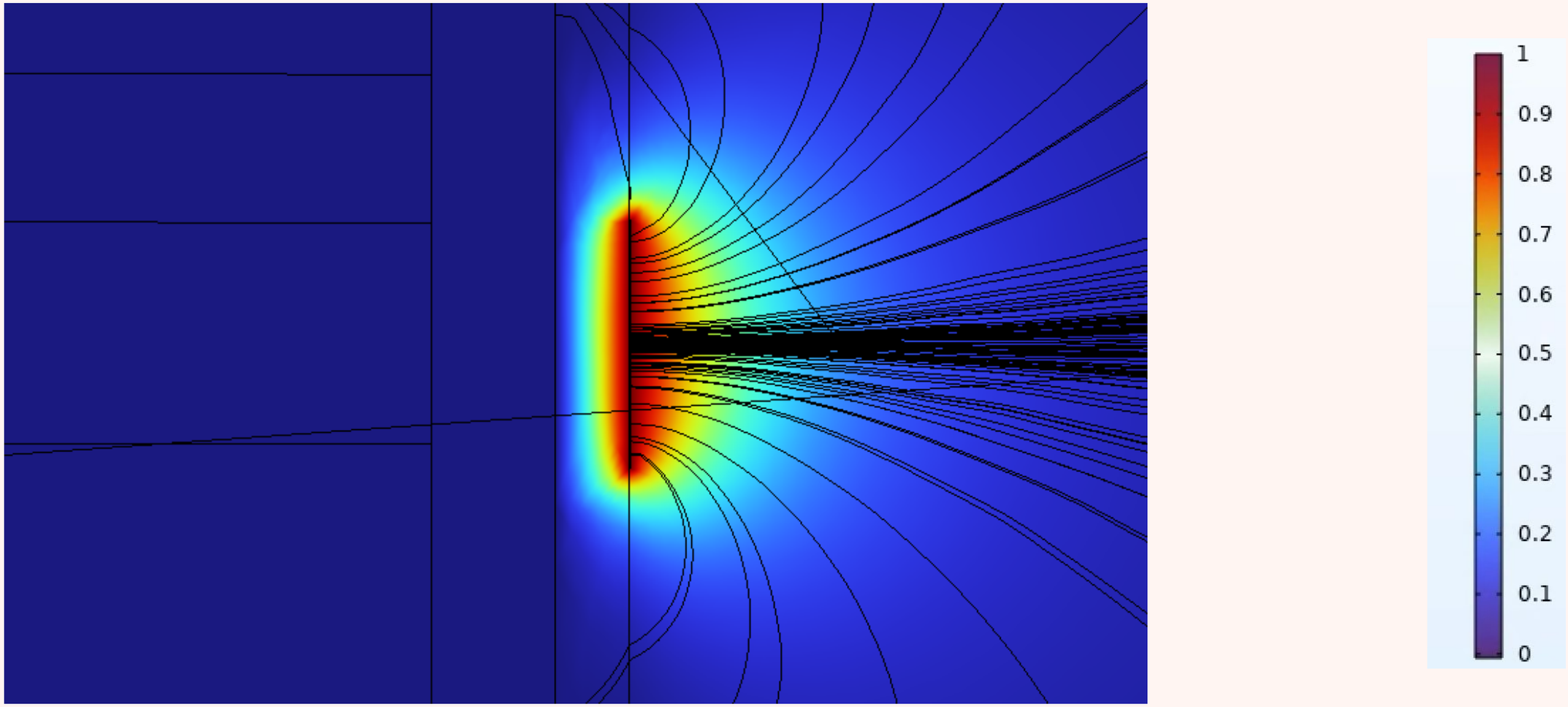
FINDINGS - FRINGE FIELDS

- **Question 1:** Simple Graphene on SiO2
- **Result:**
  - **Ideal Formula:** 0.115 fF
  - **Our Simulation:** 0.233 fF
- **Why? The "Fringe Effect."**
  - Because the Graphene electrode is so small compared to the substrate, field lines don't just go down; they loop out and around.
  - **Takeaway:** The parallel-plate formula loses accuracy for nanoscale electrodes because it neglects fringing fields.



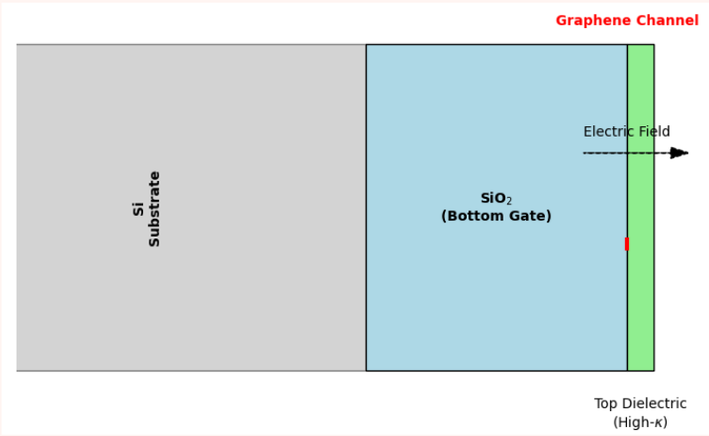


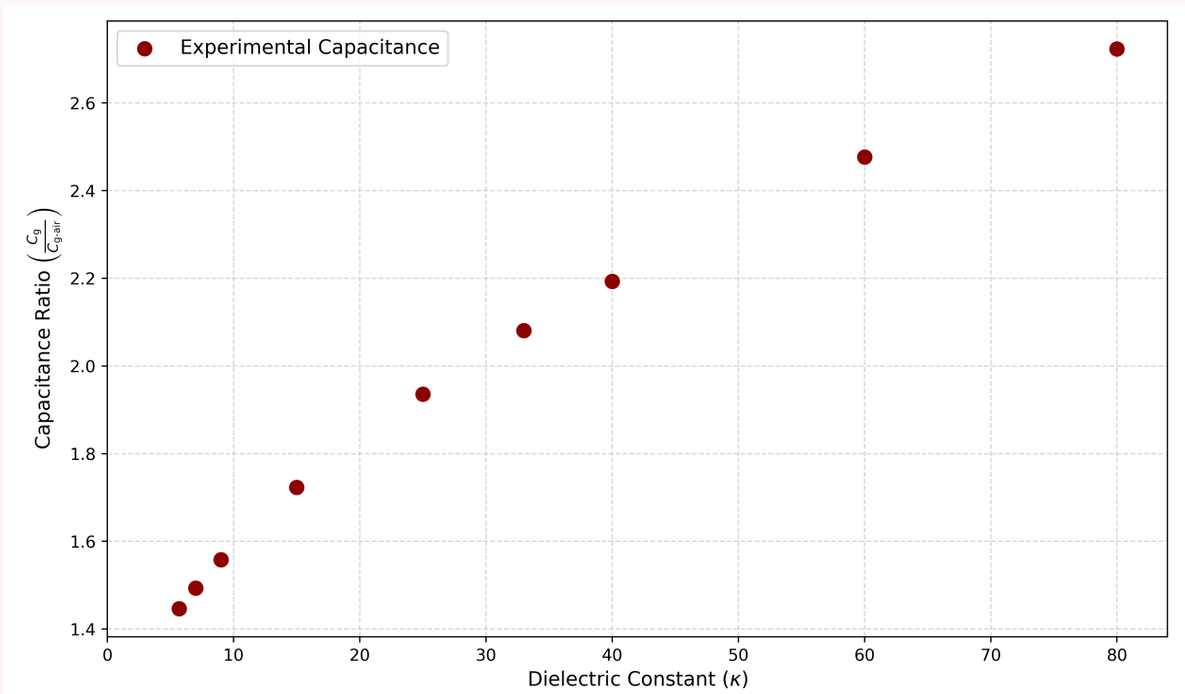

Experimental
Ideal
Ideal Fit ($C \propto L^2$)
Capacitance (F)
10^{-13}
10^{-14}
10^{-15}
10^{-16}
10^{0}
10^{1}
Length (μm)


1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

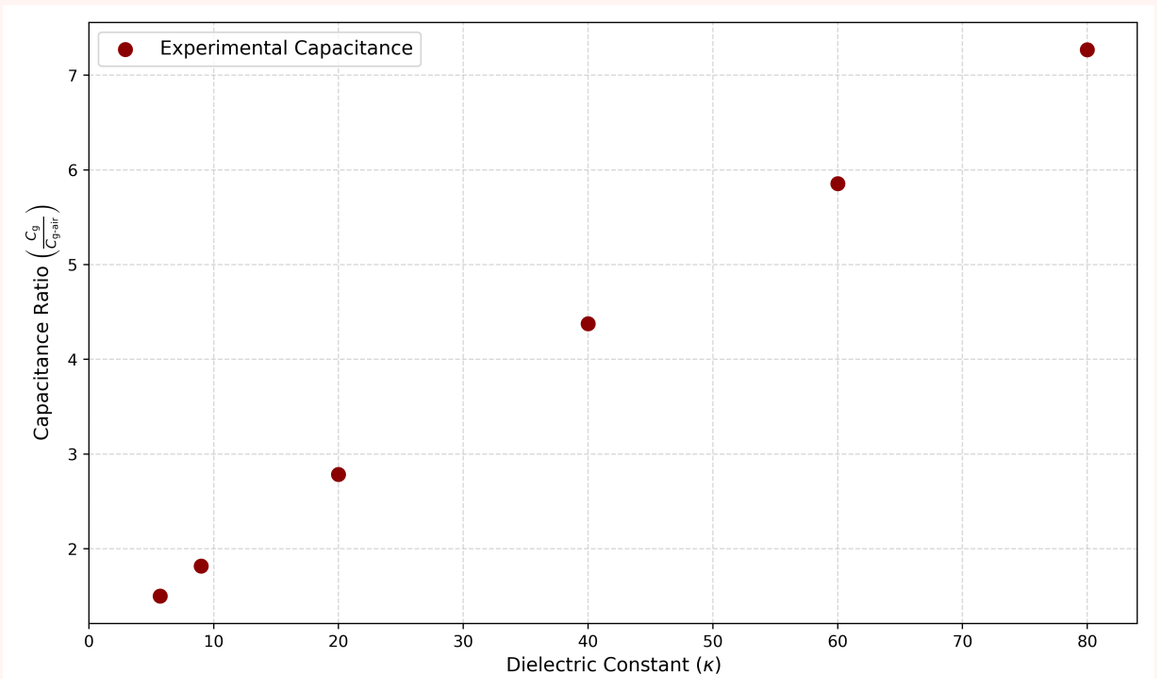
FINDING - DIELECTRIC INFLUENCE

- **Question 2:** Add 30nm layer of Al2O3 on top of Graphene
- **Result:**
  - Capacitance increased by ~45%
    - **Significance:** Even though the "main" capacitor is underneath (Graphene-to-Silicon), changing the material above drastically alters the device physics.
  - We observed an almost linear relationship: As the dielectric constant (κ) of the top material goes up, the total capacitance goes up

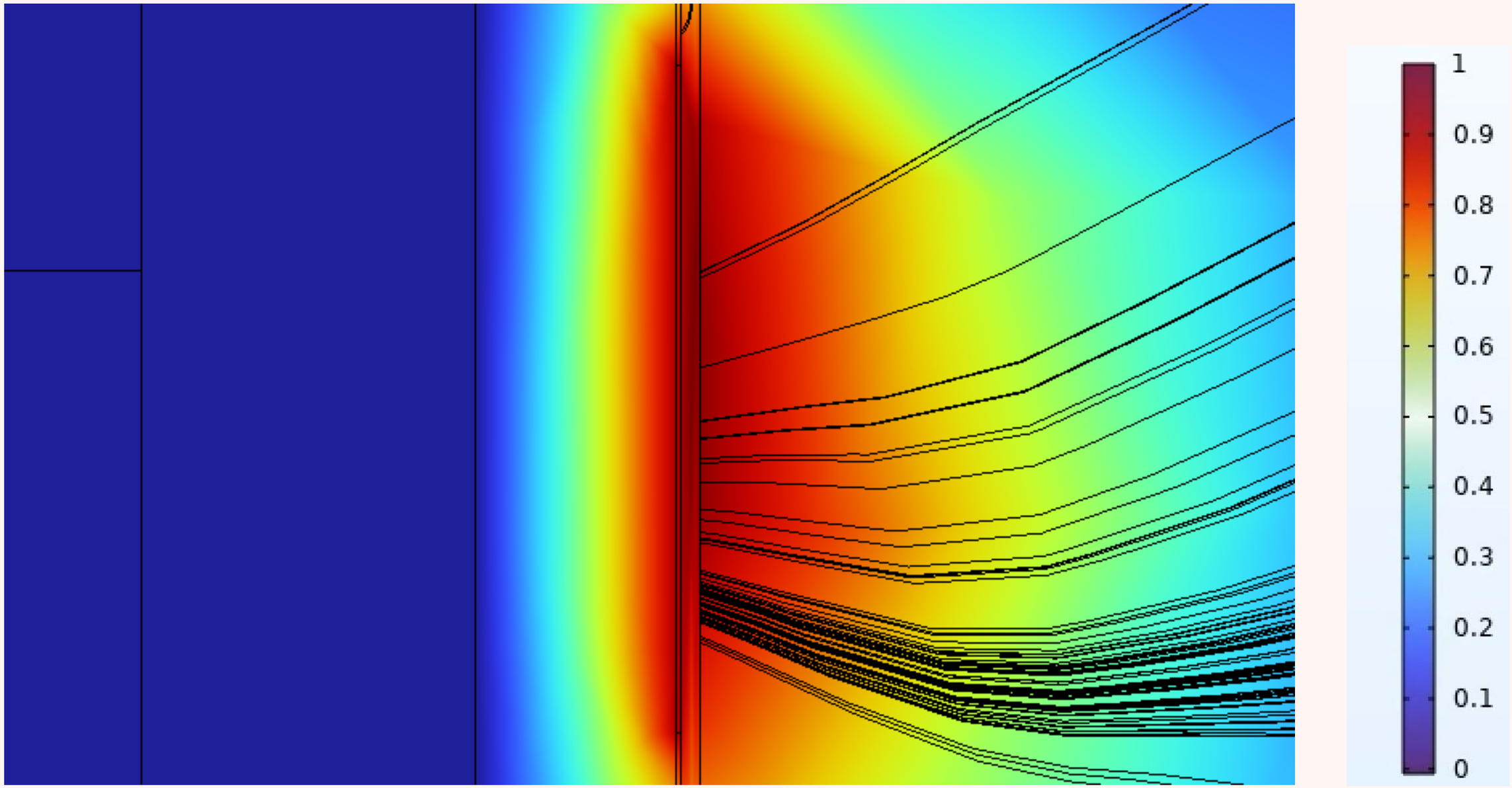



Experimental Capacitance
Capacitance Ratio $\left(\frac{C_g}{C_{g\text{-air}}}\right)$
Dielectric Constant (κ)
1.4
1.6
1.8
2.0
2.2
2.4
2.6
0
10
20
30
40
50
60
70
80

30nm

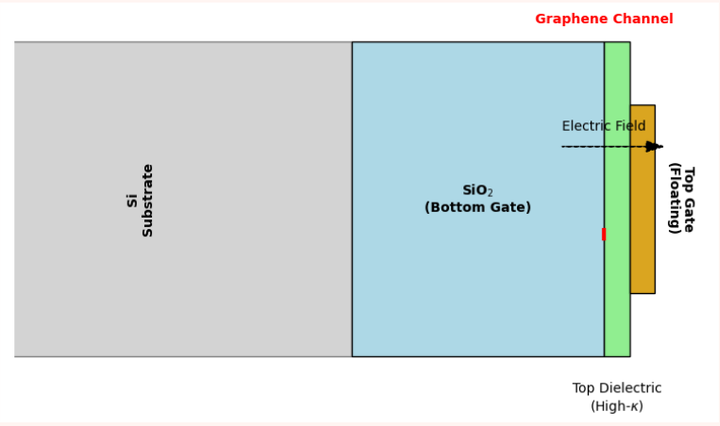

Experimental Capacitance
Capacitance Ratio $\left(\frac{C_g}{C_{g\text{-air}}}\right)$
Dielectric Constant (κ)
2
3
4
5
6
7
0
10
20
30
40
50
60
70
80

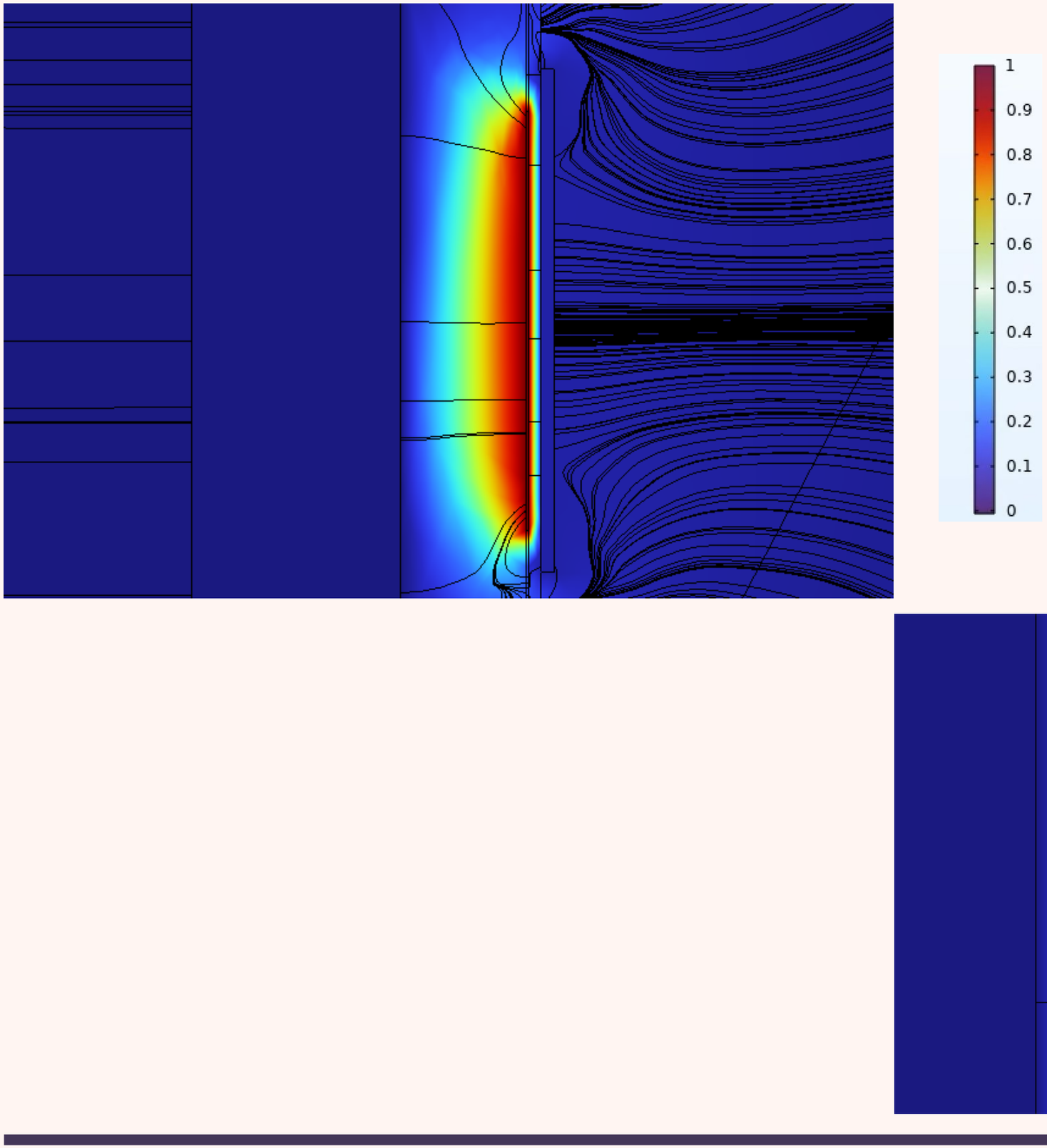
1μm


1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

FINDING - THE FLOATING GATE

- **Question 3:** What happens if we put a metal pad on top (floating potential)?
- **The Result:** Capacitance jumped to 2.02 fF
  - This is an **8.7x** increase compared to the baseline
- **The Reason:** We created two capacitors in parallel.
  - **Bottom Capacitor** (Graphene to Substrate): ≈ 0.283 fF
  - **Top Capacitor** (Graphene to Top Metal): ≈ 16.815 fF




1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0

CONCLUSION

- **Verification:** We confirmed the Xia et al. hypothesis. The performance boost in Graphene FETs is due to Capacitance Scaling, not Mobility
- **Design Lesson:** When designing 2D FETS, you cannot ignore the environment. Anything placed on top becomes part of the gate capacitor.
- **Summary:**
  - Fringe fields increase the capacitance for small devices.
  - Top structures act as parallel capacitors, increasing sensitivity by nearly order of magnitude

THANK YOU