2025

CS 1105

Digital Electronics & Computer Architecture

ASSIGNMENT ACTIVITY UNIT 3

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SEQUENTIAL CIRCUIT DESIGN: DIGITAL PARKING METER CONTROLLER

INTRODUCTION

Sequential circuits form the backbone of modern digital systems by incorporating memory elements that allow circuits to maintain state information and produce outputs based on both current inputs and previous circuit conditions. This fundamental capability enables the creation of complex digital systems that can perform time-dependent operations and maintain operational history. This project demonstrates the practical application of sequential circuits, specifically registers and counters, through the design and analysis of a digital parking meter controller system that manages parking time allocation, payment processing, and display functionality.

PROJECT SCENARIO SELECTION AND JUSTIFICATION

The chosen scenario involves designing a digital parking meter controller that accepts coin inputs, tracks remaining parking time, and displays current status to users. This practical application provides an ideal demonstration of sequential circuit principles because it requires multiple interconnected components working in harmony: payment processing registers, countdown timers, and user interface displays.

This scenario effectively illustrates real-world applications of digital electronics while remaining sufficiently complex to showcase various sequential circuit concepts. The parking meter controller requires state memory to track payment status, temporal counting mechanisms for time management, and register operations for coin value accumulation. According to Harris and Harris (2021), such practical applications help bridge the gap between theoretical understanding and real-world implementation of digital systems.

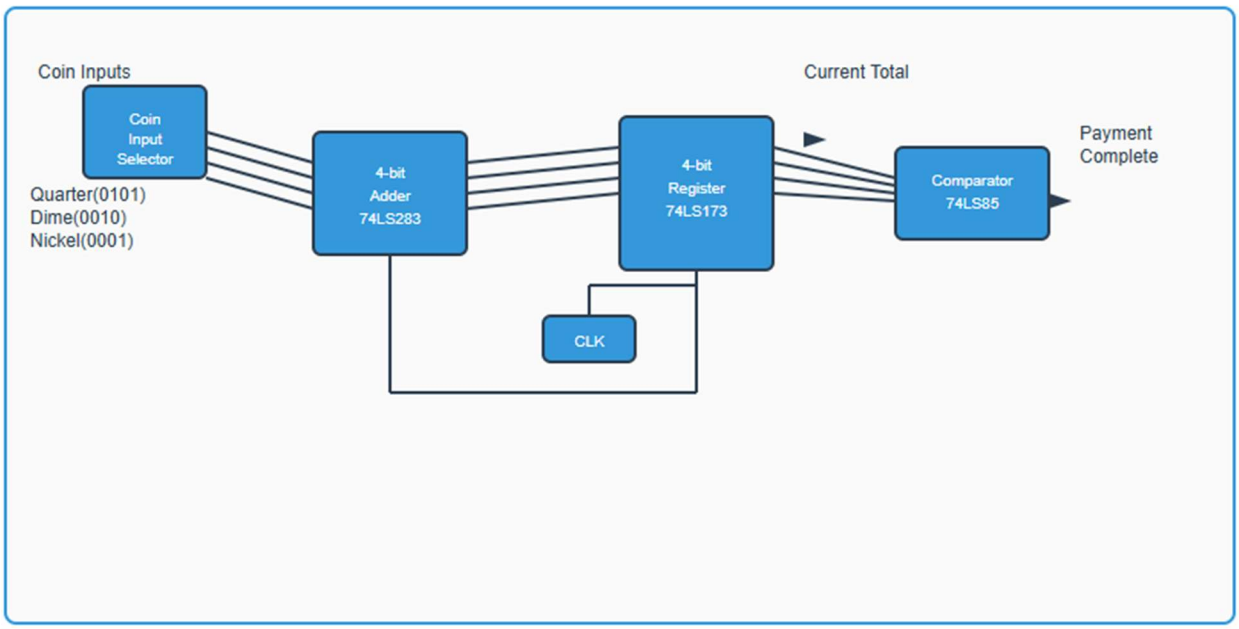
STEP-BY-STEP CIRCUIT DESIGN ANALYSIS

PAYMENT PROCESSING MODULE

The payment processing module utilizes a 4-bit register to accumulate coin values entered by users. The register receives parallel input data representing coin denominations (quarters = 0101, dimes = 0010, nickels = 0001)

and maintains running totals through synchronous loading operations. The accumulator register connects to a comparator circuit that determines when sufficient payment has been received for parking time allocation.

Payment Processing Register Circuit



Circuit Operation:

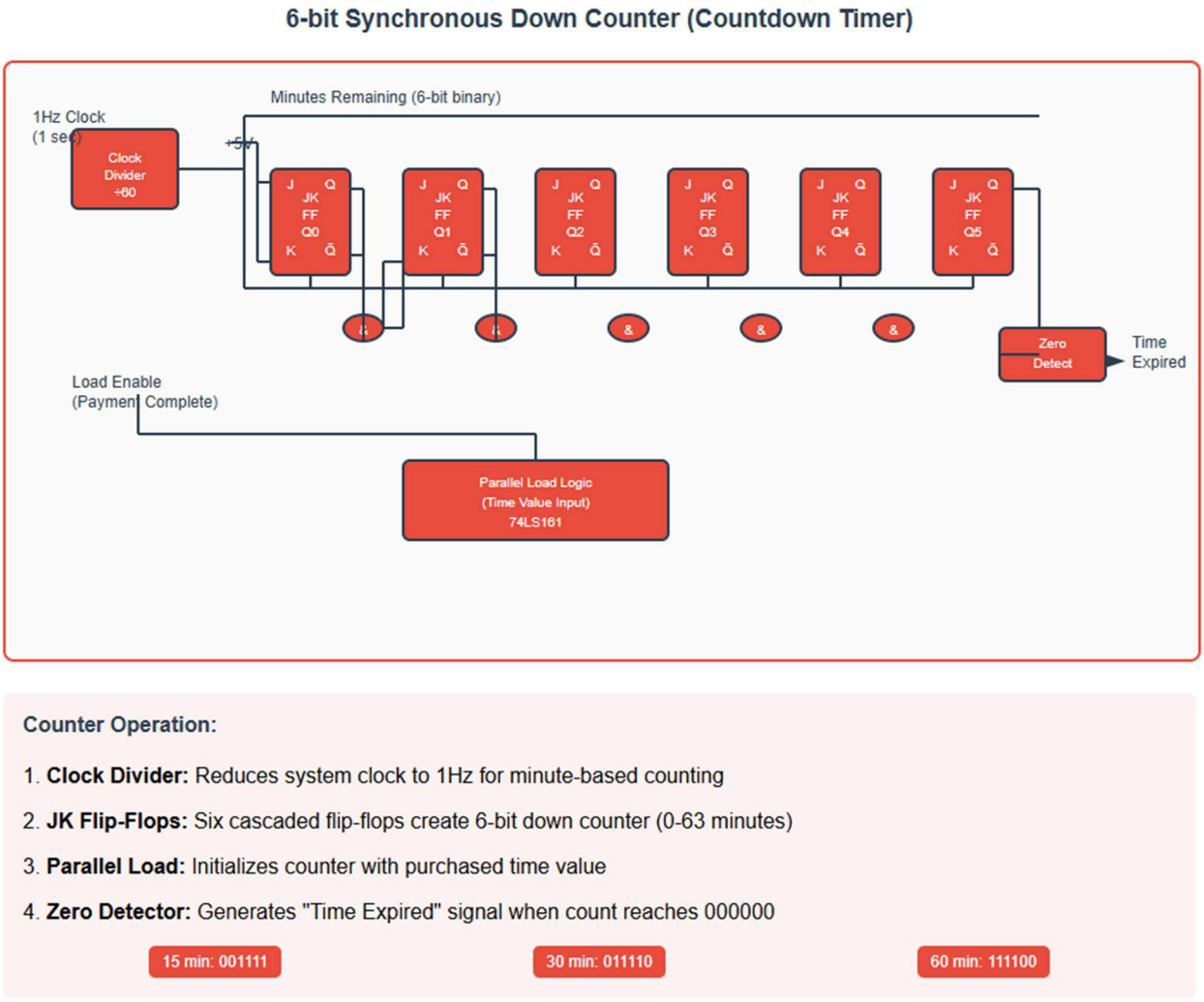
1. **Coin Input Selector:** Receives coin type and outputs corresponding 4-bit value
2. **4-bit Adder:** Adds new coin value to current accumulated total
3. **4-bit Register:** Stores accumulated payment total (clocked operation)
4. **Comparator:** Checks if accumulated amount meets parking time thresholds

Quarter: 0101 (5¢) | Dime: 0010 (2¢) | Nickel: 0001 (1¢)

The register implementation employs D-type flip-flops configured with enable signals that activate during coin insertion events. Clock synchronization ensures stable data transfer and prevents metastability issues during input transitions. The accumulated value feeds into a binary-to-decimal decoder that drives the payment display, providing immediate feedback to users about their current payment status.

COUNTDOWN TIMER IMPLEMENTATION

The core timing functionality relies on a synchronous down-counter implemented using JK flip-flops connected in cascade configuration. The counter initializes with values corresponding to purchased parking time (typically 15, 30, or 60 minutes represented in binary). The system clock, divided through a prescaler circuit to generate one-minute intervals, decrements the counter value continuously during active parking periods.

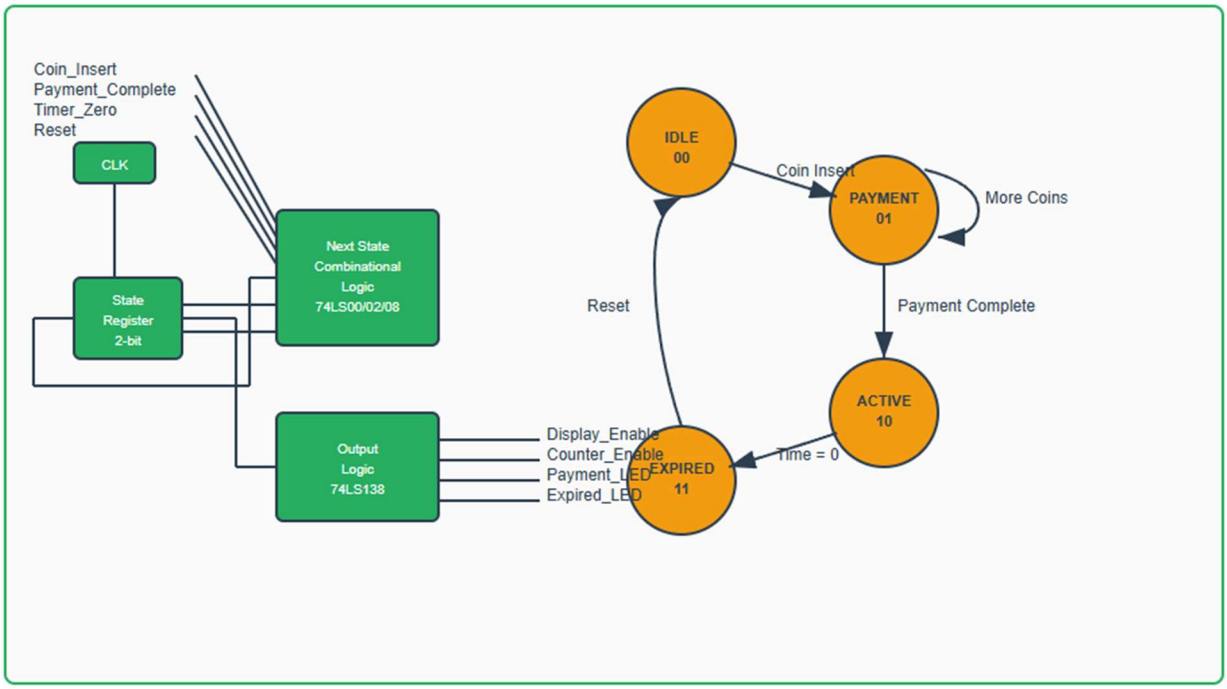


The counter design incorporates parallel load capability, enabling initialization with different time values based on payment amounts received. Terminal count detection logic monitors the counter output and generates timeout signals when the count reaches zero. This approach ensures accurate time tracking while providing clear termination conditions for parking sessions.

DISPLAY AND CONTROL LOGIC

The display subsystem combines multiple registers and decoders to present information to users effectively. A 7-segment display driver register receives time and payment data through multiplexing operations, alternating between different display modes based on system state. The control logic implemented through finite state machine principles manages transitions between idle, payment, active, and expired states.

Finite State Machine Control Logic



State Machine Operation:

The finite state machine controls the overall parking meter behavior through four distinct states:

State	Binary	Condition	Outputs Active
IDLE	00	Waiting for coins	None
PAYMENT	01	Coins being inserted	Payment_LED
ACTIVE	10	Parking time counting down	Display_Enable, Counter_Enable
EXPIRED	11	Time has run out	Expired_LED

Transition Logic: Combinational logic determines next state based on current state and input conditions. Output logic generates control signals for display, LEDs, and counter enable.

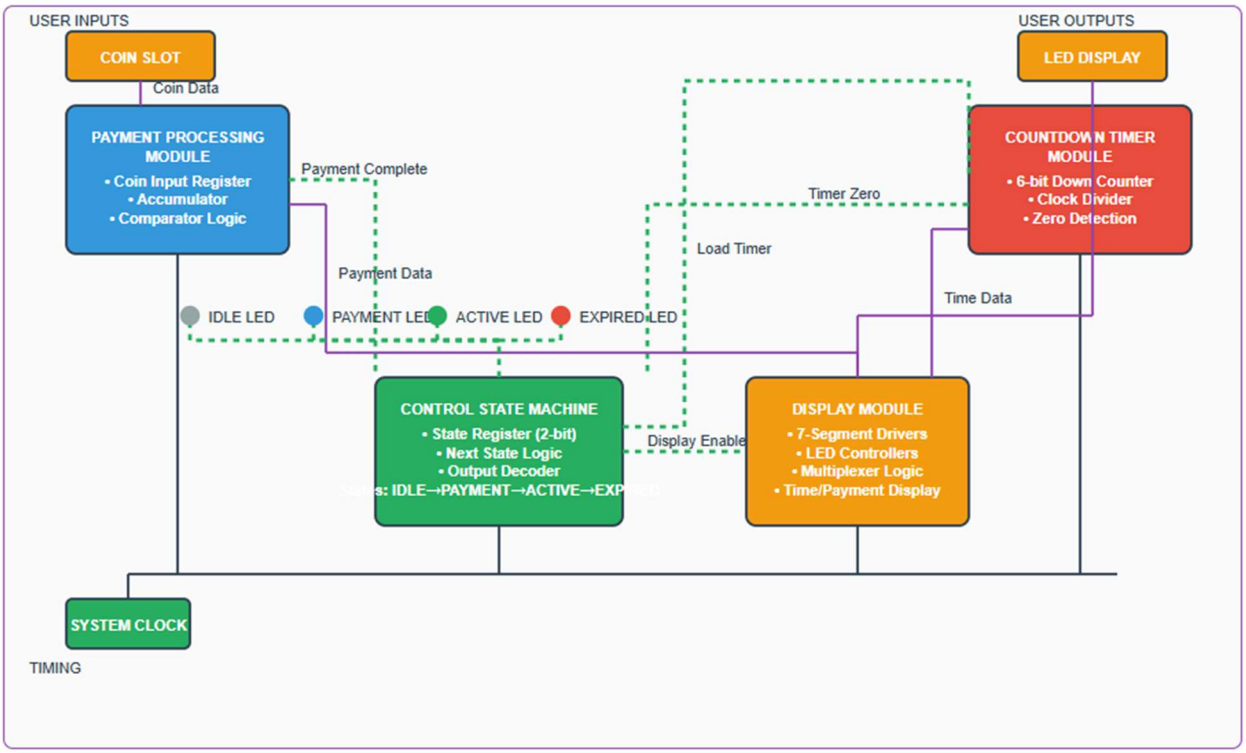
State register implementation uses 3-bit encoding to represent system states, with combinational logic determining state transitions based on input conditions and timer status. The state machine coordinates all subsystem

operations, ensuring proper sequencing of payment processing, time allocation, and display updates throughout parking sessions.

COMPLETE SYSTEM INTEGRATION

The final integrated system combines all subsystems through a comprehensive interconnection scheme that demonstrates the collaborative nature of sequential circuits in complex digital systems.

Complete Digital Parking Meter System Integration



System Integration Overview:

The complete parking meter system demonstrates seamless integration of sequential circuits working collaboratively:

Control Signals | Data Buses | Clock Distribution

Operation Flow:

1. **Coin Insertion:** Payment module accumulates coin values using register operations
2. **State Transition:** Control FSM transitions from IDLE to PAYMENT to ACTIVE states
3. **Timer Initialization:** Counter loads with time value based on payment amount
4. **Active Counting:** Timer decrements while display shows remaining time
5. **Expiration:** Zero detection triggers EXPIRED state and appropriate user notifications

Key Features: Synchronous operation, fault tolerance through state machine control, modular design enabling easy maintenance and upgrades.

Register and Counter Integration

Registers and counters collaborate seamlessly within the parking meter system to create comprehensive functionality. The payment register accumulates monetary inputs while interfacing with the time counter through value comparison logic. When payment thresholds are met, the control system loads corresponding time values into the countdown counter, establishing direct correlation between payment amounts and parking duration.

The integration demonstrates how sequential circuits can maintain multiple data streams simultaneously. While the countdown counter tracks remaining time, display registers continuously update user interfaces with current information. Buffer registers prevent data corruption during transitions between operational modes, ensuring system reliability throughout various operating conditions.

According to Mano and Ciletti (2019), effective register and counter integration requires careful attention to timing relationships and data flow management to prevent race conditions and ensure predictable system behavior.

Synchronization and Timing Considerations

Clock domain management plays a crucial role in system operation, with different subsystems operating at appropriate frequencies for their specific functions. The payment processing operates at higher frequencies to provide responsive user interaction, while the countdown timer utilizes slower clock rates for accurate time measurement. Clock domain crossing circuits ensure proper data transfer between subsystems operating at different rates.

Project Component Overview and Integration

The complete parking meter controller integrates five primary components working in coordinated fashion. The coin input interface captures user payments and validates coin types through pattern recognition circuits. The payment accumulator register maintains running totals and interfaces with threshold detection logic. The time counter provides core timing functionality with parallel load capability for flexible time allocation.

The display management system coordinates information presentation through multiplexed operations, while the central control unit manages system states and coordinates inter-component communication. Each component

utilizes sequential circuit principles while contributing to overall system functionality through carefully designed interfaces and timing protocols.

The system architecture demonstrates how complex digital systems emerge from fundamental sequential circuit building blocks. As noted by Floyd (2018), such hierarchical design approaches enable creation of sophisticated systems while maintaining manageable complexity at each architectural level.

CONCLUSION

This digital parking meter controller project effectively demonstrates the practical application of sequential circuits, registers, and counters in creating functional digital systems. The design showcases how memory elements enable state-dependent behavior while counters provide temporal functionality essential for time-based applications. The integration of multiple sequential circuit types illustrates the collaborative nature of digital system design, where individual components contribute specialized capabilities while working together to achieve complex operational requirements. Through systematic analysis of input/output behavior and careful attention to timing relationships, the project provides valuable insights into practical digital electronics design principles that extend far beyond academic exercises into real-world applications.

References:

Floyd, T. L. (2018). *Digital fundamentals* (12th ed.). Pearson.

Harris, S. L., & Harris, D. M. (2021). *Digital design and computer architecture* (2nd ed.). Morgan Kaufmann.

Mano, M. M., & Ciletti, M. D. (2019). *Digital design: With an introduction to the Verilog HDL, VHDL, and SystemVerilog* (6th ed.). Pearson.

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