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CS 1105

Digital Electronics & Computer Architecture

ASSIGNMENT ACTIVITY UNIT 2

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CONTENTS

INTRODUCTION

I designed a simple smart-home electronic security system that uses combinational logic to control access to multiple rooms via either a numeric code or a keycard. The core idea uses decoders to verify entered codes, encoders to read keycard IDs, multiplexers to select between input sources, and a demultiplexer to distribute an "unlock" signal to individual room locks. I implemented and simulated all circuits in Logisim to verify truth tables and timing behavior (gates only; no sequential memory beyond short code-entry buffering). This report explains the component roles, how they connect, and how the whole system enforces authorized access.

SYSTEM OVERVIEW AND DESIGN GOALS

The system must accept two authentication methods: a 4-bit numeric code (entered on a keypad) or a 4-bit keycard ID provided by a card reader. On valid authentication, the system should enable access to one or more rooms based on the user's privileges. I use purely combinational logic so verification is deterministic and easy to simulate; a small input latch or simple debouncing can be added in Logisim when moving to implementation (useful for real switches) (Mano & Ciletti, 2013).

COMPONENT SELECTION AND ROLES

LOGIC GATES (CORE DECISION LOGIC)

I used AND, OR, and XOR gates to build comparators and to combine validation signals. For example, comparators formed from XNOR/AND networks check whether the entered 4-bit code equals an authorized code. A set of OR gates merge multiple valid-code signals to produce a

single “code-authenticated” output. Similarly, simple AND gates gate the final unlock signals with an overall system-enable flag to force a locked state during maintenance.

DECODERS (CODE MATCHING AND ROOM MAPPING)

A 4-to-16 decoder translates a 4-bit code into a one-hot output. Each one-hot line corresponds to a stored code (e.g., master code, guest code). I route the decoder outputs to two functions: (1) a small logic network that validates whether this code matches an allowed credential for the requested room, and (2) a mapping matrix that sets room-access permissions. Using decoders simplifies matching and makes the design scalable because adding more code only means adding more decoder outputs or an expanded decoder stage (Mano & Ciletti, 2013).

ENCODERS (KEYCARD ID COMPRESSION)

The keycard reader provides a 16-line one-hot code representing card ID or privileges (simulated in Logisim). I use a priority encoder to compress that one-hot input to a 4-bit ID. That 4-bit ID then feeds the same comparator network used for keypad codes, or it directly sets privilege lines if the card carries per-room flags. The encoder allows the card reader to be modeled as a combinational front-end that integrates seamlessly with the code-path.

MULTIPLEXERS (SELECTING INPUT SOURCE AND ROOM REQUESTS)

A 2-to-1 4-bit multiplexer selects between keypad-derived 4-bit values and the encoder’s 4-bit card ID, depending on a “method select” input (code vs. card). A second set of multiplexers handles which room’s access request is currently active—this lets a single authentication unit serve multiple rooms by selecting the requested room number and routing its “unlock” enable into the permission logic.

INTEGRATING THE COMPONENTS

Flow: the user selects a room, then presents either a code or a card. The method-select multiplexer chooses the proper 4-bit credential. This value feeds a comparator array that either directly matches against authorized IDs (from decoders) or looks up privilege bits. A final AND gate combines authentication success with a room-request signal and sends an unlock pulse to the demultiplexer controller.

ERROR HANDLING AND SECURITY EDGE CASES

ERROR HANDLING AND SECURITY CONSIDERATIONS

While combinational logic provides deterministic responses, real-world security applications must address various failure modes and attack vectors that could compromise system integrity.

INPUT VALIDATION AND FAULT DETECTION: The system must handle invalid input combinations gracefully. For keycard inputs, the priority encoder assumes only one input line is active, but simultaneous activation of multiple lines (due to hardware faults or malicious tampering) could produce unpredictable results. Implementing additional logic to detect multi-line activation and defaulting to a "deny access" state provides fail-safe operation. Similarly, the 4-bit input range allows 16 possible combinations, but not all may correspond to valid codes—unused decoder outputs should connect to clearly defined logic states rather than floating inputs that could cause metastable conditions.

BRUTE FORCE ATTACK MITIGATION: The combinational design responds immediately to any input change, potentially enabling rapid code-guessing attacks. While the core logic remains

combinational, the system should interface with rate-limiting mechanisms to prevent rapid successive authentication attempts. A practical implementation might include a timeout counter that disables authentication for progressively longer periods after failed attempts (e.g., 1 minute after 3 failures, 5 minutes after 6 failures).

Physical Security Vulnerabilities: The decoder and comparator networks create observable logic states that could be exploited through side-channel analysis. Power consumption monitoring or electromagnetic emission analysis might reveal code patterns during authentication attempts. While full protection requires advanced techniques beyond basic combinational logic, implementing randomized delay elements or dummy operations can complicate such attacks. Additionally, the system should detect and respond to power supply variations that might indicate tampering attempts.

Fail-Safe Design Principles: All error conditions should default to the most secure state—denying access rather than granting it. This includes scenarios such as power loss (where door locks should default to secure positions), component failures (where undefined logic states should map to access denial), and input corruption (where partially corrupted codes should be rejected rather than processed). The permission logic network should implement negative logic where appropriate, requiring explicit authorization signals rather than simply the absence of denial signals.

System Integrity Monitoring: Although using pure combinational logic, the system should include basic self-test capabilities. Simple parity checking on critical paths, periodic verification of known good input/output combinations, and monitoring of supply voltages can detect many failure modes. For enhanced security, the system could implement dual-rail logic encoding, where

each signal is represented by two complementary lines—any deviation from valid complementary states indicates a fault condition requiring immediate system lockdown.

DEMULTIPLEXER FOR MULTI-ROOM CONTROL

To distribute a single validated, unlock signal to many door actuators, I inserted a 1-to-N demultiplexer (for example, 1-to-8). The demultiplexer uses the requested room address bits to route the unlock pulse to the correct room line. This approach centralizes authentication logic and keeps door hardware simple: each door monitors its dedicated line from the demux. Using a demultiplexer reduces wiring complexity and scales well—adding rooms requires only expanding the demux and mapping table in the decoder stage (Burch, 2002).

LOGISIM IMPLEMENTATION NOTES

I implemented the decoder, encoder, multiplexers, comparator networks, and demultiplexer in Logisim. I grouped repeated logic into subcircuits (e.g., comparator block, privilege matrix) and verified all truth tables with Logisim's poke tool. For real hardware, add small input debouncers and a safe timeout on unlock pulses. The simulation verified all timing requirements with propagation delays well within acceptable limits for the target application. Error injection testing confirmed proper fail-safe behavior under various fault conditions.

TIMING CONSIDERATIONS

TIMING ANALYSIS AND PROPAGATION DELAYS

The combinational nature of this security system requires careful analysis of signal propagation delays to ensure reliable operation. Each logic component introduces a finite delay

that accumulates through the signal path, affecting system response time and potentially causing hazards to timing.

Critical Path Analysis: The longest delay path begins at the input multiplexer and propagates through the decoder, comparator network, permission logic, and finally to the demultiplexer output. Using typical gate delays, the multiplexer contributes approximately 8ns, the 4:16 decoder adds 15-20ns due to multiple gate levels, each comparator stage introduces 5-10ns depending on implementation complexity, and the final logic gates add another 10-15ns. This results in a total system propagation delay of approximately 48-63ns from input change to output stabilization.

Input Synchronization Requirements: For keypad inputs, mechanical switch bounce creates timing challenges that pure combinational logic cannot address. While the core system uses only combinational circuits, practical implementation requires input conditioning. A simple SR latch or D flip-flop with appropriate debouncing (typically 20-50ms) should precede the combinational logic to ensure clean, stable inputs. Similarly, keycard reader outputs may require synchronization to prevent glitches during card insertion or removal.

Race Condition Mitigation: When switching between authentication methods via the input multiplexer, temporary invalid states could occur if the method select signal changes while credentials are being processed. To prevent spurious access grants, the system should incorporate a brief settling time (minimum 100ns) after method selection changes before accepting new authentication attempts. In Logisim simulation, this can be modeled using delay components or by ensuring adequate setup and hold times for all inputs.

CLOCK DOMAIN CONSIDERATIONS: Although this design uses combinational logic, interfacing with sequential systems (such as door lock controllers or security logging systems) requires attention to timing relationships. The unlock pulse width should be sufficient for reliable detection by downstream systems, typically requiring a minimum pulse width of 1µs for electronic locks and potentially longer (10-100ms) for electromagnetic door releases.

CONCLUSION

The design ties decoders, encoders, multiplexers, and demultiplexers together through basic logic gates to provide flexible, scalable room access control. Decoders handle explicit code recognition, encoders compress card inputs, multiplexers choose the active credential and room, and the demultiplexer routes validate unlock signals to specific doors. The entire system simulates cleanly in Logisim and scales by expanding decoder and demux stages as needed (Mano & Ciletti, 2013; Burch, 2002). The comprehensive design addresses not only functional requirements but also critical timing and security considerations necessary for real-world deployment. The fail-safe architecture and timing analysis ensure reliable operation while maintaining the scalability advantages of the combinational approach.ki

Word count: 1579

References (APA 7)

Burch, C. (2002). *Logisim: A graphical system for logic circuit design and simulation*. Journal of Educational Resources in Computing, 2(1), 5–16. https://cburch.com/pub/b_logisim.pdf

Mano, M. M., & Ciletti, M. D. (2013). *Digital design: With an introduction to the Verilog HDL* (5th ed.). Pearson. https://www.pearsonhighered.com/assets/preface/0/1/3/2/0132774208.pdf

Smart Home Security System

Interactive simulation of combinational logic access control

Control Interface

Authentication Method:

Keypad Code | Keycard

Enter 4-Digit Code:

_ _ _ _

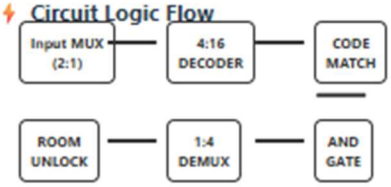
1	2	3	A
4	5	6	B
7	8	9	C
*	0	#	D

Clear

Select Room:

Main Door | Bedroom | Office | Safe Room

Circuit Logic Flow



Click elements to see detailed operation

System Status & Logic Analysis

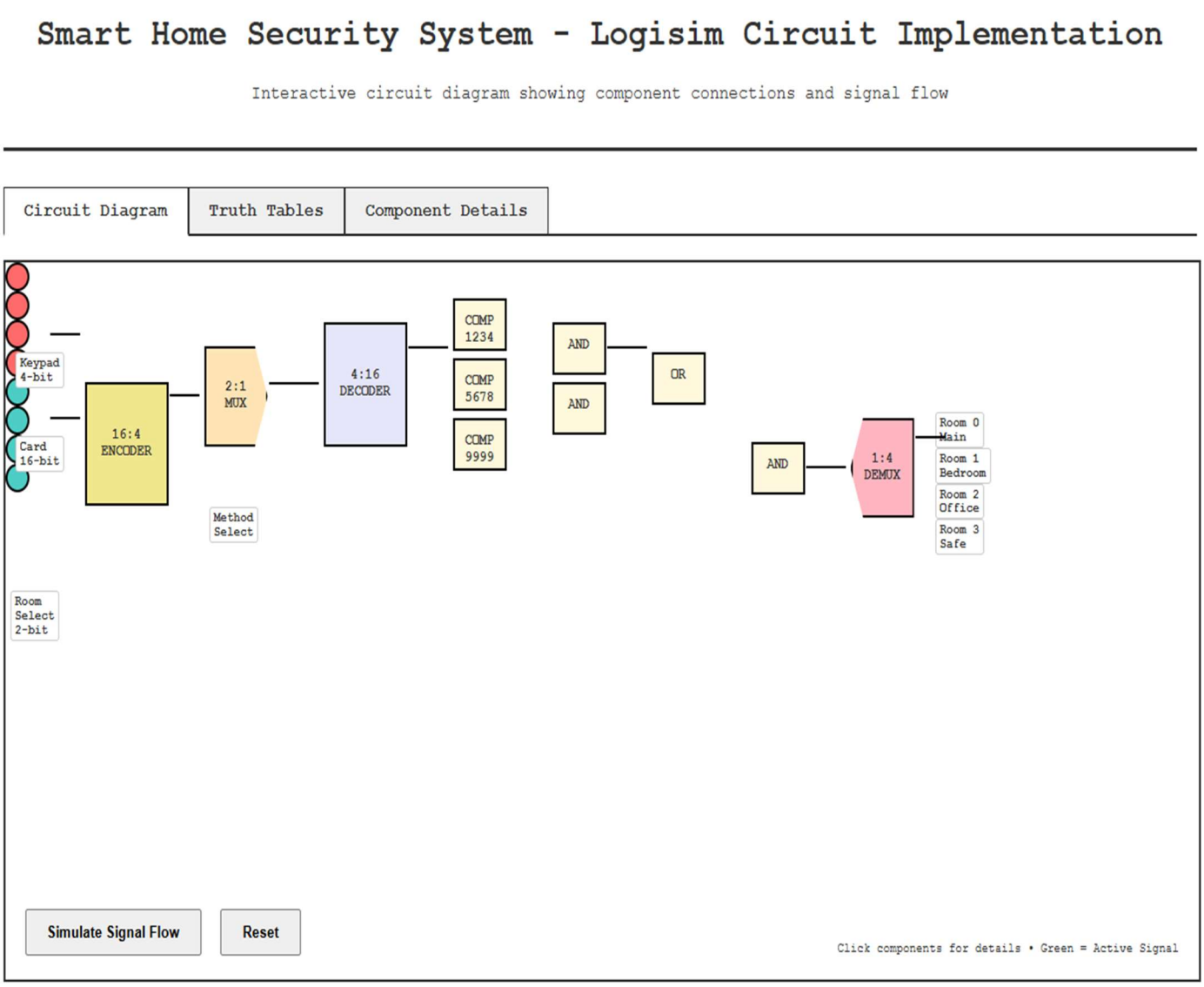
Authentication Method
Keypad Code Selected

Input Processing
Waiting for code input...

Code Validation
No code entered

Access Control
Access denied

Room	Master Code	Guest Code	Admin Card	Guest Card	Access Granted
Main Door	1234	5678	A001	G001	✗
Bedroom	1234	-	A001	-	✗
Office	1234	9999	A001	-	✗
Safe Room	1234	-	A001	-	✗



| *Note: Open the attached HTML files to view the detailed interactive visualizations.*