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CS 1105

Digital Electronics & Computer Architecture

ASSIGNMENT ACTIVITY UNIT 5

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DIGITAL CIRCUIT PROJECT USING A PROGRAMMABLE LOGIC DEVICE

INTRODUCTION

Programmable Logic Devices (PLDs) have transformed the way digital systems are designed and implemented by allowing rapid prototyping, flexibility, and reconfigurability. Unlike traditional fixed logic circuits that rely on discrete gates or custom ASICs, PLDs enable designers to modify and test logic functions directly through software, significantly reducing development time and cost (Brown & Vranesic, 2013). In this assignment, I designed a **digital combination lock circuit** that employs a PLD to control the logic sequence required to unlock a system when the correct digital code is entered.

CIRCUIT OVERVIEW

The digital combination lock circuit includes the following main components:

1. **Input Keypad** – A 4x4 matrix keypad serves as the user interface for code entry. Each key press generates a binary signal corresponding to a specific number or command.
2. **Debounce Circuit** – Implemented using simple RC filters or within the PLD, this circuit ensures that each key press registers as a single, clean signal without multiple transitions.
3. **Programmable Logic Device (PLD)** – A CPLD (Complex Programmable Logic Device) is used to implement the logic that verifies the correct sequence of inputs. The PLD stores the logic equations and controls the output based on the entered sequence.

4. **Output LED/Buzzer** – These indicate whether the input code is correct or incorrect. The LED turns on or the buzzer sounds when the correct combination is entered.

5. **Power Supply and Clock Source** – Provide the necessary voltage and timing signals to synchronize circuit operations.

Figure 1 below illustrates the system architecture and signal flow of the digital combination lock circuit:

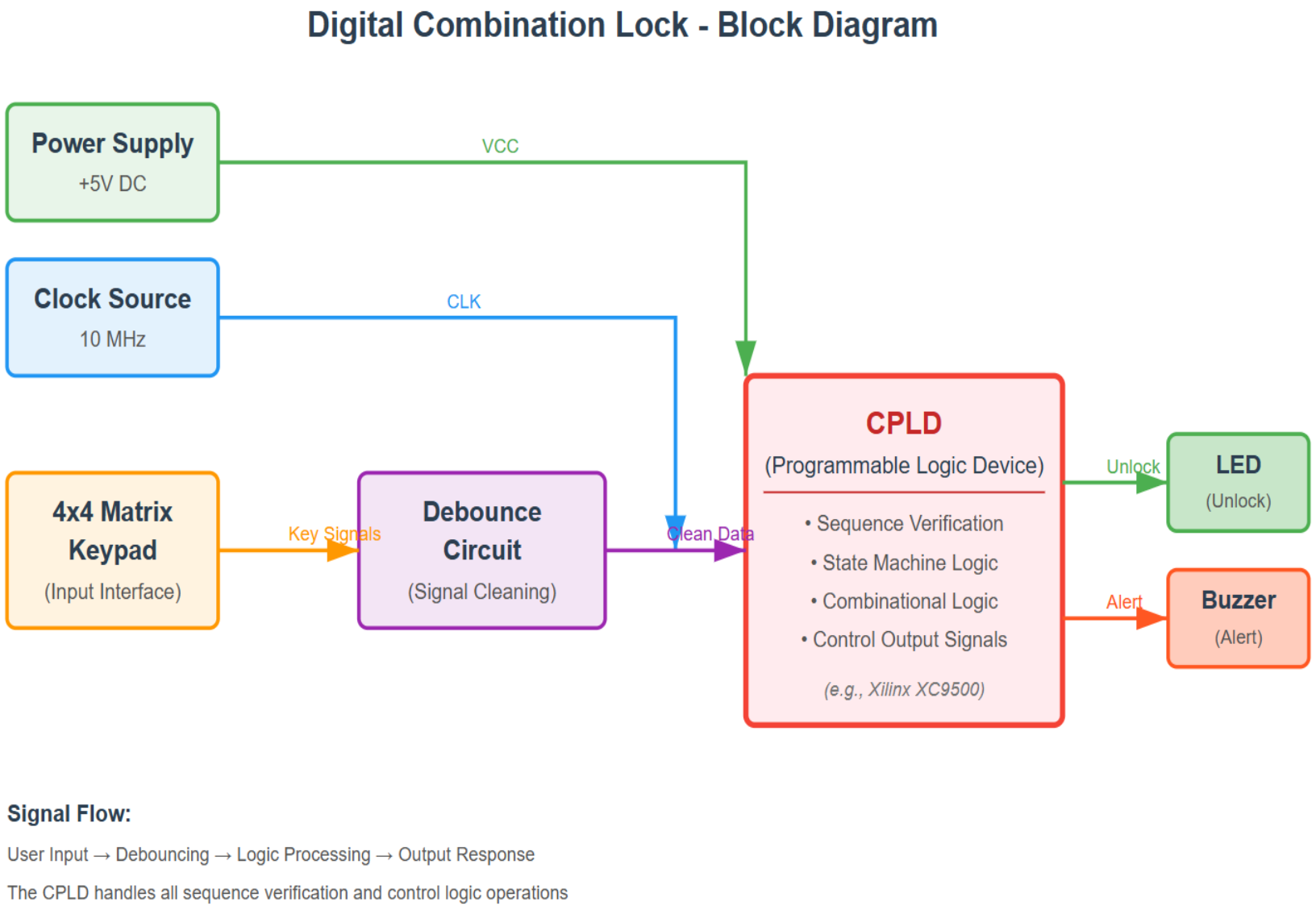

FIGURE 1: BLOCK DIAGRAM SHOWING THE INTERCONNECTION OF ALL CIRCUIT COMPONENTS

ROLE OF THE PLD IN THE CIRCUIT

In this design, the **CPLD acts as the "brain"** of the system, handling the logical sequence verification. When a user enters digits on the keypad, the PLD compares the sequence against the stored combination pattern using internal flip-flops and logic blocks. If the sequence matches, the PLD outputs a high signal to activate the "unlock" LED or buzzer. If incorrect, it resets the state machine and waits for new input.

Figure 2 demonstrates the finite state machine implemented within the CPLD for sequence verification:

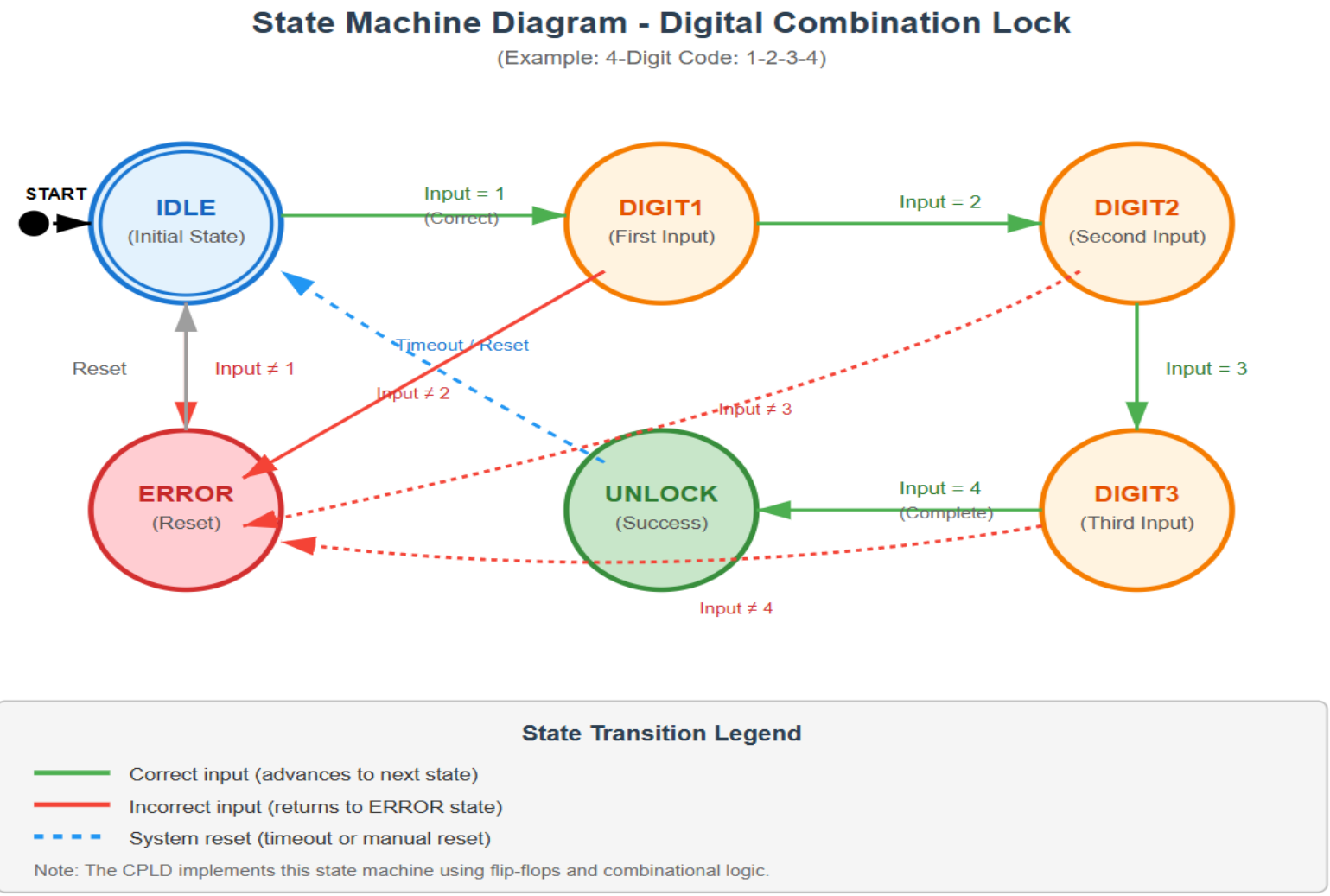

FIGURE 2: STATE TRANSITION DIAGRAM FOR THE 4-DIGIT COMBINATION LOCK (EXAMPLE CODE: 1-2-3-4)

The use of a PLD significantly improves flexibility. If the combination needs to change or if additional security features such as timing restrictions are added, these modifications can be done through reprogramming rather than redesigning the entire hardware (Pedroni, 2020). The reconfigurable nature of PLDs reduces prototyping costs and enables iterative testing without soldering or rewiring circuits.

The internal architecture of the CPLD, shown in Figure 3, reveals how programmable logic blocks process input signals through comparators and state registers:

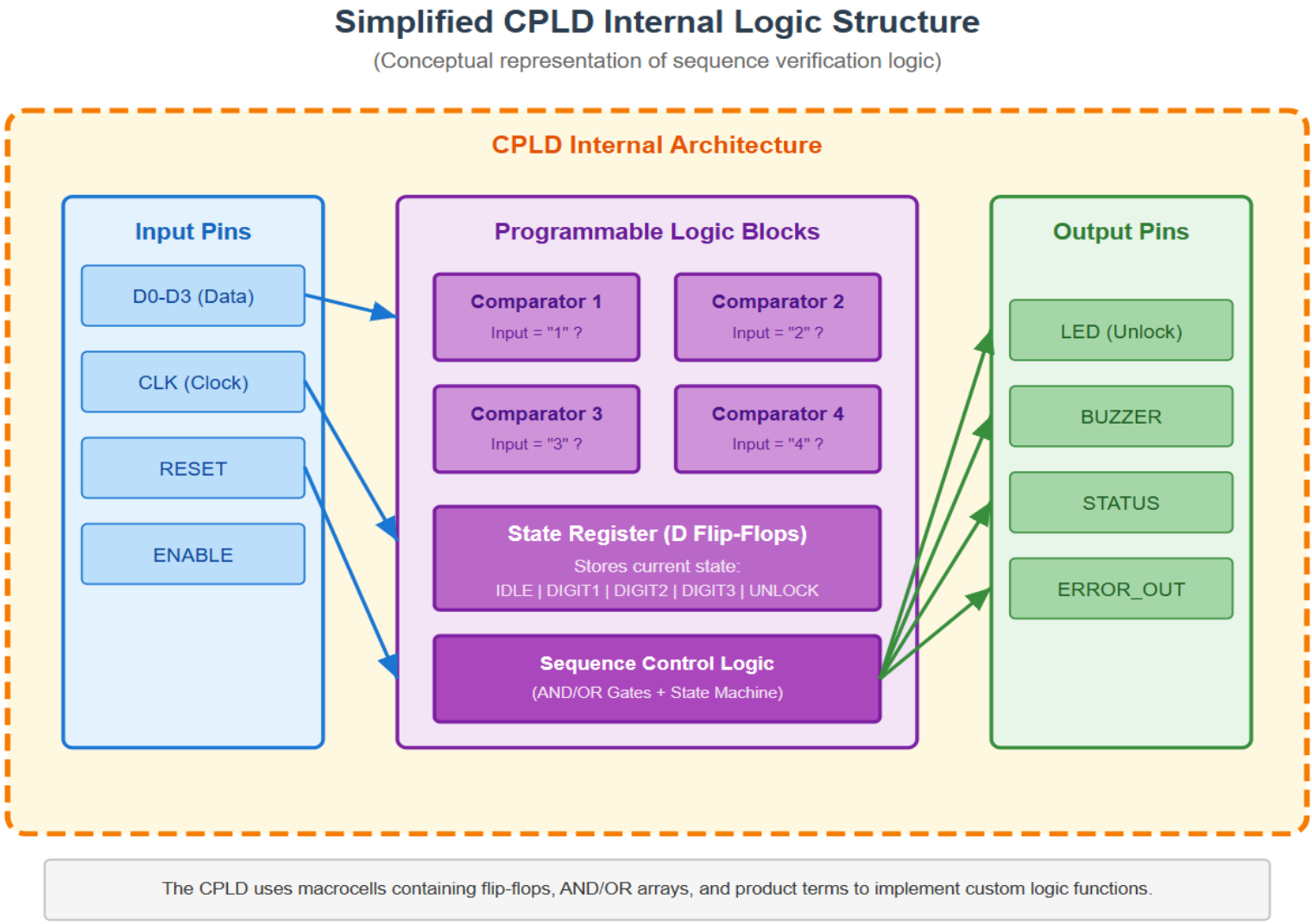

FIGURE 3: SIMPLIFIED INTERNAL LOGIC STRUCTURE OF THE CPLD SHOWING PROGRAMMABLE ELEMENTS

IMPORTANCE OF PLDS IN DIGITAL DESIGN

PLDs bridge the gap between fixed logic circuits and fully custom ASICs. They allow designers to **test multiple designs quickly**, modify logic functions in the field, and integrate multiple logic functions into a single chip (Mano & Ciletti, 2017). In educational settings, PLDs provide a hands-on platform for students to understand digital design concepts such as combinational and sequential logic, finite state machines, and timing analysis.

Furthermore, PLDs offer scalability—designs created on a small CPLD can later be migrated to larger FPGAs for higher complexity systems. This flexibility and reusability make PLDs invaluable for both prototyping and production environments (Pedroni, 2020).

CONCLUSION

The programmable logic device-based digital combination lock assignment demonstrates the practicality and versatility of PLDs in modern digital electronics. By integrating all logic operations into a single reprogrammable chip, the design achieves enhanced performance, flexibility, and ease of modification. PLDs empower designers and learners to efficiently develop, test, and improve digital systems without the constraints of fixed hardware configurations.

References

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