DIGITAL SYSTEMS AND MICROCONTROLLERS

Experiment - 2 **Monsoon 2018**

Basic Logic Gates

In this experiment, you will be introduced to some of the basic logic gates (NOT, AND, OR, NAND, NOR, XOR etc) available commercially in the IC (Integrated Circuit) form. Two families of digital ICs are commonly used: the TTL 74LSxx series and the CMOS CD 40xx series. Many of these ICs have 14 pins, and some have 16 or more. Two pins are used for power supply connections. Thus 12 pins are available in a 14-pin IC for gate inputs and outputs. A 2-input gate requires three pins per gate (two for inputs and one output), and so ICs that implement 2-input logic functions generally have 4 gates per IC. TTL ICs require a fixed d-c power supply voltage V_{CC} having the nominal value of 5V and a tolerance of 5%. Thus these ICs are not guaranteed to function with V_{CC} below 4.75V and V_{CC} in excess of 5.25V can damage the IC. A 0.1µF ceramic capacitor should be connected between the V_{CC} and Ground pins of each TTL IC to suppress spikes that may otherwise be created due to the current drawn from the power supply. Most CMOS ICs can work with $3V \leq V_{CC} \leq 15V$ and do not require capacitors at each V_{CC} pin.

Part A. Logic Levels

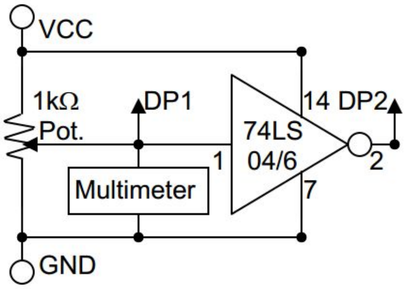


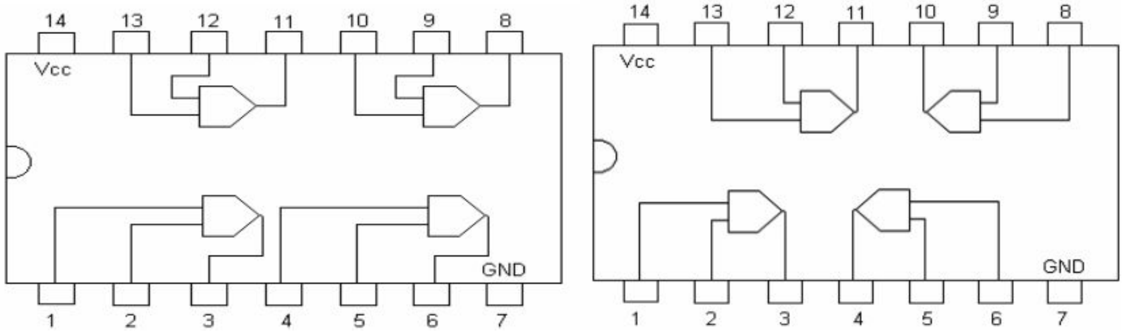
Fig. 2.1

Set up the circuit shown in Fig. 2.1 on the breadboard and turn the potentiometer shaft to one end so that the multimeter reads 0V. LG1 and LR2 should be glowing. Now rotate the potentiometer shaft gradually up to the other end and tabulate the transitions in LG1, LR2, LG2 and LR1, and the corresponding multimeter readings until one finally has LR1 and LG2 fully glowing.

Compare these voltages with the specifications for binary logic levels for a 0-5V range:

$$0 \leq V_{OL} \leq 0.4,\ 0 \leq V_{IL} \leq 0.8,\ 2.0 \leq V_{IH} \leq 5.0,\ 2.4 \leq V_{OH} \leq 5.0.$$

Part B. Gate Identification



(a) **(b)**

Fig. 2.2 Two Types of Pin Connections of Quad-2-input Gates

Six different ICs, each consisting of four AND / OR / NAND / NOR / XOR gates have been placed on the breadboard. The 4 ICs on the left belong to the TTL 74LSxx family and have the pin connections shown in Fig. 2.1(a); the remaining 2 on the right belong to the CMOS CD40xx family and have the pin connections shown in Fig. 2.1(b). Find out the logic function of each of the given ICs by proceeding step by step as follows:

1. Connect the VCC and Gnd pins of the IC to the VCC and Gnd lines on the top and the bottom of the breadboard, using RED and BLACK wires respectively.
2. Connect the two input pins of any one gate in the IC to two of the IP1-IP12 input switches, and the corresponding output pin of the IC to one of the DP1-DP8 display points provided in the Test Kit.
3. Apply the four possible combinations of (binary) values to the gate inputs one by one by means of the input switches and tabulate the corresponding values of the gate output as observed on the LED display to obtain the truth table of the gate.
4. Verify that all the four gates in the IC are identical by repeating steps 2 and 3 for the other three gates in the same IC.
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Part C. De Morgan's Theorems

De Morgan's theorems state that $(A + B)' = A' \cdot B'$ and $(A \cdot B)' = A' + B'$. Verify these theorems by proceeding step by step as follows:

1. Set up a circuit consisting of two NAND gates and one AND gate to perform the function $Y = A' \cdot B'$, using a NAND gate with its two inputs connected together to perform the NOT function.
2. Obtain the truth table of this circuit by proceeding as done in steps 1, 2 and 3 of Part A, and verify that the truth table is the same as that of a NOR gate.
3. Repeat steps 1 and 2 using an OR gate instead of an AND gate to verify that the truth table of the function $Y = A' + B'$ is the same as that of a NAND gate.

Part D. Binary Full Adder

A binary Full Adder adds two bits A and B along with a carry in C to generate SUM and CARRY bits as output. The first step to achieve this is to make a binary Half Adder, which adds two binary inputs A and B to give a sum S1 and a carry C1 according to the following Boolean expressions for the outputs S1 and C1:

$$S1 = A' \cdot B + A \cdot B' = A \oplus B \text{ and } C1 = A \cdot B.$$

Another Half Adder is then used to generate the final SUM by adding the third binary input C to the S1 bit generated by the first Half Adder:

$$SUM = S1 \oplus C.$$

The carry bit generated by this Half Adder is given by

$$C2 = S1 \cdot C.$$

Write down the complete truth table of a Full Adder, including columns for the intermediate outputs S1, C1 and C2. Find out the logic for generating the final CARRY output from C1 and C2. As XOR and AND gates are going to be used for the Half Adders, try to obtain a logic for CARRY using the same type of gates, so that the complete realisation of the Full Adder is possible without necessitating a third IC.

1. Set up the circuit of a Half Adder using an XOR gate and an AND gate. Apply the inputs A and B from two input switches and observe the outputs S1 and C1 on two LED displays for all combinations of the inputs. Tabulate these values and verify the operation of the Half Adder.
2. Set up another Half Adder using another XOR and another AND gate out of the same ICs used in step 1, and connect the C input and the S1 output generated by the first Half Adder as its inputs to generate the final SUM output and the C2 output.
3. Generate the final CARRY output from the intermediate carry outputs C1 and C2, using the unused gates in the XOR and AND ICs deployed so far.
4. Verify the truth table experimentally by applying the inputs A, B and C through three input switches and displaying the S1, C1, C2, SUM and CARRY outputs.