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Roll No - 160

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LAB 03 ALU

1. HDL Code

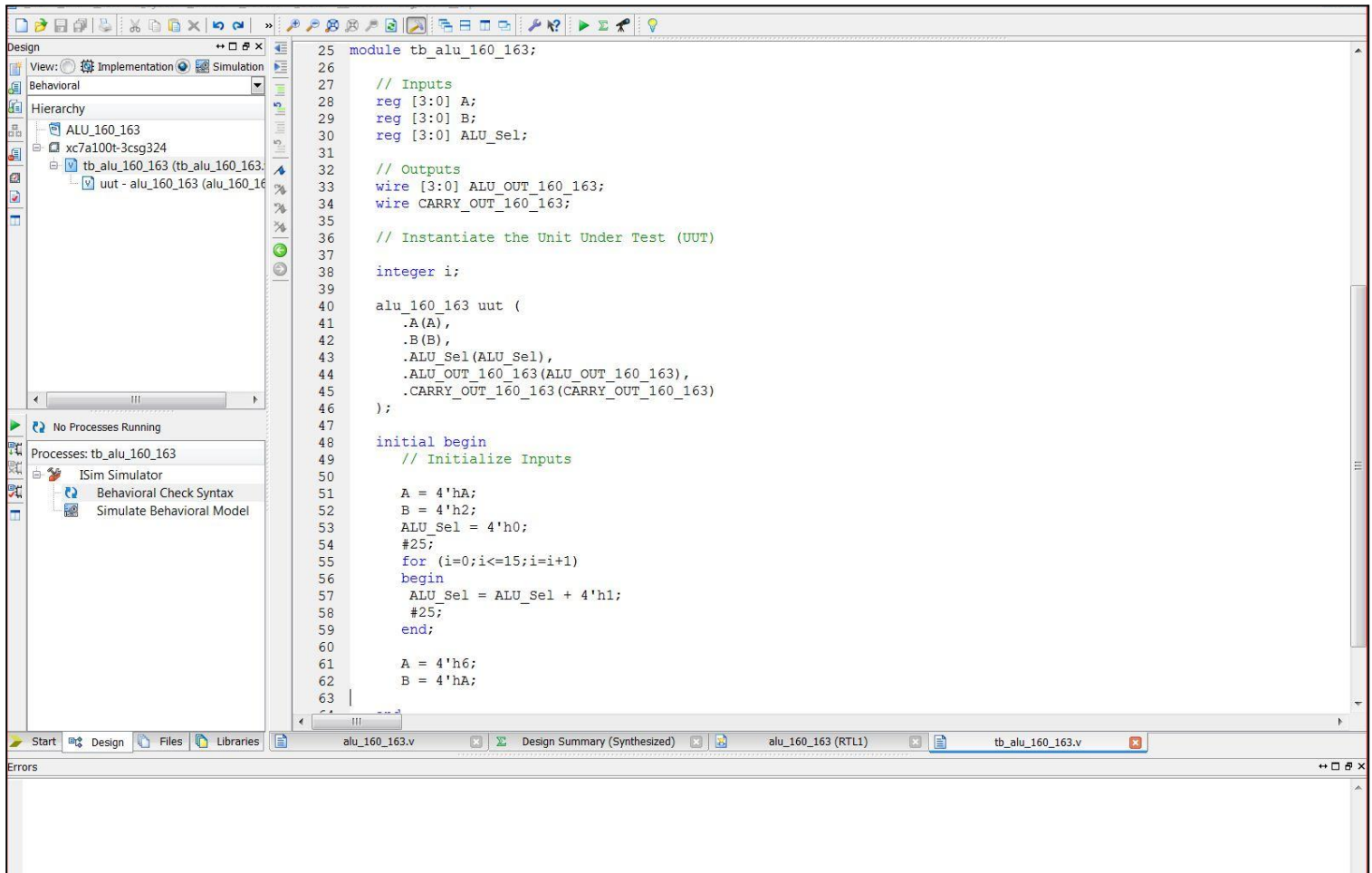
The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the HDL code for a module named `alu_160_163`. The code is as follows:

```
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////  
21 //  
22 // Pranav Unkule, 160  
23 // Rituraj Javeri, 163  
24 //  
25 module alu_160_163(  
26     input [3:0] A,  
27     input [3:0] B,  
28     input [3:0] ALU_Sel,  
29     output [3:0] ALU_OUT_160_163,  
30     output CARRY_OUT_160_163  
31 );  
32  
33 reg [3:0] ALU_Result;  
34 wire [4:0] tmp;  
35 assign ALU_OUT_160_163 = ALU_Result; // ALU out  
36 assign tmp = {1'b0,A} + {1'b0,B};  
37 assign CARRY_OUT_160_163 = tmp[4]; // Carryout flag  
38 always @(*)  
39 begin  
40     case(ALU_Sel)  
41         4'b0000: // Addition  
42             ALU_Result = A + B ;  
43         4'b0001: // Subtraction  
44             ALU_Result = A - B ;  
45         4'b0010: // Multiplication  
46             ALU_Result = A * B;  
47         4'b0011: // Division  
48             ALU_Result = A/B;  
49         4'b0100: // Logical shift left  
50             ALU_Result = A<<1;  
51         4'b0101: // Logical shift right  
52             ALU_Result = A>>1;  
53         4'b0110: // Rotate left  
54             ALU_Result = {A[2:0], A[3]};  
55     endcase  
56 end
```

The left sidebar shows the project hierarchy with `alu_160_163` selected. The bottom console window shows the following output:

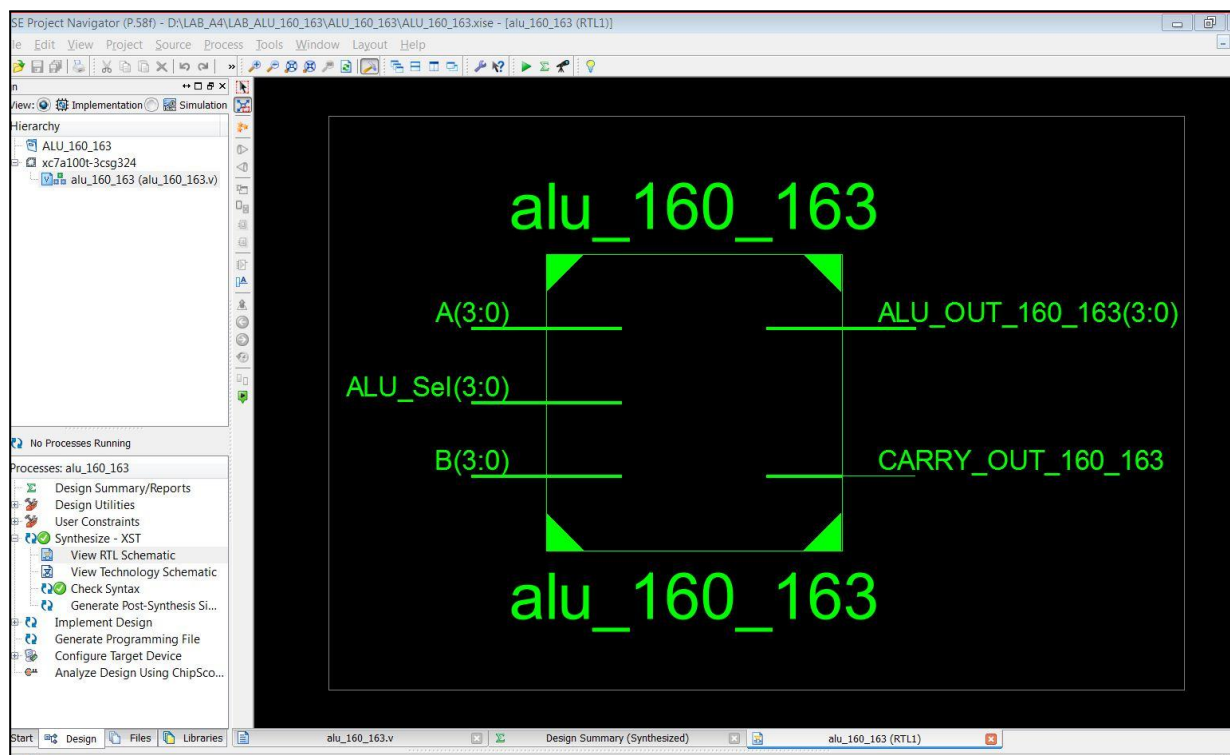
```
Number of warnings : 0 ( 0 filtered)  
Number of infos : 0 ( 0 filtered)  
  
--> Process "Check Syntax" completed successfully
```

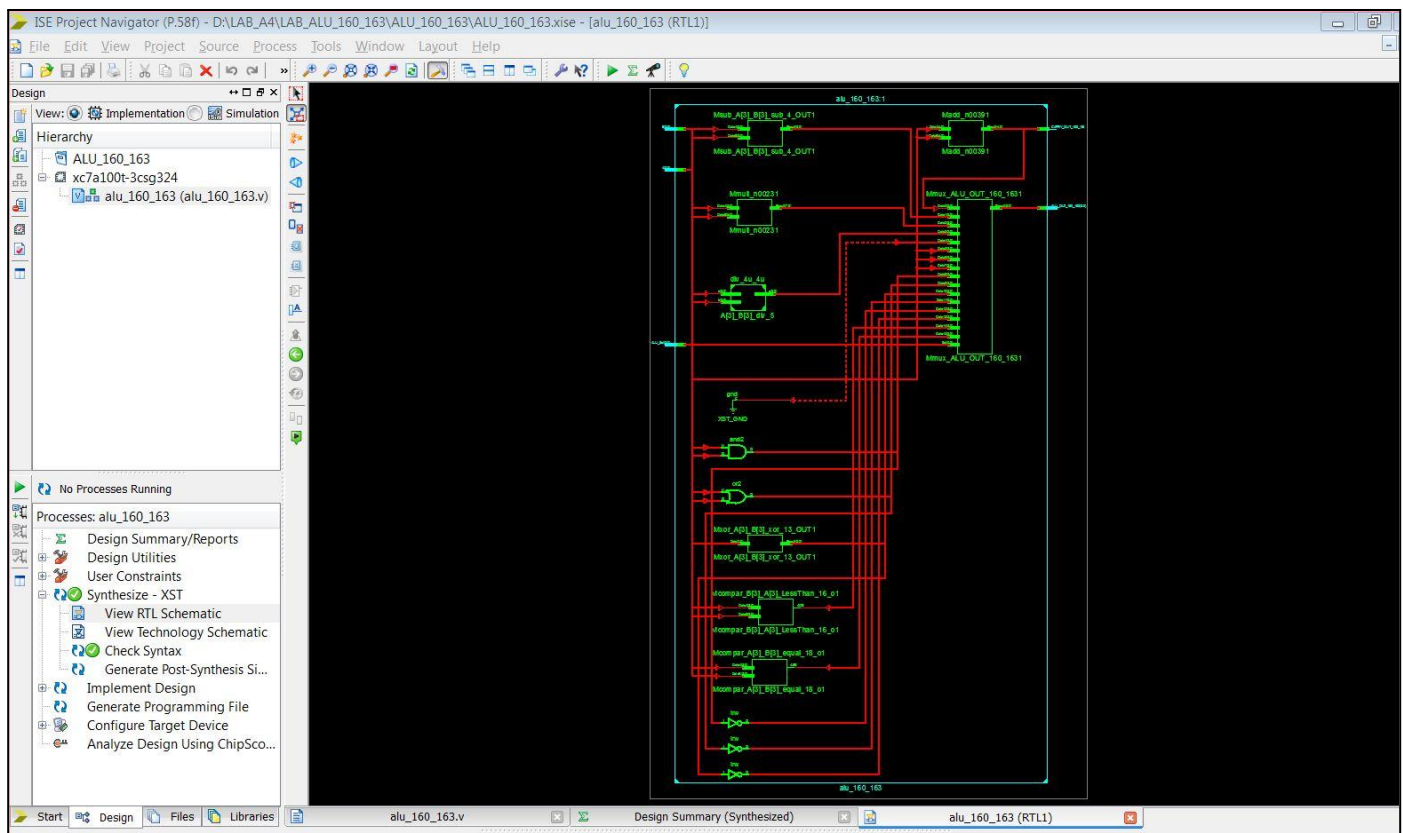
Text Bench Code



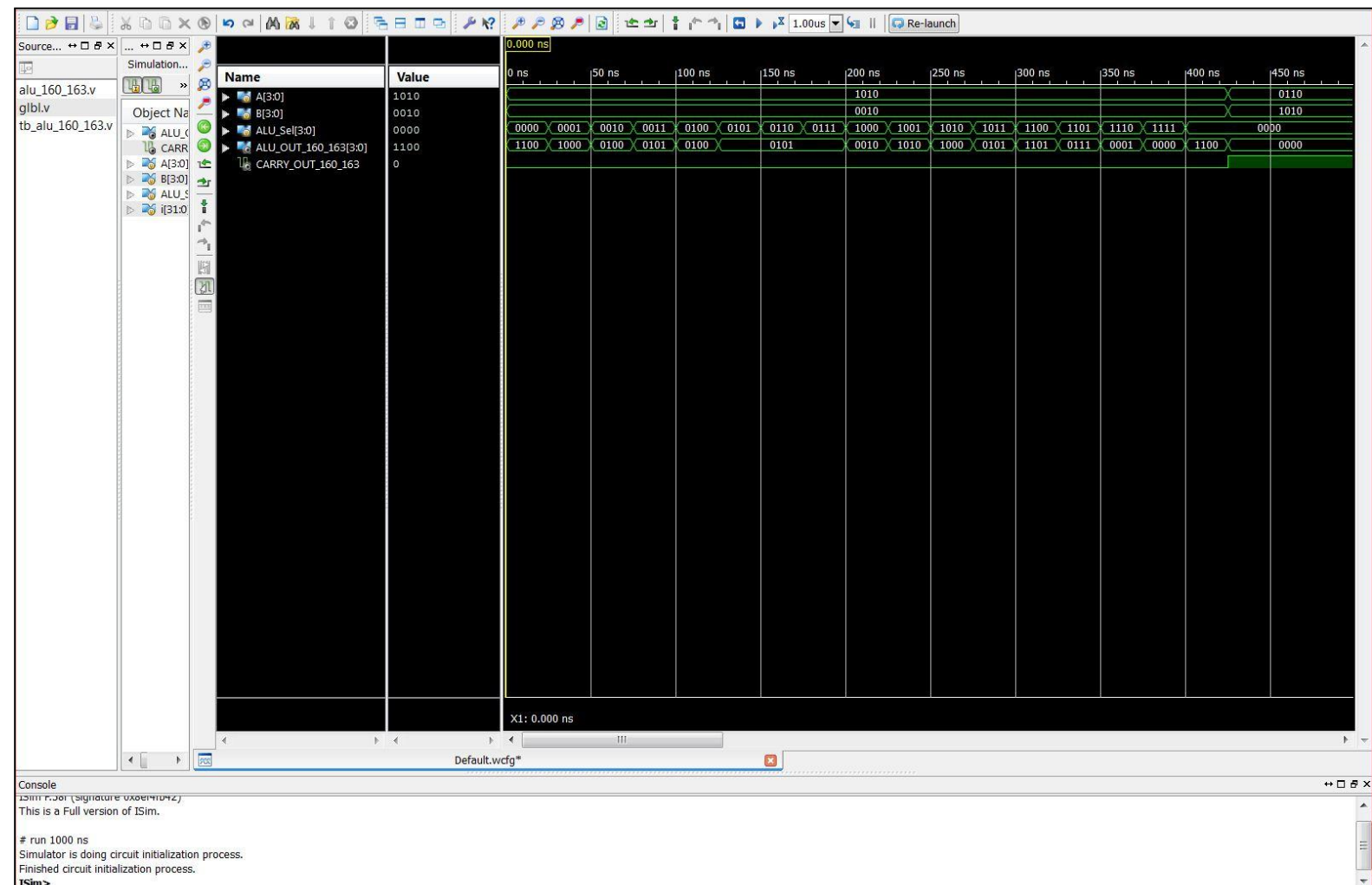
```
25 module tb_alu_160_163;
26
27 // Inputs
28 reg [3:0] A;
29 reg [3:0] B;
30 reg [3:0] ALU_Sel;
31
32 // Outputs
33 wire [3:0] ALU_OUT_160_163;
34 wire CARRY_OUT_160_163;
35
36 // Instantiate the Unit Under Test (UUT)
37
38 integer i;
39
40 alu_160_163 uut (
41     .A(A),
42     .B(B),
43     .ALU_Sel(ALU_Sel),
44     .ALU_OUT_160_163(ALU_OUT_160_163),
45     .CARRY_OUT_160_163(CARRY_OUT_160_163)
46 );
47
48 initial begin
49     // Initialize Inputs
50
51     A = 4'hA;
52     B = 4'h2;
53     ALU_Sel = 4'h0;
54     #25;
55     for (i=0;i<=15;i=i+1)
56     begin
57         ALU_Sel = ALU_Sel + 4'h1;
58         #25;
59     end;
60
61     A = 4'h6;
62     B = 4'hA;
63 end;
```

RTL Schematic





Simulation



IO Floor Plan

Synthesized Design 3

Netlist: alu_160_163, Nets (85), Primitives (73)

I/O Port Properties

Name: ALU_OUT_160_163[1]
Direction: Output
Site: U1 (Fixed)
Site type: IO_L7P_T1_34
Package pin: U1
Instance: ALU_OUT_160_163_1_OBUF

I/O Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Str...	Slew Type	Pull Type	Off-Chip ...	IN_TERM
A (4)	Input					34 LVCMOS33*	3.300				NONE	NONE	
A[3]	Input		P4	✓		34 LVCMOS33*	3.300				NONE	NONE	
A[2]	Input		P3	✓		34 LVCMOS33*	3.300				NONE	NONE	
A[1]	Input		R3	✓		34 LVCMOS33*	3.300				NONE	NONE	
A[0]	Input		T1	✓		34 LVCMOS33*	3.300				NONE	NONE	
ALU_OUT_160_163 (4)	Output					34 LVCMOS33*	3.300						
ALU_OUT_160_16...	Output		P2	✓		34 LVCMOS33*	3.300			12 SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		R2	✓		34 LVCMOS33*	3.300			12 SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		U1	✓		34 LVCMOS33*	3.300			12 SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		P5	✓		34 LVCMOS33*	3.300			12 SLOW	NONE	FP_VTT_50	
ALU_Sel (4)	Input					34 LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[3]	Input		R6	✓		34 LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[2]	Input		R7	✓		34 LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[1]	Input		U8	✓		34 LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[0]	Input		U9	✓		34 LVCMOS33*	3.300				NONE	NONE	
B (4)	Input					34 LVCMOS33*	3.300				NONE	NONE	
B[3]	Input		T3	✓		34 LVCMOS33*	3.300				NONE	NONE	
B[2]	Input		U2	✓		34 LVCMOS33*	3.300				NONE	NONE	
B[1]	Input		V2	✓		34 LVCMOS33*	3.300				NONE	NONE	
B[0]	Input		U4	✓		34 LVCMOS33*	3.300				NONE	NONE	

UCF File

ISE Project Navigator (P58f) - D:\LAB_A4\LAB_ALU_160_163\ALU_160_163\alu_160_163.ucf

File Edit View Project Source Process Tools Window Layout Help

Design: Implementation

Hierarchy: alu_160_163, xc7a100t-3csg324, alu_160_163 (alu_160_163.v), alu_160_163.ucf

No Processes Running

Processes: alu_160_163.ucf

User Constraints: Edit Constraints (Text)

```
2 # PlanAhead Generated IO constraints
3
4 NET "A[3]" IOSTANDARD = LVCMOS33;
5 NET "A[2]" IOSTANDARD = LVCMOS33;
6 NET "A[1]" IOSTANDARD = LVCMOS33;
7 NET "A[0]" IOSTANDARD = LVCMOS33;
8 NET "ALU_OUT_160_163[3]" IOSTANDARD = LVCMOS33;
9 NET "ALU_OUT_160_163[2]" IOSTANDARD = LVCMOS33;
10 NET "ALU_OUT_160_163[1]" IOSTANDARD = LVCMOS33;
11 NET "ALU_OUT_160_163[0]" IOSTANDARD = LVCMOS33;
12 NET "ALU_Sel[3]" IOSTANDARD = LVCMOS33;
13 NET "ALU_Sel[2]" IOSTANDARD = LVCMOS33;
14 NET "ALU_Sel[1]" IOSTANDARD = LVCMOS33;
15 NET "ALU_Sel[0]" IOSTANDARD = LVCMOS33;
16 NET "B[3]" IOSTANDARD = LVCMOS33;
17 NET "B[2]" IOSTANDARD = LVCMOS33;
18 NET "B[1]" IOSTANDARD = LVCMOS33;
19 NET "B[0]" IOSTANDARD = LVCMOS33;
20 NET "CARRY_OUT_160_163" IOSTANDARD = LVCMOS33;
21
22 # PlanAhead Generated physical constraints
23
24 NET "A[3]" LOC = P4;
25 NET "A[2]" LOC = P3;
26 NET "A[1]" LOC = R3;
27 NET "A[0]" LOC = T1;
28 NET "ALU_OUT_160_163[3]" LOC = P2;
29 NET "ALU_OUT_160_163[2]" LOC = R2;
30 NET "ALU_OUT_160_163[0]" LOC = P5;
31 NET "ALU_Sel[3]" LOC = R6;
32 NET "ALU_Sel[2]" LOC = R7;
33 NET "ALU_Sel[1]" LOC = U8;
34 NET "ALU_Sel[0]" LOC = U9;
35 NET "B[3]" LOC = T3;
36 NET "B[2]" LOC = U2;
37 NET "B[1]" LOC = V2;
38 NET "CARRY_OUT_160_163" LOC = T8;
39 NET "B[0]" LOC = U4;
40 NET "ALU_OUT_160_163[1]" LOC = U1;
```

Design Summary

The screenshot shows the ISE Project Navigator window with the Design Summary for the project 'alu_160_163'. The summary is divided into two main sections: Project Status and Device Utilization Summary.

alu_160_163 Project Status (09/08/2022 - 10:09:46)

Field	Value	Field	Value
Project File:	alu_160_163.xise	Parser Errors:	No Errors
Module Name:	alu_160_163	Implementation State:	Programming File Generated
Target Device:	xc7a100t-3csg324	Errors:	No Errors
Product Version:	ISE 14.5	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	126,800	0%	
Number of Slice LUTs	36	63,400	1%	
Number used as logic	36	63,400	1%	
Number using O6 output only	31			
Number using O5 output only	0			
Number using O5 and O6	5			
Number used as ROM	0			
Number used as Memory	0	19,000	0%	
Number used exclusively as route-thrus	0			
Number of occupied Slices	13	15,850	1%	
Number of LUT Flip Flop pairs used	36			
Number with an unused Flip Flop	36	36	100%	
Number with an unused LUT	0	36	0%	
Number of fully used LUT-FF pairs	0	36	0%	
Number of slice register sites lost to control set restrictions	0	126,800	0%	
Number of bonded IOBs	17	210	8%	
Number of LOCed IOBs	17	17	100%	
Number of RAMB36E1/FF036E1s	0	135	0%	
Number of RAMB18E1/FF018E1s	0	270	0%	
Number of BUFG/BUFGCTRLs	0	32	0%	

Program successfully uploaded

The screenshot shows the ISE IMPACT window with the Boundary Scan process. The 'IMPACT Flows' pane on the left lists the available operations, and the 'IMPACT Processes' pane on the right shows the progress of the 'Program' operation. The 'Boundary Scan' process is currently running, and the 'Program' operation is completed.

IMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File...)
- WebTalk Data

IMPACT Processes

Available Operations are:

- Program
- Get Device ID
- Get Device Signature/Usercode
- Read Device Status
- One Step SVF
- One Step XSVF

Boundary Scan

TOI: xc7a100t

TDQ: alu_160_163 bit

Program Succeeded