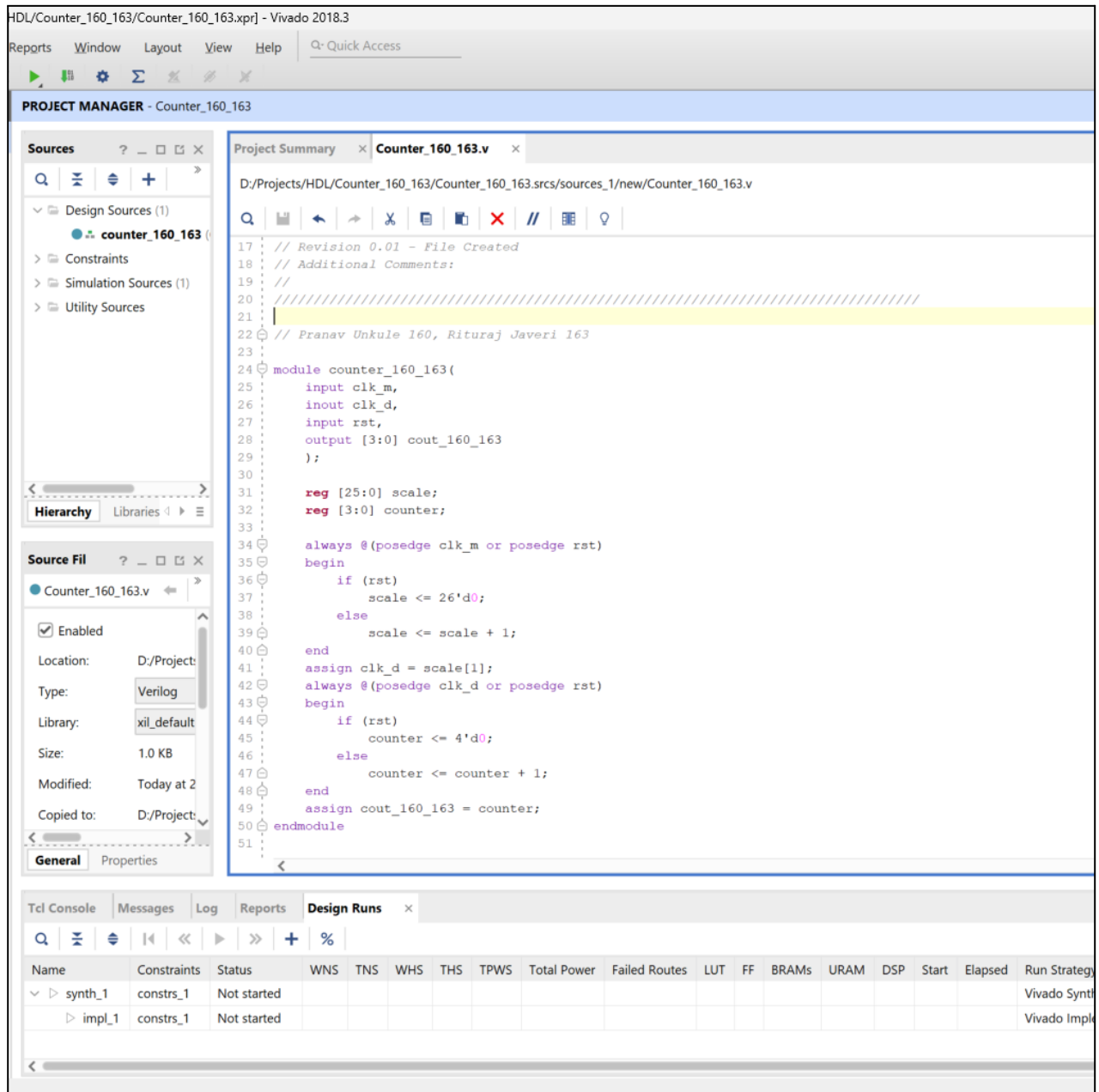
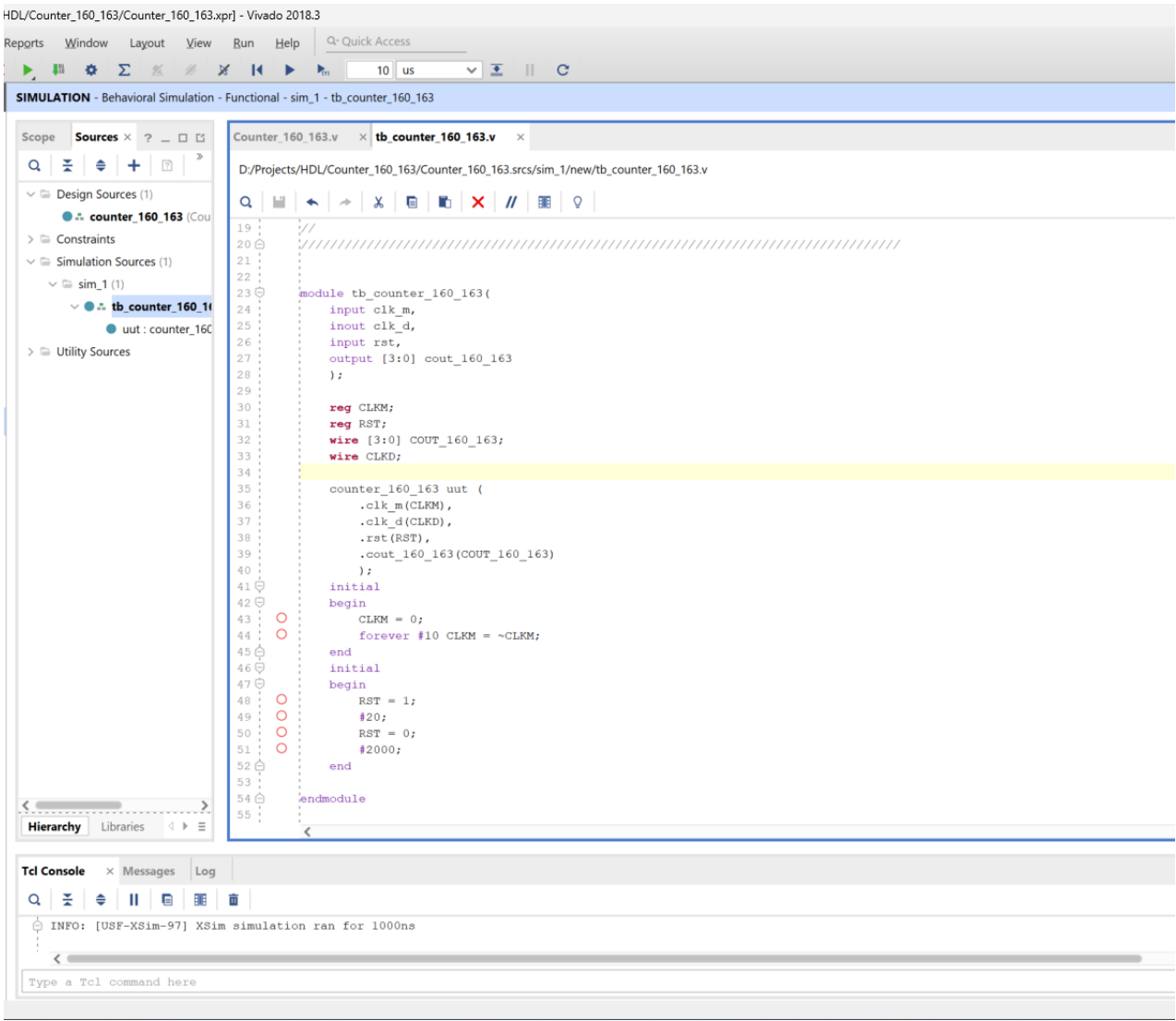


PRN - 0120190250

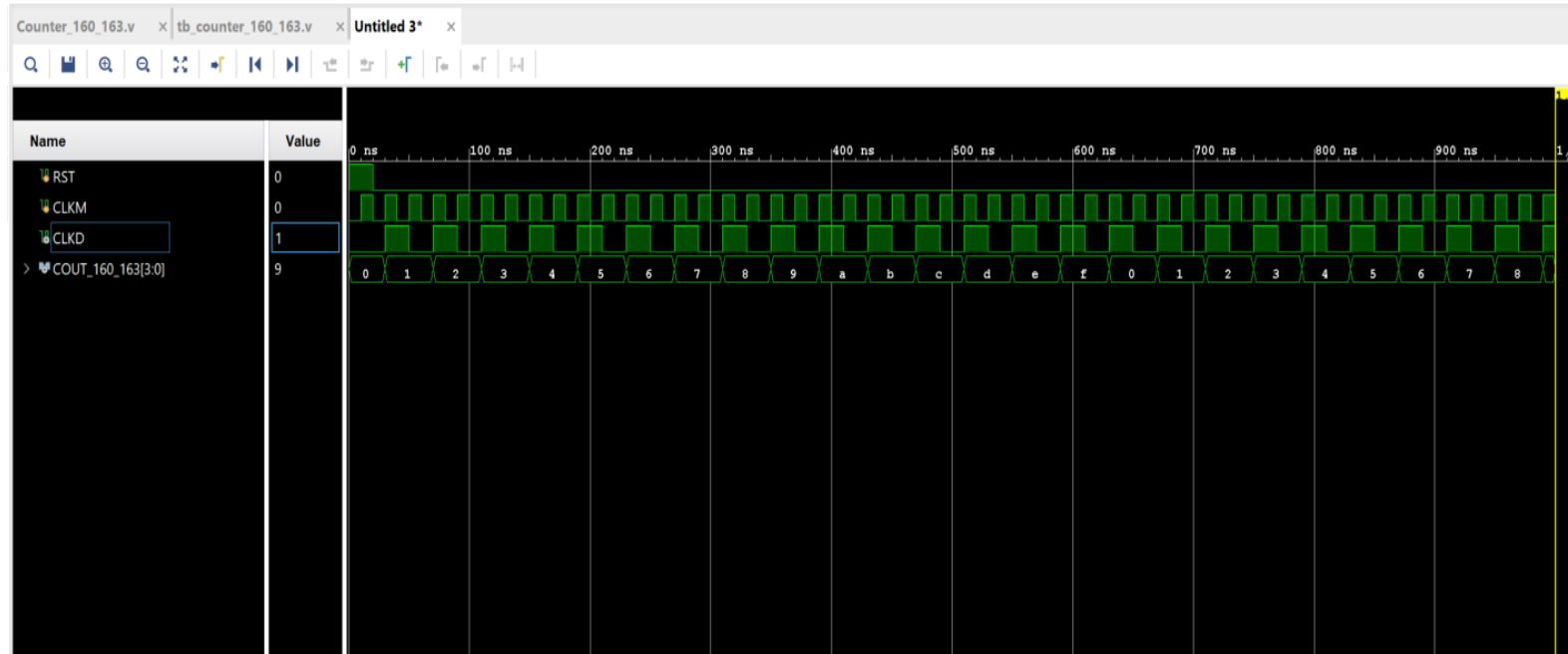
1. HDL Code



Text Bench Code



Simulation



Schematic

Counter_160_163 - [D:/Projects/HDL/Counter_160_163/Counter_160_163.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

Ready

Flow Navigator ELABORATED DESIGN - xc7a100tcs9324-1 (active)

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager

Source File Property

tb_counter_160_163.v

Location: D:/Projects/HDL/Counter_160_163/Counter_160_163.v

Type: Verilog

Library: xil_defaultlib

Size: 0.9 KB

Modified: Today at 20:51:20 PT

General Properties

Project Summary

tb_counter_160_163.v

32 Cells 7 I/O Ports 63 Nets

Schematic (2)

rst

clk_m

scale0_j

scale_reg[25:0]

RTL_ADD

RTL_REG_ASYNC

counter0_j

counter_reg[3:0]

cout_160_163[3:0]

clk_d

Tcl Console Messages Log Reports Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy	Par
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)	xc7
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)	xc7

UCF File

Counter_160_163 - [D:/Projects/HDL/Counter_160_163/Counter_160_163.xpr] - Vivado 2018.3

File Edit Flow Tools Reports Window Layout View Help Quick Access

Synthesis Out-of-date details

Flow Navigator IMPLEMENTED DESIGN - xc7a100tcs9324-1 (active)

Run Simulation

RTL ANALYSIS

- Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic

SYNTHESIS

IMPLEMENTATION

- Run Implementation
- Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager
 - Open Target
 - Program Device
 - Add Configuration Memory Device

Implemented Design is out-of-date. Implementation results were reset. Close Design

Sources

Design Sources (1)

- counter_160_163 (Counter_160_163.v)

Constraints (1)

- constrs_1 (1)

Simulation Sources (1)

- sim_1 (1)

Utility Sources

ucf.xdc (target)

ucf: counter_160_163 (Counter_160_163.v)

Project Summary

Device

Counter_160_163.v

tb_counter_160_163.v

Schematic

ucf.xdc

D:/Projects/HDL/Counter_160_163/Counter_160_163/srcs/constrs_1/new/ucf.xdc

```
1 set_property IOSTANDARD LVCMOS33 [get_ports {cout_160_163[2]}]
2 set_property IOSTANDARD LVCMOS33 [get_ports {clk_m}]
3 set_property IOSTANDARD LVCMOS33 [get_ports {cout_160_163[0]}]
4 set_property IOSTANDARD LVCMOS33 [get_ports {clk_d}]
5 set_property IOSTANDARD LVCMOS33 [get_ports {rst}]
6 set_property IOSTANDARD LVCMOS33 [get_ports {cout_160_163[3]}]
7 set_property IOSTANDARD LVCMOS33 [get_ports {cout_160_163[1]}]
8 set_property PACKAGE_PIN E3 [get_ports {clk_m}]
9 set_property PACKAGE_PIN H17 [get_ports {clk_d}]
10 set_property PACKAGE_PIN J15 [get_ports {rst}]
11 set_property PACKAGE_PIN V10 [get_ports {cout_160_163[3]}]
12 set_property PACKAGE_PIN U12 [get_ports {cout_160_163[2]}]
13 set_property PACKAGE_PIN U12 [get_ports {cout_160_163[1]}]
14 set_property PACKAGE_PIN H6 [get_ports {cout_160_163[0]}]
15
```

Hierarchy Libraries Compile Order

Tcl Console Messages Log Reports Design Runs Find Results Power DRC Methodology Timing

Name	Direction	Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM	Partition Pin Loc
clk_d	INOUT			H17	✓	15	LVCMOS33*	-	3.300	12	SLOW	NONE	FP_VTT_50	✓	N/A
clk_m	IN			E3	✓	35	LVCMOS33*	-	3.300			NONE	NONE	✓	N/A
cout_160_163[0]	OUT			H6	✓	35	LVCMOS33*	-	3.300	12	SLOW	NONE	FP_VTT_50	✓	N/A
cout_160_163[1]	OUT			U12	✓	14	LVCMOS33*	-	3.300	12	SLOW	NONE	FP_VTT_50	✓	N/A
cout_160_163[2]	OUT			U11	✓	14	LVCMOS33*	-	3.300	12	SLOW	NONE	FP_VTT_50	✓	N/A
cout_160_163[3]	OUT			V10	✓	14	LVCMOS33*	-	3.300	12	SLOW	NONE	FP_VTT_50	✓	N/A
rst	IN			J15	✓	15	LVCMOS33*	-	3.300			NONE	NONE	✓	N/A

I/O Ports in 'Schematic' (7)

15.0 Insert XDC

Design Summary

Counter_160_163.xpr] - Vivado 2018.3

LayoutViewHelpQuick Access

write_bitstream Complete

Default Layout

ELABORATED DESIGN - xc7a100tcsg324-1 (active)

SourcesNetlist

counter_160_163

Nets (63)

Leaf Cells (33)

Source File Properties

ucf.xdc

Enabled

Location: D:/Projects/HDL/Counter_160_163/C

Type: XDC

Size: 0.8 KB

Modified: Today at 21:33:40 PM

Copied to: D:/Projects/HDL/Counter_160_163/C

Read-only: No

Encrypted: No

Core Container: No

Used In

Synthesis

Implementation

Project Summary

Schematic

Counter_160_163.v

tb_counter_160_163.v

Schematic (2)

ucf.xdc

OverviewDashboard

SettingsEdit

Project name: Counter_160_163

Project location: D:/Projects/HDL/Counter_160_163

Product family: Artix-7

Project part: xc7a100tcsg324-1

Top module name: counter_160_163

Target language: Verilog

Simulator language: Mixed

Synthesis

Status: Complete

Messages: 1 warning

Part: xc7a100tcsg324-1

Strategy: Vivado Synthesis Defaults

Report Strategy: Vivado Synthesis Default Reports

Implementation

Status: Complete

Messages: 6 warnings

Part: xc7a100tcsg324-1

Strategy: Vivado Implementation Defaults

Report Strategy: Vivado Implementation Default Reports

Incremental implementation: None

DRC Violations

Summary: 2 warnings

Implemented DRC Report

Timing

Worst Negative Slack (WNS): NA

Total Negative Slack (TNS): NA

Number of Failing Endpoints: NA

Total Number of Endpoints: NA

Implemented Timing Report

Utilization

Post-Synthesis

Post-Implementation

GraphTable

LUT 1%

Power

SummaryOn-Chip

Total On-Chip Power: 17.499 W (Junction temp exceeded!)

Junction Temperature: 104.8 °C

Thermal Margin: -19.8 °C (-4.1 W)

Tcl Console

Messages

Log

Reports

Design Runs

Report

Report Type

Options

Modified

Size

Synthesis

Synth Design (synth_design)