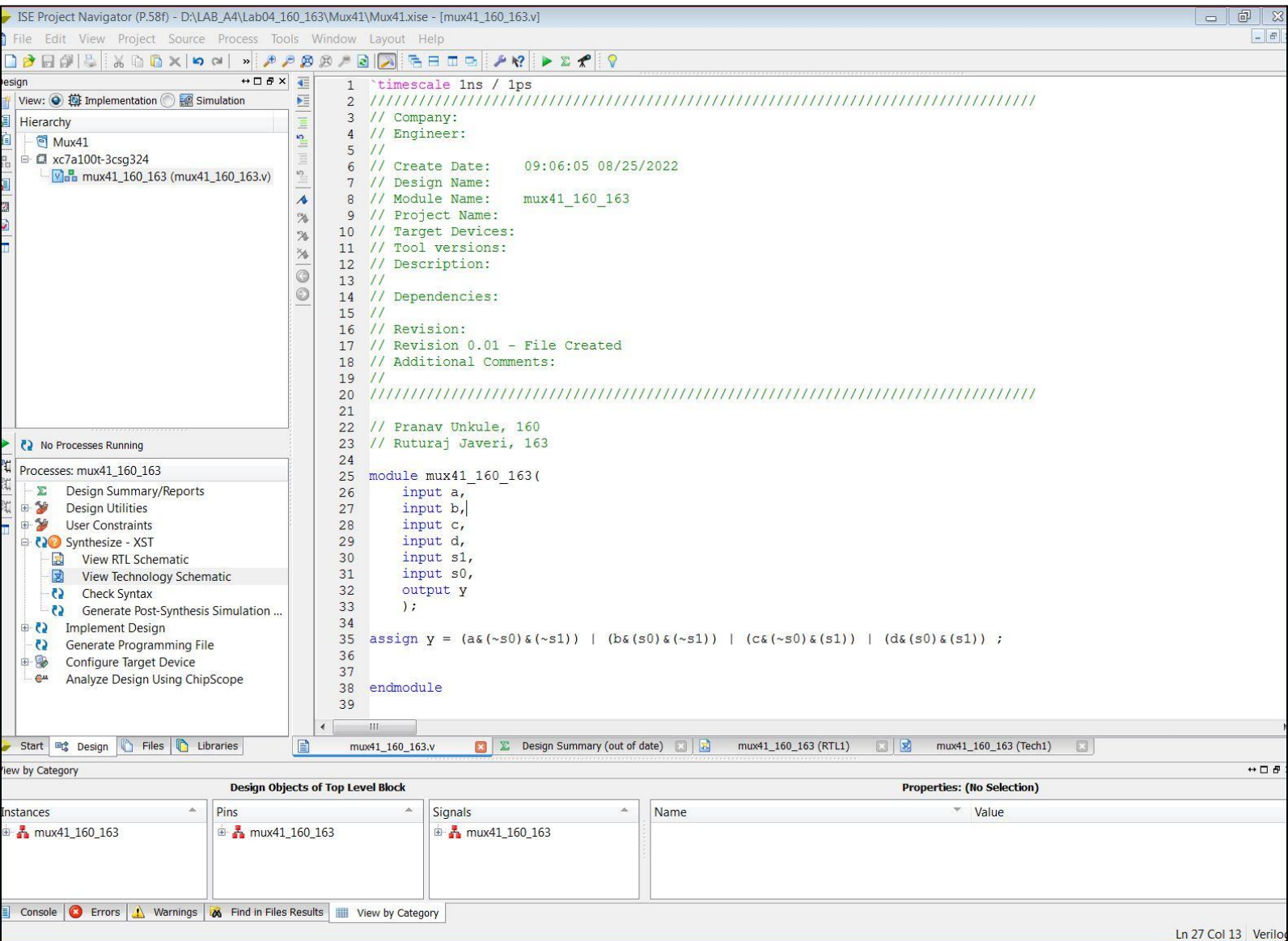


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## LAB 02 4:1 MUX

### 1. HDL Code



The screenshot displays the ISE Project Navigator interface for a project named 'mux41\_160\_163'. The main window shows the HDL code for a 4:1 MUX module. The code is as follows:

```
1 `timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    09:06:05 08/25/2022
7 // Design Name:
8 // Module Name:    mux41_160_163
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22 // Pranav Unkule, 160
23 // Ruturaj Javeri, 163
24
25 module mux41_160_163(
26     input a,
27     input b,
28     input c,
29     input d,
30     input s1,
31     input s0,
32     output y
33 );
34
35 assign y = (a & (~s0) & (~s1)) | (b & (s0) & (~s1)) | (c & (~s0) & (s1)) | (d & (s0) & (s1)) ;
36
37
38 endmodule
39
```

The interface also shows the 'Design Objects of Top Level Block' section, which includes a table of instances, pins, and signals. The 'Instances' table shows one instance of 'mux41\_160\_163'. The 'Pins' table shows the same instance with its pins. The 'Signals' table shows the same instance with its signals. The 'Properties' section is currently empty.

| Design Objects of Top Level Block |               | Properties: (No Selection) |      |       |
|-----------------------------------|---------------|----------------------------|------|-------|
| Instances                         | Pins          | Signals                    | Name | Value |
| mux41_160_163                     | mux41_160_163 | mux41_160_163              |      |       |

## 2. Test Bench Code

The screenshot displays the ISE Project Navigator interface with the Verilog test bench code for the `tb_mux41_160_163` module. The code is as follows:

```
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for module: mux41_160_163
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 ///////////////////////////////////////////////////
24
25 //Pranav Unkule, 160
26 //Ruturaj Javeri, 163
27
28 module tb_mux41_160_163;
29
30     // Inputs
31     reg a;
32     reg b;
33     reg c;
34     reg d;
35     reg s1;
36     reg s0;
37
38     // Outputs
39     wire y;
40
41     // Instantiate the Unit Under Test (UUT)
42     mux41_160_163 uut (
43         .a(a),
44         .b(b),
45         .c(c),
46         .d(d),
47         .s1(s1),
48         .s0(s0),
49         .y(y)
50     );
51
```

The interface also shows the Design Objects of Top Level Block and Properties of Instance: mux41\_160\_163.

| Design Objects of Top Level Block |               |               | Properties of Instance: mux41_160_163 |                 |
|-----------------------------------|---------------|---------------|---------------------------------------|-----------------|
| Instances                         | Pins          | Signals       | Name                                  | Value           |
| mux41_160_163                     | mux41_160_163 | mux41_160_163 | Type                                  | mux41_160_163:1 |
|                                   |               |               | SHREG_MIN_SIZE                        | 2               |
|                                   |               |               | SHREG_EXTRACT_NGC                     | YES             |
|                                   |               |               | OriginalSymbol                        | mux41_160_163   |

Ln 26 Col 22 | Verilog

### 3. RTL Schematic

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the RTL Schematic for the block `mux41_160_163`. The schematic is a large rectangle with a black background and green text. The text `mux41_160_163` is written in green at the top and bottom. On the left side, there are four input signals labeled `a`, `b`, `c`, and `d`. On the right side, there are two output signals labeled `y` and `s1`. The signal `s0` is also labeled on the left side. The interface includes a Hierarchy pane on the left showing the project structure, a Processes pane showing the synthesis process, and a Design Objects of Top Level Block pane at the bottom. The Design Objects pane shows the block `mux41_160_163` with its pins and signals. The Properties pane on the right shows the properties for the selected block.

SE Project Navigator (P.58f) - D:\LAB\_A4\Lab04\_160\_163\Mux41\Mux41.xise - [mux41\_160\_163 (RTL2)]

File Edit View Project Source Process Tools Window Layout Help

View: Implementation Simulation

Hierarchy

- Mux41
  - xc7a100t-3csg324
    - mux41\_160\_163 (mux41\_160\_163.v)

No Processes Running

Processes: mux41\_160\_163

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
  - View RTL Schematic
  - View Technology Schematic
  - Check Syntax
  - Generate Post-Synthesis Simulation ...
- Implement Design
  - Generate Programming File
  - Configure Target Device
  - Analyze Design Using ChipScope

Start Design Files Libraries

Design Objects of Top Level Block

| Name | Value |
|------|-------|
|      |       |

Console Errors Warnings Find in Files Results View by Category

[124]

SE Project Navigator (P.58f) - D:\LAB\_A4\Lab04\_160\_163\Mux41\Mux41.xise - [mux41\_160\_163 (Tech3)]

FileEditViewProjectSourceProcessToolsWindowLayoutHelp

View: ImplementationSimulation

Hierarchy

Mux41xc7a100t-3csg324mux41\_160\_163 (mux41\_160\_163.v)

No Processes Running

Processes: mux41\_160\_163

Design Summary/ReportsDesign UtilitiesUser ConstraintsSynthesize - XSTView RTL SchematicView Technology SchematicCheck SyntaxGenerate Post-Synthesis Simulation ...Implement DesignGenerate Programming FileConfigure Target DeviceAnalyze Design Using ChipScope

mux41\_160\_163.vDesign Summary (Synthesized)mux41\_160\_163 (RTL2)mux41\_160\_163 (Tech2)mux41\_160\_163 (Tech3)

by Category

Design Objects of Top Level Block

Instances

mux41\_160\_163

Pins

mux41\_160\_163

Signals

mux41\_160\_163

Properties of Instance: mux41\_160\_163

| Name              | Value           |
|-------------------|-----------------|
| Type              | mux41_160_163:1 |
| SHREG_MIN_SIZE    | 2               |
| SHREG_EXTRACT_NGC | YES             |
| OriginalSymbol    | mux41_160_163   |

ConsoleErrorsWarningsFind in Files ResultsView by Category

f-444

mux41\_160\_163:1

ibufc\_IBUF

ibufa\_IBUF

ibufb\_IBUF

ibufd\_IBUF

ibufs1\_IBUF

ibufs0\_IBUF

lut6

y1

obufy\_OBUF

mux41\_160\_163

ISE Project Navigator (P.58f) - D:\LAB\_A4\Lab04\_160\_163\Mux41\Mux41.xise - [mux41\_160\_163 (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

Mux41

xc7a100t-3csg324

mux41\_160\_163 (mux41\_160\_163.v)

No Processes Running

Processes: mux41\_160\_163

Design Summary/Reports

Design Utilities

User Constraints

Synthesize - XST

View RTL Schematic

View Technology Schematic

Check Syntax

Generate Post-Synthesis Simulation ...

Implement Design

Generate Programming File

Configure Target Device

Analyze Design Using ChipScope

Start

Design

Files

Libraries

mux41\_160\_163.v

Design Summary (out of date)

mux41\_160\_163 (RTL1)

mux41\_160\_163 (Tech1)

View by Category

Design Objects of Top Level Block

Instances

mux41\_160\_163

Pins

mux41\_160\_163

Signals

mux41\_160\_163

Properties: (No Selection)

Name

Value

Console

Errors

Warnings

Find in Files Results

View by Category

[ -192,996 ]

mux41\_160\_163:1

s1

s0

s

c

b

a

and3

d\_s1\_AND\_8\_o1

and3b1

c\_s1\_AND\_6\_o1

and3b1

b\_s1\_AND\_4\_o1

and3b2

a\_s1\_AND\_2\_o1

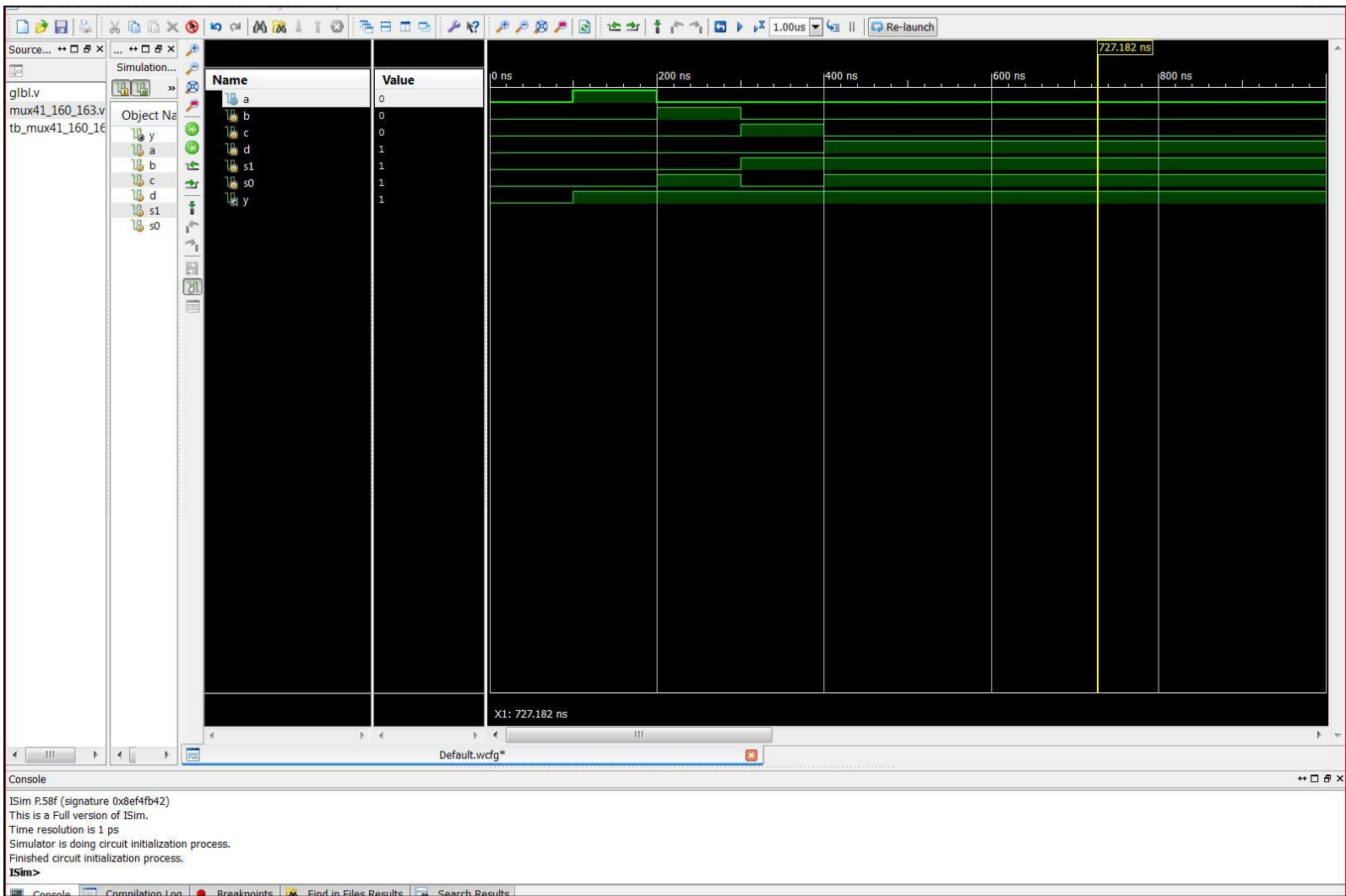
or4

y1

y

mux41\_160\_163

## 4. Simulation





5. IO Planning

File Edit Tools Window Layout View Help

Netlist

mux41\_160\_163

Nets (14)

Primitives (8)

I/O Port Properties

Name: a

Direction: Input

Site: P4 ☒ Fixed

Site type: IO\_L14P\_T2\_SRCC\_34

Package pin: P4

Instance: a\_IBUF

Net: a

Bank: I/O Bank: 34 (High Range)

Tile: R10B33\_X57Y71

Clock region: X1Y1

General

Attributes

Configure

Power

Properties

Clock Regions

Package x Device x Schematic x

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

T

U

V

I/O Ports

| Name             | Direction | Neg Diff Pair | Site | Fixed                               | Bank | I/O Std      | Vcco  | Vref | Drive Str... | Slew Type | Pull Type | Off-Chip ... | IN_TERM |
|------------------|-----------|---------------|------|-------------------------------------|------|--------------|-------|------|--------------|-----------|-----------|--------------|---------|
| All ports (7)    |           |               |      |                                     |      |              |       |      |              |           |           |              |         |
| Scalar ports (7) |           |               |      |                                     |      |              |       |      |              |           |           |              |         |
| a                | Input     |               | P4   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| b                | Input     |               | P3   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| c                | Input     |               | R3   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| d                | Input     |               | T1   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| s0               | Input     |               | U8   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| s1               | Input     |               | U9   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      |              |           | NONE      | NONE         |         |
| y                | Output    |               | P2   | <input checked="" type="checkbox"/> |      | 34 LVCMOS33* | 3.300 |      | 12 SLOW      |           | NONE      | FP_VTT_50    |         |

## 6. UCF File

The screenshot displays the Xilinx ISE Project Navigator interface. The main editor window shows the content of the UCF file, which is divided into two sections: PlanAhead Generated IO constraints and PlanAhead Generated physical constraints. The left sidebar shows the project hierarchy, and the bottom status bar indicates the current file is mux41\_160\_163.ucf.

```
1
2 # PlanAhead Generated IO constraints
3
4 NET "a" IOSTANDARD = LVCMOS33;
5 NET "b" IOSTANDARD = LVCMOS33;
6 NET "c" IOSTANDARD = LVCMOS33;
7 NET "d" IOSTANDARD = LVCMOS33;
8 NET "s0" IOSTANDARD = LVCMOS33;
9 NET "s1" IOSTANDARD = LVCMOS33;
10 NET "y" IOSTANDARD = LVCMOS33;
11
12 # PlanAhead Generated physical constraints
13
14 NET "b" LOC = P3;
15 NET "c" LOC = R3;
16 NET "d" LOC = T1;
17 NET "s0" LOC = U8;
18 NET "s1" LOC = U9;
19 NET "y" LOC = P2;
20 NET "a" LOC = P4;
21
```

The bottom status bar shows the following information:

- Start Design Files Libraries
- Design Summary (running)
- mux41\_160\_163 (RTL2)
- mux41\_160\_163 (Tech2)
- mux41\_160\_163 (Tech3)
- tb\_mux41\_160\_163.v
- mux41\_160\_163.ucf

The bottom panel shows the Design Objects of Top Level Block and Properties of Instance: mux41\_160\_163.

| Design Objects of Top Level Block |               |               | Properties of Instance: mux41_160_163 |                 |
|-----------------------------------|---------------|---------------|---------------------------------------|-----------------|
| Instances                         | Pins          | Signals       | Name                                  | Value           |
| mux41_160_163                     | mux41_160_163 | mux41_160_163 | Type                                  | mux41_160_163:1 |
|                                   |               |               | SHREG_MIN_SIZE                        | 2               |
|                                   |               |               | SHREG_EXTRACT_NGC                     | YES             |
|                                   |               |               | OriginalSymbol                        | mux41_160_163   |

Ln 1 Col 1 UCF



## 7. Design Summary

ISE Project Navigator (P.58f) - D:\LAB\_A4\Lab04\_160\_163\Mux41\Mux41.xise - [Design Summary (Programming File Generated)]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- Mux41
  - xc7a100t-3csg324
    - mux41\_160\_163 (mux41\_160\_163.v)
      - mux41\_160\_163.ucf

Design Overview

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- Static Timing
- Errors and Warnings
  - Parser Messages
  - Synthesis Messages
  - Translation Messages
  - Map Messages
  - Place and Route Messages
  - Timing Messages
  - Bitgen Messages
  - All Implementation Messages
- Detailed Reports
  - Synthesis Report
  - Translation Report
  - Map Report
  - Place and Route Report
  - Post-PAR Static Timing ...
  - Power Report
  - Bitgen Report
- Secondary Reports
- Design Properties
  - Enable Message Filtering
- Optional Design Summary Contents
  - Show Clock Report
  - Show Failing Constraints
  - Show Warnings
  - Show Errors

No Processes Running

Processes: mux41\_160\_163

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- Implement Design
  - Translate
  - Map
  - Place & Route
  - Generate Programming File
  - Configure Target Device
  - Analyze Design Using ChipScope

mux41\_160\_163 Project Status (08/25/2022 - 09:37:34)

|                  |                           |                       |                               |
|------------------|---------------------------|-----------------------|-------------------------------|
| Project File:    | Mux41.xise                | Parser Errors:        | No Errors                     |
| Module Name:     | mux41_160_163             | Implementation State: | Programming File Generated    |
| Target Device:   | xc7a100t-3csg324          | Errors:               | No Errors                     |
| Product Version: | ISE 14.5                  | Warnings:             | No Warnings                   |
| Design Goal:     | Balanced                  | Routing Results:      | All Signals Completely Routed |
| Design Strategy: | Xilinx Default (unlocked) | Timing Constraints:   |                               |
| Environment:     | System Settings           | Final Timing Score:   | 0 (Timing Report)             |

Device Utilization Summary

| Slice Logic Utilization   | Used | Available | Utilization | Note(s) |
|---|------|-----------|-------------|---------|
| Number of Slice Registers                                       | 0    | 126,800   | 0%          |         |
| Number of Slice LUTs  | 1    | 63,400    | 1%          |         |
| Number used as logic  | 1    | 63,400    | 1%          |         |
| Number using O6 output only                                     | 1    |           |             |         |
| Number using O5 output only                                     | 0    |           |             |         |
| Number using O5 and O6  | 0    |           |             |         |
| Number used as ROM  | 0    |           |             |         |
| Number used as Memory   | 0    | 19,000    | 0%          |         |
| Number used exclusively as route-thrus                          | 0    |           |             |         |
| Number of occupied Slices                                       | 1    | 15,850    | 1%          |         |
| Number of LUT Flip Flop pairs used                              | 1    |           |             |         |
| Number with an unused Flip Flop                                 | 1    | 1         | 100%        |         |
| Number with an unused LUT                                       | 0    | 1         | 0%          |         |
| Number of fully used LUT-FF pairs                               | 0    | 1         | 0%          |         |
| Number of slice register sites lost to control set restrictions | 0    | 126,800   | 0%          |         |
| Number of bonded IOBs   | 7    | 210       | 3%          |         |
| Number of LOCed IOBs  | 7    | 7         | 100%        |         |
| Number of RAMB36E1/FIFO36E1s                                    | 0    | 135       | 0%          |         |
| Number of RAMB18E1/FIFO18E1s                                    | 0    | 270       | 0%          |         |
| Number of BUFG/BUFGCTRLs  | 0    | 32        | 0%          |         |

Start Design Files Libraries

mux41\_160\_163.v Design Summary (Programming File Generated) mux41\_160\_163 (RTL2) mux41\_160\_163 (Tech2) mux41\_160\_163 (Tech3) tb\_mux

View by Category

Design Objects of Top Level Block

Instances

- mux41\_160\_163

Pins

- mux41\_160\_163

Signals

- mux41\_160\_163

Properties of Instance: mux41\_160\_163

| Name              | Value           |
|-------------------|-----------------|
| Type              | mux41_160_163:1 |
| SHREG_MIN_SIZE    | 2               |
| SHREG_EXTRACT_NGC | YES             |
| OriginalSymbol    | mux41_160_163   |

Console Errors Warnings Find in Files Results View by Category

## 8. Program successfully uploaded

