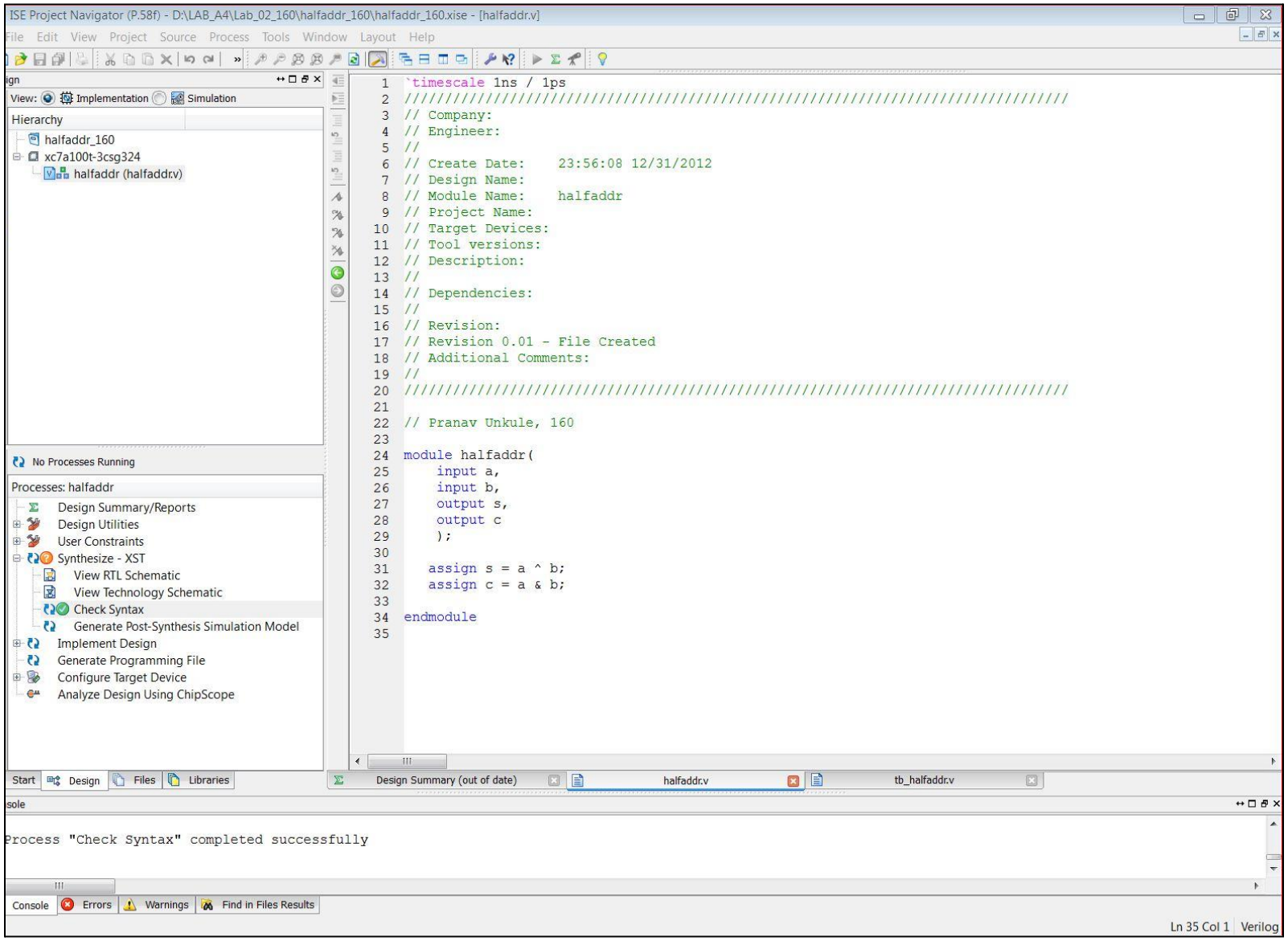
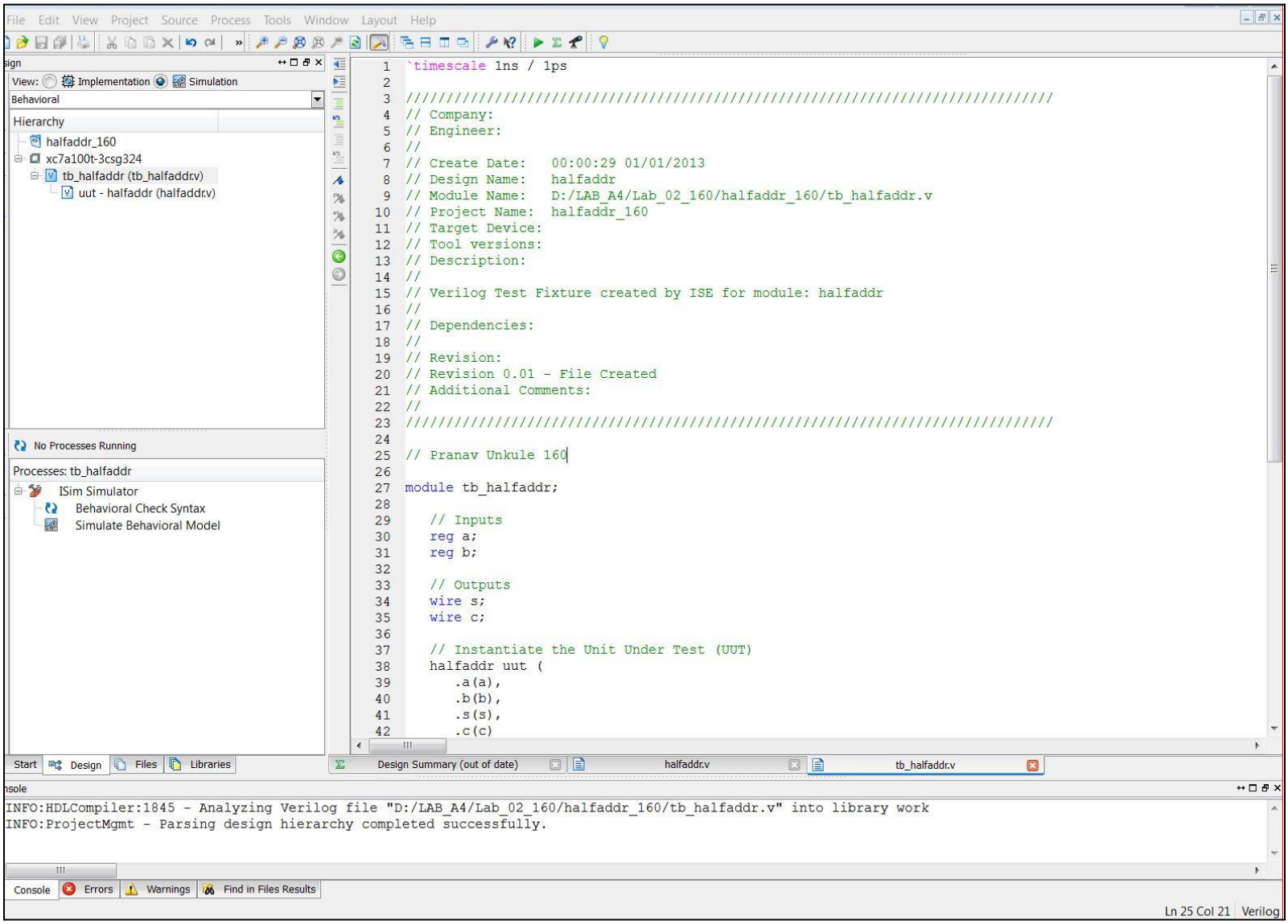
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

LAB 01 Half Adder

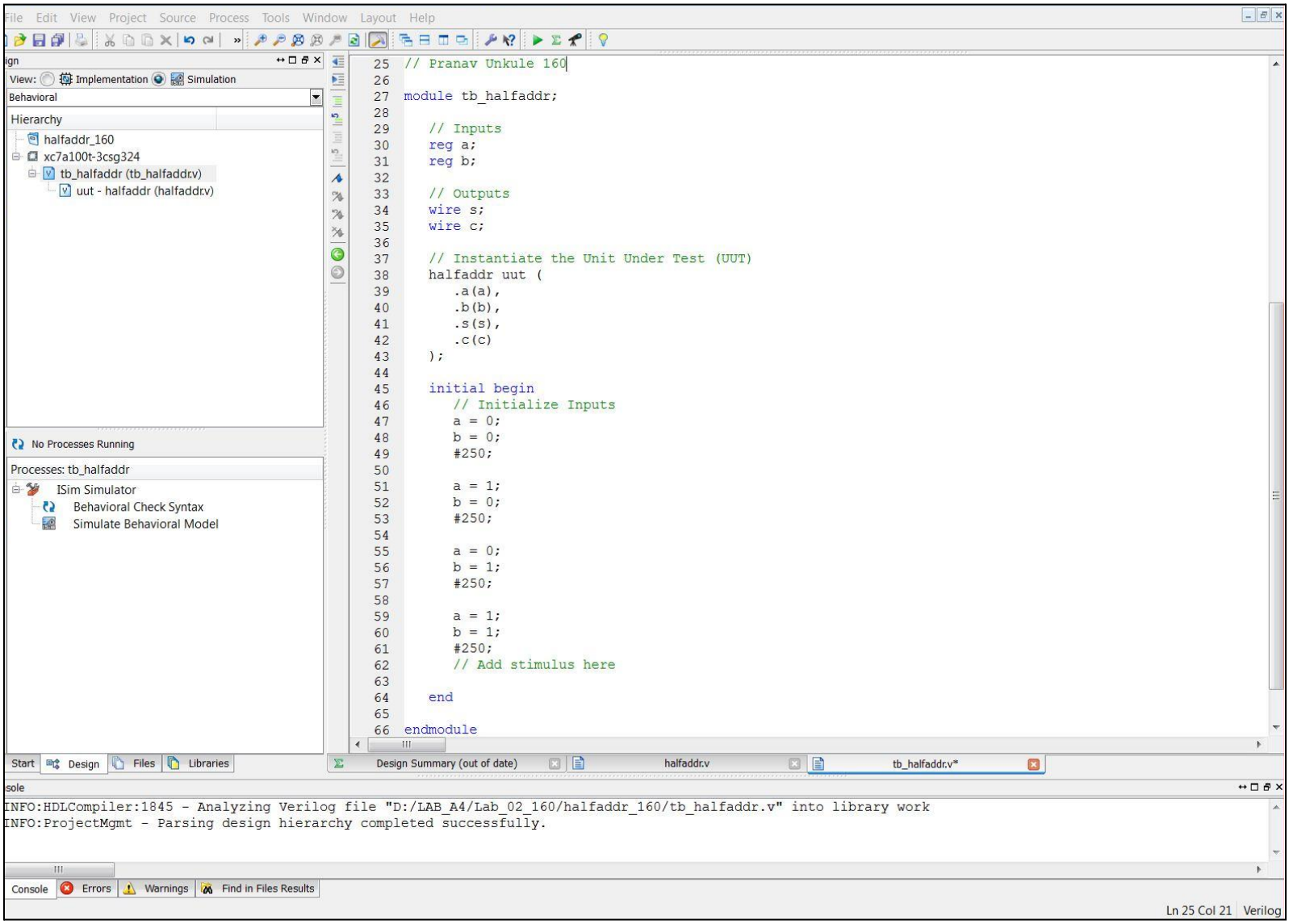
1. HDL Code



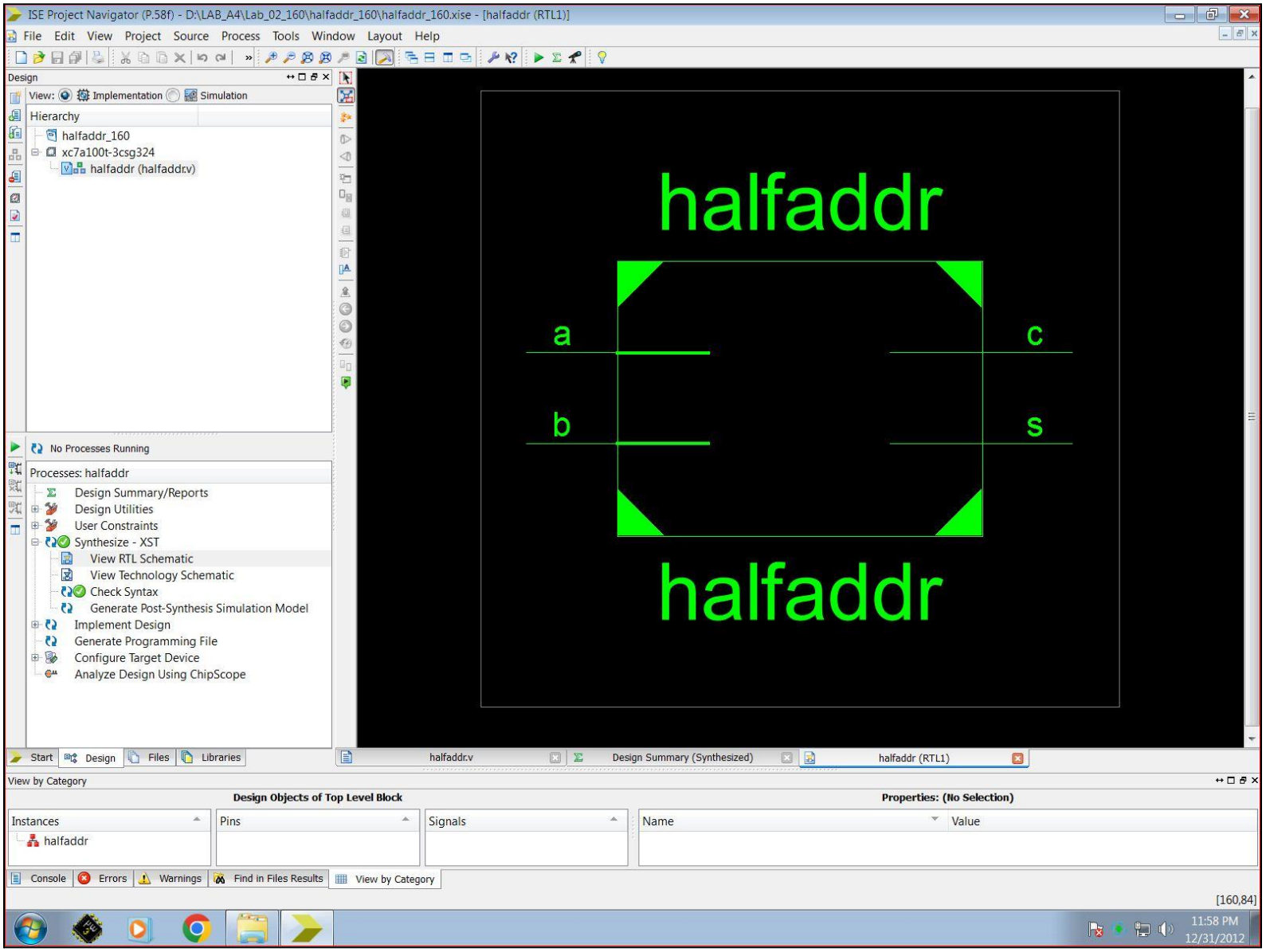
2. Test Bench Code

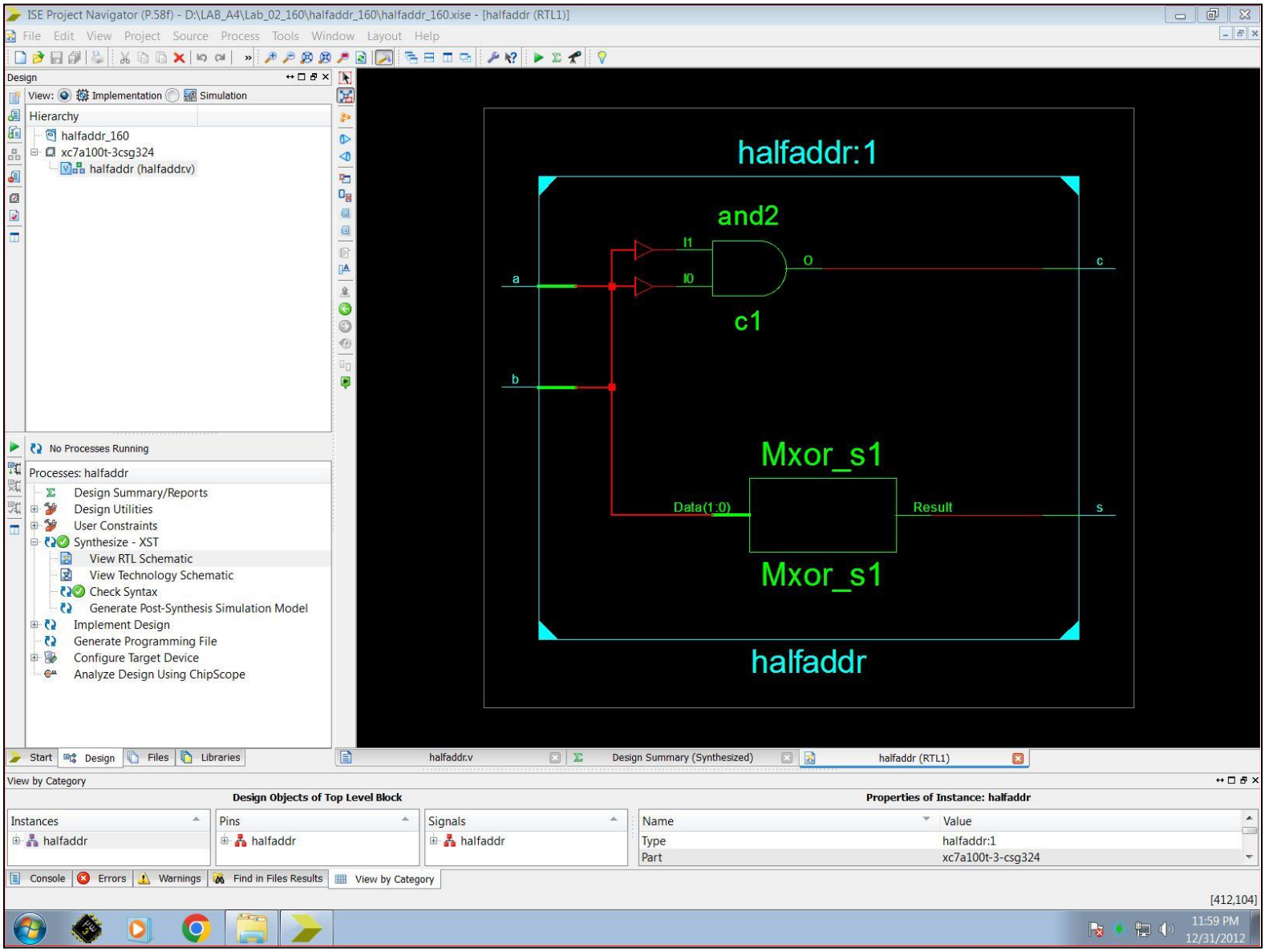



```
1  `timescale 1ns / 1ps
2
3  //////////////////////////////////////////////////////////////////////////////////
4  // Company:
5  // Engineer:
6  //
7  // Create Date:   00:00:29 01/01/2013
8  // Design Name:   halfaddr
9  // Module Name:   D:/LAB_A4/Lab_02_160/halfaddr_160/tb_halfaddr.v
10 // Project Name:  halfaddr_160
11 // Target Device:
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for module: halfaddr
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 //////////////////////////////////////////////////////////////////////////////////
24
25 // Pranav Unkule 160
26
27 module tb_halfaddr;
28
29    // Inputs
30    reg a;
31    reg b;
32
33    // Outputs
34    wire s;
35    wire c;
36
37    // Instantiate the Unit Under Test (UUT)
38    halfaddr uut (
39       .a(a),
40       .b(b),
41       .s(s),
42       .c(c)
```

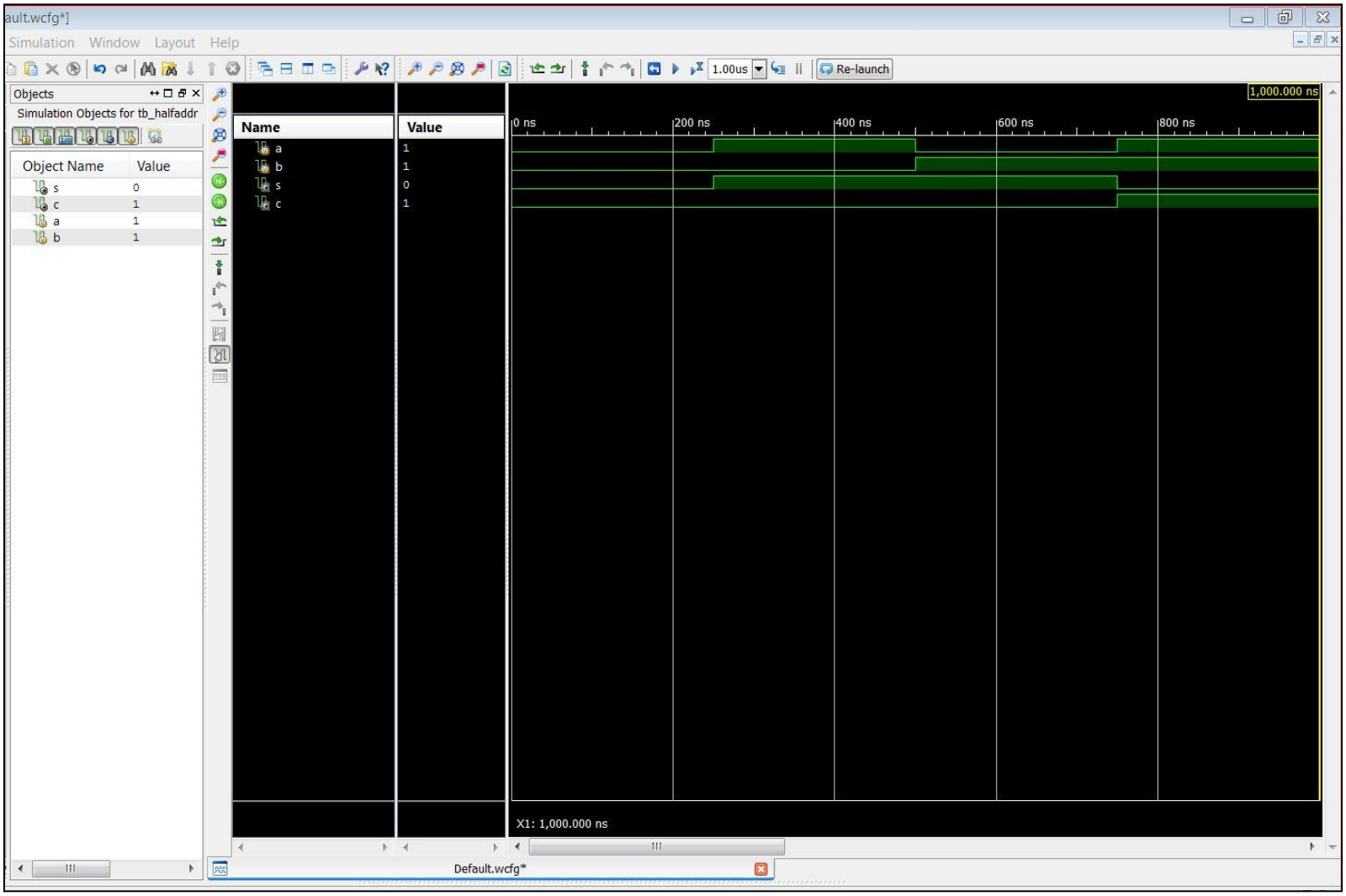

File Edit View Project Source Process Tools Window Layout Help
View: Implementation Simulation
Behavioral
Hierarchy
halfaddr_160
xc7a100t-3csg324
tb_halfaddr (tb_halfaddr.v)
uut - halfaddr (halfaddr.v)
No Processes Running
Processes: tb_halfaddr
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
Start Design Files Libraries
25 // Pranav Unkule 160
26
27 module tb_halfaddr;
28
29 // Inputs
30 reg a;
31 reg b;
32
33 // Outputs
34 wire s;
35 wire c;
36
37 // Instantiate the Unit Under Test (UUT)
38 halfaddr uut (
39 .a(a),
40 .b(b),
41 .s(s),
42 .c(c)
43);
44
45 initial begin
46 // Initialize Inputs
47 a = 0;
48 b = 0;
49 #250;
50
51 a = 1;
52 b = 0;
53 #250;
54
55 a = 0;
56 b = 1;
57 #250;
58
59 a = 1;
60 b = 1;
61 #250;
62 // Add stimulus here
63
64 end
65
66 endmodule
Design Summary (out of date)
halfaddr.v
tb_halfaddr.v*
INFO:HDLCompiler:1845 - Analyzing Verilog file "D:/LAB_A4/Lab_02_160/halfaddr_160/tb_halfaddr.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Console Errors Warnings Find in Files Results
Ln 25 Col 21 Verilog

3. RTL Schematic

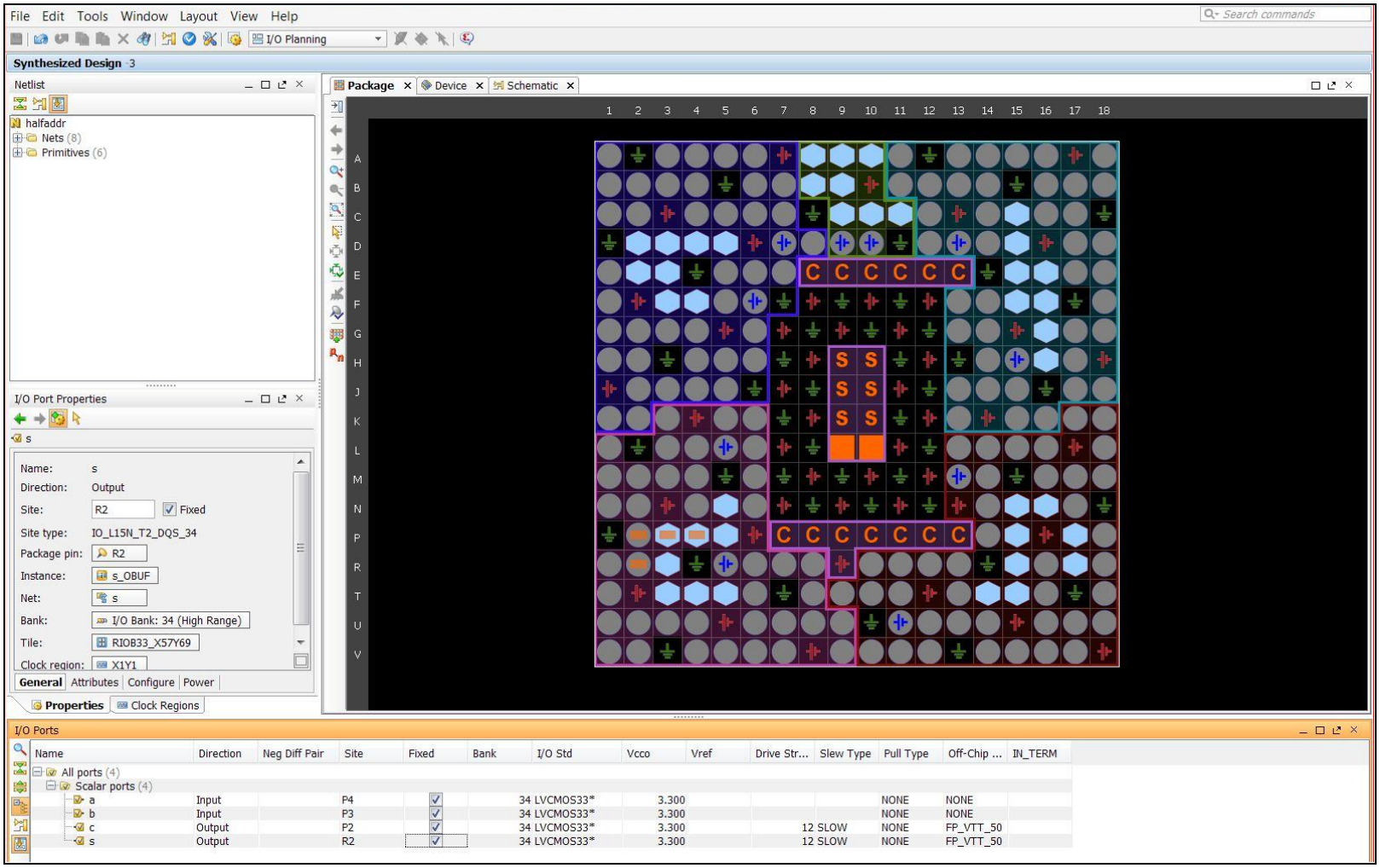



ISE Project Navigator (P.58f) - D:\LAB_A4\Lab_02_160\halfaddr_160\halfaddr_160.xise - [halfaddr (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
halfaddr_160
xc7a100t-3csg324
halfaddr (halfaddr.v)
No Processes Running
Processes: halfaddr
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation Model
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
halfaddr:1
and2
I1
I0
O
a
b
c
c1
Mxor_s1
Data(1:0)
Result
s
Mxor_s1
halfaddr
Start Design Files Libraries
halfaddr.v
Design Summary (Synthesized)
halfaddr (RTL1)
View by Category
Design Objects of Top Level Block
Instances
halfaddr
Pins
halfaddr
Signals
halfaddr
Properties of Instance: halfaddr
Name
Value
Type
halfaddr:1
Part
xc7a100t-3-csg324
Console Errors Warnings Find in Files Results View by Category
[412,104]
11:59 PM
12/31/2012

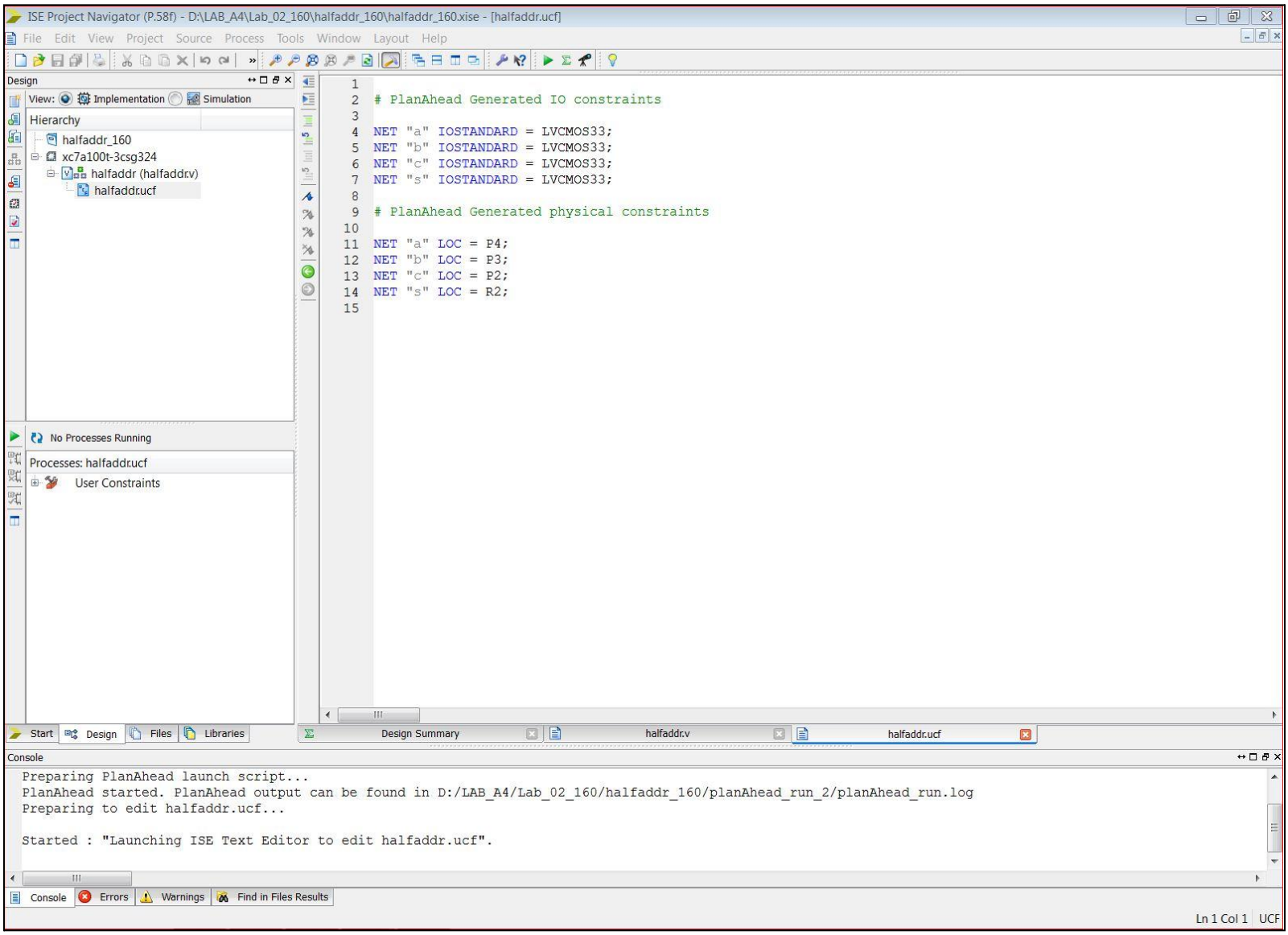
4. Simulation



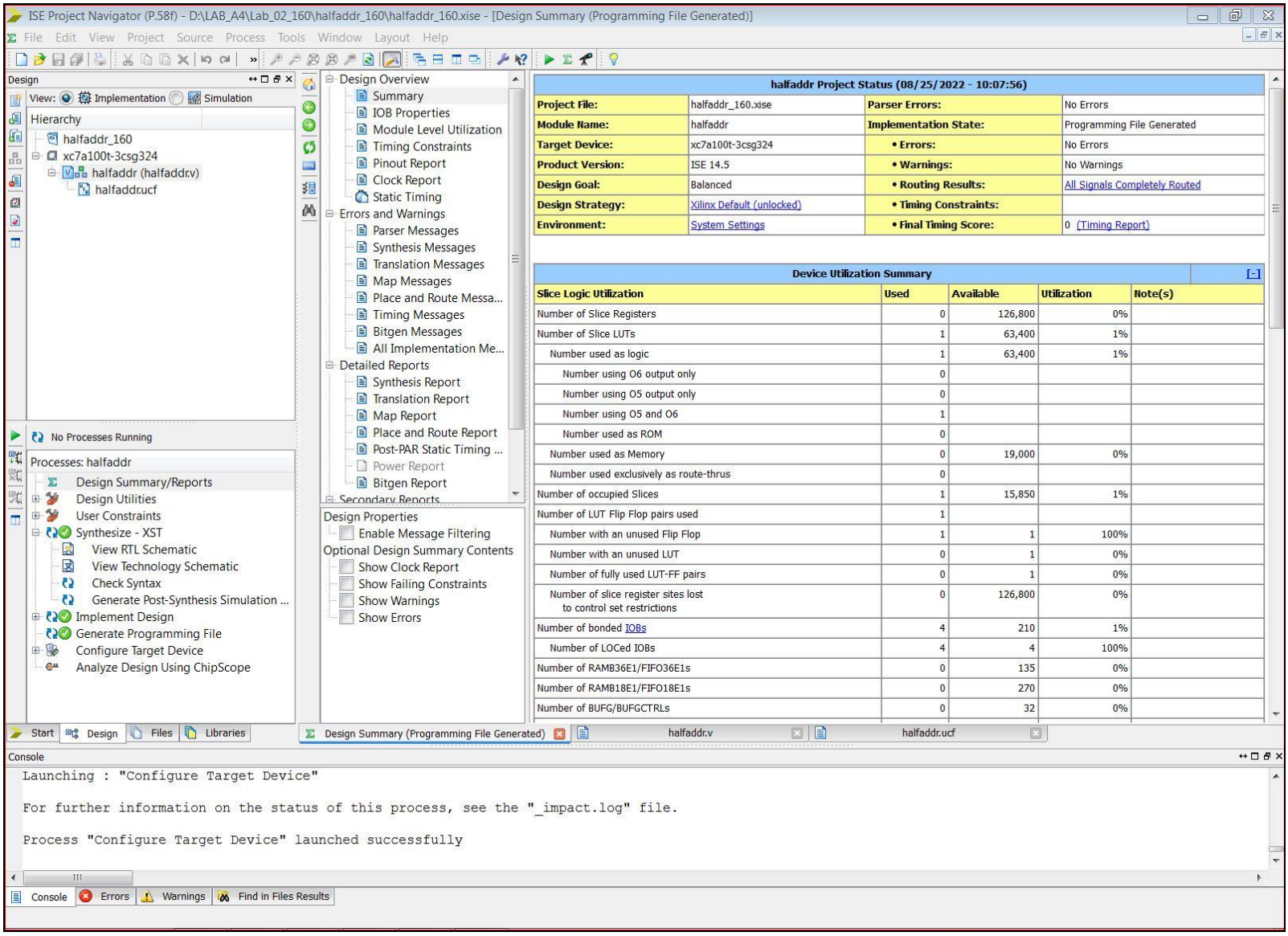
5. IO Planning



6. UCF File


ISE Project Navigator (P.58f) - D:\LAB_A4\Lab_02_160\halfaddr_160\halfaddr_160.xise - [halfaddr.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
halfaddr_160
xc7a100t-3csg324
halfaddr (halfaddr.v)
halfaddr.ucf
No Processes Running
Processes: halfaddr.ucf
User Constraints
Start Design Files Libraries
1 # PlanAhead Generated IO constraints
2
3 NET "a" IOSTANDARD = LVCMOS33;
4 NET "b" IOSTANDARD = LVCMOS33;
5 NET "c" IOSTANDARD = LVCMOS33;
6 NET "s" IOSTANDARD = LVCMOS33;
7
8 # PlanAhead Generated physical constraints
9
10 NET "a" LOC = P4;
11 NET "b" LOC = P3;
12 NET "c" LOC = P2;
13 NET "s" LOC = R2;
14
Design Summary
halfaddr.v
halfaddr.ucf
Console
Preparing PlanAhead launch script...
PlanAhead started. PlanAhead output can be found in D:/LAB_A4/Lab_02_160/halfaddr_160/planAhead_run_2/planAhead_run.log
Preparing to edit halfaddr.ucf...
Started : "Launching ISE Text Editor to edit halfaddr.ucf".
Console Errors Warnings Find in Files Results
Ln 1 Col 1 UCF

7. Design Summary



8. Program successfully uploaded