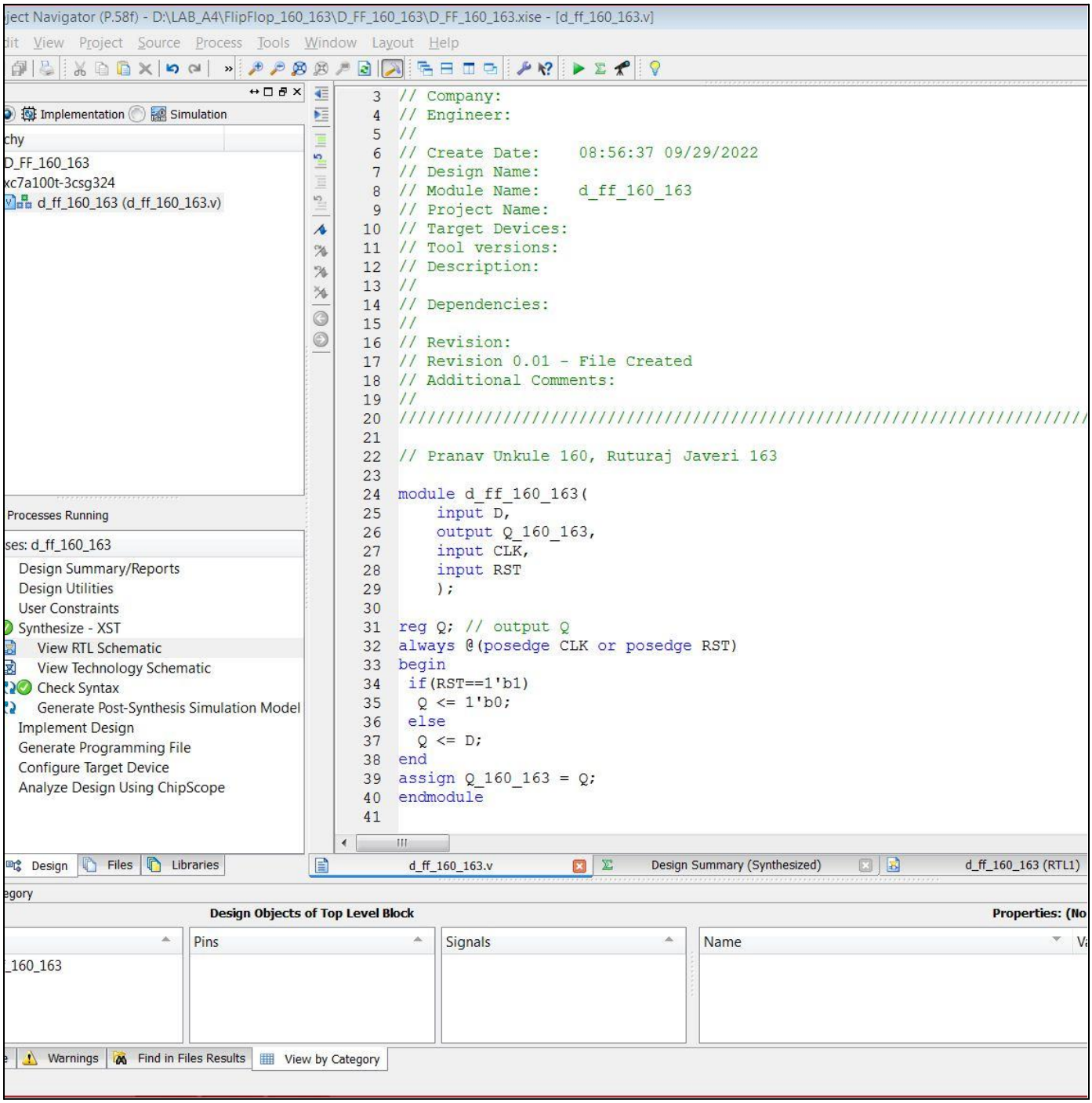
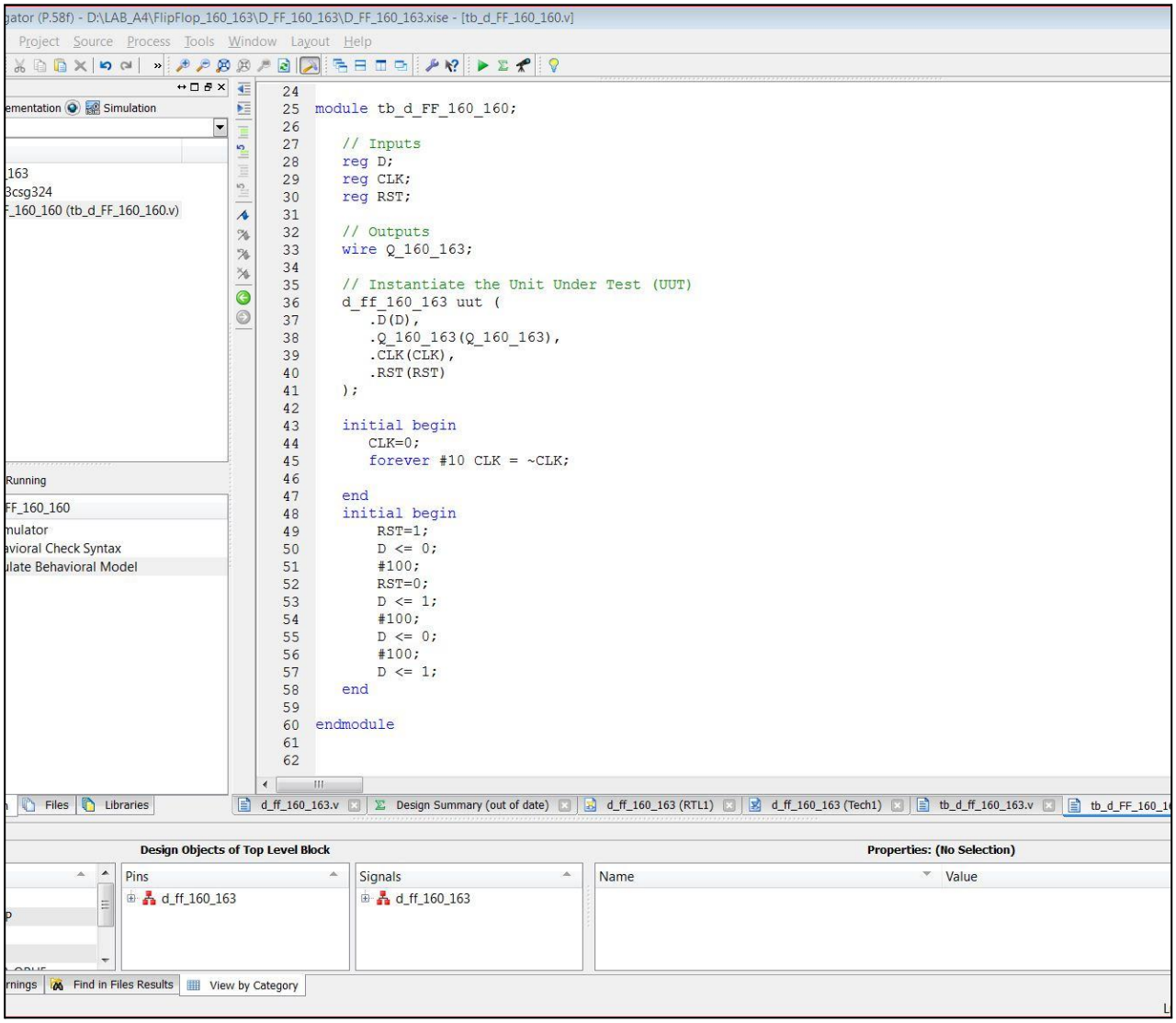
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

LAB: D Flipflop

1. HDL Code

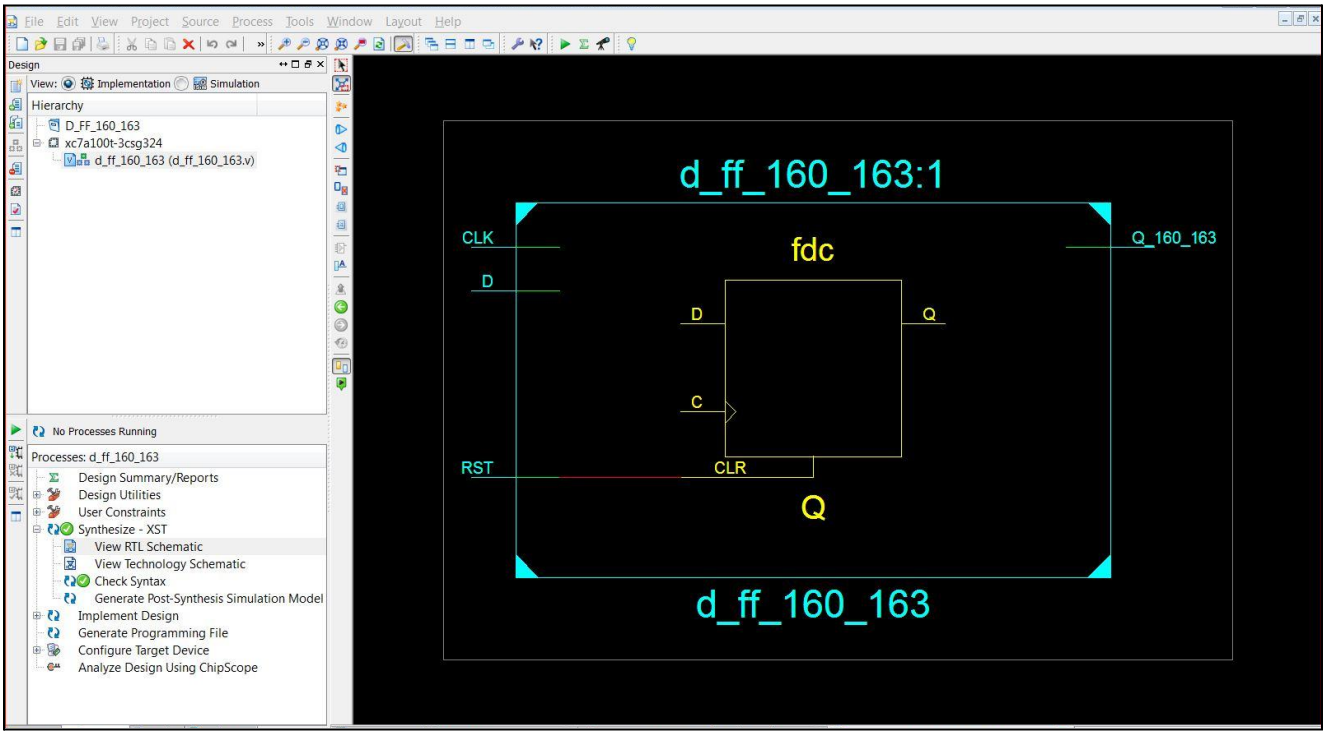


Text Bench Code

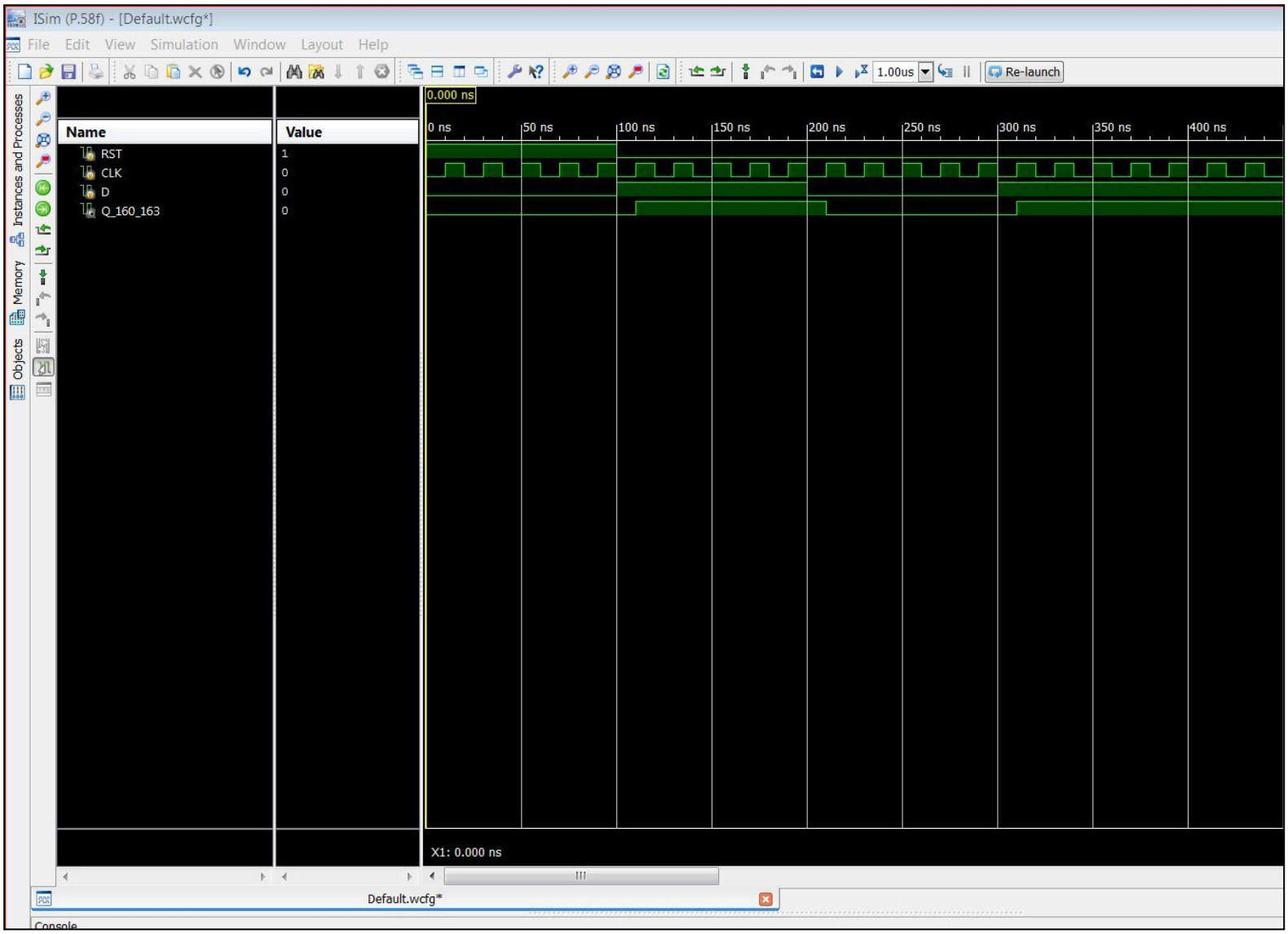


```
module tb_d_FF_160_160;

    // Inputs
    reg D;
    reg CLK;
    reg RST;

    // Outputs
    wire Q_160_163;

    // Instantiate the Unit Under Test (UUT)
    d_ff_160_163 uut (
        .D(D),
        .Q_160_163(Q_160_163),
        .CLK(CLK),
        .RST(RST)
    );

    initial begin
        CLK=0;
        forever #10 CLK = ~CLK;

    end
    initial begin
        RST=1;
        D <= 0;
        #100;
        RST=0;
        D <= 1;
        #100;
        D <= 0;
        #100;
        D <= 1;
    end

endmodule
```

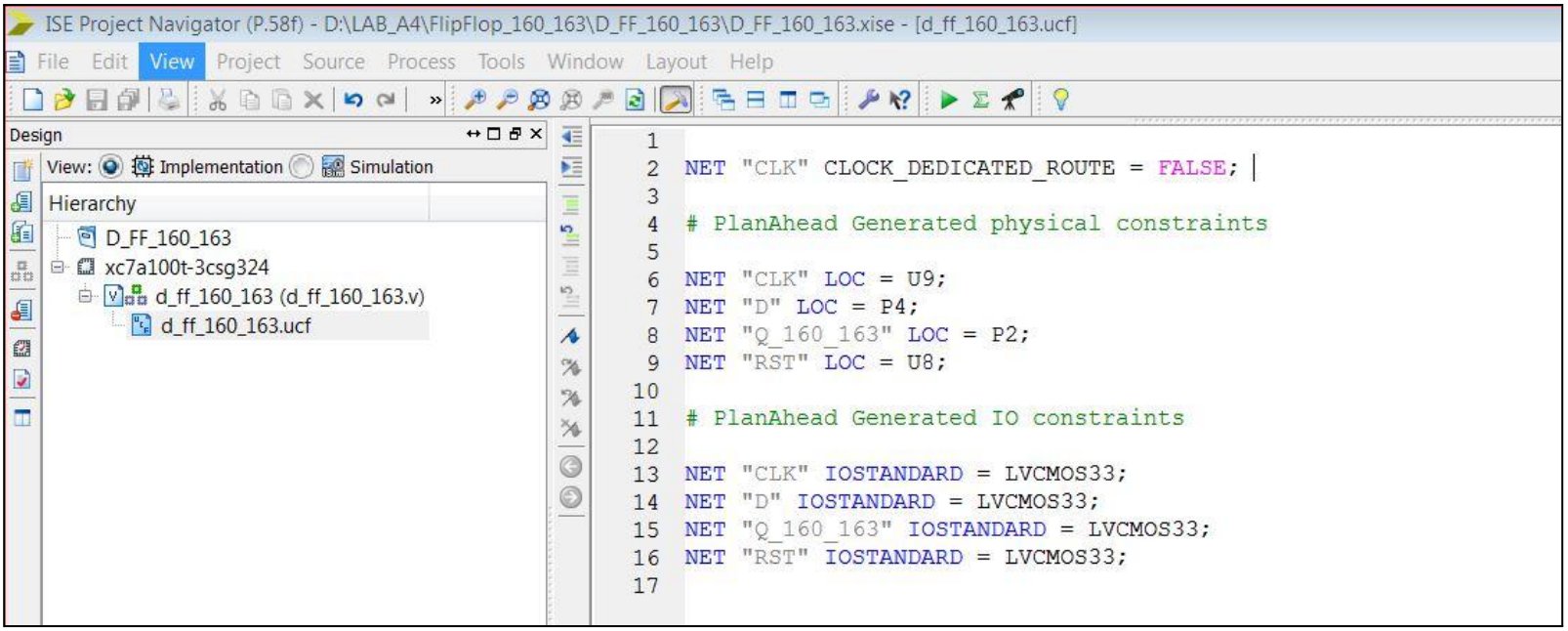
Schematic



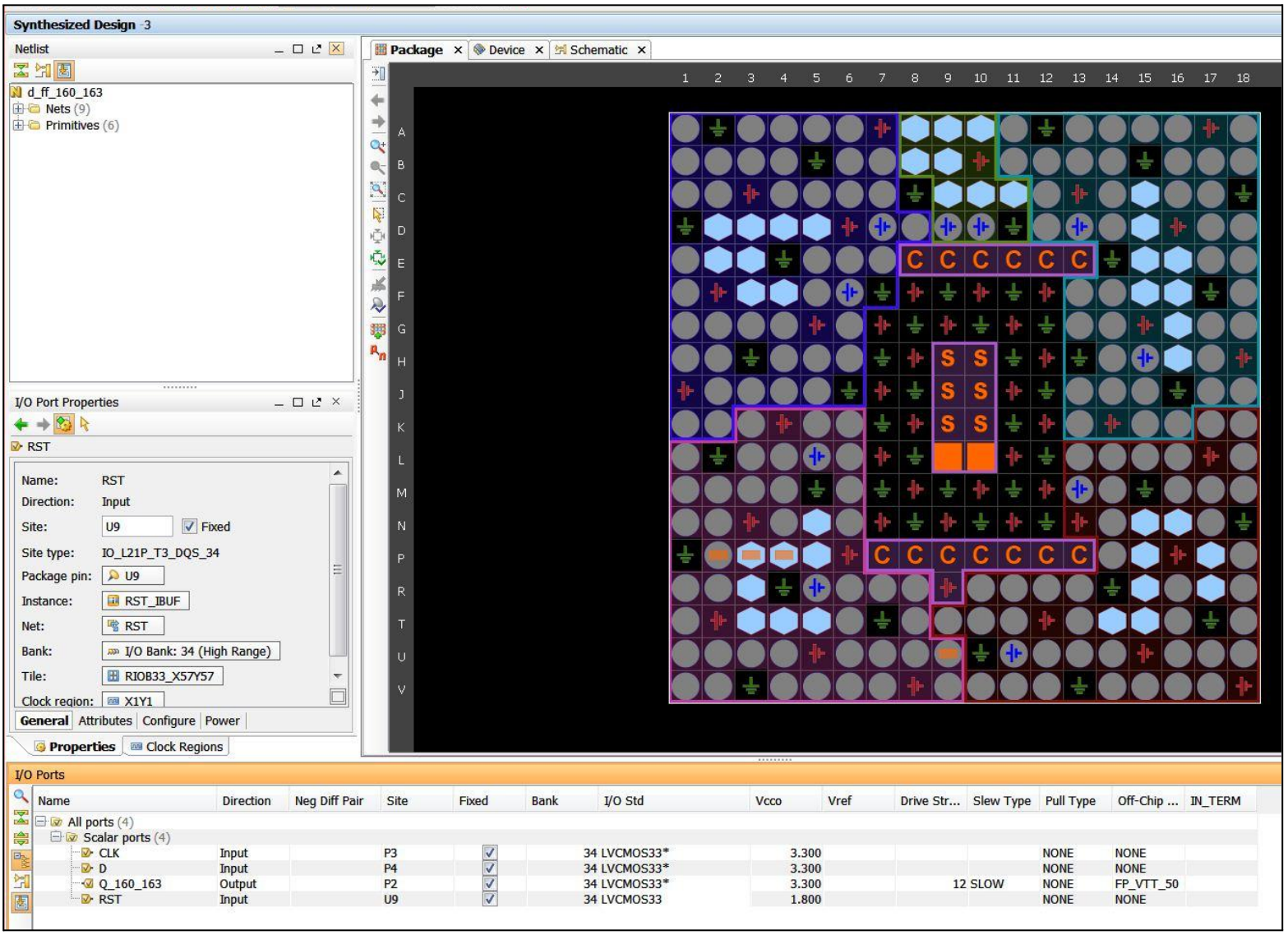
Simulation



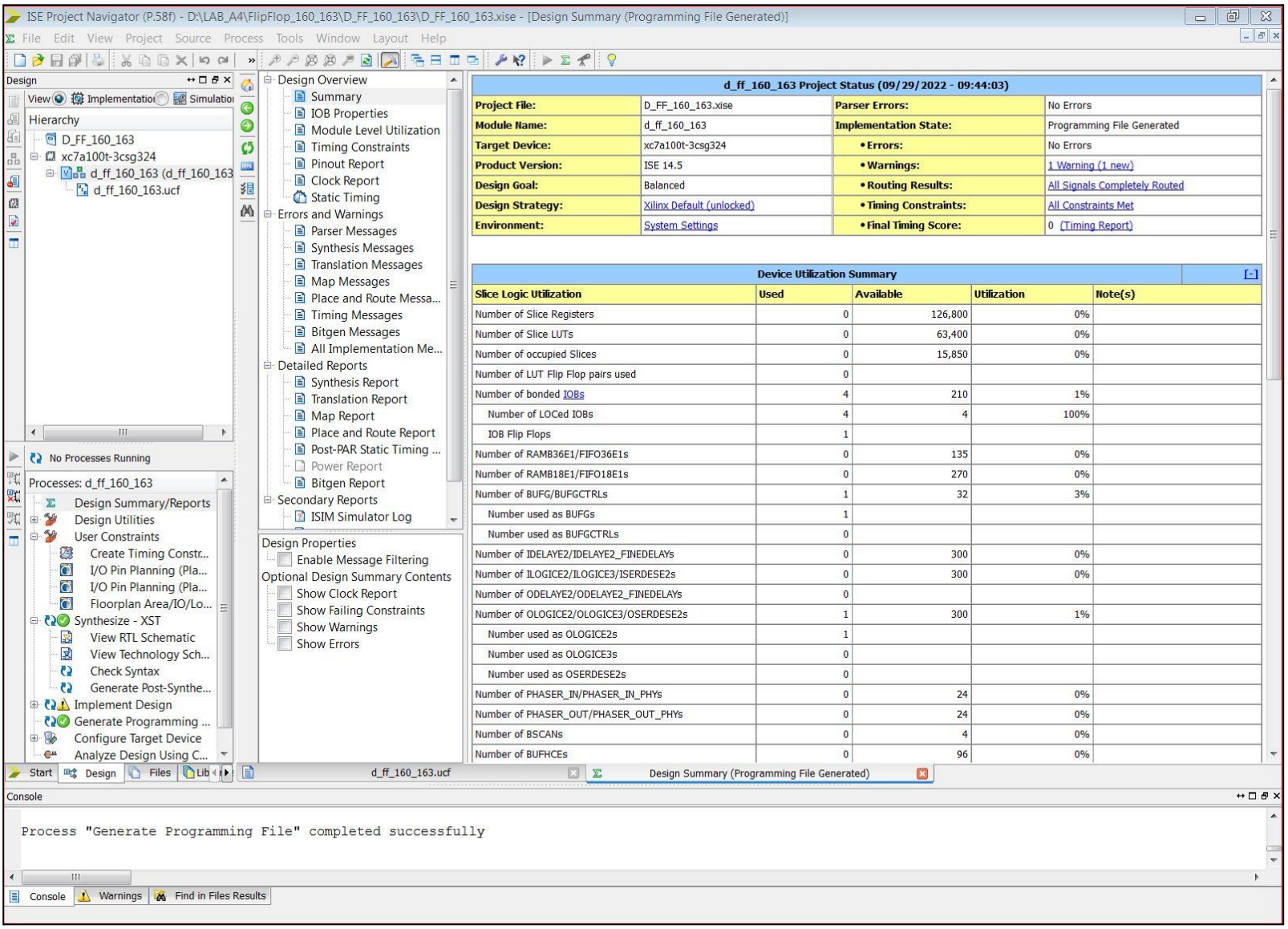
UCF File



IO Planning


Synthesized Design 3
Netlist
d_ff_160_163
Nets (9)
Primitives (6)
Package
Device
Schematic
I/O Port Properties
RST
Name: RST
Direction: Input
Site: U9
Fixed
Site type: IO_L21P_T3_DQS_34
Package pin: U9
Instance: RST_IBUF
Net: RST
Bank: I/O Bank: 34 (High Range)
Tile: RIOB33_X57Y57
Clock region: X1Y1
General
Attributes
Configure
Power
Properties
Clock Regions
I/O Ports
Name
Direction
Neg Diff Pair
Site
Fixed
Bank
I/O Std
Vcco
Vref
Drive Str...
Slew Type
Pull Type
Off-Chip ...
IN_TERM
All ports (4)
Scalar ports (4)
CLK Input P3 34 LVCMOS33* 3.300 NONE NONE
D Input P4 34 LVCMOS33* 3.300 NONE NONE
Q_160_163 Output P2 34 LVCMOS33* 3.300 12 SLOW NONE FP_VTT_50
RST Input U9 34 LVCMOS33 1.800 NONE NONE

Design Summary



Program Succeeded