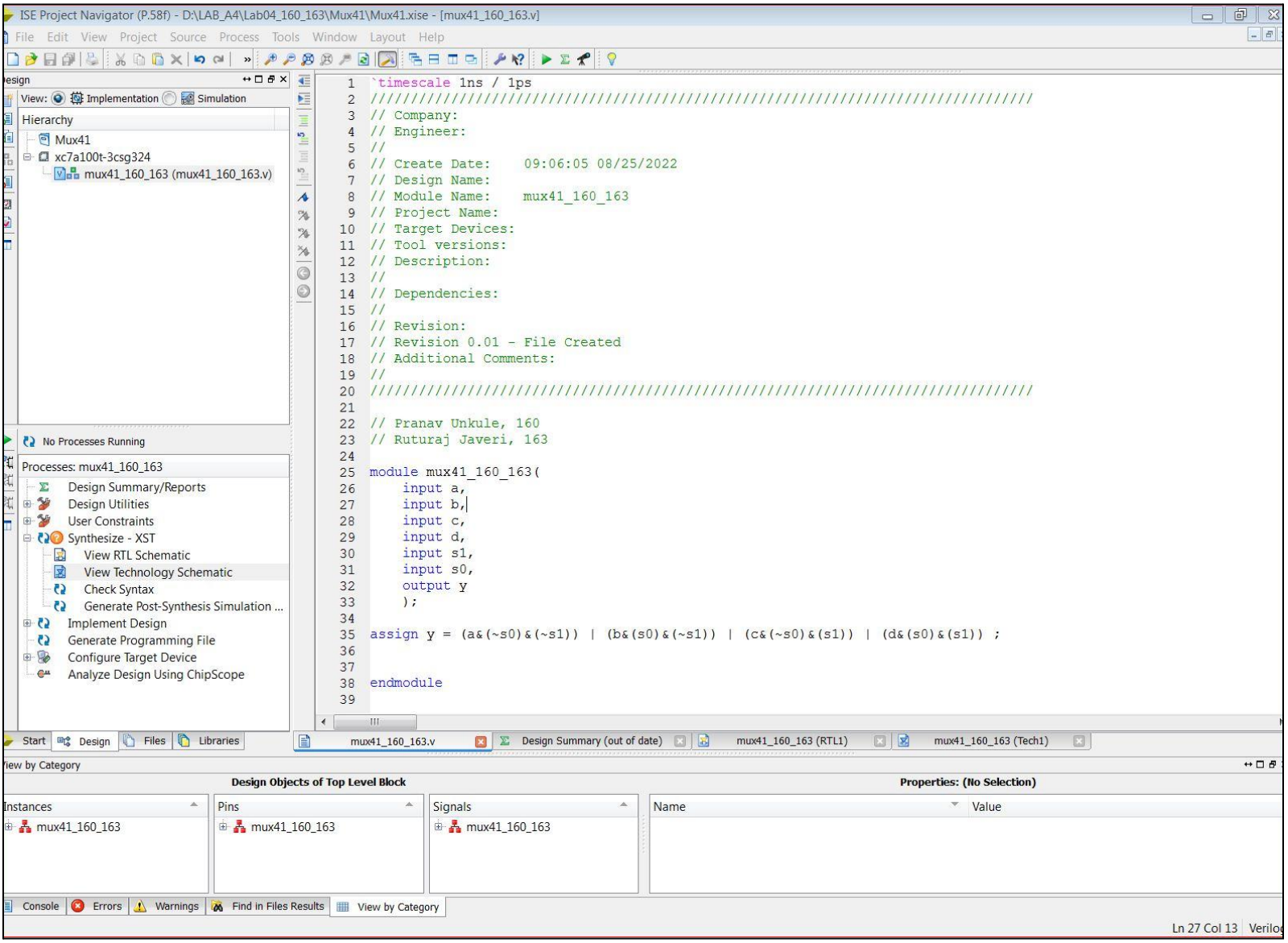
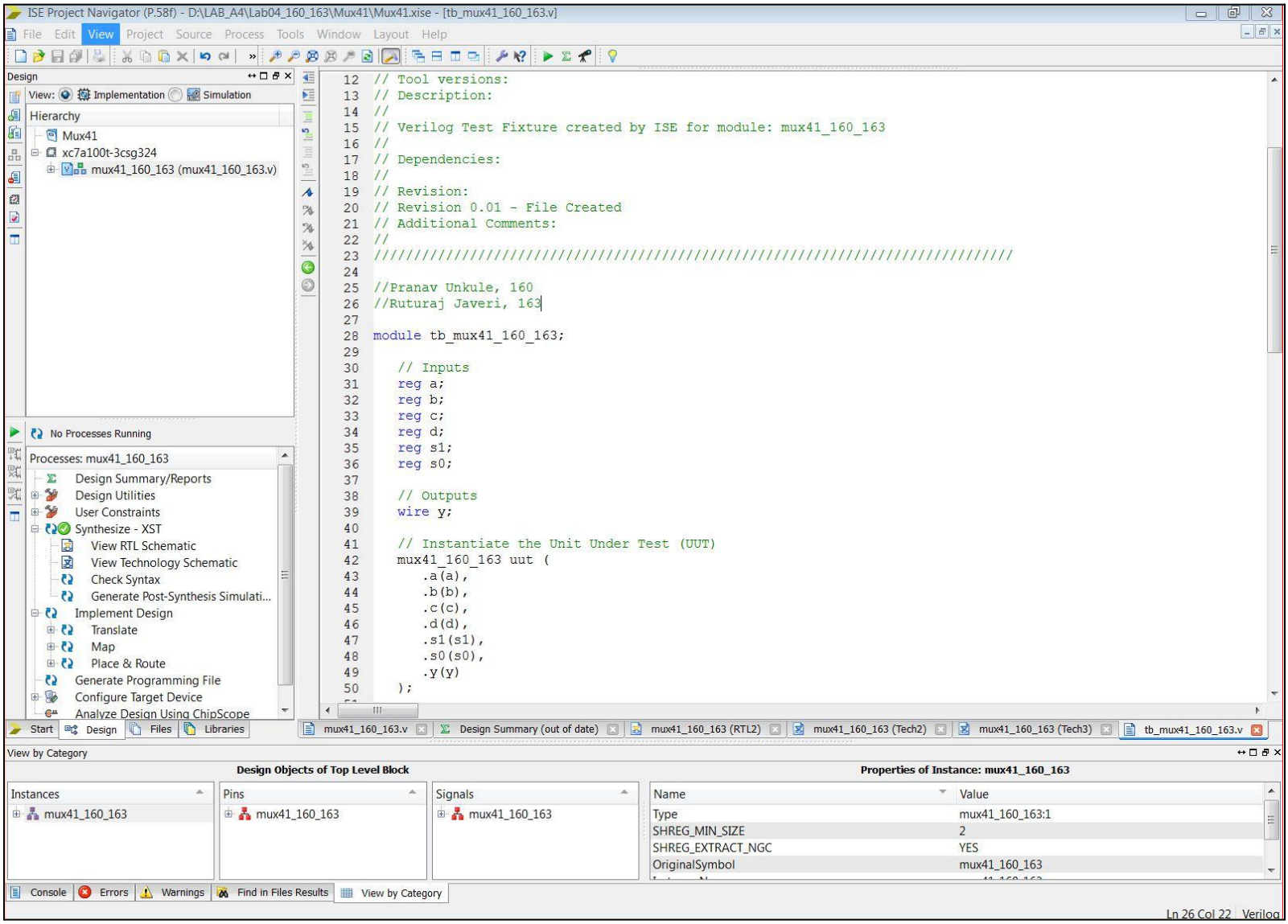
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

# LAB 02 4:1 MUX

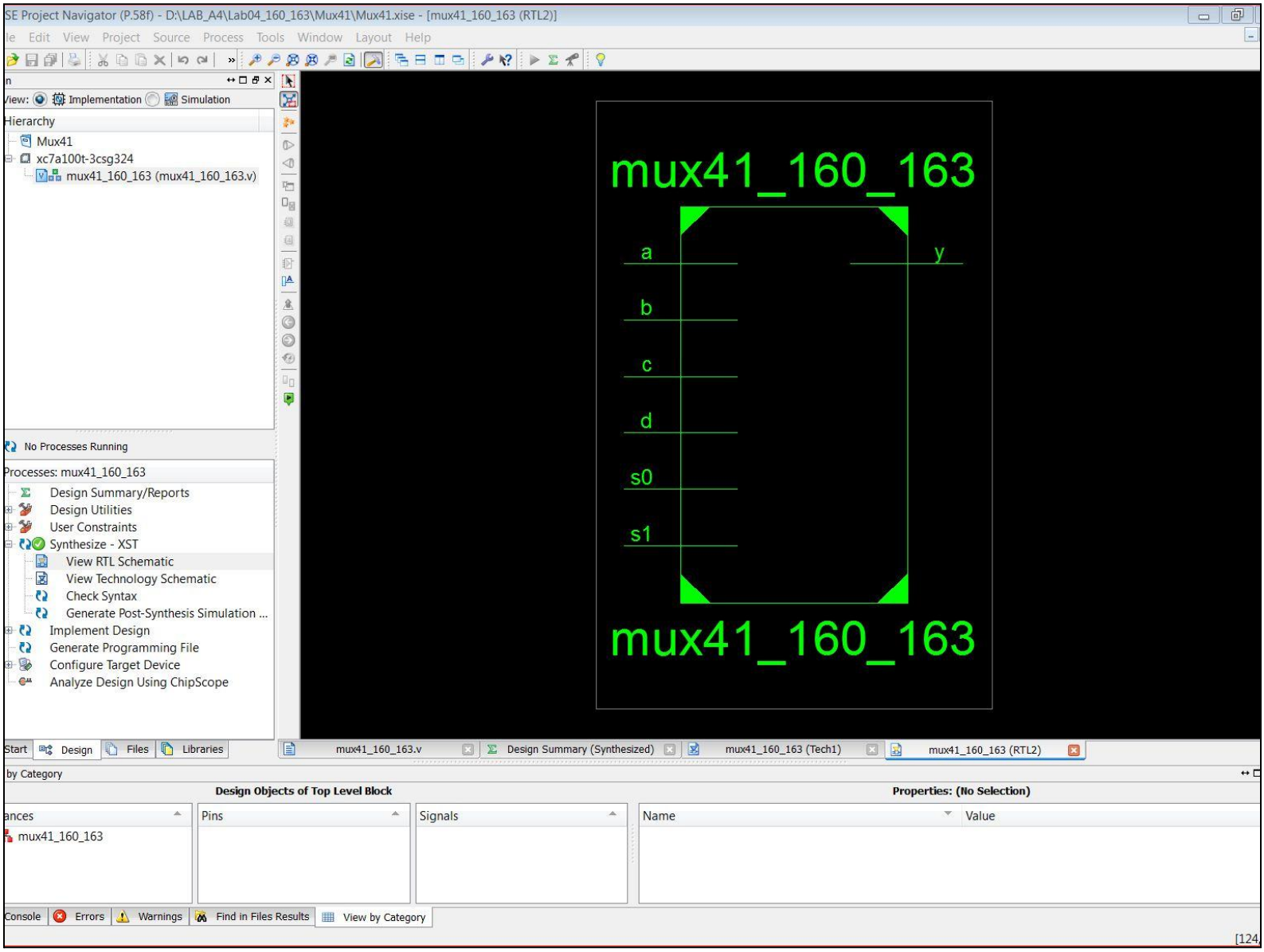
## 1. HDL Code

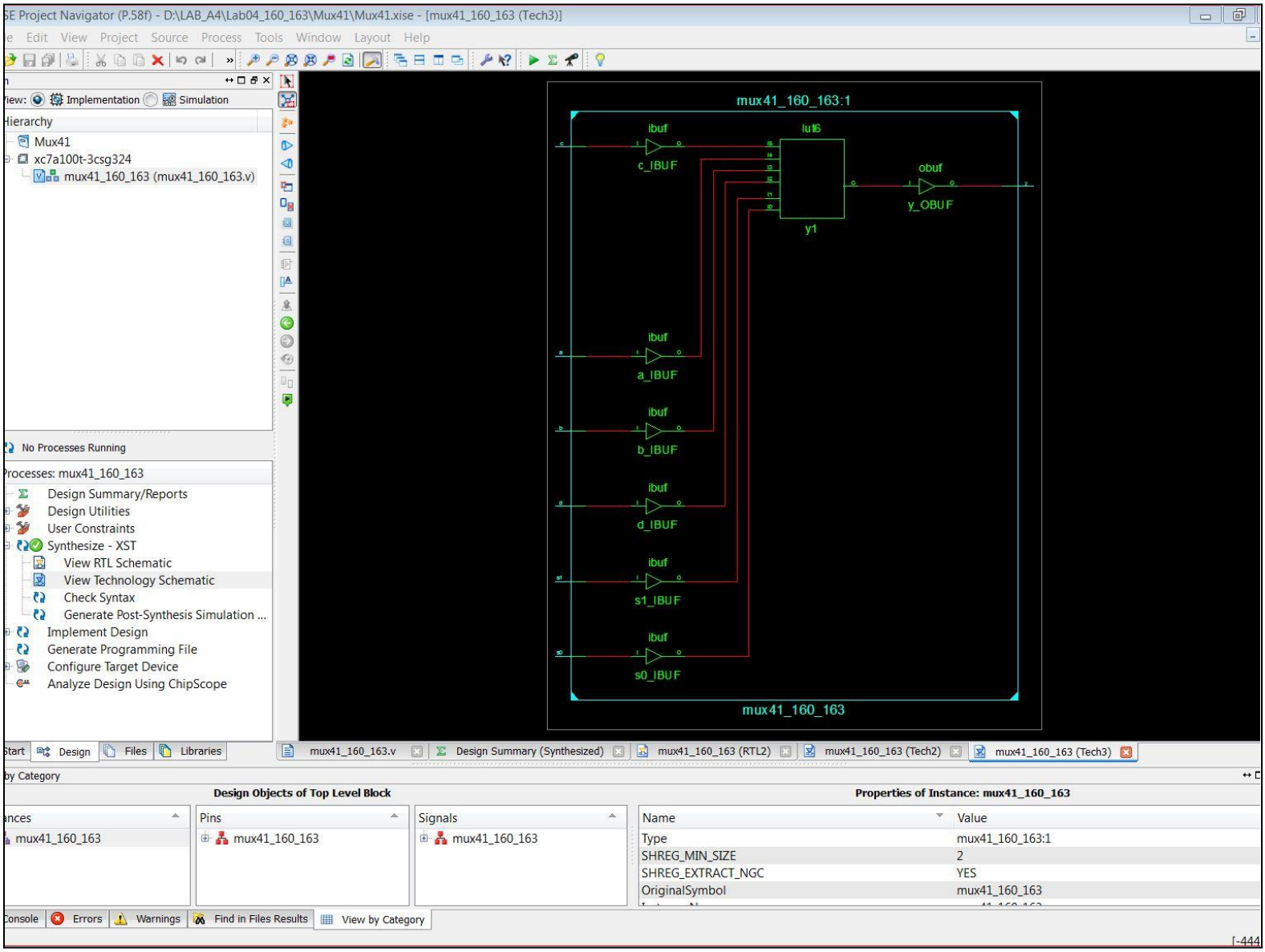


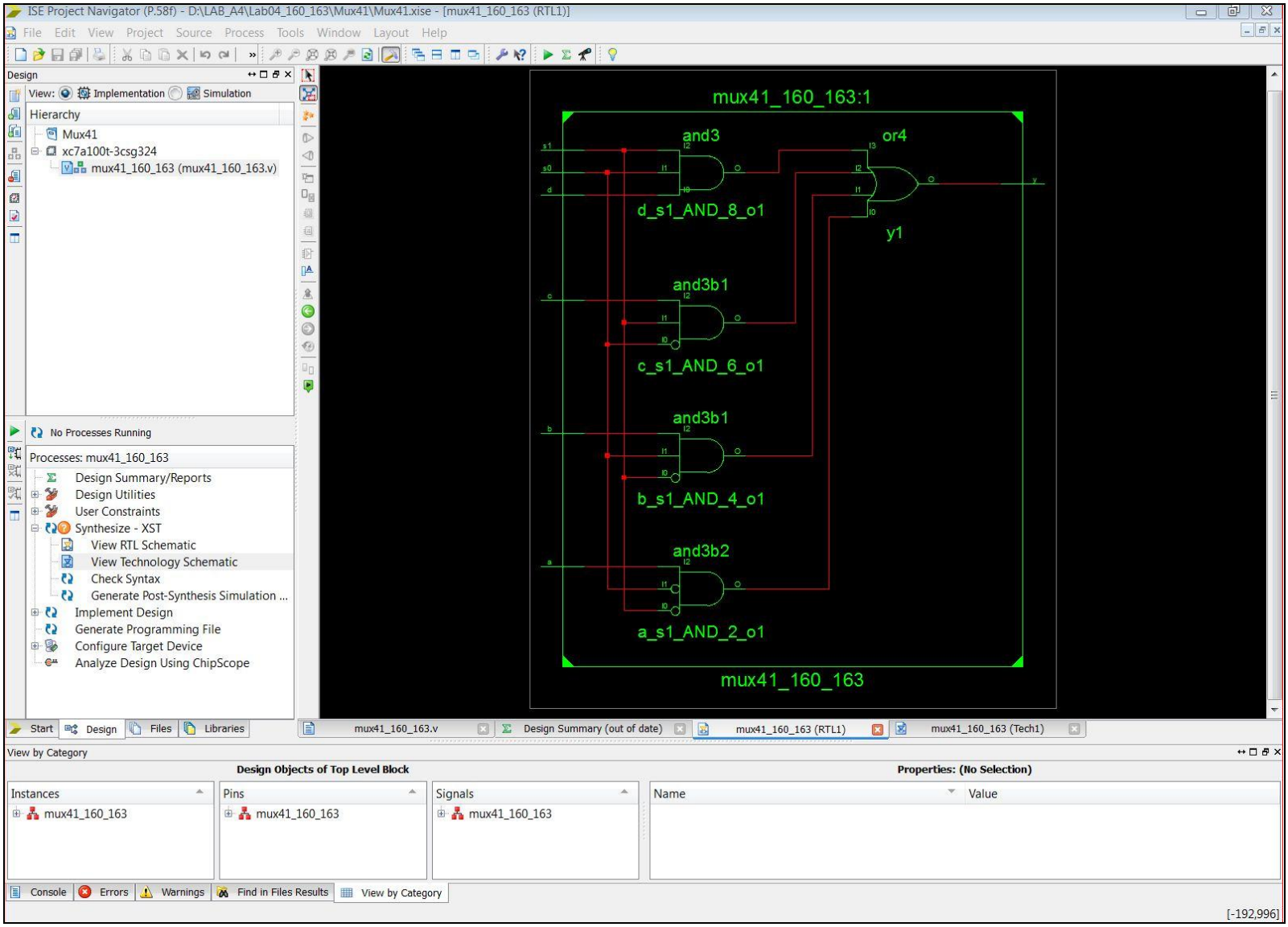
## 2. Test Bench Code



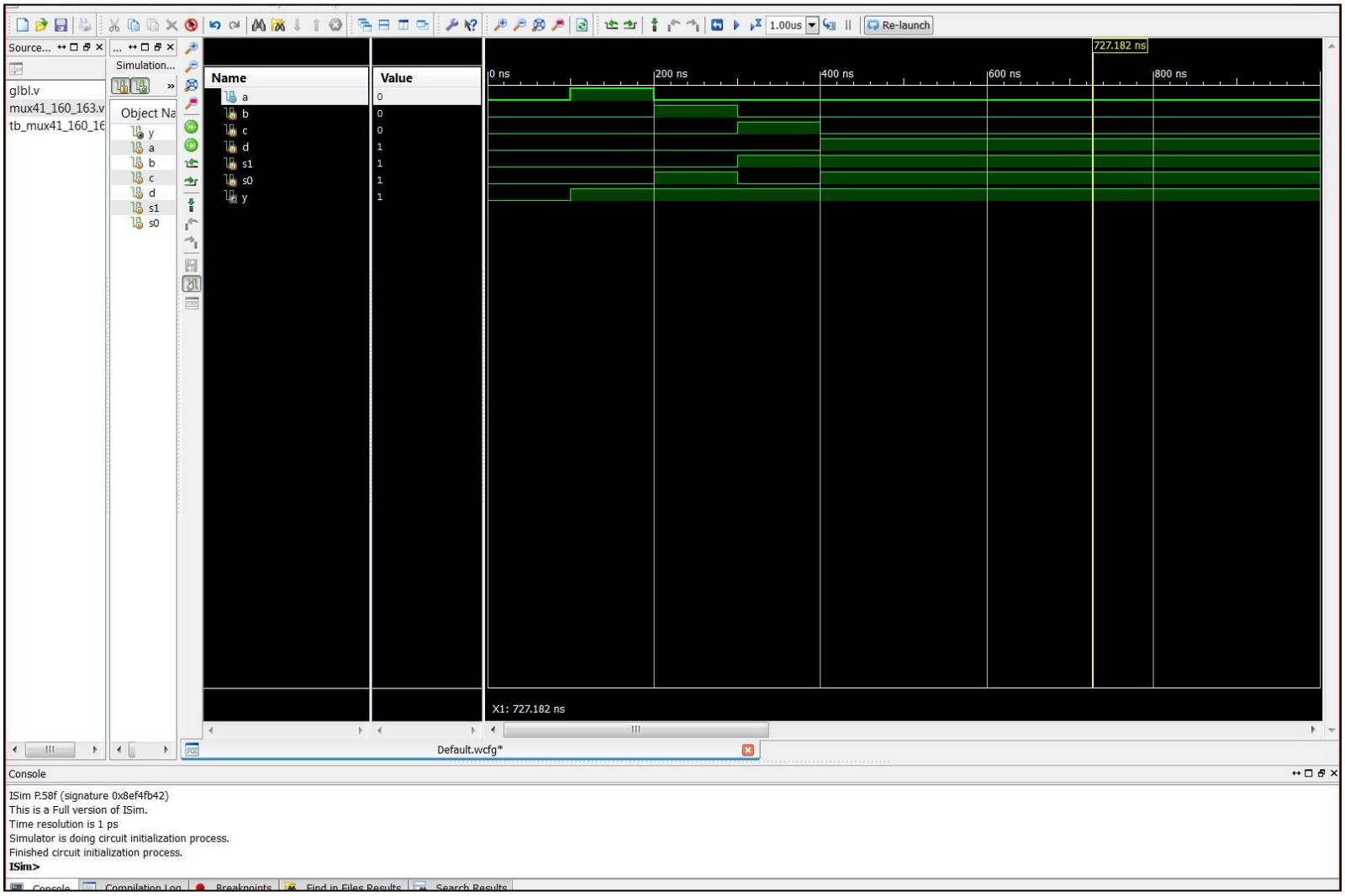
## 3. RTL Schematic



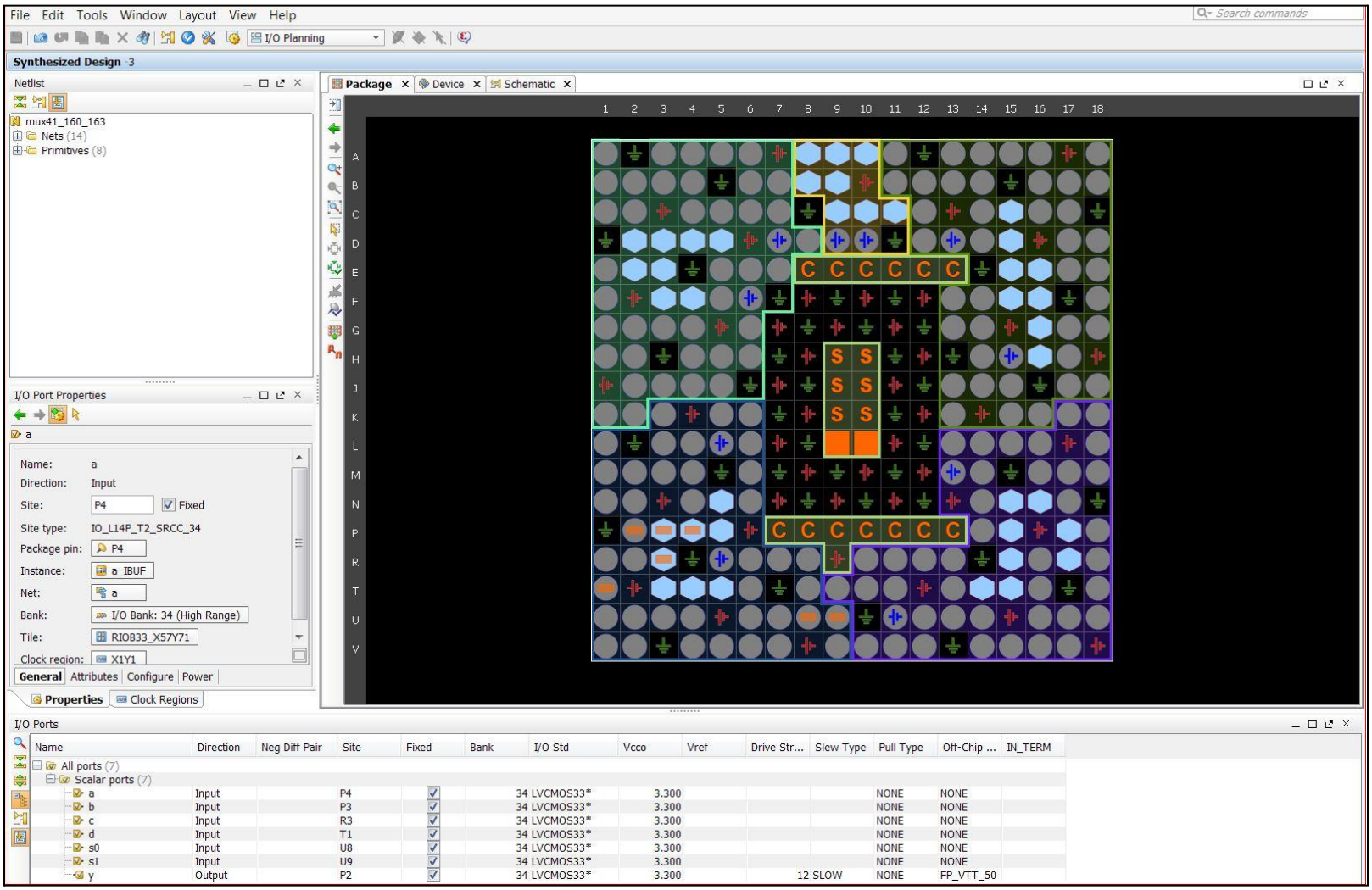

SE Project Navigator (P.58f) - D:\LAB_A4\Lab04_160_163\Mux41\Mux41.xise - [mux41_160_163 (Tech3)]
Edit View Project Source Process Tools Window Layout Help
View: Implementation Simulation
Hierarchy
Mux41
xc7a100t-3csg324
mux41_160_163 (mux41_160_163.v)
No Processes Running
Processes: mux41_160_163
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation ...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
mux41_160_163:1
ibuf
c_IBUF
lut6
y1
obuf
y_OBUF
a_IBUF
b_IBUF
d_IBUF
s1_IBUF
s0_IBUF
mux41_160_163
Start
Design
Files
Libraries
mux41_160_163.v
Design Summary (Synthesized)
mux41_160_163 (RTL2)
mux41_160_163 (Tech2)
mux41_160_163 (Tech3)
by Category
Design Objects of Top Level Block
Properties of Instance: mux41_160_163
Pins
Signals
Name
Value
Type
mux41_160_163:1
SHREG_MIN_SIZE
2
SHREG_EXTRACT_NGC
YES
OriginalSymbol
Console
Errors
Warnings
Find in Files Results
View by Category


ISE Project Navigator (P.58f) - D:\LAB_A4\Lab04_160_163\Mux41\Mux41.xise - [mux41_160_163 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Mux41
xc7a100t-3csg324
mux41_160_163 (mux41_160_163.v)
No Processes Running
Processes: mux41_160_163
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Simulation ...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipScope
mux41_160_163:1
and3
or4
d_s1_AND_8_o1
y1
and3b1
c_s1_AND_6_o1
and3b1
b_s1_AND_4_o1
and3b2
a_s1_AND_2_o1
mux41_160_163
Start Design Files Libraries
mux41_160_163.v
Design Summary (out of date)
mux41_160_163 (RTL1)
mux41_160_163 (Tech1)
View by Category
Design Objects of Top Level Block
Properties: (No Selection)
Instances
Pins
Signals
Name
Value
mux41_160_163
Console Errors Warnings Find in Files Results View by Category
[-192,996]

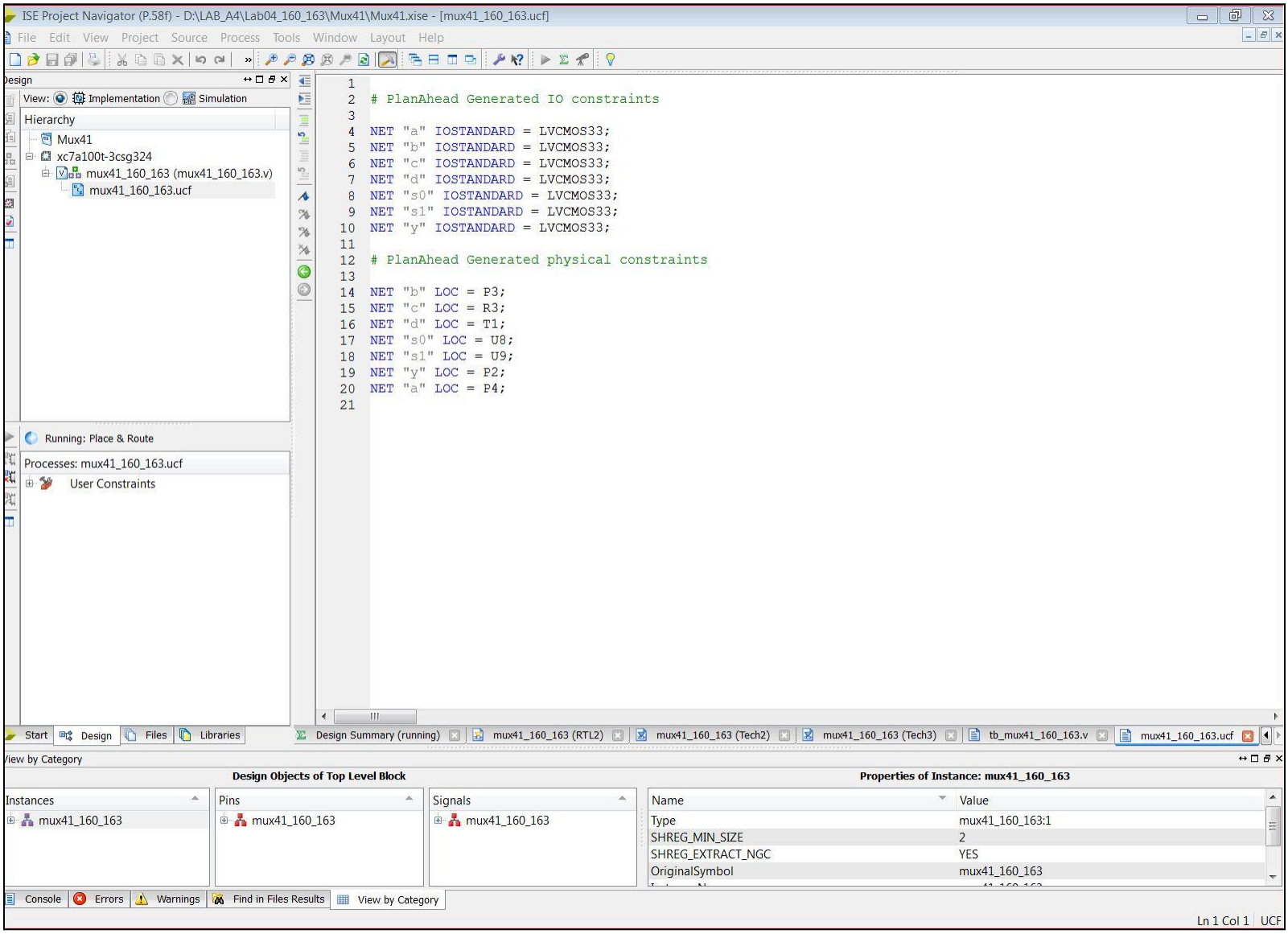
## 4. Simulation



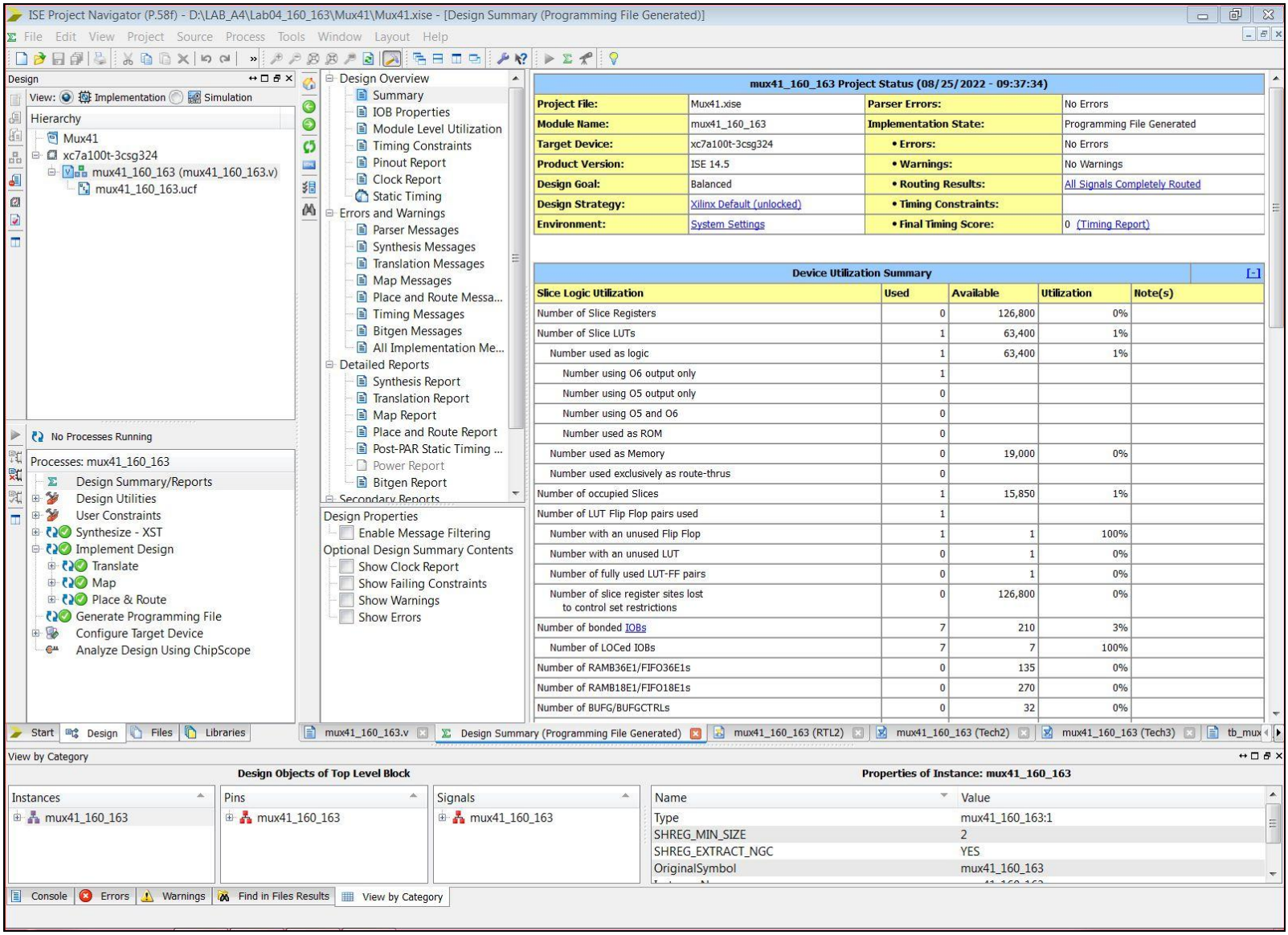
## 5. IO Planning



## 6. UCF File


ISE Project Navigator (P.58f) - D:\LAB_A4\Lab04_160_163\Mux41\Mux41.xise - [mux41_160_163.ucf]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
Mux41
xc7a100t-3csg324
mux41_160_163 (mux41_160_163.v)
mux41_160_163.ucf
Running: Place & Route
Processes: mux41_160_163.ucf
User Constraints
1 # PlanAhead Generated IO constraints
2
3 NET "a" IOSTANDARD = LVCMOS33;
4 NET "b" IOSTANDARD = LVCMOS33;
5 NET "c" IOSTANDARD = LVCMOS33;
6 NET "d" IOSTANDARD = LVCMOS33;
7 NET "s0" IOSTANDARD = LVCMOS33;
8 NET "s1" IOSTANDARD = LVCMOS33;
9 NET "y" IOSTANDARD = LVCMOS33;
10
11 # PlanAhead Generated physical constraints
12
13 NET "b" LOC = P3;
14 NET "c" LOC = R3;
15 NET "d" LOC = T1;
16 NET "s0" LOC = U8;
17 NET "s1" LOC = U9;
18 NET "y" LOC = P2;
19 NET "a" LOC = P4;
20
21
Start Design Files Libraries
Design Summary (running) mux41_160_163 (RTL2) mux41_160_163 (Tech2) mux41_160_163 (Tech3) tb_mux41_160_163.v mux41_160_163.ucf
View by Category
Design Objects of Top Level Block
Instances
mux41_160_163
Pins
mux41_160_163
Signals
mux41_160_163
Properties of Instance: mux41_160_163
Name Value
Type mux41_160_163:1
SHREG_MIN_SIZE 2
SHREG_EXTRACT_NGC YES
OriginalSymbol mux41_160_163
Console Errors Warnings Find in Files Results View by Category
Ln 1 Col 1 UCF

## 7. Design Summary



## 8. Program successfully uploaded