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LAB 01 Half Adder

1. HDL Code

The screenshot displays the ISE Project Navigator interface. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. The left pane shows the Project Hierarchy with the following structure:

- halfaddr_160
 - xc7a100t-3csg324
 - halfaddr (halfaddr.v)

The main editor window shows the Verilog code for the halfadder module. The code is as follows:

```
1 `timescale 1ns / 1ps
2 //////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    23:56:08 12/31/2012
7 // Design Name:
8 // Module Name:    halfaddr
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////
21
22 // Pranav Unkule, 160
23
24 module halfaddr(
25     input a,
26     input b,
27     output s,
28     output c
29 );
30
31     assign s = a ^ b;
32     assign c = a & b;
33
34 endmodule
35
```

The bottom pane shows the Process "Check Syntax" completed successfully. The status bar at the bottom indicates "Ln 35 Col 1 Verilog".

2. Test Bench Code

The screenshot displays the Xilinx ISE IDE interface. The main editor window shows a Verilog test bench for the `halfaddr` module. The code includes a header with project information, a module definition for `tb_halfaddr`, and an instantiation of the `halfaddr` module as `uut` . The test bench defines two input registers (`a` and `b`) and two output wires (`s` and `c`). The `uut` is instantiated with these signals connected to its ports.

```
1 `timescale 1ns / 1ps
2
3 //////////////////////////////////////////////////
4 // Company:
5 // Engineer:
6 //
7 // Create Date:    00:00:29 01/01/2013
8 // Design Name:    halfaddr
9 // Module Name:    D:/LAB_A4/Lab_02_160/halfaddr_160/tb_halfaddr.v
10 // Project Name:   halfaddr_160
11 // Target Device:
12 // Tool versions:
13 // Description:
14 //
15 // Verilog Test Fixture created by ISE for module: halfaddr
16 //
17 // Dependencies:
18 //
19 // Revision:
20 // Revision 0.01 - File Created
21 // Additional Comments:
22 //
23 //////////////////////////////////////////////////
24
25 // Pranav Unkule 160
26
27 module tb_halfaddr;
28
29     // Inputs
30     reg a;
31     reg b;
32
33     // Outputs
34     wire s;
35     wire c;
36
37     // Instantiate the Unit Under Test (UUT)
38     halfaddr uut (
39         .a(a),
40         .b(b),
41         .s(s),
42         .c(c)
43     );
44 endmodule
```

The left sidebar shows the project hierarchy with the following structure:

- halfaddr_160
 - xc7a100t-3csg324
 - tb_halfaddr (tb_halfaddr.v)
 - uut - halfaddr (halfaddr.v)

The bottom status bar indicates the current line and column: `Ln 25 Col 21 | Verilog`.

File Edit View Project Source Process Tools Window Layout Help

View: Implementation Simulation

Behavioral

Hierarchy

- halfaddr_160
 - xc7a100t-3csg324
 - tb_halfaddr (tb_halfaddr.v)
 - uut - halfaddr (halfaddr.v)

No Processes Running

Processes: tb_halfaddr

- ISim Simulator
 - Behavioral Check Syntax
 - Simulate Behavioral Model

```
25 // Pranav Unkule 160
26
27 module tb_halfaddr;
28
29     // Inputs
30     reg a;
31     reg b;
32
33     // Outputs
34     wire s;
35     wire c;
36
37     // Instantiate the Unit Under Test (UUT)
38     halfaddr uut (
39         .a(a),
40         .b(b),
41         .s(s),
42         .c(c)
43     );
44
45     initial begin
46         // Initialize Inputs
47         a = 0;
48         b = 0;
49         #250;
50
51         a = 1;
52         b = 0;
53         #250;
54
55         a = 0;
56         b = 1;
57         #250;
58
59         a = 1;
60         b = 1;
61         #250;
62         // Add stimulus here
63
64     end
65
66 endmodule
```

Start Design Files Libraries

Design Summary (out of date) halfaddr.v tb_halfaddr.v*

sole

INFO:HDLCompiler:1845 - Analyzing Verilog file "D:/LAB_A4/Lab_02_160/halfaddr_160/tb_halfaddr.v" into library work

INFO:ProjectMgmt - Parsing design hierarchy completed successfully.

Console Errors Warnings Find in Files Results

Ln 25 Col 21 Verilog

3. RTL Schematic

The screenshot displays the Xilinx ISE Project Navigator interface. The main window shows the RTL Schematic for a block named 'halfaddr'. The schematic consists of a central rectangle with four input/output ports labeled 'a', 'b', 'c', and 's'. The text 'halfaddr' is written in large green font above and below the rectangle. The left pane shows the Project Navigator with the hierarchy: halfaddr_160 > xc7a100t-3csg324 > halfaddr (halfaddrrv). The bottom pane shows the 'Design Objects of Top Level Block' table.

Design Objects of Top Level Block			Properties: (No Selection)	
Instances	Pins	Signals	Name	Value
halfaddr				

The bottom status bar shows the date and time: 11:58 PM 12/31/2012.

ISE Project Navigator (P.58f) - D:\LAB_A4\Lab_02_160\halfaddr_160\halfaddr_160.xise - [halfaddr (RTL1)]

File Edit View Project Source Process Tools Window Layout Help

Design View: Implementation Simulation

Hierarchy

- halfaddr_160
 - xc7a100t-3csg324
 - halfaddr (halfaddr)

No Processes Running

Processes: halfaddr

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simulation Model
- Implement Design
 - Generate Programming File
 - Configure Target Device
 - Analyze Design Using ChipScope

Start Design Files Libraries

halfaddrcv Design Summary (Synthesized) halfaddr (RTL1)

View by Category

Design Objects of Top Level Block

Instances

- halfaddr

Pins

- halfaddr

Signals

- halfaddr

Properties of Instance: halfaddr

Name	Value
Type	halfaddr:1
Part	xc7a100t-3-csg324

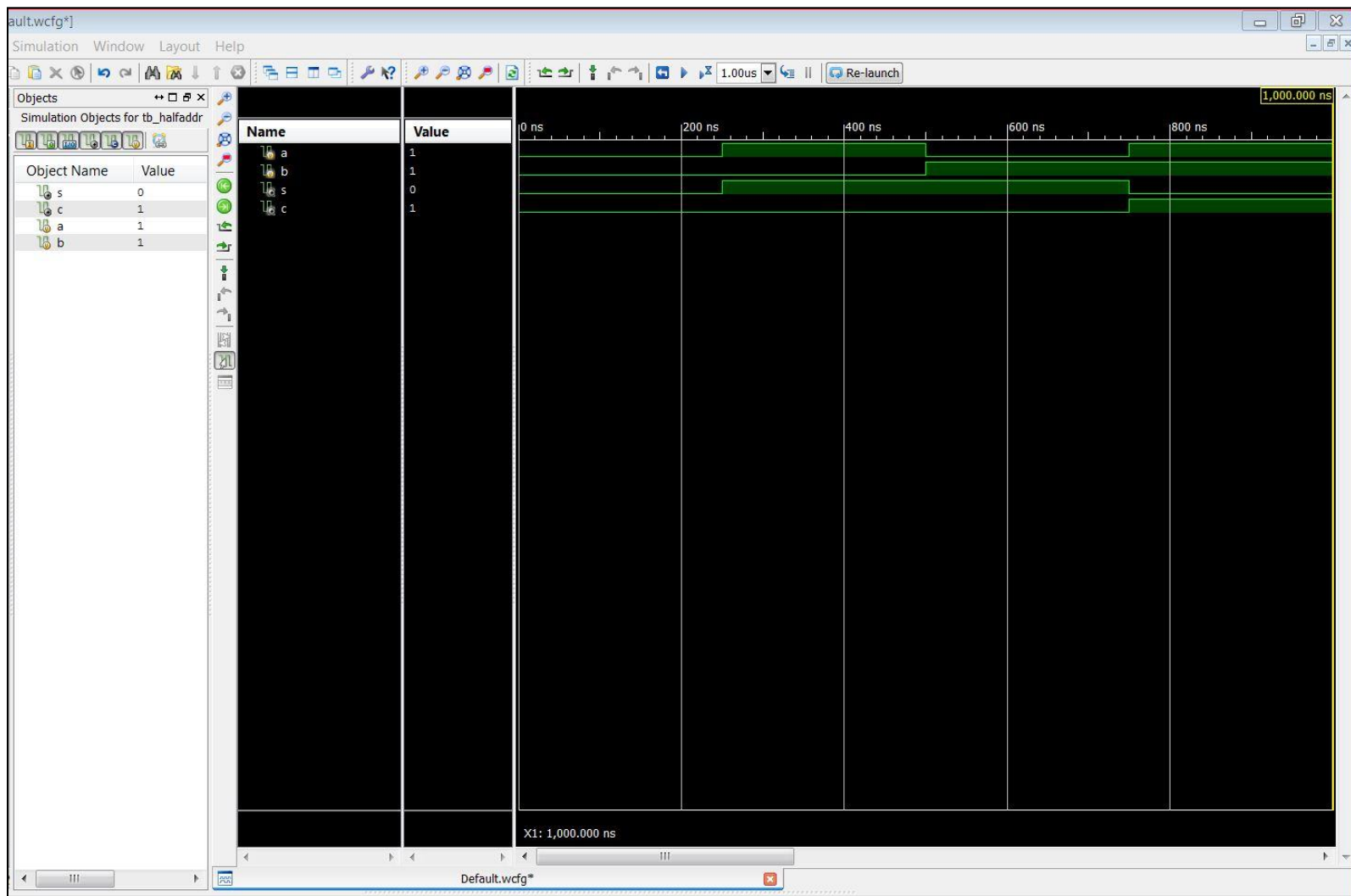
Console Errors Warnings Find in Files Results View by Category

[412,104]

11:59 PM 12/31/2012

```
graph LR
    a((a)) --> and2[and2]
    b((b)) --> and2
    and2 -- c --> c((c))
    Data[Data(1:0)] --> Mxor_s1[Mxor_s1]
    Mxor_s1 -- Result --> s((s))
```

4. Simulation



5. IO Planning

File Edit Tools Window Layout View Help

I/O Planning

Synthesized Design - 3

Netlist

halfaddr
Nets (8)
Primitives (6)

I/O Port Properties

s

Name: s
Direction: Output
Site: R2 ☒ Fixed
Site type: IO_L15N_T2_DQS_34
Package pin: R2
Instance: s_OBUF
Net: s
Bank: I/O Bank: 34 (High Range)
Tile: R10B33_X57Y69
Clock region: X1Y1

General Attributes Configure Power

Properties Clock Regions

Package Device Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T
U
V

I/O Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Str...	Slew Type	Pull Type	Off-Chip ...	IN_TERM
All ports (4)													
Scalar ports (4)													
a	Input		P4	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300				NONE	NONE	
b	Input		P3	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300				NONE	NONE	
c	Output		P2	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300		12 SLOW		NONE	FP_VTT_50	
s	Output		R2	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300		12 SLOW		NONE	FP_VTT_50	

6. UCF File

The screenshot displays the Xilinx ISE Project Navigator interface. The main editor window shows the content of the `halfaddr.ucf` file, which contains PlanAhead generated IO and physical constraints. The left-hand pane shows the project hierarchy with `halfaddr.ucf` selected. The bottom console window shows the execution of the PlanAhead script.

UCF File Content:

```
1
2 # PlanAhead Generated IO constraints
3
4 NET "a" IOSTANDARD = LVCMOS33;
5 NET "b" IOSTANDARD = LVCMOS33;
6 NET "c" IOSTANDARD = LVCMOS33;
7 NET "s" IOSTANDARD = LVCMOS33;
8
9 # PlanAhead Generated physical constraints
10
11 NET "a" LOC = P4;
12 NET "b" LOC = P3;
13 NET "c" LOC = P2;
14 NET "s" LOC = R2;
15
```

Console Output:

```
Preparing PlanAhead launch script...
PlanAhead started. PlanAhead output can be found in D:/LAB_A4/Lab_02_160/halfaddr_160/planAhead_run_2/planAhead_run.log
Preparing to edit halfaddr.ucf...

Started : "Launching ISE Text Editor to edit halfaddr.ucf".
```

The status bar at the bottom right indicates the current position is `Ln 1 Col 1` in the `UCF` file.

7. Design Summary

ISE Project Navigator (P.58f) - D:\LAB_A4\Lab_02_160\halfaddr_160\halfaddr_160.xise - [Design Summary (Programming File Generated)]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

View: Implementation Simulation

Hierarchy

- halfaddr_160
 - xc7a100t-3csg324
 - halfaddr (halfaddr.v)
 - halfaddr.ucf

Design Summary (Programming File Generated)

halfaddr Project Status (08/25/2022 - 10:07:56)

Project File:	halfaddr_160.xise	Parser Errors:	No Errors
Module Name:	halfaddr	Implementation State:	Programming File Generated
Target Device:	xc7a100t-3csg324	Errors:	No Errors
Product Version:	ISE 14.5	Warnings:	No Warnings
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	126,800	0%	
Number of Slice LUTs	1	63,400	1%	
Number used as logic	1	63,400	1%	
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	19,000	0%	
Number used exclusively as route-thrus	0			
Number of occupied Slices	1	15,850	1%	
Number of LUT Flip Flop pairs used	1			
Number with an unused Flip Flop	1	1	100%	
Number with an unused LUT	0	1	0%	
Number of fully used LUT-FF pairs	0	1	0%	
Number of slice register sites lost to control set restrictions	0	126,800	0%	
Number of bonded IOBs	4	210	1%	
Number of LOCed IOBs	4	4	100%	
Number of RAMB36E1/FIFO36E1s	0	135	0%	
Number of RAMB18E1/FIFO18E1s	0	270	0%	
Number of BUFG/BUFGCTRLs	0	32	0%	

Design Properties

- Enable Message Filtering
- Optional Design Summary Contents
 - Show Clock Report
 - Show Failing Constraints
 - Show Warnings
 - Show Errors

Processes: halfaddr

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
 - View RTL Schematic
 - View Technology Schematic
 - Check Syntax
 - Generate Post-Synthesis Simulation ...
- Implement Design
 - Generate Programming File
 - Configure Target Device
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Start Design Files Libraries

Design Summary (Programming File Generated) halfaddr halfaddr.ucf

Console

Launching : "Configure Target Device"

For further information on the status of this process, see the "_impact.log" file.

Process "Configure Target Device" launched successfully

Console Errors Warnings Find in Files Results

8. Program successfully uploaded

