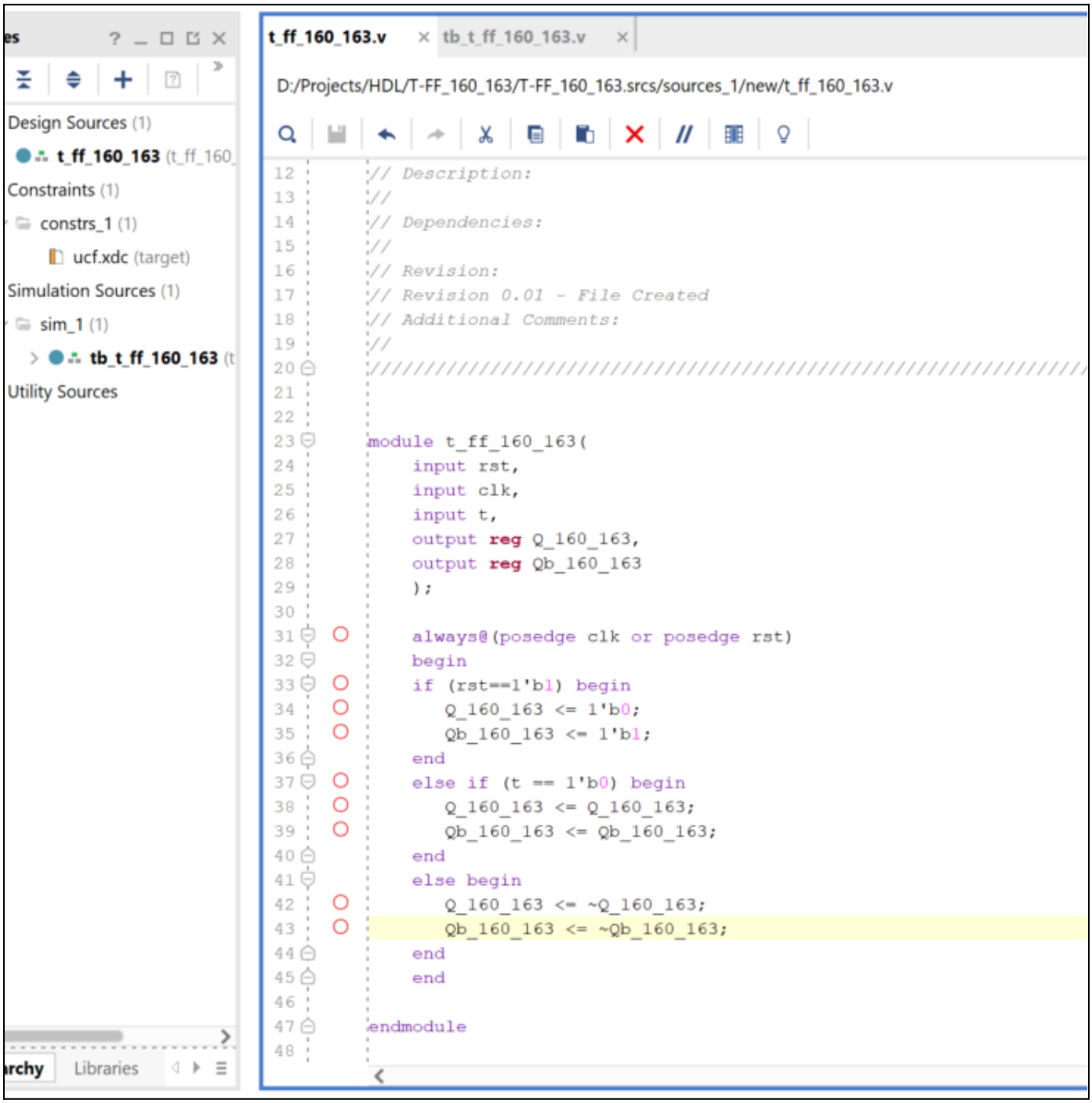
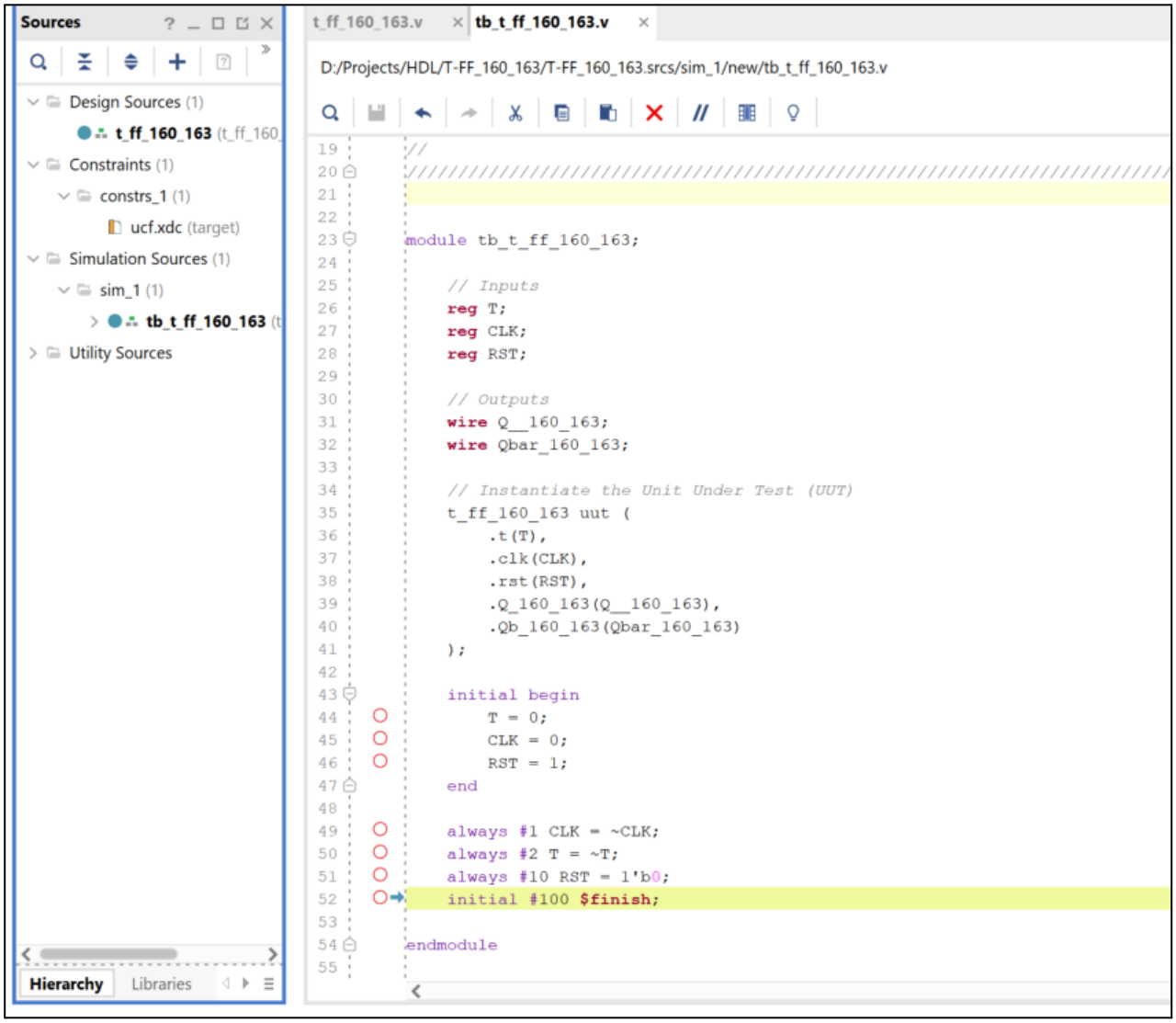
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

LAB: T Flipflop

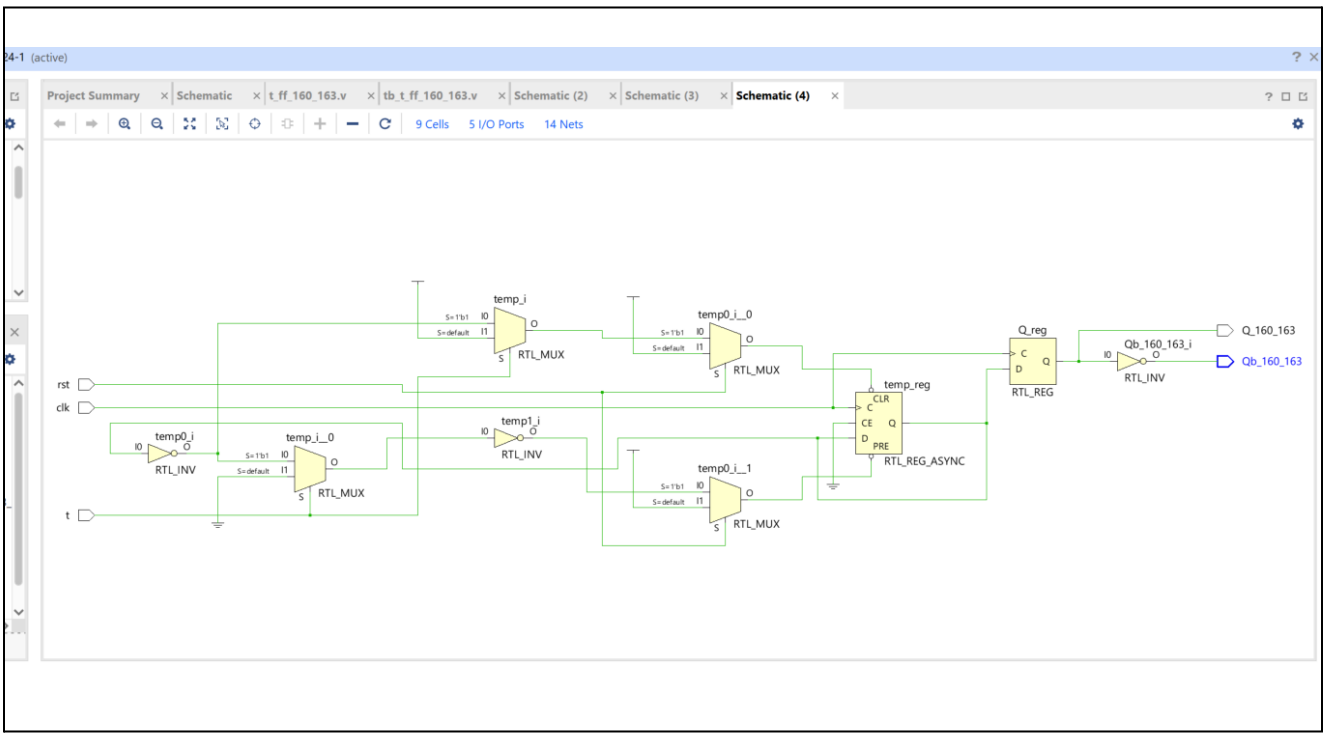
1. HDL Code



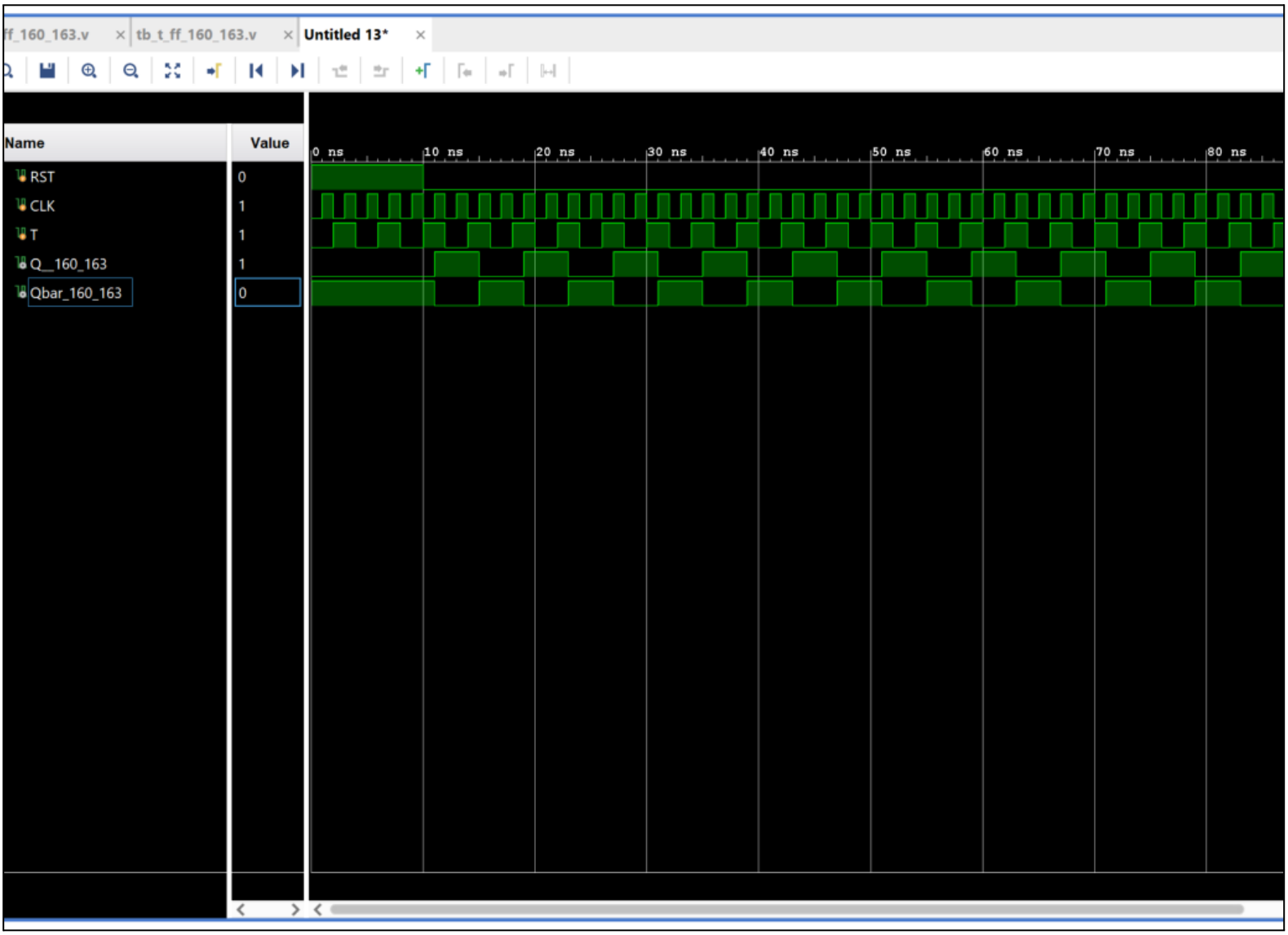
Text Bench Code



Schematic



Simulation



UCF File

t_ff_160_163.v | tb_t_ff_160_163.v | ucf.xdc

D:/Projects/HDL/T-FF_160_163/T-FF_160_163.srcs/constrs_1/new/ucf.xdc

```
1  create_pblock pblock_1
2  add_cells_to_pblock [get_pblocks pblock_1] -top
3  set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
4  set_property IOSTANDARD LVCMOS33 [get_ports clk]
5  set_property IOSTANDARD LVCMOS33 [get_ports Q_160_163]
6  set_property IOSTANDARD LVCMOS33 [get_ports Qb_160_163]
7  set_property IOSTANDARD LVCMOS33 [get_ports rst]
8  set_property IOSTANDARD LVCMOS33 [get_ports t]
9  set_property PACKAGE_PIN J15 [get_ports rst]
10 set_property PACKAGE_PIN V10 [get_ports clk]
11 set_property PACKAGE_PIN U11 [get_ports t]
12 set_property PACKAGE_PIN V11 [get_ports Q_160_163]
13 set_property PACKAGE_PIN V12 [get_ports Qb_160_163]
14
```

Design Summary