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LAB: Sequence Detector 1011

1. HDL Code

seqdet1011_160_163.v × tb_seq_det_160_163.v * ×

D:/Projects/HDL/SequenceDetector1011_160_163/SequenceDetector1011_160_163.srcs/sources_1/new/seqdet1011_160_163.v

```
21
22
23  module seqdet1011_160_163(rst,clk,ip,op_160_163);
24
25      input clk, rst, ip;
26      output reg op_160_163;
27
28
29       reg [2:0] state;
30       reg [2:0] next_state;
31
32       parameter [1:0] s0=2'b00; // state -> 0
33       parameter [1:0] s1=2'b01; // state -> 1
34       parameter [1:0] s2=2'b10; // state -> 10
35       parameter [1:0] s3=2'b11; // state -> 101
36
37
38       always @(posedge clk, posedge rst)
39       begin
40          if (rst)
41              state<=s0;
42          else
43              state<=next_state;
44       end
45
46       always @(state, ip)
47       begin
48          case(state)
49          s0:
50              if (ip)
51              begin
52                      next_state<=s1;
53                      op_160_163<=1'b0;
54              end
55              else
56              begin
```

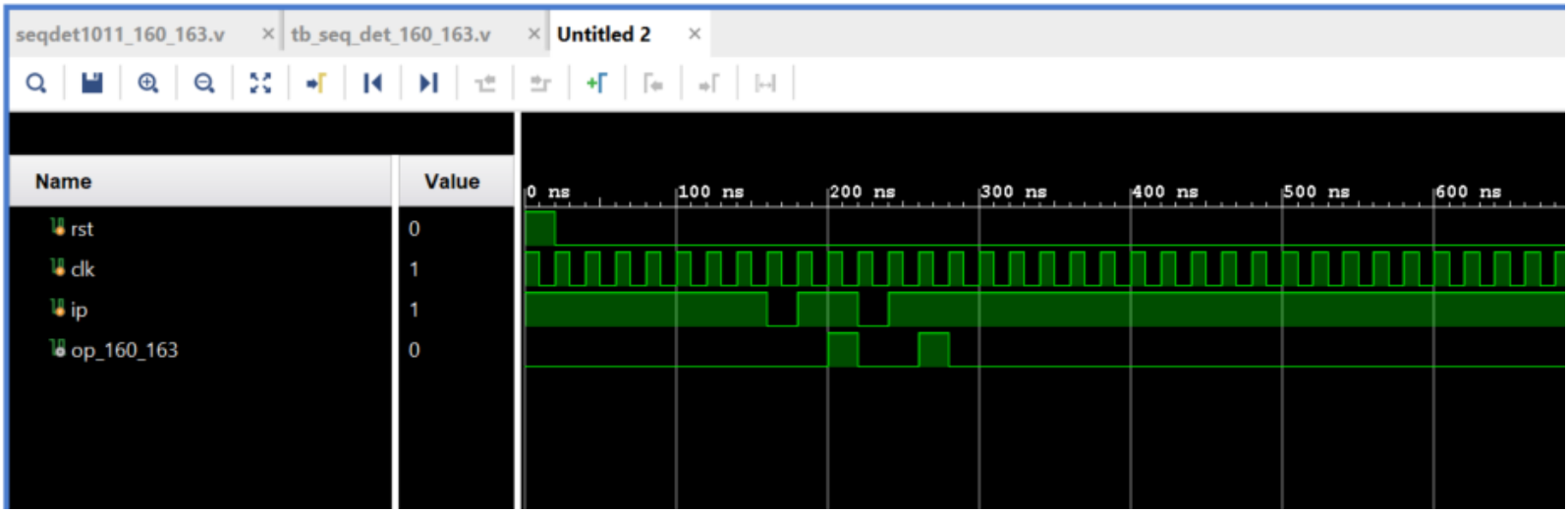
Text Bench Code

seqdet1011_160_163.v | tb_seq_det_160_163.v | Untitled 2

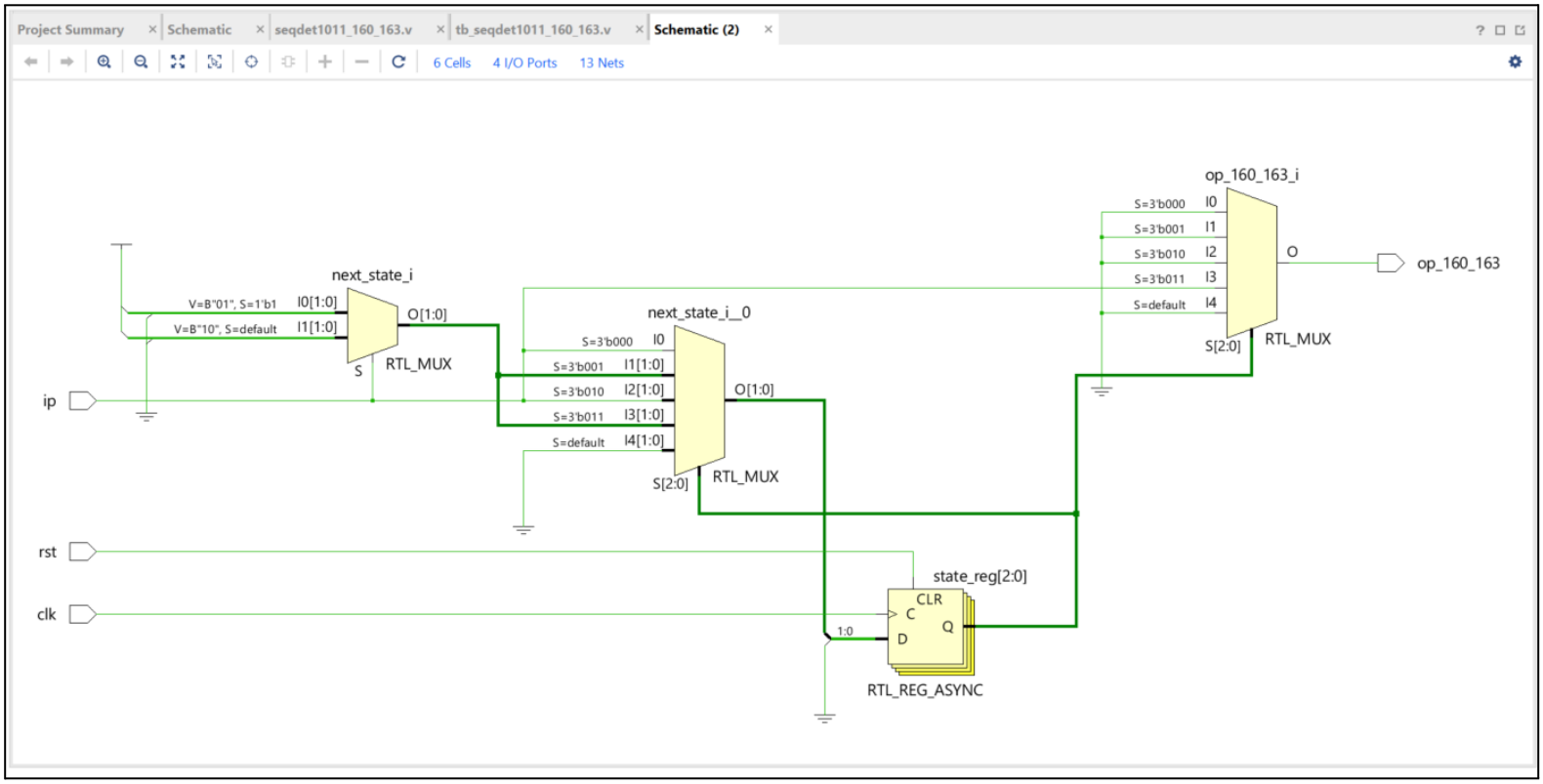
D:/Projects/HDL/SequenceDetector1011_160_163/SequenceDetector1011_160_163.srcs/sim_1/new/tb_seq_det_160_163.v

```
31
32      // Instantiate the Unit Under Test (UUT)
33      seqdet1011_160_163 uut (
34          .rst(rst),
35          .clk(clk),
36          .ip(ip),
37          .op_160_163(op_160_163)
38      );
39
40      initial begin
41          // Initialize Inputs
42          clk = 1;
43          forever #10 clk=~clk;
44          end
45
46          initial begin
47          // Initialize Inputs
48          rst = 1;
49           #20;
50           rst = 0;
51           #1000;
52
53          end
54
55
56          initial begin
57          // Initialize Inputs
58          ip = 1;
59           #40;
60           ip = 1;
61           #20;
62           ip = 1;
63           #20;
64           ip = 1;
65           #20;
66           ip = 1;
```

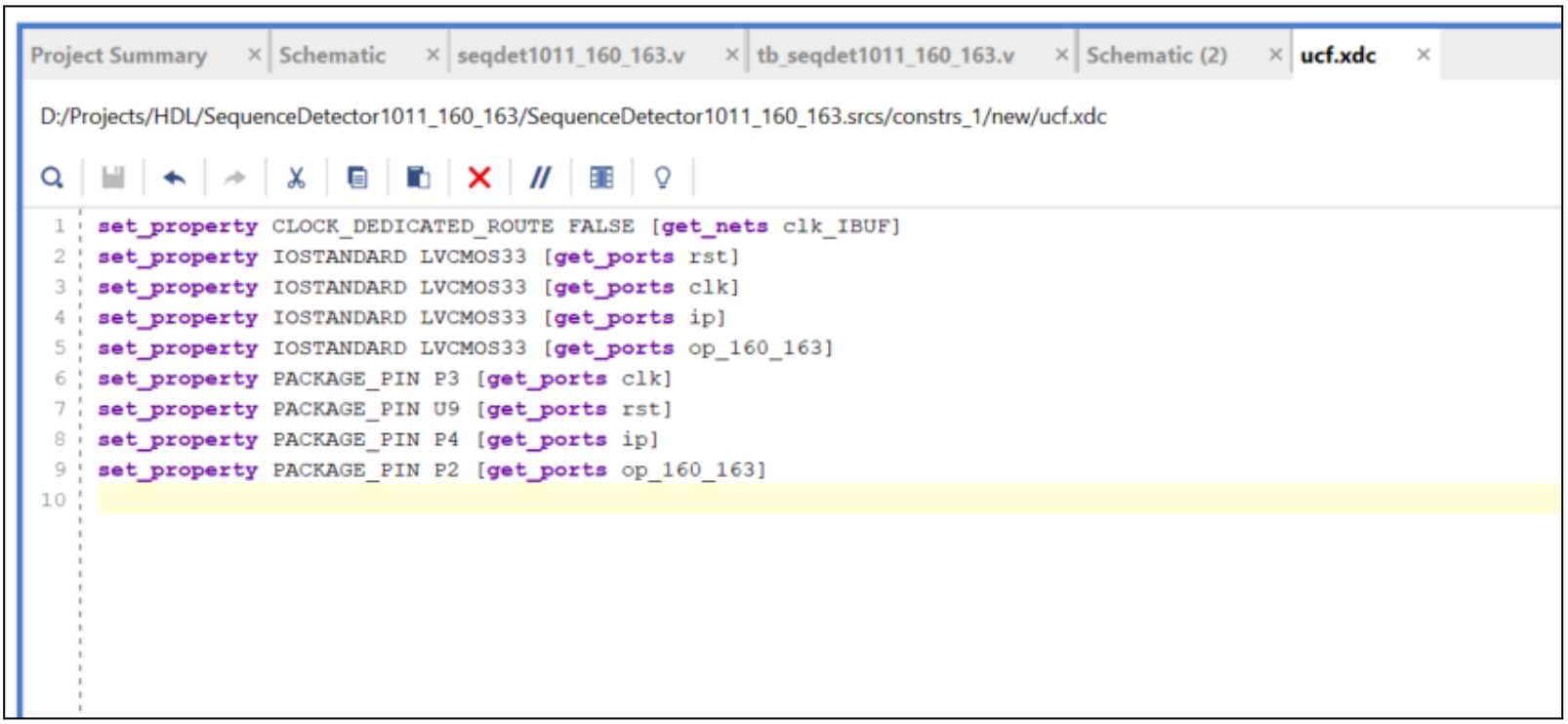
Simulation



Schematic



UCF File



Project Summary