

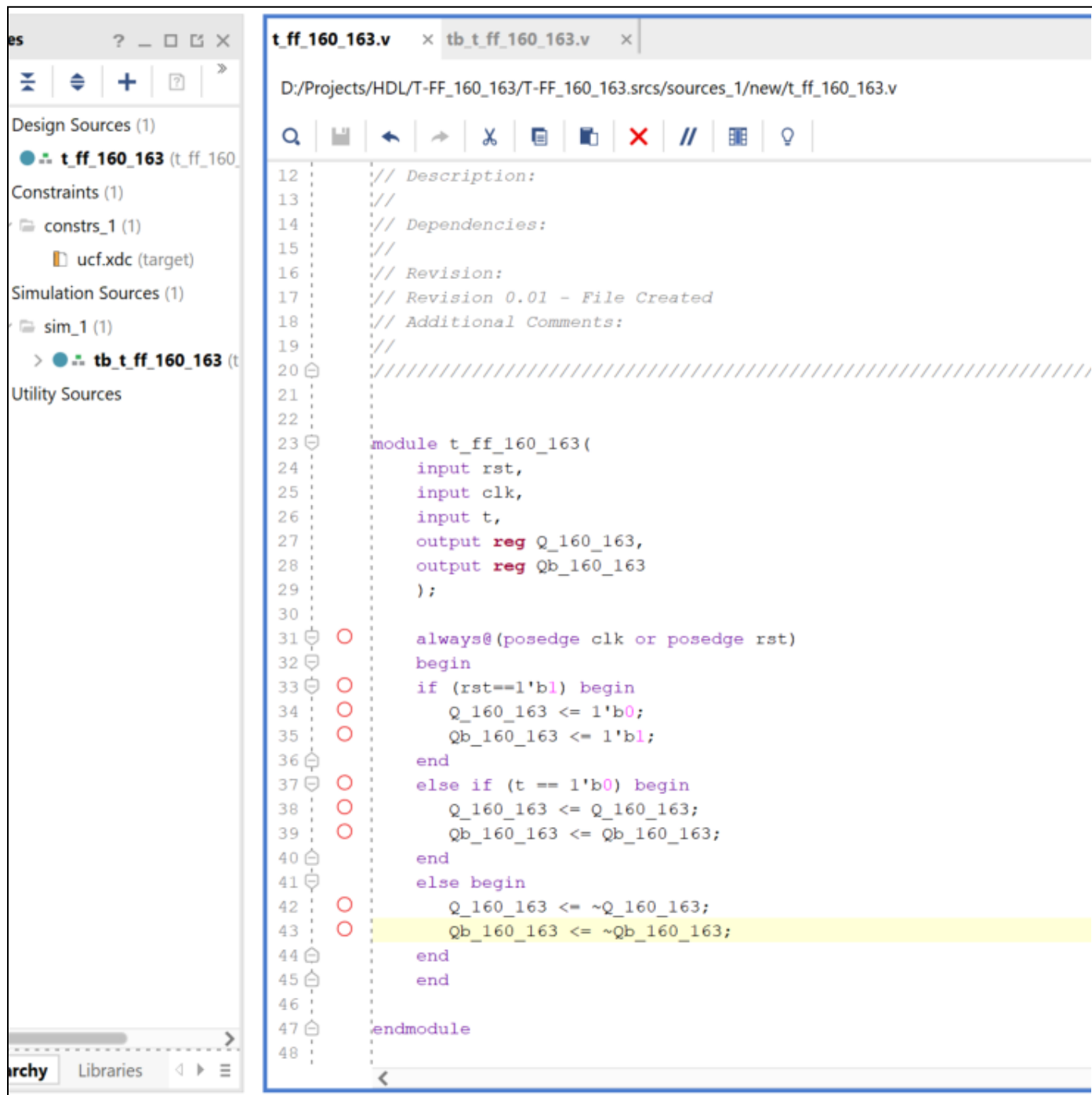
Name - Pranav Unkule

Roll No - 160

PRN - 0120190250

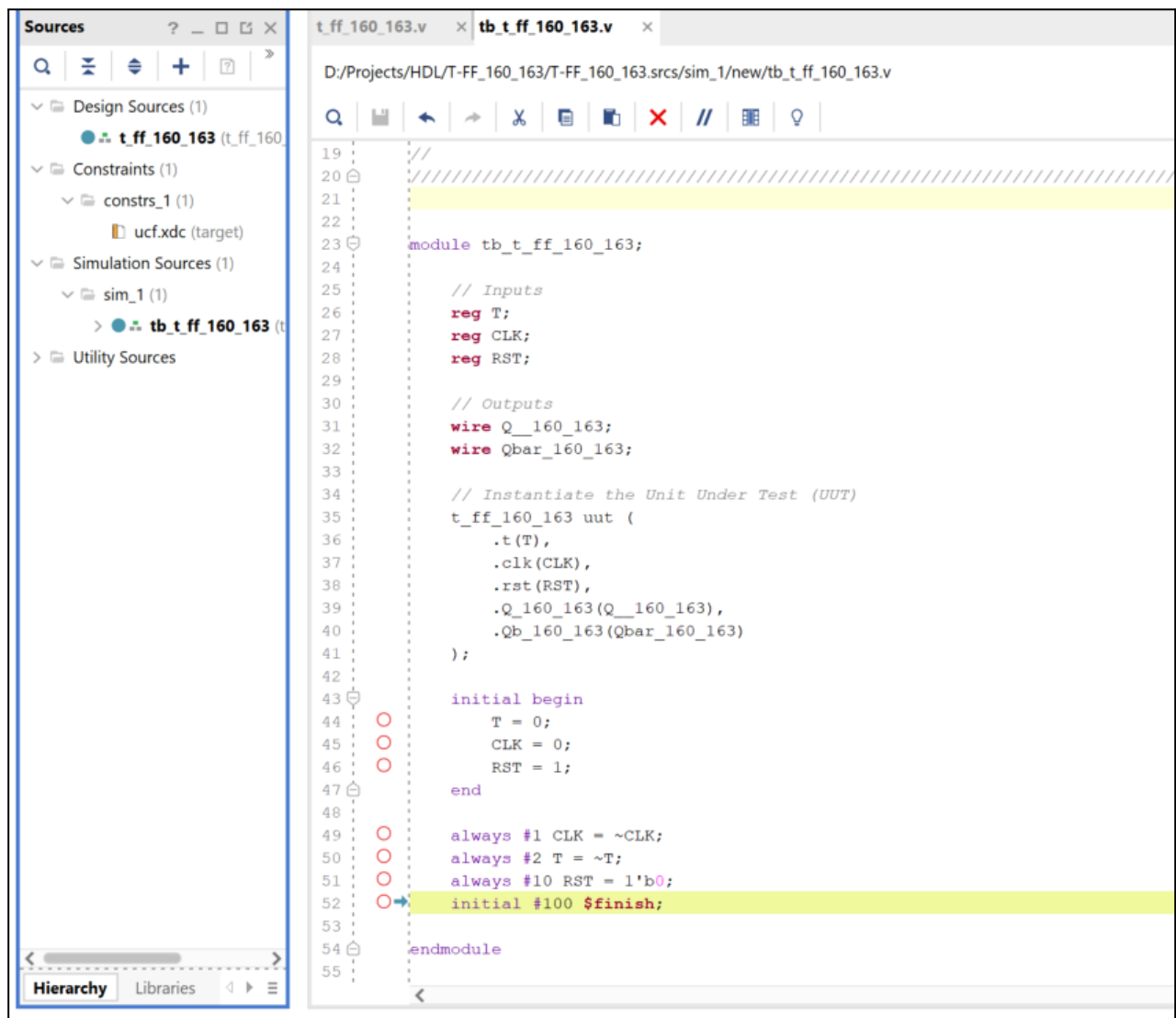
LAB: T Flipflop

1. HDL Code

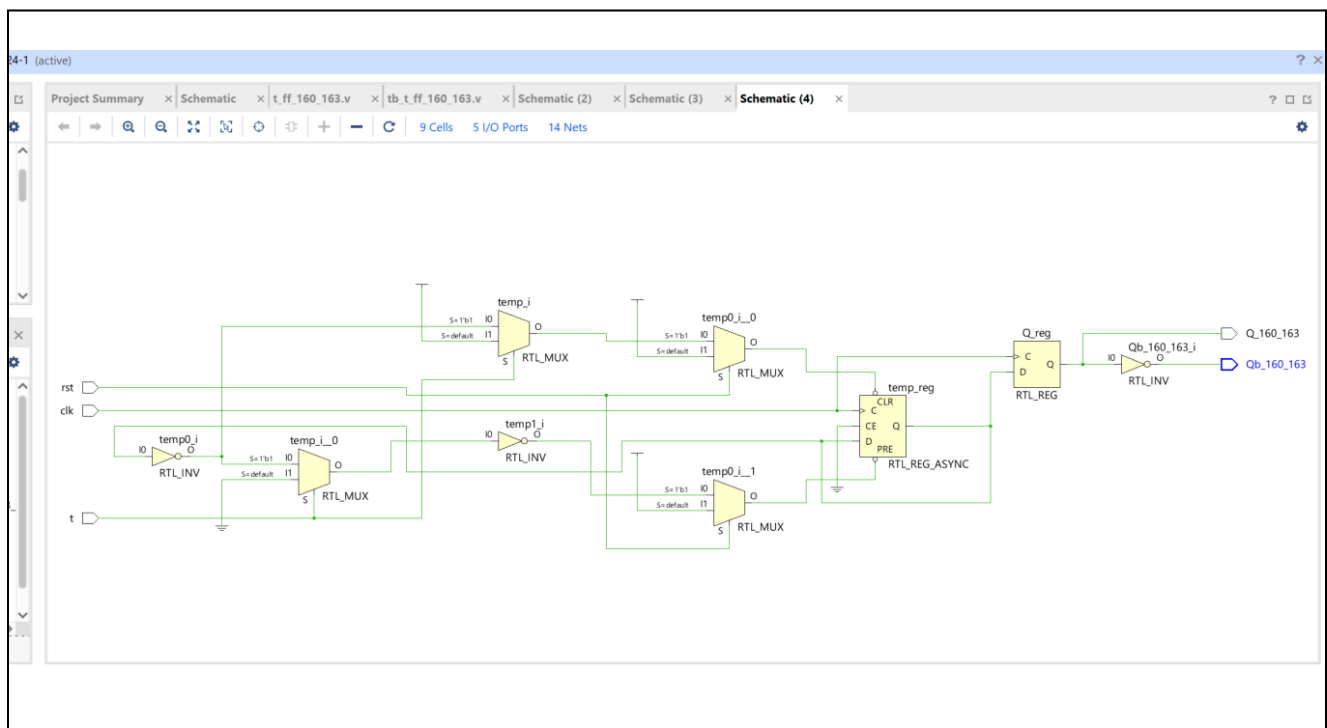


```
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22
23 module t_ff_160_163(
24     input rst,
25     input clk,
26     input t,
27     output reg Q_160_163,
28     output reg Qb_160_163
29 );
30
31 always@(posedge clk or posedge rst)
32 begin
33     if (rst==1'b1) begin
34         Q_160_163 <= 1'b0;
35         Qb_160_163 <= 1'b1;
36     end
37     else if (t == 1'b0) begin
38         Q_160_163 <= Q_160_163;
39         Qb_160_163 <= Qb_160_163;
40     end
41     else begin
42         Q_160_163 <= ~Q_160_163;
43         Qb_160_163 <= ~Qb_160_163;
44     end
45 end
46
47 endmodule
48
```

Text Bench Code



Schematic



Simulation



UCF File

```
t_ff_160_163.v x tb_t_ff_160_163.v x ucf.xdc x
D:/Projects/HDL/T-FF_160_163/T-FF_160_163.srscs/constrs_1/new/ucf.xdc

1 create_pblock pblock_1
2 add_cells_to_pblock [get_pblocks pblock_1] -top
3 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
4 set_property IOSTANDARD LVCMOS33 [get_ports clk]
5 set_property IOSTANDARD LVCMOS33 [get_ports Q_160_163]
6 set_property IOSTANDARD LVCMOS33 [get_ports Qb_160_163]
7 set_property IOSTANDARD LVCMOS33 [get_ports rst]
8 set_property IOSTANDARD LVCMOS33 [get_ports t]
9 set_property PACKAGE_PIN J15 [get_ports rst]
10 set_property PACKAGE_PIN V10 [get_ports clk]
11 set_property PACKAGE_PIN U11 [get_ports t]
12 set_property PACKAGE_PIN V11 [get_ports Q_160_163]
13 set_property PACKAGE_PIN V12 [get_ports Qb_160_163]
14
```

Design Summary

t_ff_160_163.v

tb_t_ff_160_163.v

ucf.xdc

Project Summary

?

□

⌵

Overview | Dashboard

Settings

Edit

Project name:

T-FF_160_163

Project location:

D:/Projects/HDL/T-FF_160_163

Product family:

Artix-7

Project part:

xc7a100tcsg324-1

Top module name:

t_ff_160_163

Target language:

Verilog

Simulator language:

Mixed

Synthesis

Summary

Status:

Complete

Messages:

1 critical warning

2 warnings

Part:

xc7a100tcsg324-1

Strategy:

Vivado Synthesis Defaults

Report Strategy:

Vivado Synthesis Default Reports

Implementation

Summary

Route Status

Status:

Complete

Messages:

6 warnings

Part:

xc7a100tcsg324-1

Strategy:

Vivado Implementation Defaults

Report Strategy:

Vivado Implementation Default Reports

Incremental implementation:

None

DRC Violations

Summary

Summary:

2 warnings

Implemented DRC Report

Timing

Setup

Hold

Pulse Width

Worst Negative Slack (WNS):

NA

Total Negative Slack (TNS):

NA

Number of Failing Endpoints:

NA

Total Number of Endpoints:

NA

Implemented Timing Report

Utilization

Implementation

Graph

Table

LUT

1%

FF

1%

IO

2%

BUFG

3%

0

25

Power

Summary

On-Chip

Total On-Chip Power:

11.877 W

Junction Temperature:

79.2 °C

Thermal Margin:

5.8 °C (1.3 W)

Effective θJA:

4.6 °C/W

Power supplied to off-chip devices:

0 W

Confidence level:

Low

Implemented Power Report

Bitstream Generation Completed

×

Bitstream Generation successfully completed.

Next

☒ Open Implemented Design

☐ View Reports

☐ Open Hardware Manager

☐ Generate Memory Configuration File

☐ Don't show this dialog again

OK

Cancel