

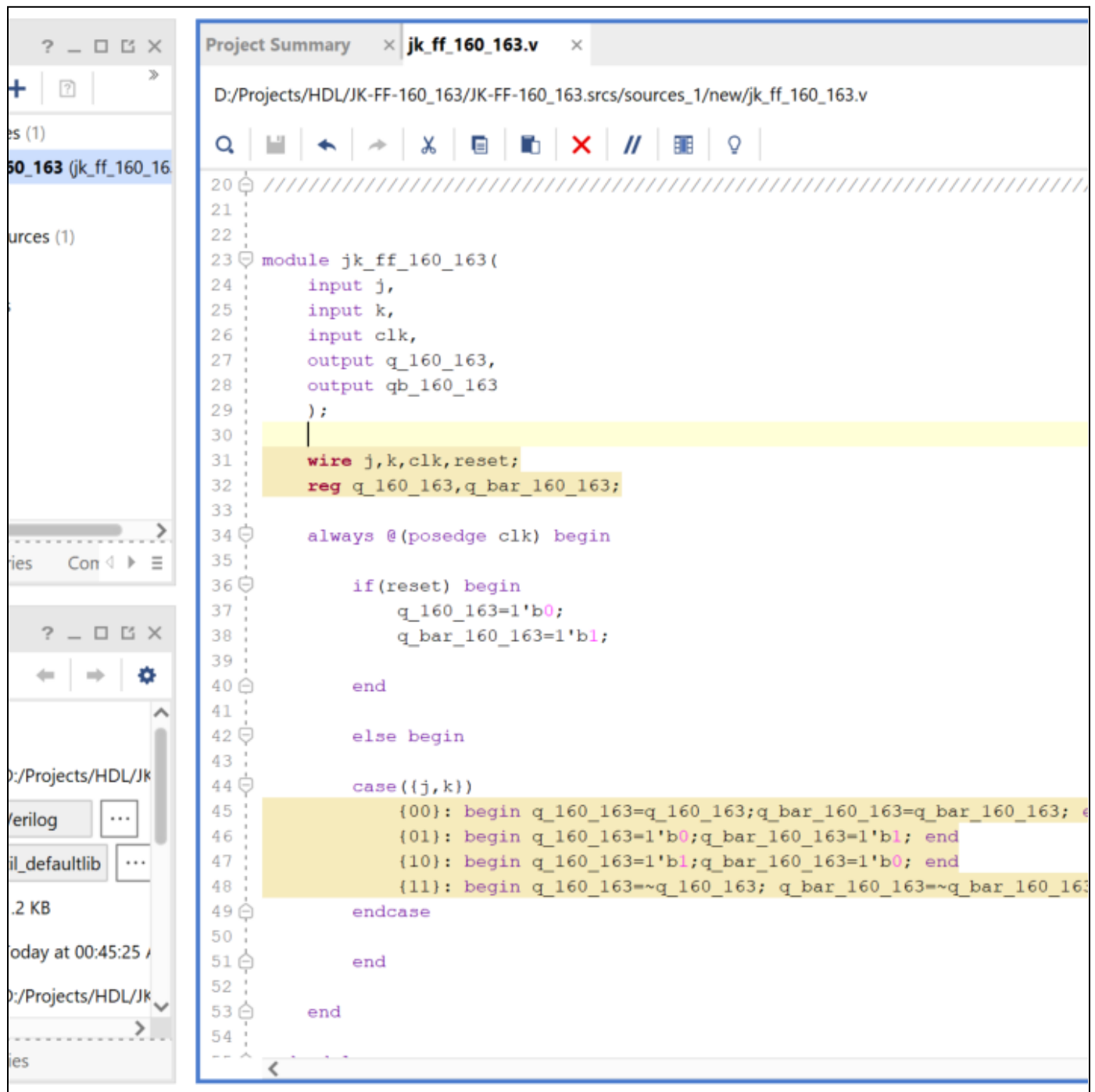
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Roll No - 160

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LAB: JK Flipflop

1. HDL Code



```
20 ///////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
21
22
23 module jk_ff_160_163(
24     input j,
25     input k,
26     input clk,
27     output q_160_163,
28     output qb_160_163
29 );
30
31 wire j,k,clk,reset;
32 reg q_160_163,q_bar_160_163;
33
34 always @(posedge clk) begin
35
36     if(reset) begin
37         q_160_163=1'b0;
38         q_bar_160_163=1'b1;
39
40     end
41
42     else begin
43
44         case({j,k})
45             {00}: begin q_160_163=q_160_163;q_bar_160_163=q_bar_160_163; end
46             {01}: begin q_160_163=1'b0;q_bar_160_163=1'b1; end
47             {10}: begin q_160_163=1'b1;q_bar_160_163=1'b0; end
48             {11}: begin q_160_163=~q_160_163; q_bar_160_163=~q_bar_160_163; end
49         endcase
50
51     end
52
53 end
54
```

Text Bench Code

Design Sources (1)

tb_jk_ff_160_163 (jk_ff_160_163)

Simulation Sources (1)

sim_1 (1)

Utility Sources

tb_jk_ff_160_163.v

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// Additional Comments:

//

////////////////////////////////////

module tb_jk_ff_160_163;

reg clk;

reg reset;

reg j,k;

wire q_160_163;

wire q_bar_160_163;

jk_ff_160_163 uut (.clk(clk), .reset(reset), .j(j), .k(k),

q_160_163(q_160_163), .q_bar_160_163(q_bar_160_163));

initial begin

j = 1'b0;

k = 1'b0;

reset = 1;

clk=1;

#10

reset=0;

j=1'b1;

k=1'b0;

#100

reset=0;

j=1'b0;

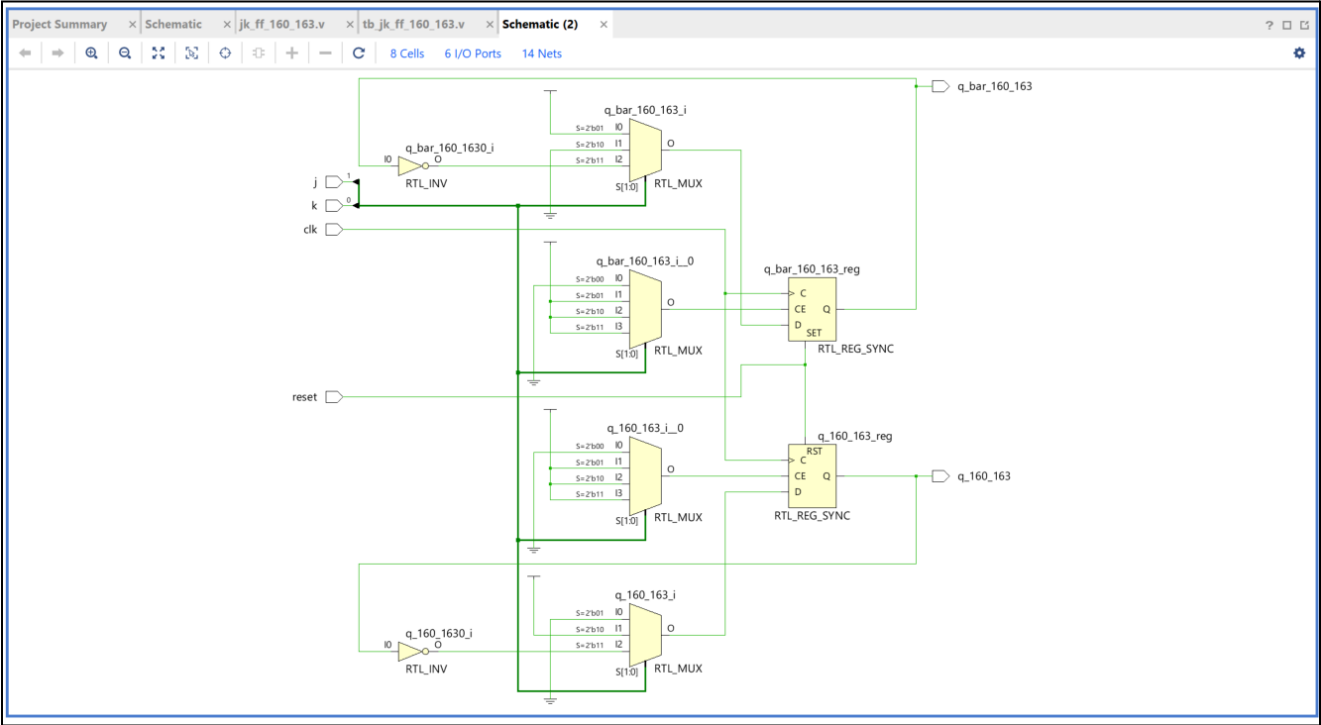
k=1'b1;

#100

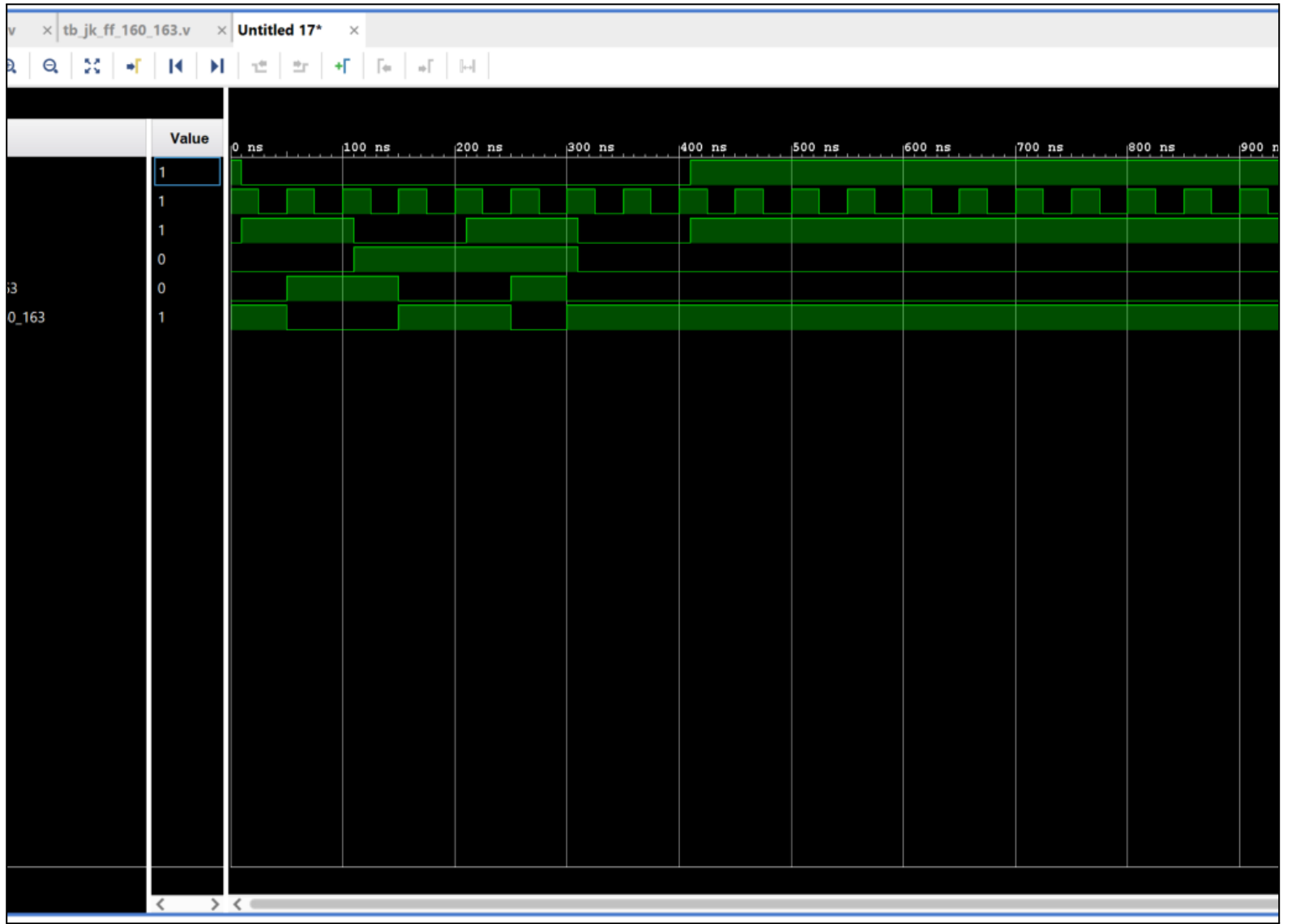
reset=0;

j=1'b1;

Schematic



Simulation



UCF File

```
Schematic x jk_ff_160_163.v x tb_jk_ff_160_163.v x Schematic (2) x ucf.xdc x
D:/Projects/HDL/JK-FF-160_163/JK-FF-160_163.srcs/constrs_1/new/ucf.xdc
1 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
2
3 set_property IOSTANDARD LVCOS33 [get_ports j]
4 set_property IOSTANDARD LVCOS33 [get_ports k]
5 set_property IOSTANDARD LVCOS33 [get_ports clk]
6 set_property IOSTANDARD LVCOS33 [get_ports reset]
7 set_property IOSTANDARD LVCOS33 [get_ports q_160_163]
8 set_property IOSTANDARD LVCOS33 [get_ports q_bar_160_163]
9 set_property PACKAGE_PIN V10 [get_ports j]
10 set_property PACKAGE_PIN U11 [get_ports k]
11 set_property PACKAGE_PIN J15 [get_ports clk]
12 set_property PACKAGE_PIN U12 [get_ports reset]
13 set_property PACKAGE_PIN V11 [get_ports q_160_163]
14 set_property PACKAGE_PIN V12 [get_ports q_bar_160_163]
15
```

Design Summary

Schematicxjk_ff_160_163.vxtb_jk_ff_160_163.vxSchematic (2)xucf.xdcxProject Summaryx

Overview | Dashboard

SettingsEdit

Project name:JK-FF-160_163

Project location:D:/Projects/HDL/JK-FF-160_163

Product family:Artix-7

Project part:xc7a100tcsg324-1

Top module name:jk_ff_160_163

Target language:Verilog

Simulator language:Mixed

Synthesis

Status:Complete

Messages:1 critical warning8 warnings

Part:xc7a100tcsg324-1

Strategy:Vivado Synthesis Defaults

Report Strategy:Vivado Synthesis Default Reports

DRC Violations

Summary:2 warnings

Implemented DRC Report

Utilization

Post-Synthesis | Post-Implementation

Graph | Table

LUT1%

FF1%

IO3%

BUFG3%

0255075100

Utilization (%)

Implementation

Status:Complete

Messages:6 warnings

Part:xc7a100tcsg324-1

Strategy:Vivado Implementation Defaults

Report Strategy:Vivado Implementation Default Reports

Incremental implementation:None

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS):NA

Total Negative Slack (TNS):NA

Number of Failing Endpoints:NA

Total Number of Endpoints:NA

Implemented Timing Report

Power

Total On-Chip Power:2.486 W

Junction Temperature:36.3 °C

Thermal Margin:48.7 °C (10.5 W)

Effective θJA:4.6 °C/W

Power supplied to off-chip devices: 0 W

Confidence level:Low

Implemented Power Report

Summary | Route Status

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

Open Implemented Design

View Reports

Open Hardware Manager

Generate Memory Configuration File

Don't show this dialog again

OK

Cancel