

Name - Pranav Unkule

Roll No - 160

PRN - 0120190250

## LAB: Sequence Detector 1011

### 1. HDL Code

```
seqdet1011_160_163.v x tb_seq_det_160_163.v* x
D:/Projects/HDL/SequenceDetector1011_160_163/SequenceDetector1011_160_163.srscs/sources_1/new/seqdet1011_160_163.v

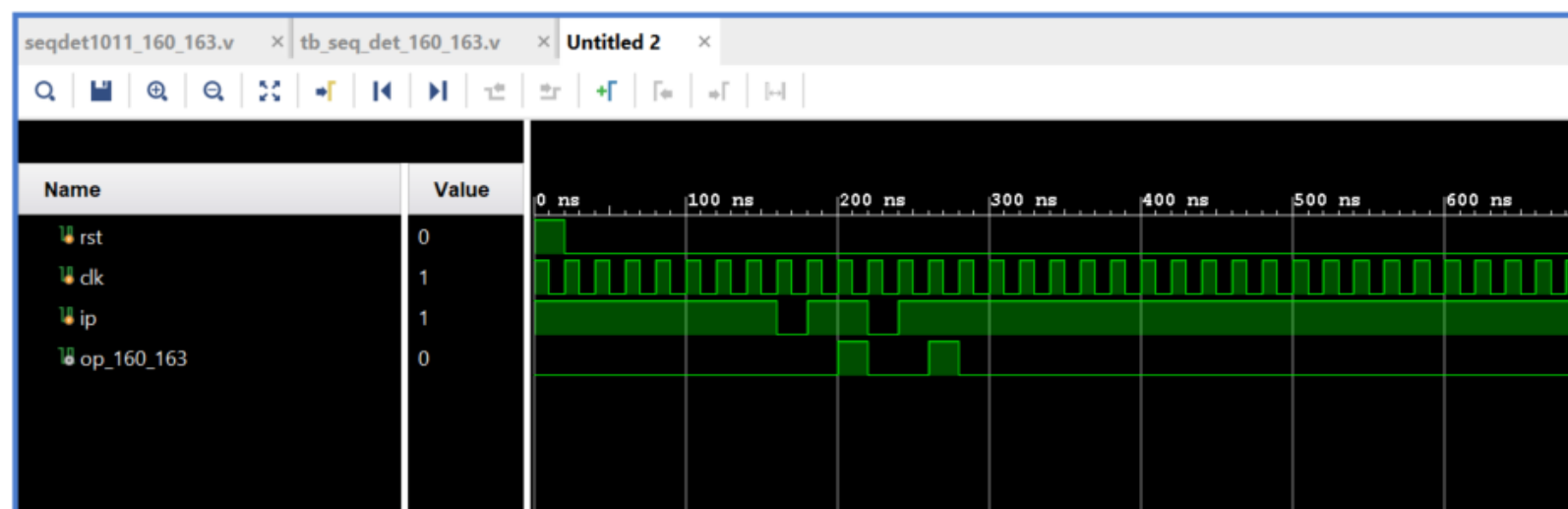
21
22
23 module seqdet1011_160_163(rst,clk,ip,op_160_163);
24
25     input clk, rst, ip;
26     output reg op_160_163;
27
28
29     reg [2:0] state;
30     reg [2:0] next_state;
31
32     parameter [1:0] s0=2'b00; // state -> 0
33     parameter [1:0] s1=2'b01; // state -> 1
34     parameter [1:0] s2=2'b10; // state -> 10
35     parameter [1:0] s3=2'b11; // state -> 101
36
37
38     always @(posedge clk, posedge rst)
39     begin
40         if (rst)
41             state<=s0;
42         else
43             state<=next_state;
44     end
45
46     always @(state, ip)
47     begin
48         case(state)
49         s0:
50             if (ip)
51             begin
52                 next_state<=s1;
53                 op_160_163<=1'b0;
54             end
55         else
56             begin
57                 next_state<=s0;
58             end
59         endcase
60     end
61 endmodule
```

## Text Bench Code

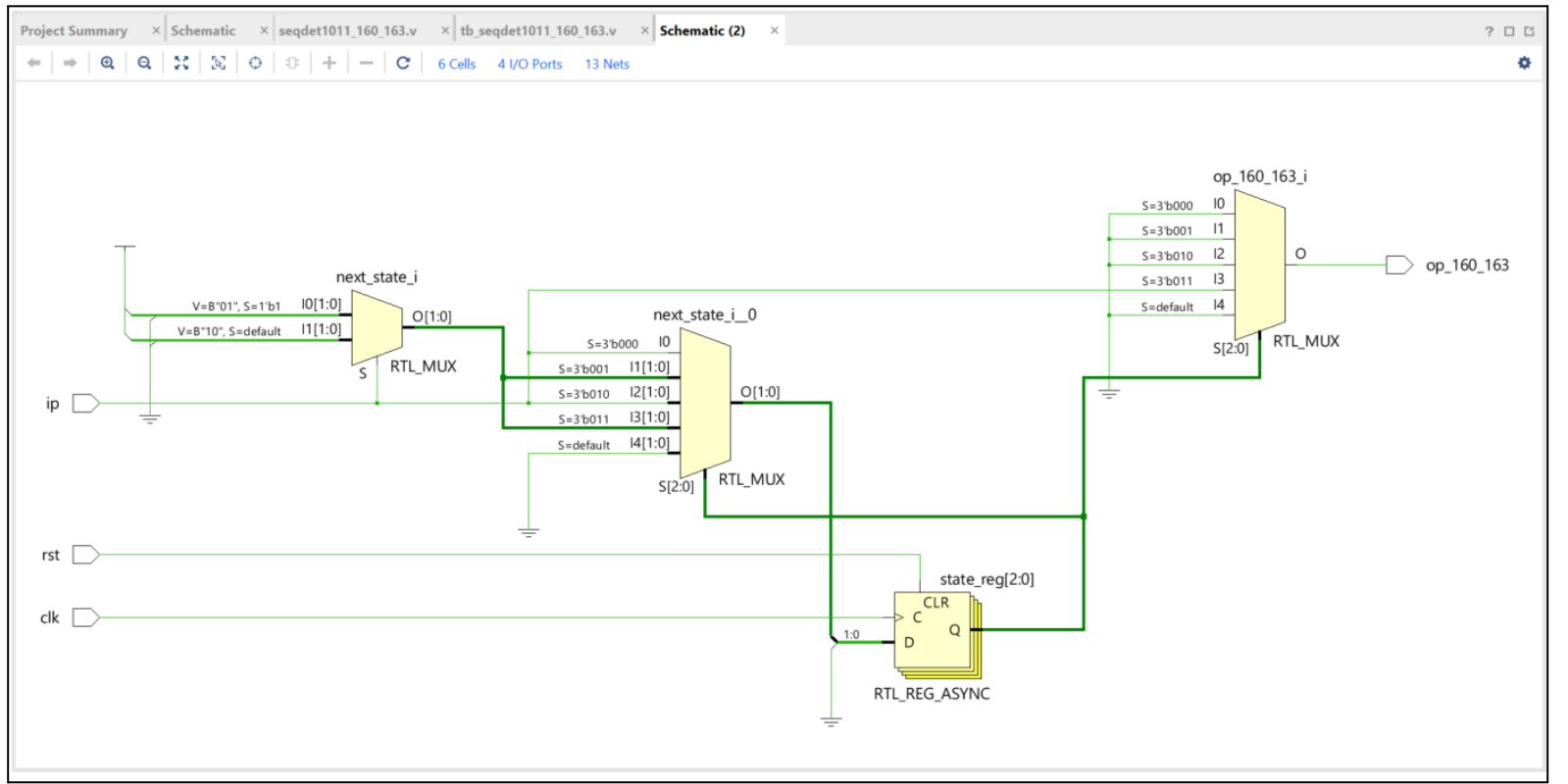
```
seqdet1011_160_163.v  x  tb_seq_det_160_163.v  x  Untitled 2  x
D:/Projects/HDL/SequenceDetector1011_160_163/SequenceDetector1011_160_163.srscs/sim_1/new/tb_seq_det_160_163.v

31
32 // Instantiate the Unit Under Test (UUT)
33 seqdet1011_160_163 uut (
34     .rst(rst),
35     .clk(clk),
36     .ip(ip),
37     .op_160_163(op_160_163)
38 );
39
40 initial begin
41     // Initialize Inputs
42     clk = 1;
43     forever #10 clk=~clk;
44 end
45
46 initial begin
47     // Initialize Inputs
48     rst = 1;
49     #20;
50     rst = 0;
51     #1000;
52
53 end
54
55
56 initial begin
57     // Initialize Inputs
58     ip = 1;
59     #40;
60     ip = 1;
61     #20;
62     ip = 1;
63     #20;
64     ip = 1;
65     #20;
66     ip = 1;
67     #20;
```

## Simulation



Schematic



UCF File

```
Project Summary x Schematic x seqdet1011_160_163.v x tb_seqdet1011_160_163.v x Schematic (2) x ucf.xdc x
D:/Projects/HDL/SequenceDetector1011_160_163/SequenceDetector1011_160_163.srscs/constrs_1/new/ucf.xdc

1 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
2 set_property IOSTANDARD LVCMOS33 [get_ports rst]
3 set_property IOSTANDARD LVCMOS33 [get_ports clk]
4 set_property IOSTANDARD LVCMOS33 [get_ports ip]
5 set_property IOSTANDARD LVCMOS33 [get_ports op_160_163]
6 set_property PACKAGE_PIN P3 [get_ports clk]
7 set_property PACKAGE_PIN U9 [get_ports rst]
8 set_property PACKAGE_PIN P4 [get_ports ip]
9 set_property PACKAGE_PIN P2 [get_ports op_160_163]
10
```

# Project Summary

Project Summary

Overview | Dashboard

Settings | Edit

Project name:

SequenceDetector1011\_160\_163

Project location:

D:/Projects/HDL/SequenceDetector1011\_160\_163

Product family:

Artix-7

Project part:

[xc7a100tcsg324-2](#)

Top module name:

seqdet1011\_160\_163

Target language:

Verilog

Simulator language:

Mixed

Synthesis

Status:

✔ Complete

Messages:

1 critical warning

2 warnings

Part:

xc7a100tcsg324-2

Strategy:

[Vivado Synthesis Defaults](#)

Report Strategy:

[Vivado Synthesis Default Reports](#)

Implementation

Summary | Route Status

Status:

✔ Complete

Messages:

6 warnings

Part:

xc7a100tcsg324-2

Strategy:

[Vivado Implementation Defaults](#)

Report Strategy:

[Vivado Implementation Default Reports](#)

Incremental implementation:

None

DRC Violations

Summary:

2

Implemented DRC

Timing

Setup | Hold | Pulse Width

Worst Negative Slack (WNS):

NA

Total Negative Slack (TNS):

NA

Number of Failing Endpoints:

NA

Total Number of Endpoints:

NA

[Implemented Timing Report](#)

Power

Summary | On-Chip

Total On-Chip Power:

0.5 W

Junction Temperature:

27.3 °C

Thermal Margin:

57.7 °C (12.5 W)

Effective θJA:

4.6 °C/W

Power supplied to off-chip devices:

0 W

Confidence level:

[Low](#)

[Implemented Power Report](#)

Utilization

LUT

1%

FF

1%

IO

2%

BUFG

3%

0

Bitstream Generation Completed

✔

Bitstream Generation successfully completed.

Next

☒ Open Implemented Design

☐ View Reports

☐ Open Hardware Manager

☐ Generate Memory Configuration File

☐ Don't show this dialog again

OK

Cancel