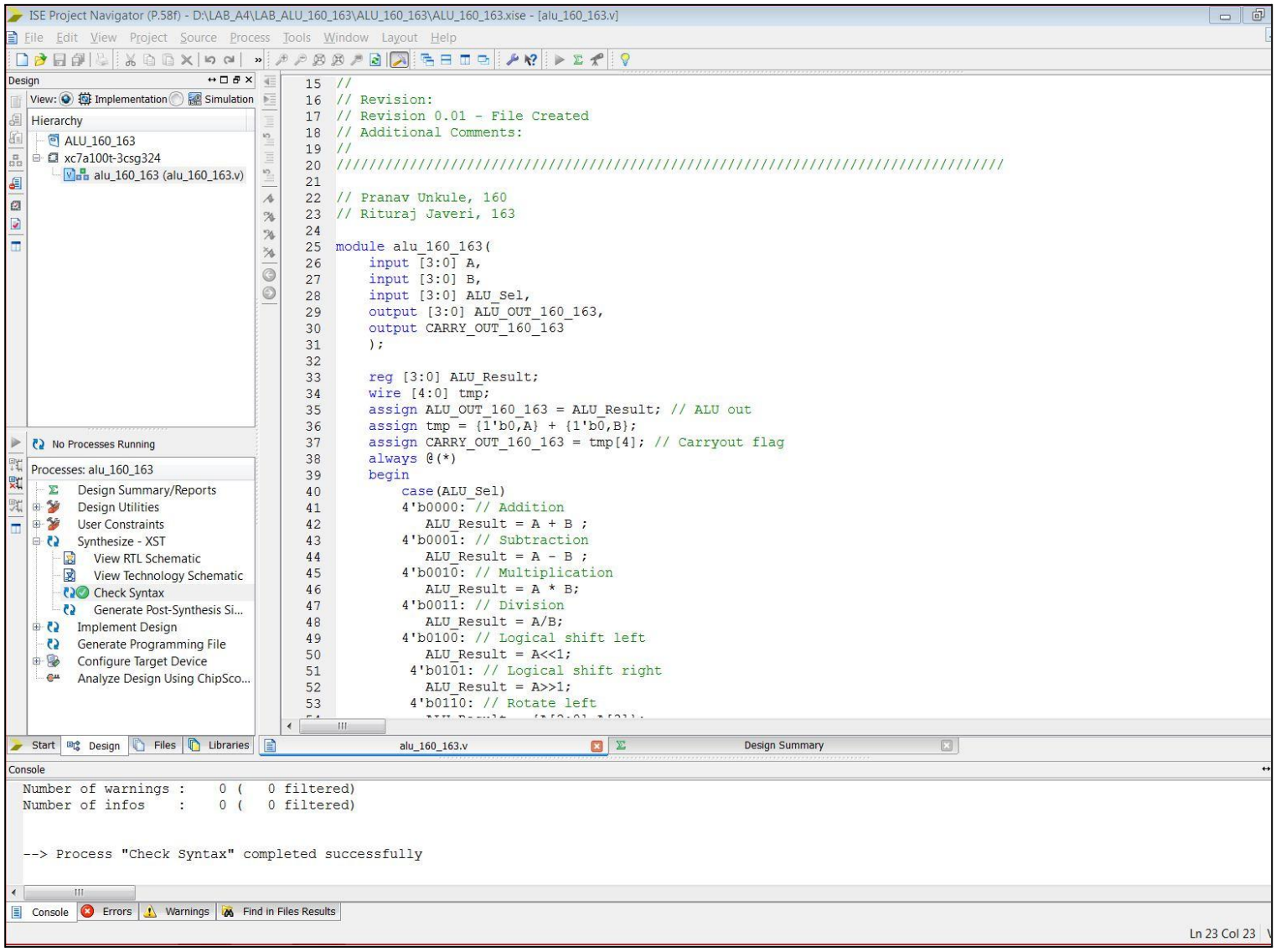
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

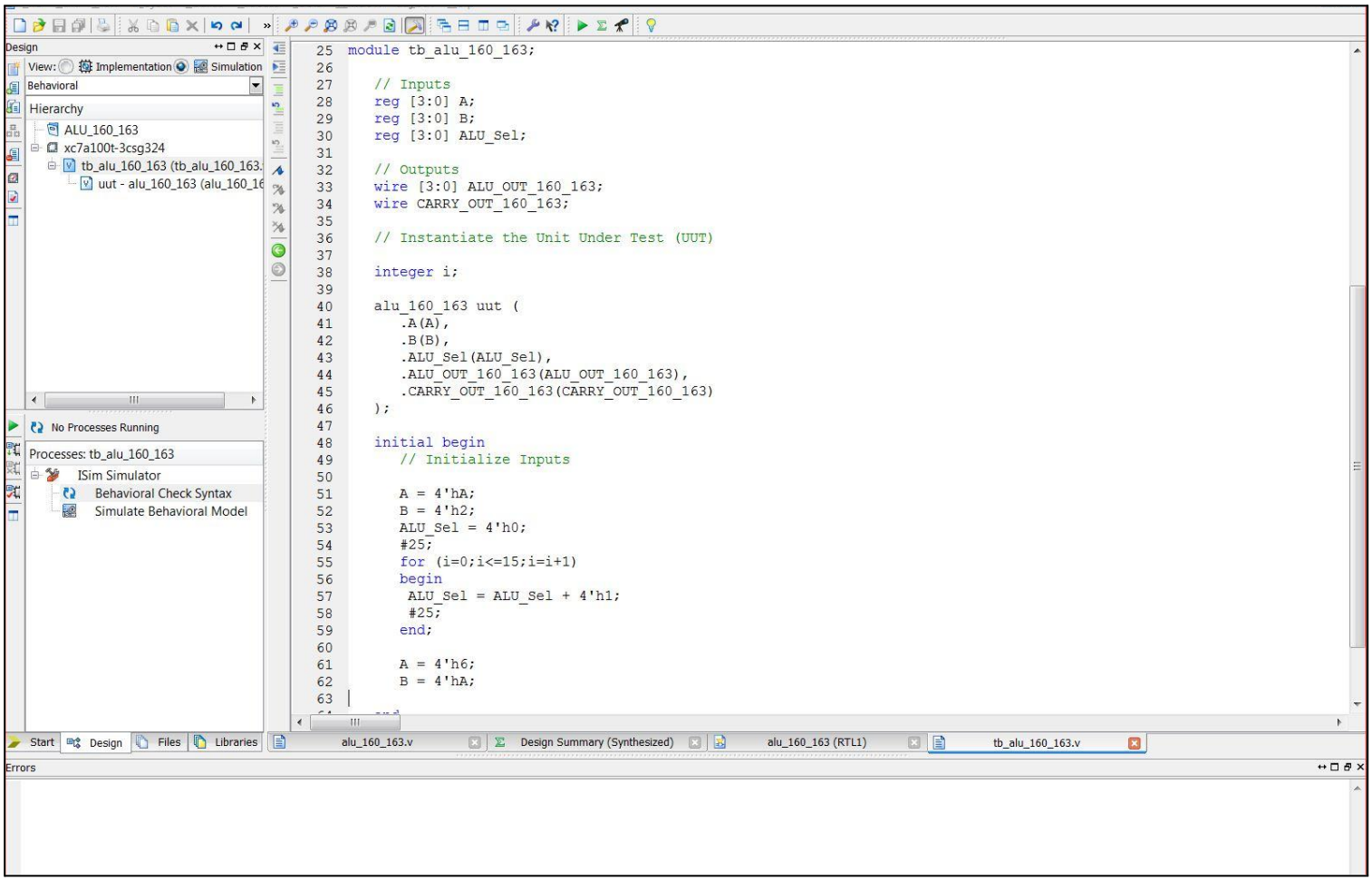
LAB 03 ALU

1. HDL Code



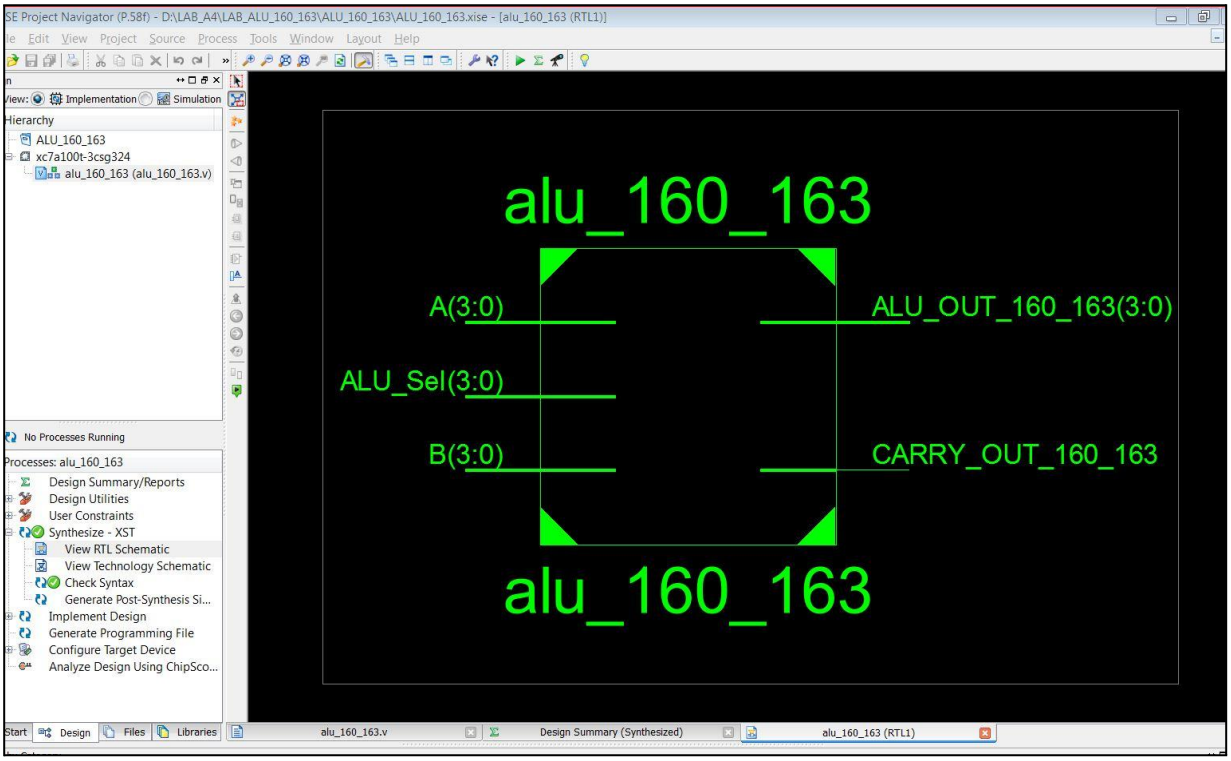

```
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22  // Pranav Unkule, 160
23  // Rituraj Javeri, 163
24
25  module alu_160_163(
26      input [3:0] A,
27      input [3:0] B,
28      input [3:0] ALU_Sel,
29      output [3:0] ALU_OUT_160_163,
30      output CARRY_OUT_160_163
31      );
32
33      reg [3:0] ALU_Result;
34      wire [4:0] tmp;
35      assign ALU_OUT_160_163 = ALU_Result; // ALU out
36      assign tmp = {1'b0,A} + {1'b0,B};
37      assign CARRY_OUT_160_163 = tmp[4]; // Carryout flag
38      always @(*)
39      begin
40          case(ALU_Sel)
41          4'b0000: // Addition
42             ALU_Result = A + B ;
43          4'b0001: // Subtraction
44             ALU_Result = A - B ;
45          4'b0010: // Multiplication
46             ALU_Result = A * B;
47          4'b0011: // Division
48             ALU_Result = A/B;
49          4'b0100: // Logical shift left
50             ALU_Result = A<<1;
51           4'b0101: // Logical shift right
52             ALU_Result = A>>1;
53           4'b0110: // Rotate left
```

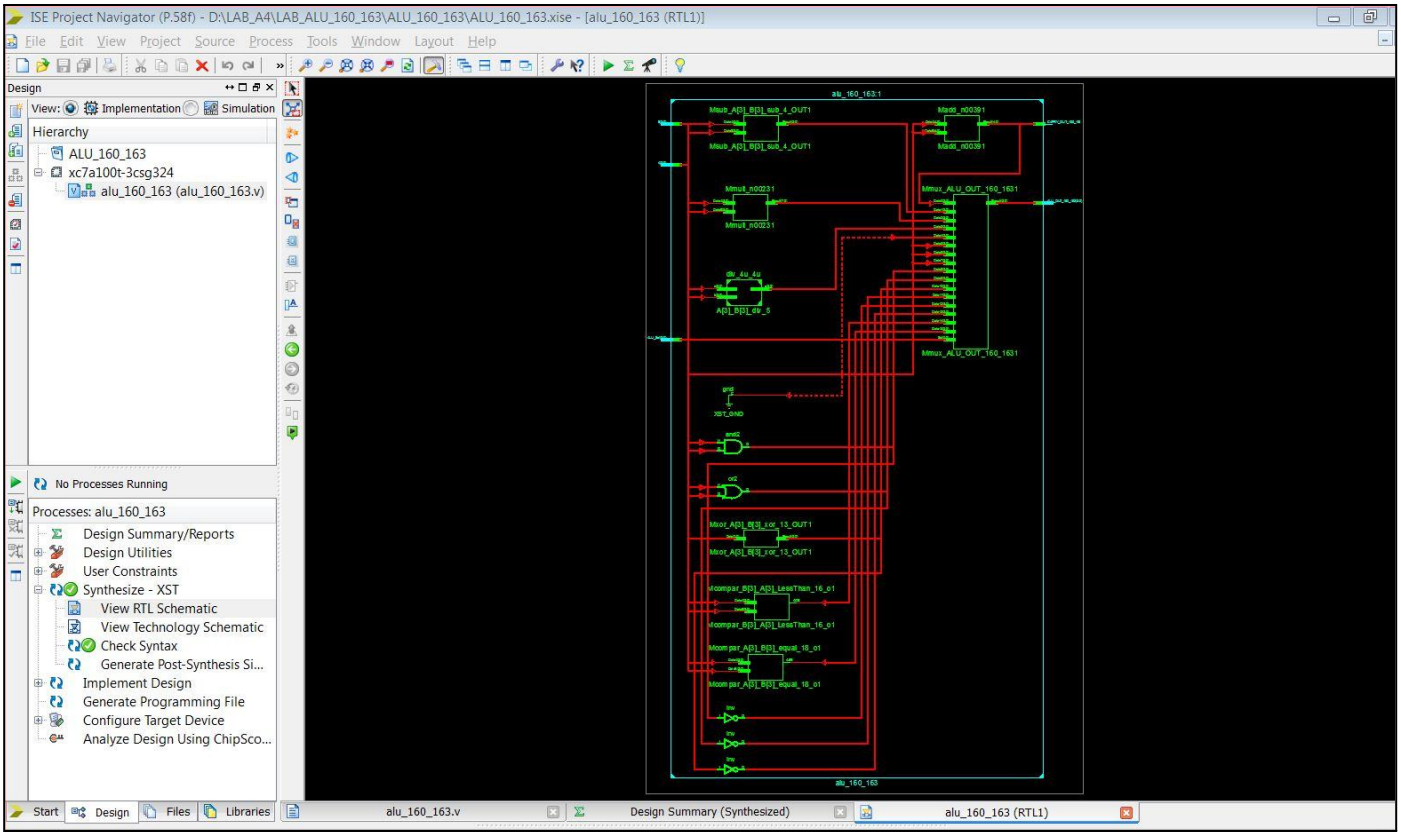
Text Bench Code



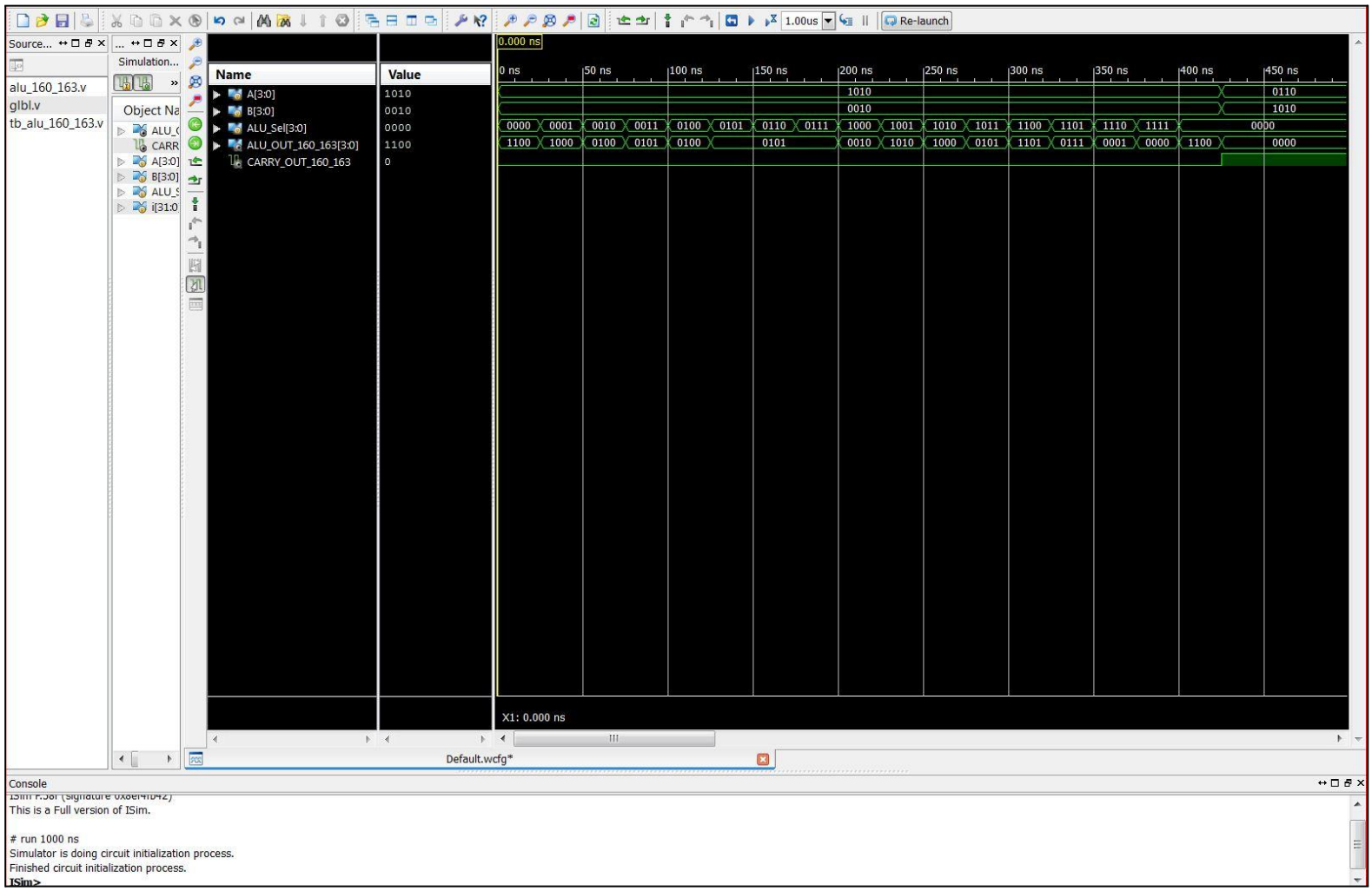
```
module tb_alu_160_163;

    // Inputs
    reg [3:0] A;
    reg [3:0] B;
    reg [3:0] ALU_Sel;

    // Outputs
    wire [3:0] ALU_OUT_160_163;
    wire CARRY_OUT_160_163;

    // Instantiate the Unit Under Test (UUT)

    integer i;

    alu_160_163 uut (
        .A(A),
        .B(B),
        .ALU_Sel(ALU_Sel),
        .ALU_OUT_160_163(ALU_OUT_160_163),
        .CARRY_OUT_160_163(CARRY_OUT_160_163)
    );

    initial begin
        // Initialize Inputs

        A = 4'hA;
        B = 4'h2;
        ALU_Sel = 4'h0;
        #25;
        for (i=0;i<=15;i=i+1)
        begin
         ALU_Sel = ALU_Sel + 4'h1;
         #25;
        end;

        A = 4'h6;
        B = 4'hA;
```

RTL Schematic

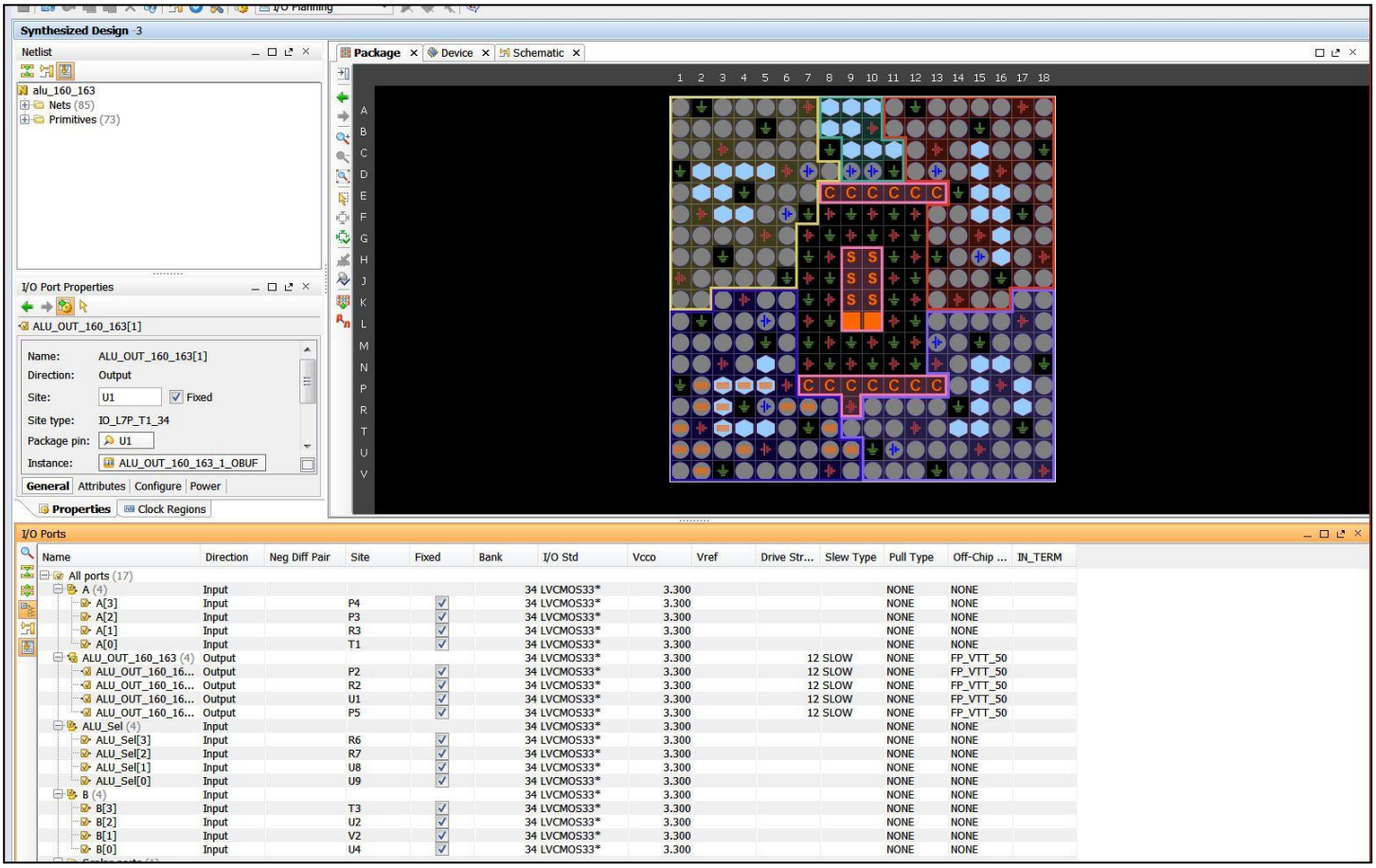



ISE Project Navigator (P.58f) - D:\LAB_A4\LAB_ALU_160_163\ALU_160_163\ALU_160_163.xise - [alu_160_163 (RTL1)]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
ALU_160_163
xc7a100t-3csg324
alu_160_163 (alu_160_163.v)
No Processes Running
Processes: alu_160_163
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Schematic
Check Syntax
Generate Post-Synthesis Si...
Implement Design
Generate Programming File
Configure Target Device
Analyze Design Using ChipSco...
Start Design Files Libraries
alu_160_163.v
Design Summary (Synthesized)
alu_160_163 (RTL1)

Simulation

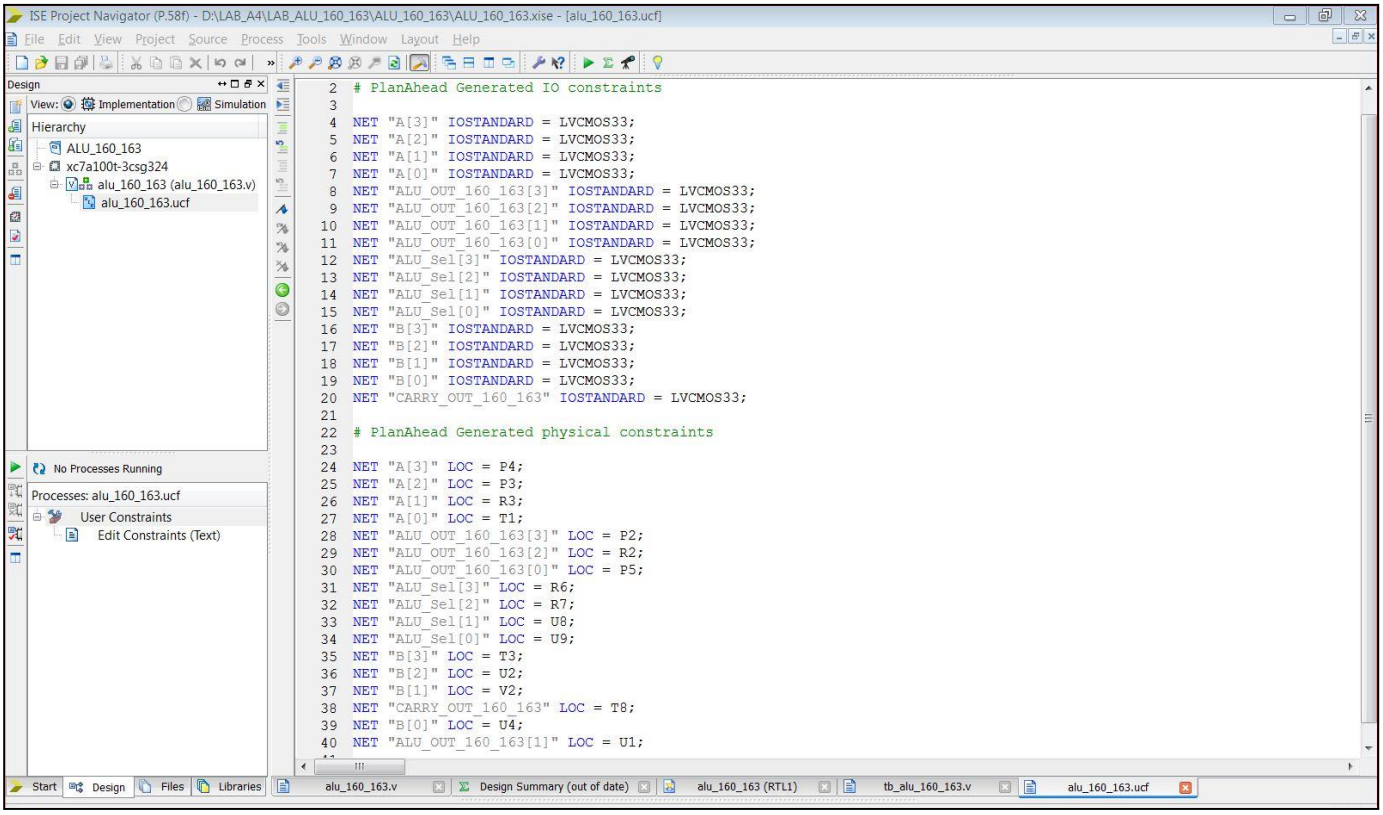

Re-launch
1.00us
Source...
alu_160_163.v
glbl.v
tb_alu_160_163.v
Simulation...
Object Na
Name
Value
A[3:0]
1010
B[3:0]
0010
ALU_Sel[3:0]
0000
ALU_OUT_160_163[3:0]
1100
CARRY_OUT_160_163
0
0.000 ns
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
X1: 0.000 ns
Default.wcfg*
Console
This is a Full version of ISim.
run 1000 ns
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>

IO Floor Plan



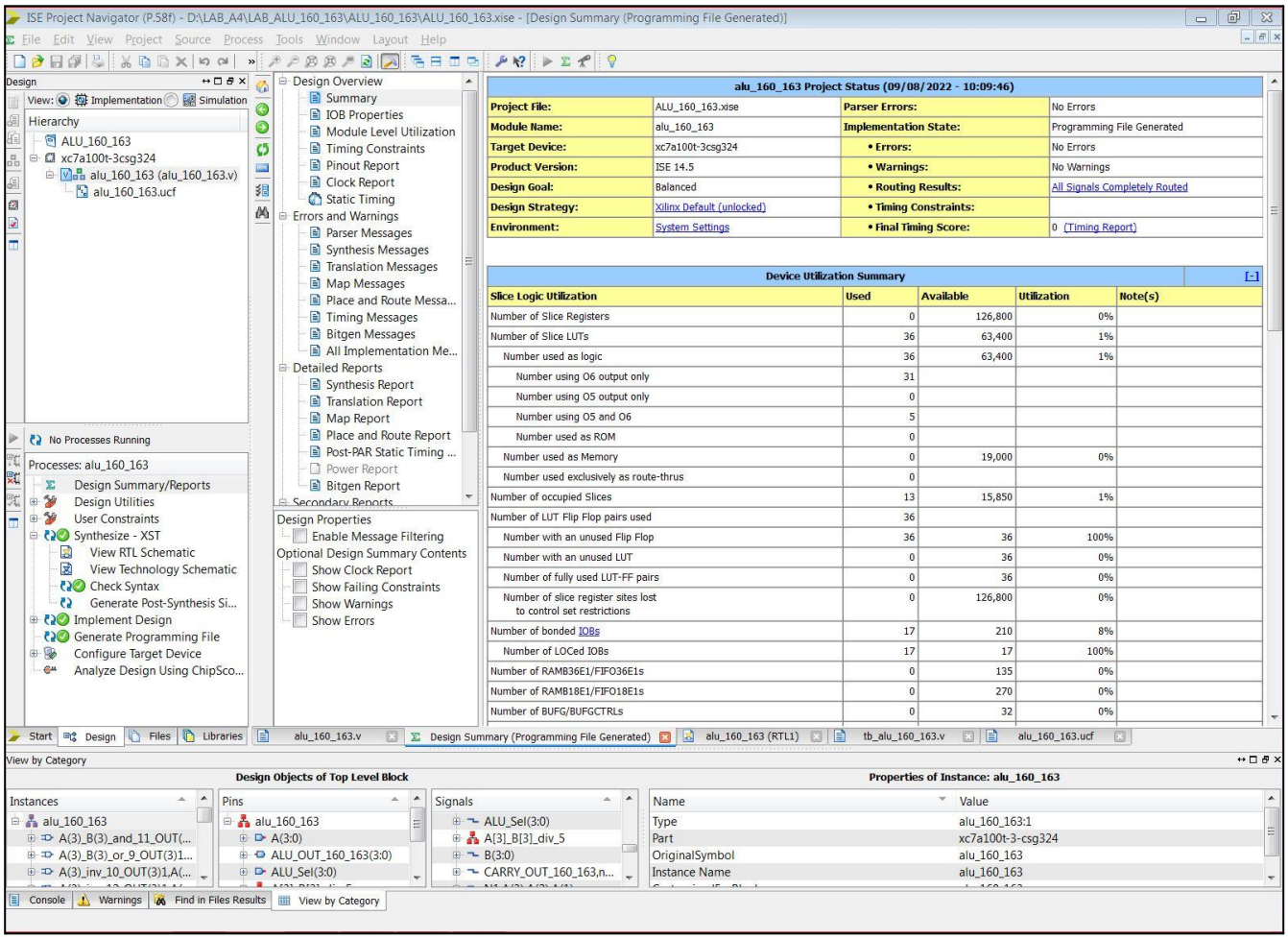
Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Str...	Slew Type	Pull Type	Off-Chip ...	IN_TERM
All ports (17)													
A (4)	Input				34	LVCMOS33*	3.300				NONE	NONE	
A[3]	Input		P4	✓	34	LVCMOS33*	3.300				NONE	NONE	
A[2]	Input		P3	✓	34	LVCMOS33*	3.300				NONE	NONE	
A[1]	Input		R3	✓	34	LVCMOS33*	3.300				NONE	NONE	
A[0]	Input		T1	✓	34	LVCMOS33*	3.300				NONE	NONE	
ALU_OUT_160_163 (4)	Output				34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		P2	✓	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		R2	✓	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		U1	✓	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
ALU_OUT_160_16...	Output		P5	✓	34	LVCMOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
ALU_Sel (4)	Input				34	LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[3]	Input		R6	✓	34	LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[2]	Input		R7	✓	34	LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[1]	Input		U8	✓	34	LVCMOS33*	3.300				NONE	NONE	
ALU_Sel[0]	Input		U9	✓	34	LVCMOS33*	3.300				NONE	NONE	
B (4)	Input				34	LVCMOS33*	3.300				NONE	NONE	
B[3]	Input		T3	✓	34	LVCMOS33*	3.300				NONE	NONE	
B[2]	Input		U2	✓	34	LVCMOS33*	3.300				NONE	NONE	
B[1]	Input		V2	✓	34	LVCMOS33*	3.300				NONE	NONE	
B[0]	Input		U4	✓	34	LVCMOS33*	3.300				NONE	NONE	

UCF File




```
# PlanAhead Generated IO constraints

NET "A[3]" IOSTANDARD = LVCMOS33;
NET "A[2]" IOSTANDARD = LVCMOS33;
NET "A[1]" IOSTANDARD = LVCMOS33;
NET "A[0]" IOSTANDARD = LVCMOS33;
NET "ALU_OUT_160_163[3]" IOSTANDARD = LVCMOS33;
NET "ALU_OUT_160_163[2]" IOSTANDARD = LVCMOS33;
NET "ALU_OUT_160_163[1]" IOSTANDARD = LVCMOS33;
NET "ALU_OUT_160_163[0]" IOSTANDARD = LVCMOS33;
NET "ALU_Sel[3]" IOSTANDARD = LVCMOS33;
NET "ALU_Sel[2]" IOSTANDARD = LVCMOS33;
NET "ALU_Sel[1]" IOSTANDARD = LVCMOS33;
NET "ALU_Sel[0]" IOSTANDARD = LVCMOS33;
NET "B[3]" IOSTANDARD = LVCMOS33;
NET "B[2]" IOSTANDARD = LVCMOS33;
NET "B[1]" IOSTANDARD = LVCMOS33;
NET "B[0]" IOSTANDARD = LVCMOS33;
NET "CARRY_OUT_160_163" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "A[3]" LOC = P4;
NET "A[2]" LOC = P3;
NET "A[1]" LOC = R3;
NET "A[0]" LOC = T1;
NET "ALU_OUT_160_163[3]" LOC = P2;
NET "ALU_OUT_160_163[2]" LOC = R2;
NET "ALU_OUT_160_163[0]" LOC = P5;
NET "ALU_Sel[3]" LOC = R6;
NET "ALU_Sel[2]" LOC = R7;
NET "ALU_Sel[1]" LOC = U8;
NET "ALU_Sel[0]" LOC = U9;
NET "B[3]" LOC = T3;
NET "B[2]" LOC = U2;
NET "B[1]" LOC = V2;
NET "CARRY_OUT_160_163" LOC = T8;
NET "B[0]" LOC = U4;
NET "ALU_OUT_160_163[1]" LOC = U1;
```

Design Summary



Program successfully uploaded