

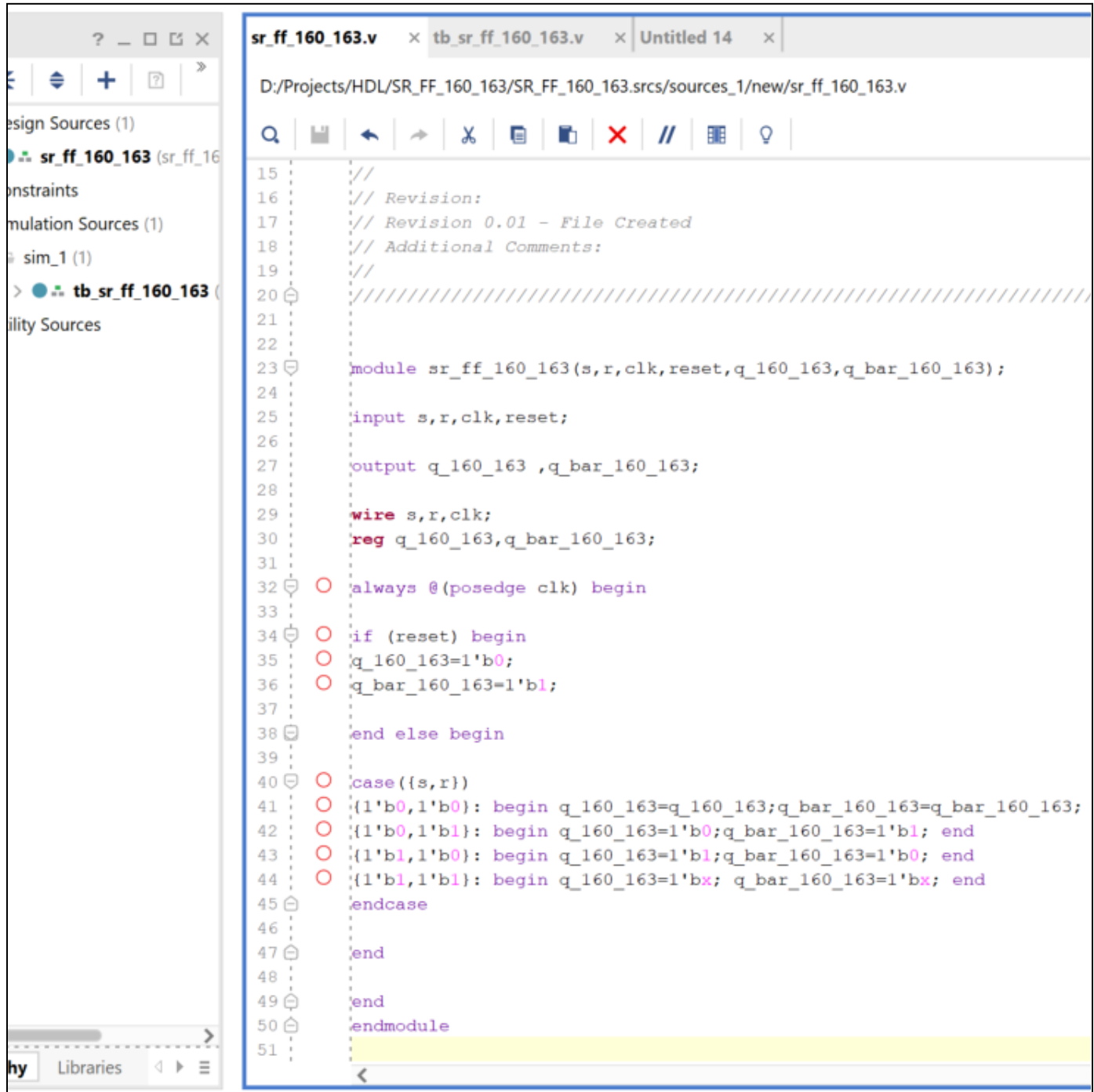
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Roll No - 160

PRN - 0120190250

LAB: SR Flipflop

1. HDL Code



```
15 //  
16 // Revision:  
17 // Revision 0.01 - File Created  
18 // Additional Comments:  
19 //  
20 ///////////////////////////////////////  
21  
22  
23 module sr_ff_160_163(s,r,clk,reset,q_160_163,q_bar_160_163);  
24  
25 input s,r,clk,reset;  
26  
27 output q_160_163 ,q_bar_160_163;  
28  
29 wire s,r,clk;  
30 reg q_160_163,q_bar_160_163;  
31  
32 always @(posedge clk) begin  
33  
34 if (reset) begin  
35 q_160_163=1'b0;  
36 q_bar_160_163=1'b1;  
37  
38 end else begin  
39  
40 case({s,r})  
41 {1'b0,1'b0}: begin q_160_163=q_160_163;q_bar_160_163=q_bar_160_163;  
42 {1'b0,1'b1}: begin q_160_163=1'b0;q_bar_160_163=1'b1; end  
43 {1'b1,1'b0}: begin q_160_163=1'b1;q_bar_160_163=1'b0; end  
44 {1'b1,1'b1}: begin q_160_163=1'bx; q_bar_160_163=1'bx; end  
45 endcase  
46  
47 end  
48  
49 end  
50 endmodule  
51
```

Text Bench Code

Sources

Design Sources (1)

sr_ff_160_163 (sr_ff_163)

Constraints

Simulation Sources (1)

sim_1 (1)

tb_sr_ff_160_163 (tb_sr_ff_163)

Utility Sources

sr_ff_160_163.v

tb_sr_ff_160_163.v

Untitled 14

D:/Projects/HDL/SR_FF_160_163/SR_FF_160_163.srsrcs/sim_1/new/tb_sr_ff_160_163.v

19

//

20

////////////////////////////////////

21

22

module tb_sr_ff_160_163;

23

24

reg clk;

25

reg reset;

26

reg s,r;

27

28

wire q_160_163;

29

wire qb_160_163;

30

31

sr_ff_160_163 uut (.clk(clk), .reset(reset), .s(s), .r(r), .q_160_163(q_160_163

32

33

initial begin

34

35

o s = 1'b0;

36

o r = 1'b0;

37

o reset = 1;

38

o clk=1;

39

40

o #10

41

o reset=0;

42

o s=1'b1;

43

o r=1'b0;

44

45

o #100

46

o reset=0;

47

o s=1'b0;

48

o r=1'b1;

49

50

o #100

51

o reset=0;

52

o s=1'b1;

53

o r=1'b1;

54

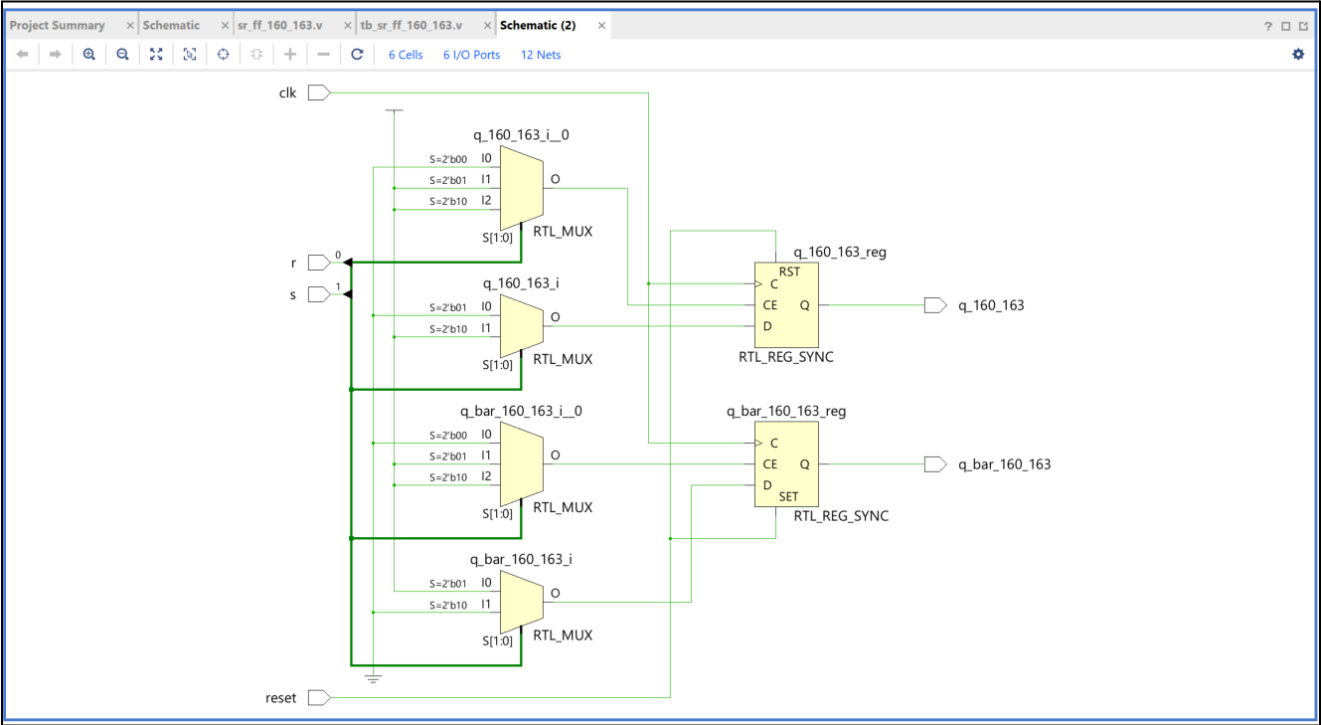
55

o #100

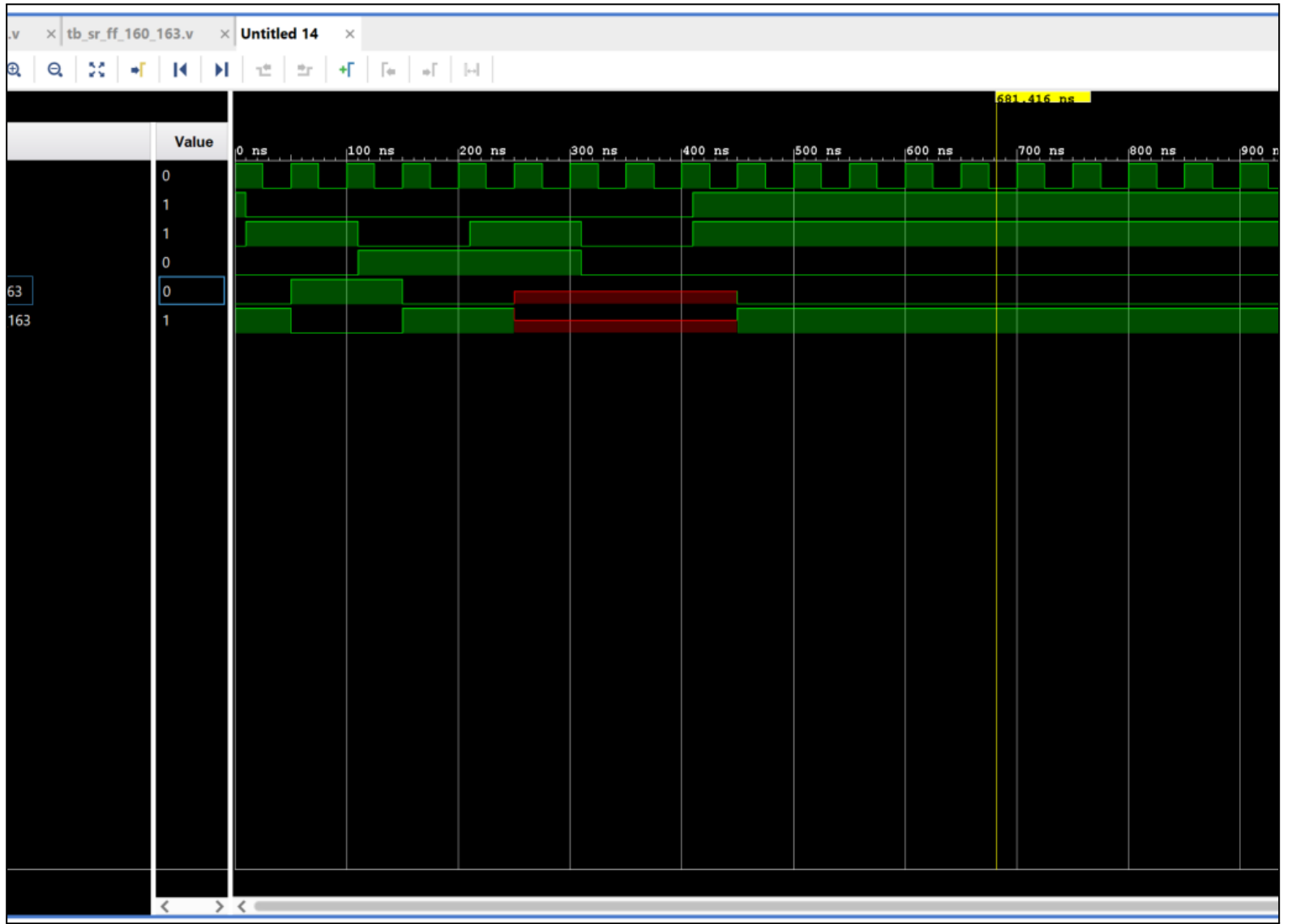
Hierarchy

Libraries

Schematic



Simulation



UCF File

```
Project Summary | Schematic | sr_ff_160_163.v | tb_sr_ff_160_163.v | Schematic (2) | ucf.xdc |
D:/Projects/HDL/SR_FF_160_163/SR_FF_160_163.srsrcs/constrs_1/new/ucf.xdc

1 set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
2
3 set_property IOSTANDARD LVCOS33 [get_ports r]
4 set_property IOSTANDARD LVCOS33 [get_ports clk]
5 set_property IOSTANDARD LVCOS33 [get_ports s]
6 set_property IOSTANDARD LVCOS33 [get_ports reset]
7 set_property IOSTANDARD LVCOS33 [get_ports q_160_163]
8 set_property IOSTANDARD LVCOS33 [get_ports q_bar_160_163]
9 set_property PACKAGE_PIN U12 [get_ports r]
10 set_property PACKAGE_PIN U11 [get_ports s]
11 set_property PACKAGE_PIN V10 [get_ports clk]
12 set_property PACKAGE_PIN J15 [get_ports reset]
13 set_property PACKAGE_PIN V11 [get_ports q_160_163]
14 set_property PACKAGE_PIN V12 [get_ports q_bar_160_163]
15
```

Design Summary

Project Summary

Schematic

sr_ff_160_163.v

tb_sr_ff_160_163.v

Schematic (2)

ucf.xdc

Overview | Dashboard

Settings

Edit

Project name:

SR_FF_160_163

Project location:

D:/Projects/HDL/SR_FF_160_163

Product family:

Artix-7

Project part:

xc7a100tcsq324-1

Top module name:

sr_ff_160_163

Target language:

Verilog

Simulator language:

Mixed

Synthesis

Status:

Complete

Messages:

1 critical warning

2 warnings

Part:

xc7a100tcsq324-1

Strategy:

Vivado Synthesis Defaults

Report Strategy:

Vivado Synthesis Default Reports

Implementation

Status:

Complete

Messages:

6 warnings

Part:

xc7a100tcsq324-1

Strategy:

Vivado Implementation Defaults

Report Strategy:

Vivado Implementation Default Reports

Incremental implementation:

None

DRC Violations

Summary:

2 warnings

Implemented DRC Report

Timing

Worst Negative Slack (WNS):

NA

Total Negative Slack (TNS):

NA

Number of Failing Endpoints:

NA

Total Number of Endpoints:

NA

Implemented Timing Report

Power

Total On-Chip Power:

1.238 W

Junction Temperature:

30.6 °C

Thermal Margin:

54.4 °C (11.8 W)

Effective θJA:

4.6 °C/W

Power supplied to off-chip devices:

0 W

Confidence level:

Low

Implemented Power Report

Utilization

Post-Synthesis

Post-Implementation

Graph

Table

LUT

1%

FF

1%

IO

3%

BUFG

3%

Utilization (%)

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

Open Implemented Design

View Reports

Open Hardware Manager

Generate Memory Configuration File

Don't show this dialog again

OK

Cancel