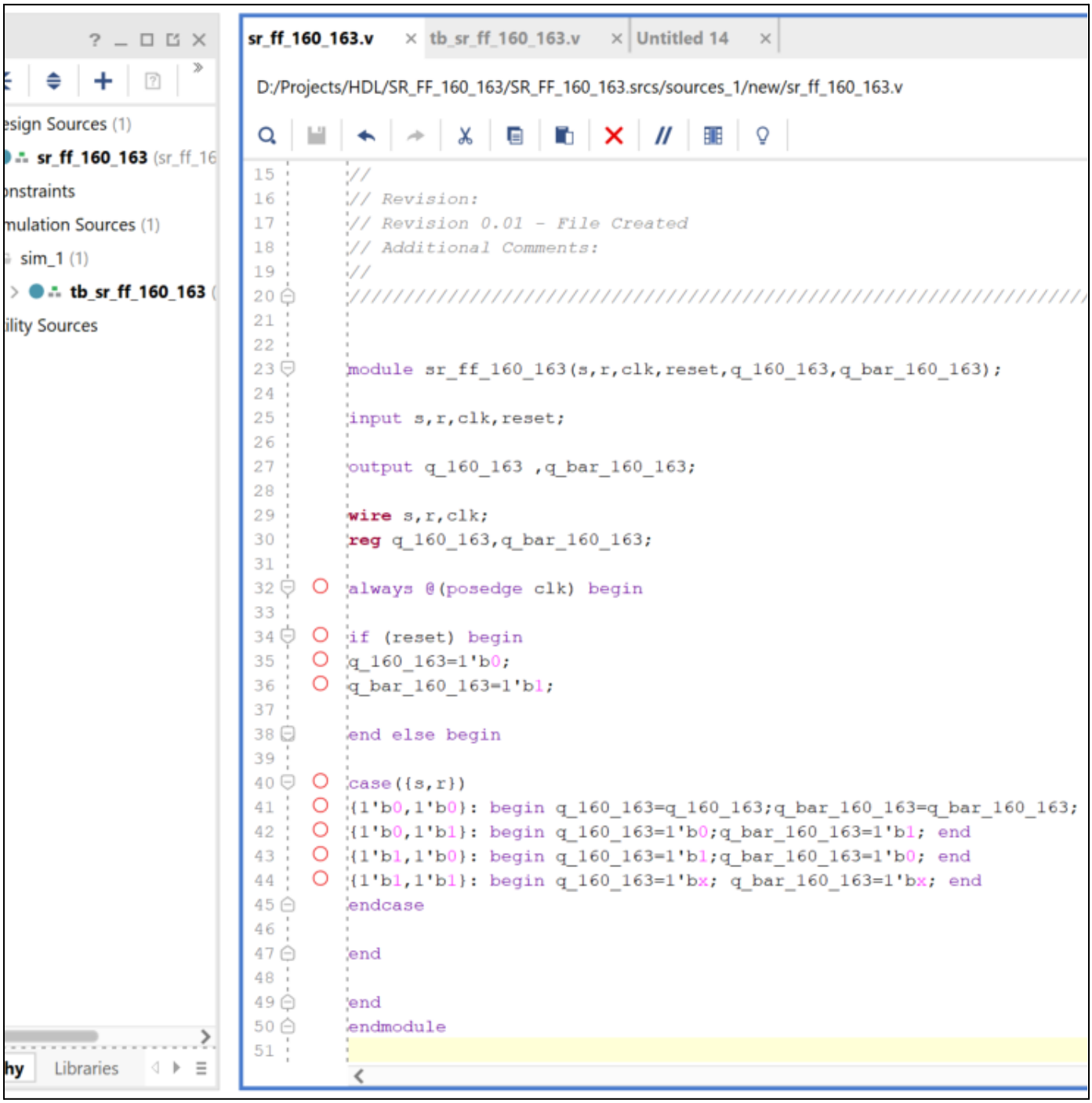
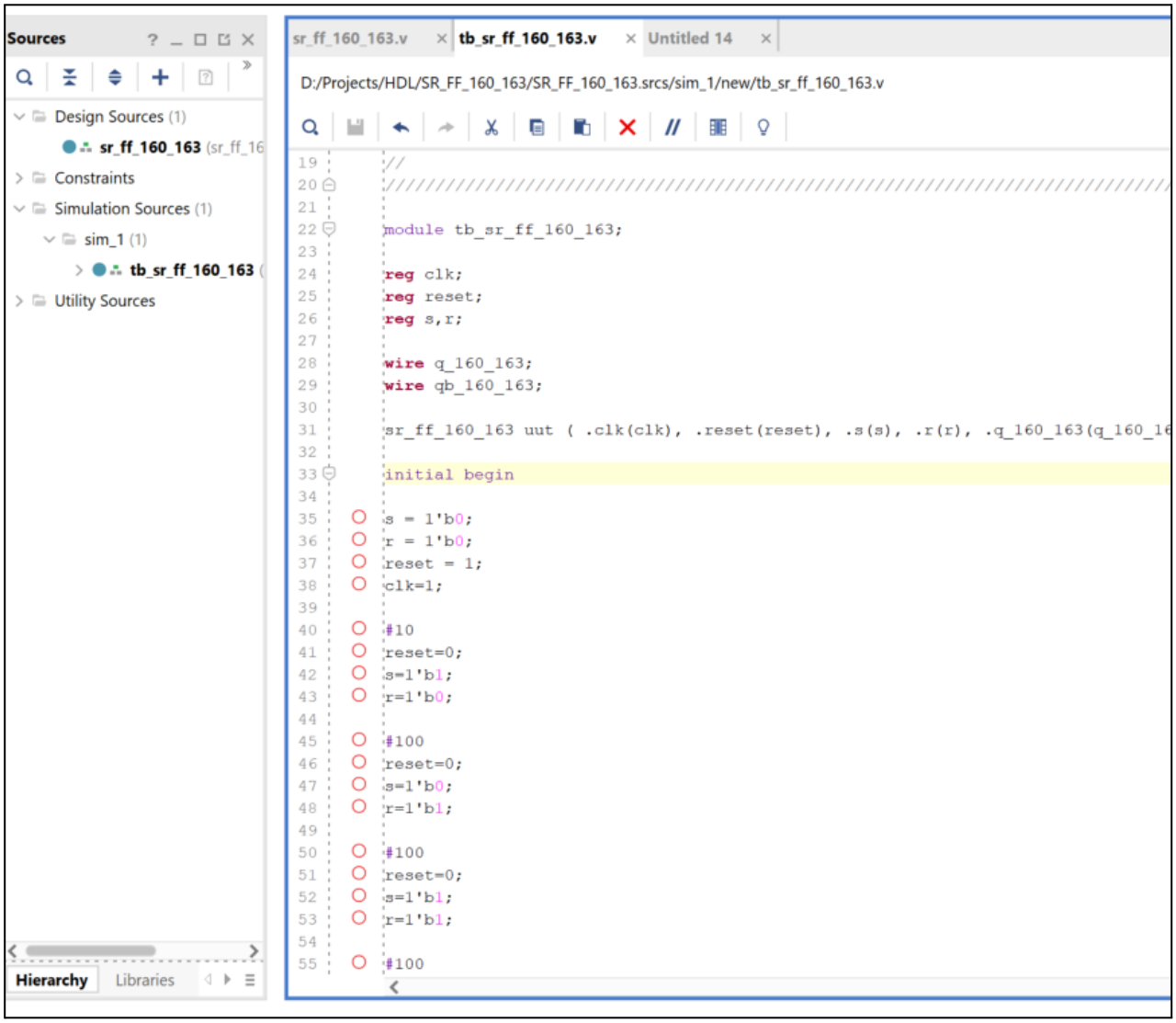
Name - Pranav Unkule
Roll No - 160
PRN - 0120190250

LAB: SR Flipflop

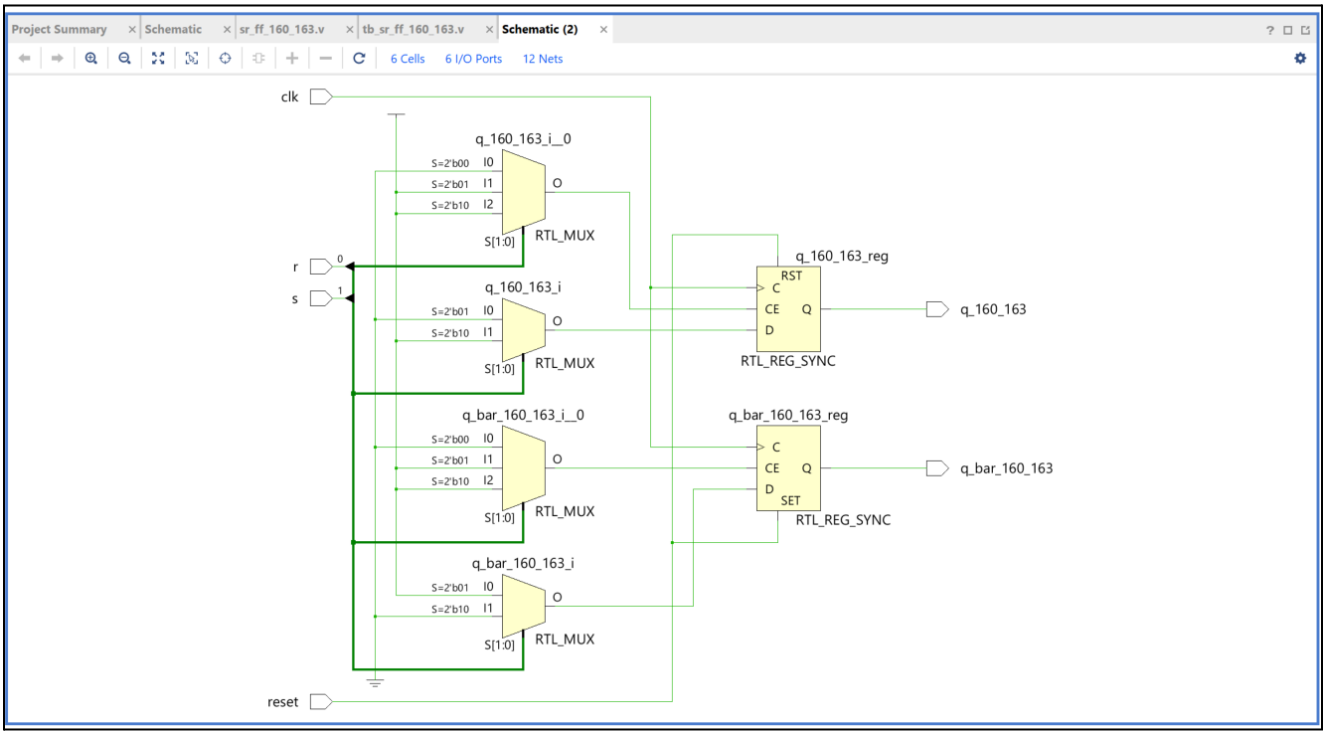
1. HDL Code



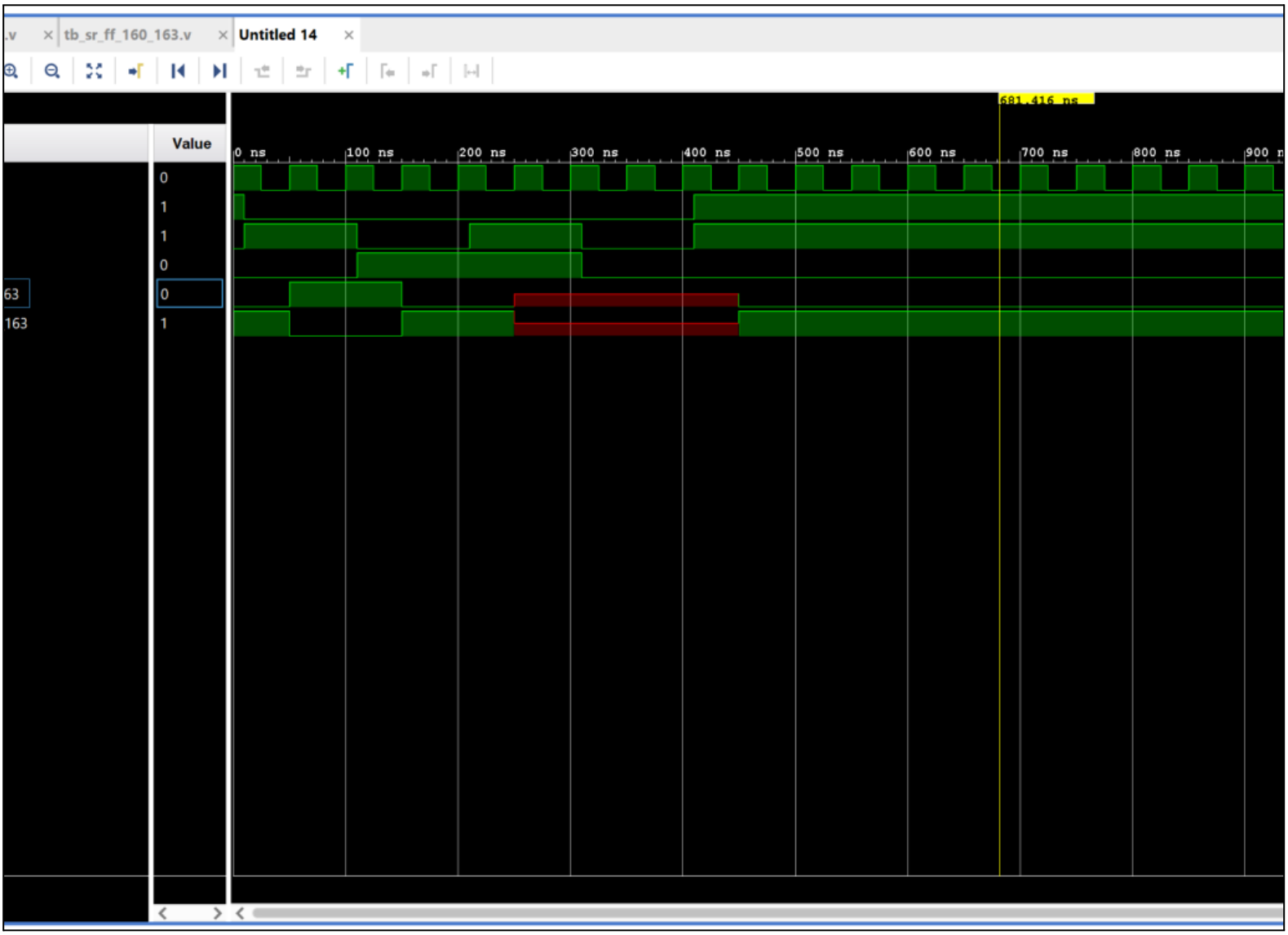
Text Bench Code



Schematic



Simulation



UCF File

Project Summary | Schematic | sr_ff_160_163.v | tb_sr_ff_160_163.v | Schematic (2) | ucf.xdc

D:/Projects/HDL/SR_FF_160_163/SR_FF_160_163.srcs/constrs_1/new/ucf.xdc

```
1  set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets clk_IBUF]
2
3  set_property IOSTANDARD LVCMOS33 [get_ports r]
4  set_property IOSTANDARD LVCMOS33 [get_ports clk]
5  set_property IOSTANDARD LVCMOS33 [get_ports s]
6  set_property IOSTANDARD LVCMOS33 [get_ports reset]
7  set_property IOSTANDARD LVCMOS33 [get_ports q_160_163]
8  set_property IOSTANDARD LVCMOS33 [get_ports q_bar_160_163]
9  set_property PACKAGE_PIN U12 [get_ports r]
10 set_property PACKAGE_PIN U11 [get_ports s]
11 set_property PACKAGE_PIN V10 [get_ports clk]
12 set_property PACKAGE_PIN J15 [get_ports reset]
13 set_property PACKAGE_PIN V11 [get_ports q_160_163]
14 set_property PACKAGE_PIN V12 [get_ports q_bar_160_163]
15
```

Design Summary