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LAB: D Flipflop

1. HDL Code

The screenshot displays the Xilinx ISE IDE interface. The top menu bar includes File, Edit, View, Project, Source, Process, Tools, Window, Layout, and Help. The left-hand pane shows the Project Navigator with the following structure:

- ch1
- D_FF_160_163
- xc7a100t-3csg324
- d_ff_160_163 (d_ff_160_163.v)

Below the Project Navigator is the 'Processes Running' section, which lists the following tasks for 'ses: d_ff_160_163':

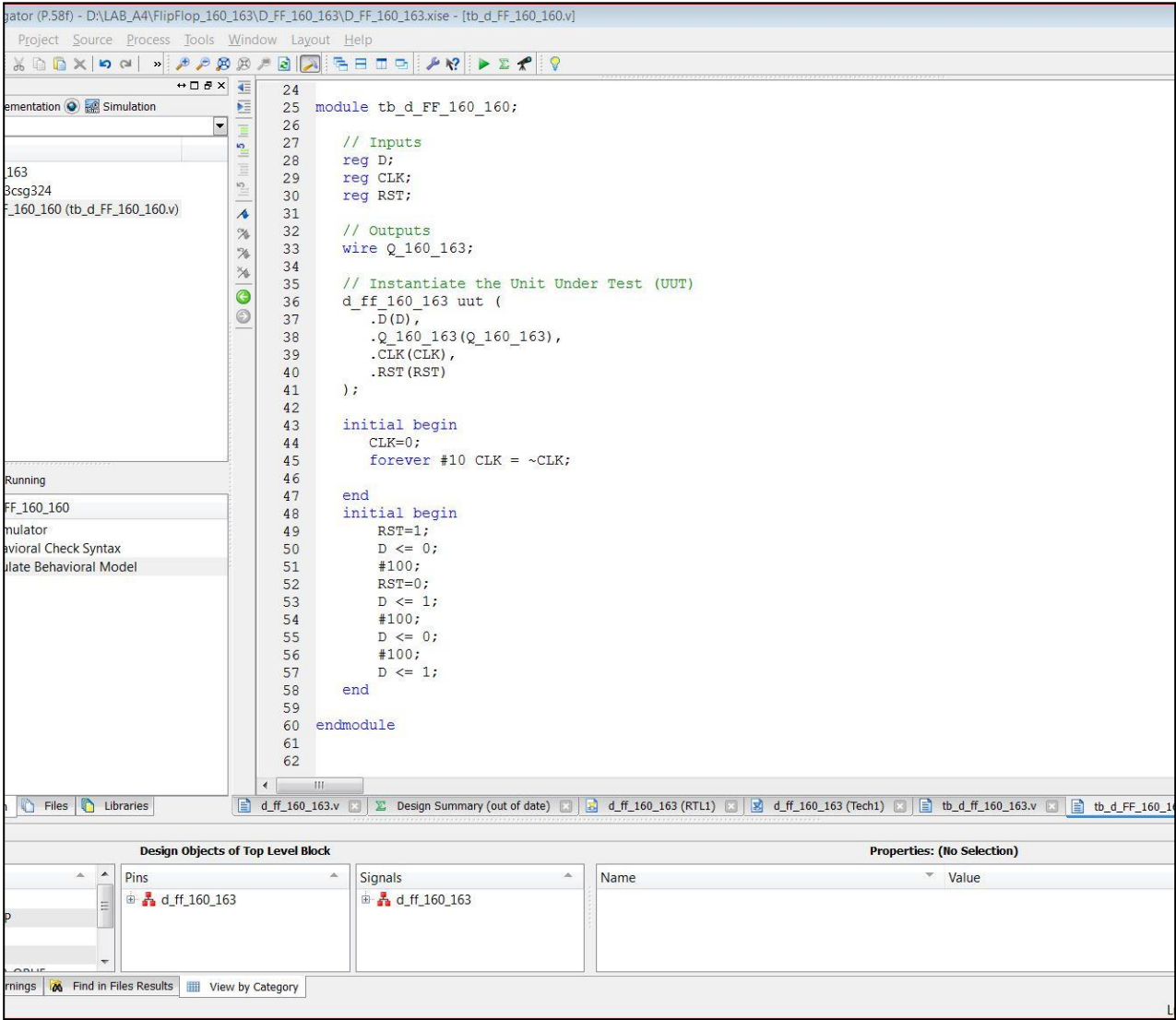
- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- View RTL Schematic
- View Technology Schematic
- Check Syntax
- Generate Post-Synthesis Simulation Model
- Implement Design
- Generate Programming File
- Configure Target Device
- Analyze Design Using ChipScope

The main editor window displays the HDL code for the D Flipflop:

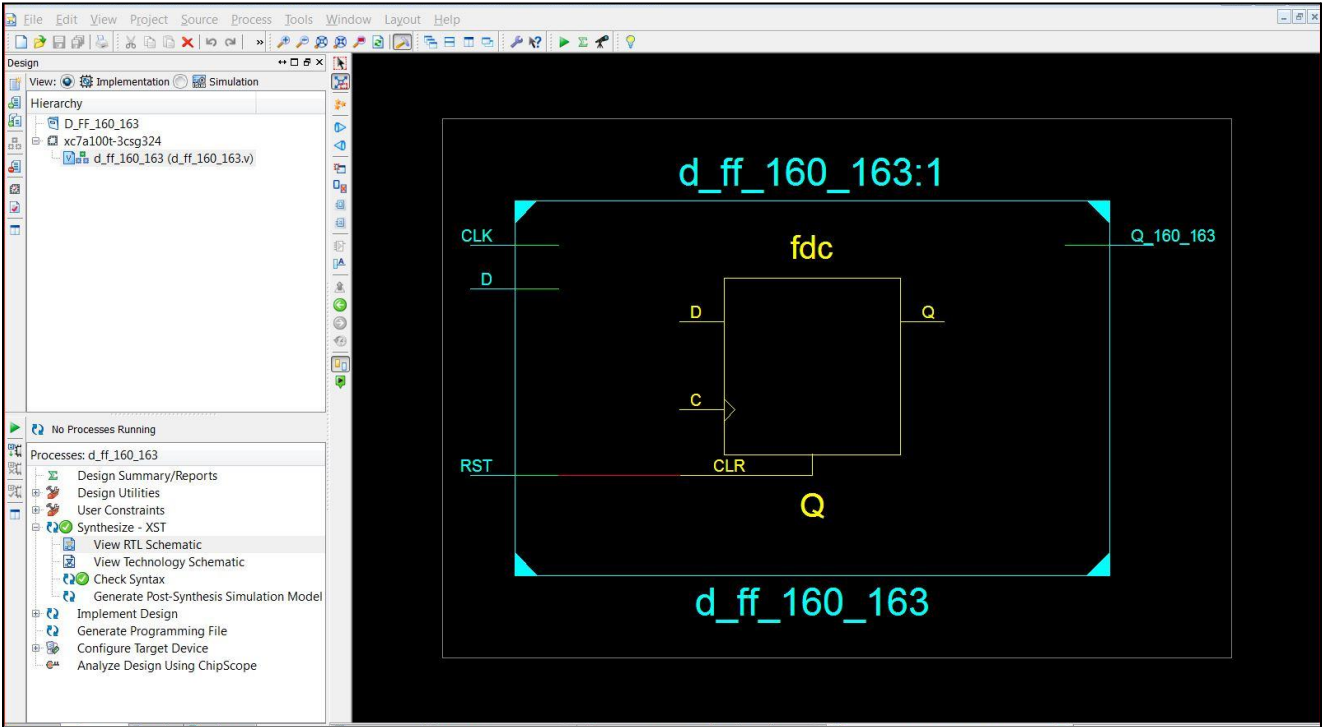
```
3 // Company:
4 // Engineer:
5 //
6 // Create Date:    08:56:37 09/29/2022
7 // Design Name:
8 // Module Name:    d_ff_160_163
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 ///////////////////////////////////////////////////////////////////
21
22 // Pranav Unkule 160, Ruturaj Javeri 163
23
24 module d_ff_160_163(
25     input D,
26     output Q_160_163,
27     input CLK,
28     input RST
29 );
30
31 reg Q; // output Q
32 always @(posedge CLK or posedge RST)
33 begin
34     if(RST==1'b1)
35         Q <= 1'b0;
36     else
37         Q <= D;
38     end
39 assign Q_160_163 = Q;
40 endmodule
41
```

The bottom of the IDE shows the 'Design Objects of Top Level Block' section, which is currently empty. The status bar at the bottom indicates 'Warnings', 'Find in Files Results', and 'View by Category'.

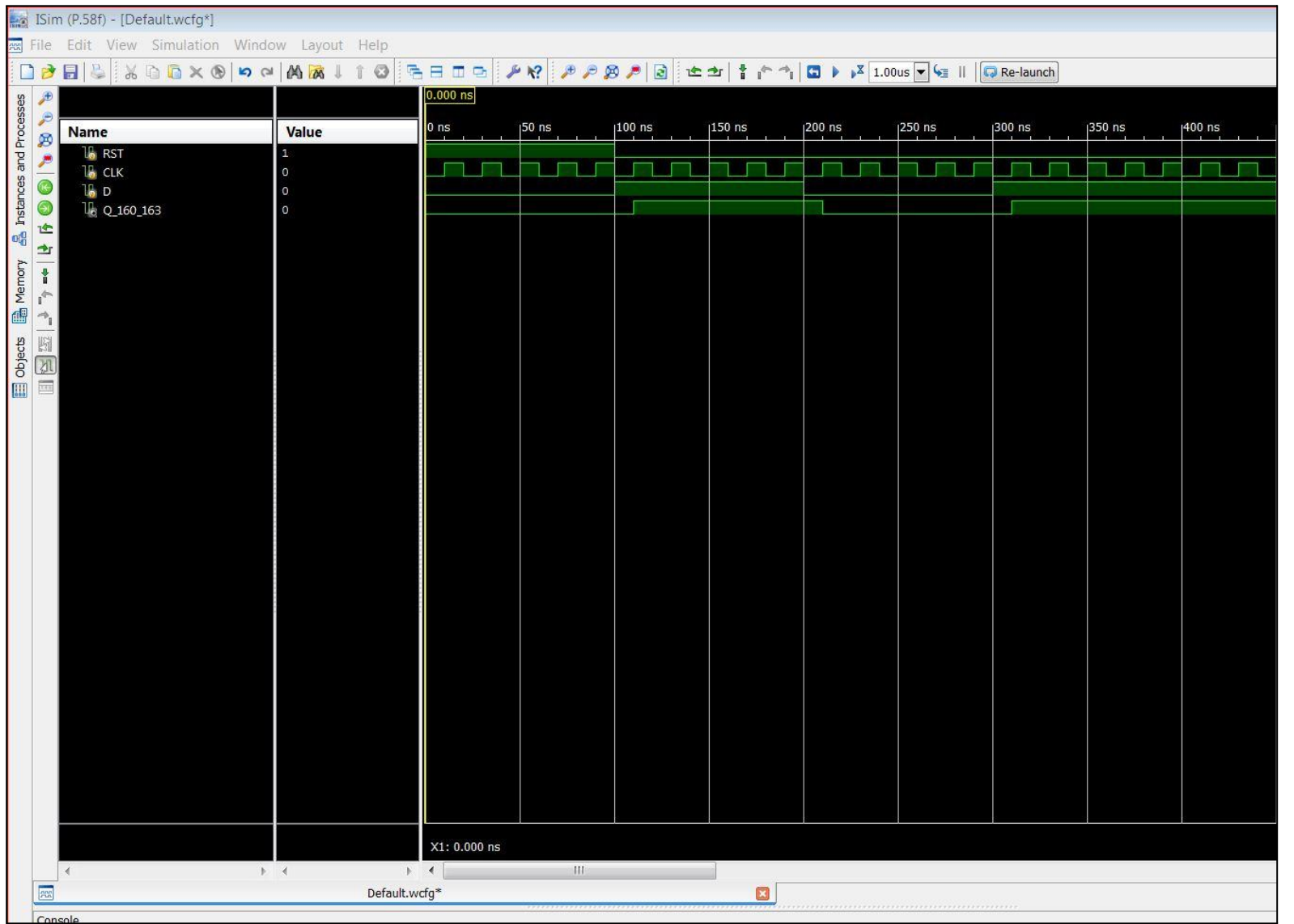
Text Bench Code



Schematic



Simulation



UCF File

ISE Project Navigator (P.58f) - D:\LAB_A4\Flop_160_163\D_FF_160_163\D_FF_160_163.xise - [d_ff_160_163.ucf]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- D_FF_160_163
 - xc7a100t-3csg324
 - d_ff_160_163 (d_ff_160_163.v)
 - d_ff_160_163.ucf

```
1
2 NET "CLK" CLOCK_DEDICATED_ROUTE = FALSE; |
3
4 # PlanAhead Generated physical constraints
5
6 NET "CLK" LOC = U9;
7 NET "D" LOC = P4;
8 NET "Q_160_163" LOC = P2;
9 NET "RST" LOC = U8;
10
11 # PlanAhead Generated IO constraints
12
13 NET "CLK" IOSTANDARD = LVCMOS33;
14 NET "D" IOSTANDARD = LVCMOS33;
15 NET "Q_160_163" IOSTANDARD = LVCMOS33;
16 NET "RST" IOSTANDARD = LVCMOS33;
17
```

IO Planning

Synthesized Design 3

Netlist

d_ff_160_163

Nets (9)

Primitives (6)

I/O Port Properties

RST

Name: RST

Direction: Input

Site: U9 ☒ Fixed

Site type: IO_L21P_T3_DQS_34

Package pin: U9

Instance: RST_IBUF

Net: RST

Bank: I/O Bank: 34 (High Range)

Tile: RIOB33_X57Y57

Clock region: X1Y1

General Attributes Configure Power

Properties Clock Regions

Package Device Schematic

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

T

U

V

I/O Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Str...	Slew Type	Pull Type	Off-Chip ...	IN_TERM
All ports (4)													
Scalar ports (4)													
CLK	Input		P3	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300				NONE	NONE	
D	Input		P4	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300				NONE	NONE	
Q_160_163	Output		P2	<input checked="" type="checkbox"/>		34 LVCMOS33*	3.300		12 SLOW		NONE	FP_VTT_50	
RST	Input		U9	<input checked="" type="checkbox"/>		34 LVCMOS33	1.800				NONE	NONE	

Design Summary

ISE Project Navigator (P.58f) - D:\LAB_A4\Flop_160_163\D_FF_160_163\D_FF_160_163.xise - [Design Summary (Programming File Generated)]

File Edit View Project Source Process Tools Window Layout Help

Design

View Implementation Simulation

Hierarchy

D_FF_160_163

xc7a100t-3csg324

d_ff_160_163 (d_ff_160_163)

d_ff_160_163.ucf

No Processes Running

Processes: d_ff_160_163

Design Summary/Reports

Design Utilities

User Constraints

Create Timing Constr...

I/O Pin Planning (Pla...

I/O Pin Planning (Pla...

Floorplan Area/IO/Lo...

Synthesize - XST

View RTL Schematic

View Technology Sch...

Check Syntax

Generate Post-Synthe...

Implement Design

Generate Programming ...

Configure Target Device

Analyze Design Using C...

Design Overview

Summary

IOB Properties

Module Level Utilization

Timing Constraints

Pinout Report

Clock Report

Static Timing

Errors and Warnings

Parser Messages

Synthesis Messages

Translation Messages

Map Messages

Place and Route Messa...

Timing Messages

Bitgen Messages

All Implementation Me...

Detailed Reports

Synthesis Report

Translation Report

Map Report

Place and Route Report

Post-PAR Static Timing ...

Power Report

Bitgen Report

Secondary Reports

ISIM Simulator Log

Design Properties

Enable Message Filtering

Optional Design Summary Contents

Show Clock Report

Show Failing Constraints

Show Warnings

Show Errors

d_ff_160_163 Project Status (09/29/2022 - 09:44:03)

Project File:	D_FF_160_163.xise	Parser Errors:	No Errors
Module Name:	d_ff_160_163	Implementation State:	Programming File Generated
Target Device:	xc7a100t-3csg324	Errors:	No Errors
Product Version:	ISE 14.5	Warnings:	1 Warning (1 new)
Design Goal:	Balanced	Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	All Constraints Met
Environment:	System Settings	Final Timing Score:	0 (Timing Report)

Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	0	126,800	0%	
Number of Slice LUTs	0	63,400	0%	
Number of occupied Slices	0	15,850	0%	
Number of LUT Flip Flop pairs used	0			
Number of bonded IOBs	4	210	1%	
Number of LOCed IOBs	4	4	100%	
IOB Flip Flops	1			
Number of RAMB36E1/FIFO36E1s	0	135	0%	
Number of RAMB18E1/FIFO18E1s	0	270	0%	
Number of BUFG/BUFFCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFFCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYS	0	300	0%	
Number of ILOGICE2/ILOGICE3/USERDESE2s	0	300	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYS	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	1	300	1%	
Number used as OLOGICE2s	1			
Number used as OLOGICE3s	0			
Number used as OSERDESE2s	0			
Number of PHASER_IN/PHASER_IN_PHYs	0	24	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	24	0%	
Number of BSCANS	0	4	0%	
Number of BUFHCEs	0	96	0%	

Start Design Files Lib

d_ff_160_163.ucf

Design Summary (Programming File Generated)

Console

Process "Generate Programming File" completed successfully

Console Warnings Find in Files Results

Program Succeeded

ISE (IMPACT (P.58f)) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

IMPACT Flows

Boundary Scan

SystemACE

Create PROM File (PROM File...

WebTalk Data

IMPACT Processes

Available Operations are:

Program

Get Device ID

Get Device Signature/Usercode

Read Device Status

One Step SVF

One Step XSUF

2000000

...

TDI

xc7a100t

d_ff_160_163 bit

TDO

Program Succeeded