Institute of Infrastructure, Technology, Research And Management

(An Autonomous University Established by Government of Gujarat)

End-semester Examination: Computer Organization and Architecture (CS 242003)

Marks: 100 Time: 3 hours

The paper contains two sections (A and B). Attempt any four (4) questions from each section. In Section A, each question carries a weightage of 10 marks, whereas in Section B, each question is allotted 15 marks. Make the suitable assumptions wherever necessary and state them clearly.

(Section A)

1. (a) Explain cache updation policies. Briefly describe cache coherence.

   (b) A system contains a cache memory which is 5 times faster than main memory. The hit ratio of cache is 0.8. The average memory access time is 60ns. If the average memory access time is increased by 20% then what will be % change in hit ratio. Assume that the system can access one type of memory (cache or main) at a time. **[5+5]**

2. (a) How does the data transfer take place in *programmed I/O*. Describe all steps using the diagram.

   (b) Explain software and hardware solutions for handling priority interrupts. **[5+5]**

3. (a) Consider a direct-mapped cache of size 16Kbytes. The size of a cache line is 256 bytes. The size of main memory is 128Kbytes. Find out number of bits required for tag.

   (b) Consider an array $A[100]$ which is stored in main memory. Each array element occupies 4 memory words. The size of cache is 32 words. Each cache line/block contains 8 words. Compute the hit ratio of the cache for running the following statement: **[5+5]**

   $for(i = 0;\ i < 100;\ i++)\{$
   $\quad A[i] = A[i] + 10;\}$

4. (a) Explain following addressing modes with examples. (i) Implied, (ii) Direct, (iii) Indirect, (iv) Relative, (v) Register-indirect addressing mode.

   (b) Solve the expression $Y = (A + B)/(C + D * E)$ using one-address, two-address, and three-address instructions. **[5+5]**

5. (a) Describe the properties of RISC (Reduced Instruction Set Computer) architectures.

   (b) Solve $Y = (A + B) * (C + D)$ using RISC instructions.

   (c) Explain the concept of overlapped register window using one example. **[3 + 3 + 4]**

(Section B)

6. (a) Describe the methods of implementing control unit.

   (b) What are the functions of a microprogram sequencer. Explain the methods of generating next address in the control memory. **[5 + 10]**

7. (a) Why is Input/Output (I/O) interface required in a computer architecture? Explain the functions of I/O interface.

   (b) What are different modes for transferring data between CPU and peripherals? Compare these modes based on important properties.

   (c) Describe the steps of Direct Memory Access (DMA) using its block diagram. **[5+5+5]**

8. (a) Explain pipeline hazards/dependencies using suitable examples.

   (b) We have two designs D1 and D2 for a pipelined processor. The design D1 contains 5 stages with stage processing times (1ns, 1ns, 5ns, 4ns, 2ns). The design D2 consists of 8 stages and each stage takes 2ns. How much time can be saved for D2 over D1 for running 1000 instructions. Assume there is no buffer delays.

   (c) Assume that we have n number of instructions in a program and there is a probability p that an instruction is a conditional instruction (given that there is no unconditional branch instructions). If the instruction is conditional, there is a probability q with which the condition evaluates to be true. Assume that our pipeline is of m stages and only after executing m stages the target instruction address will be found. Compute average clock cycle per instruction (CPI_{avg}). **[5+5+5]**

9. Write short notes on following: (a) general register organization, (b) stack organization, (c) instruction cycle, (d) general purpose registers in 8085, (e) Interrupts **[3*5]**

10. (a) Consider a pipelined processor which contains 4 stages. Compute the speedups achieved by this pipelined processor over a non-pipelined processor in executing 5, 10, 15, 20, 25, and 30 instructions. Draw a graph to show the behavior of the processor in executing different number of instructions. Consider number of instructions on X-axis and speedups achieved on Y-axis.

    (b) How many cycles would be needed to execute the following four instructions (I1; I2; I3; I4) in a pipelined processor containing four stages: S1, S2, S3, and S4? **[8+7]**

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	2	2	2
I3	2	1	1	3
I4	1	2	2	2

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