Digital IC Design

EE5311

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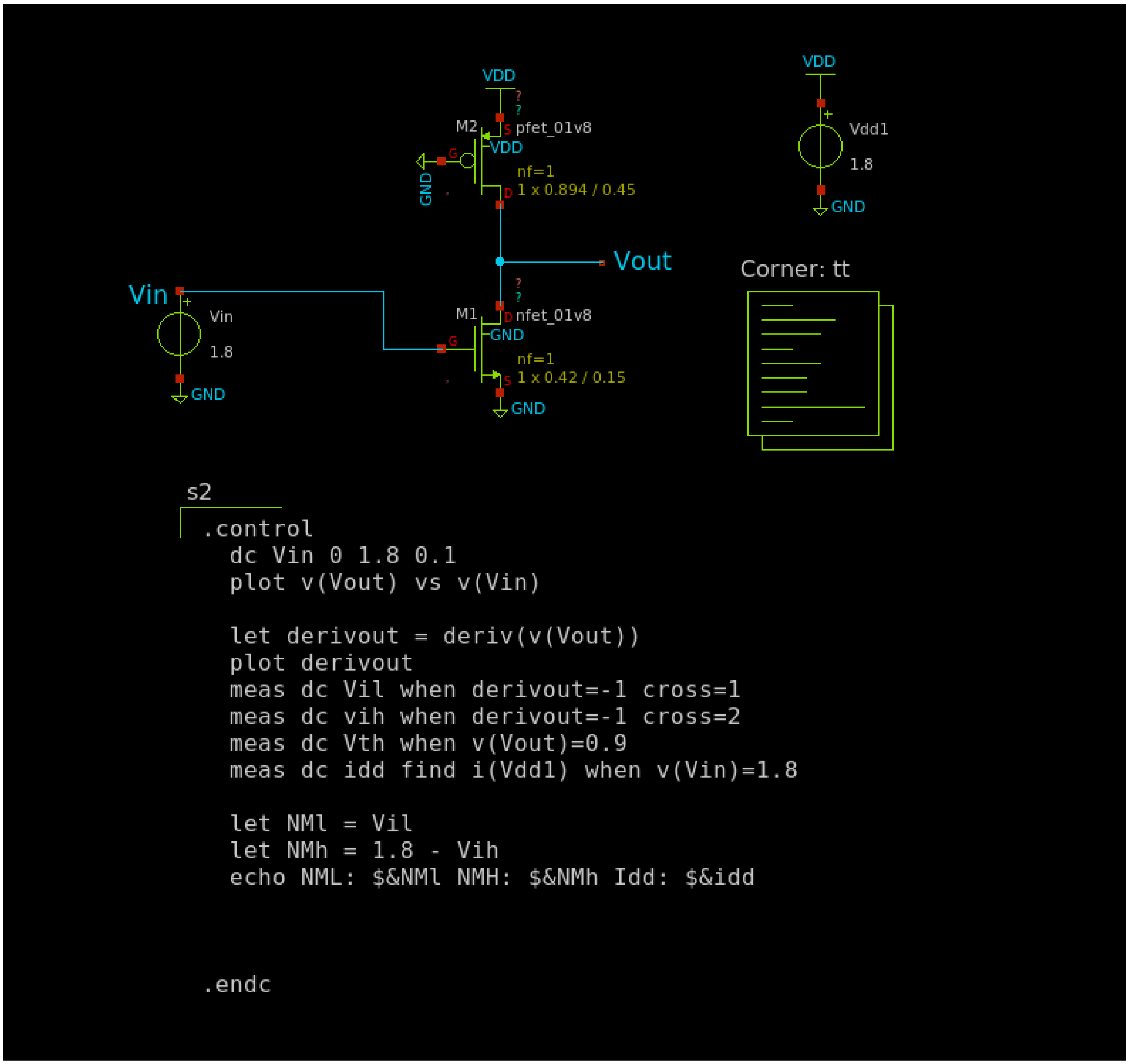
EE22B045

Tutorial - 2

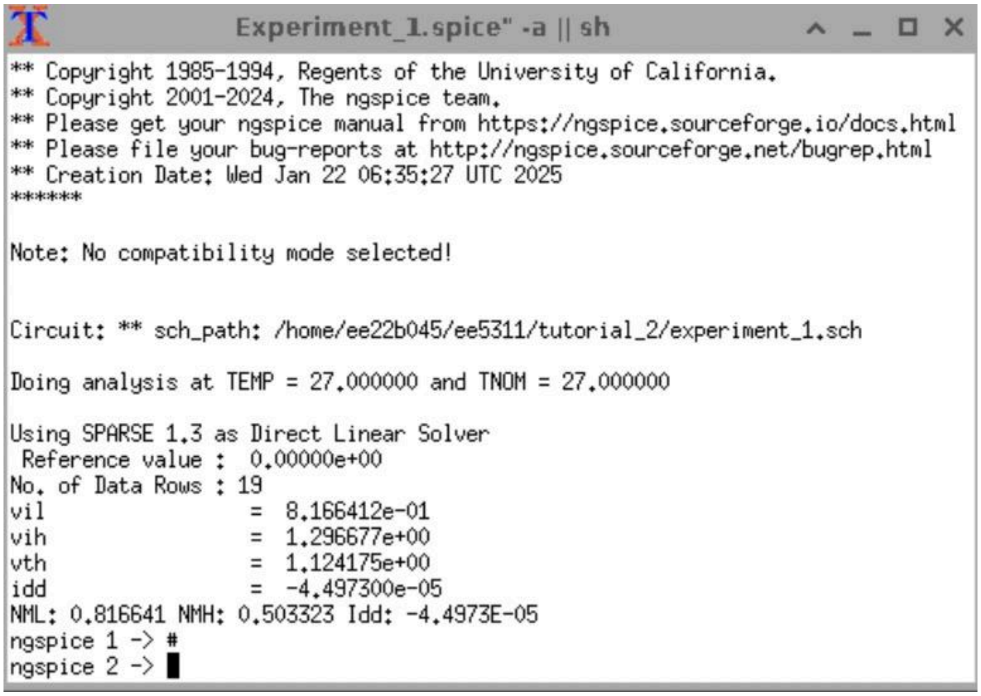
Report

Experiment - 1

Schematic:



NgSpice response:



Experiment_1.spice" -a || sh

```
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2024, The ngspice team.
** Please get your ngspice manual from https://ngspice.sourceforge.io/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Wed Jan 22 06:35:27 UTC 2025
******

Note: No compatibility mode selected!


Circuit: ** sch_path: /home/ee22b045/ee5311/tutorial_2/experiment_1.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 19
vil                 =  8.166412e-01
vih                 =  1.296677e+00
vth                 =  1.124175e+00
idd                 =  -4.497300e-05
NML: 0.816641 NMH: 0.503323 Idd: -4.4973E-05
ngspice 1 -> #
ngspice 2 ->
```

Calculation:

Tutorial-2 DIC:-

(1) ↳ $V_{OL} = 0.1V$; ie when $v_{in} = V_{DD}$

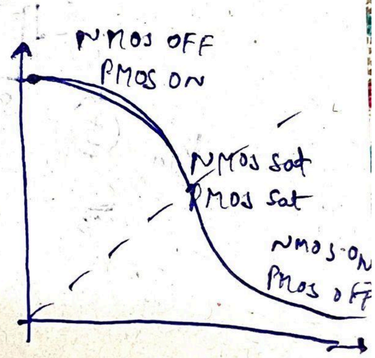
∴ $V_{out} = V_{OL} = 0.1V$

$$\left(W/L\right)_n = \frac{0.42}{0.15}$$

$$I_{DSp} = -I_{DSn}$$

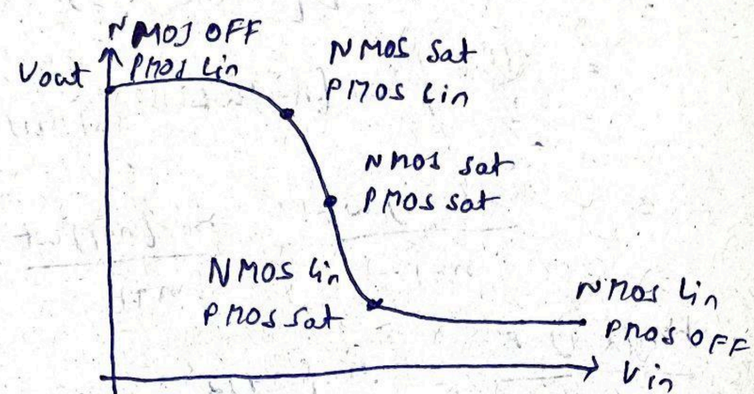
$V_{GSn} = v_{in}$; $V_{GSp} = v_{in} - V_{DD}$

$V_{DSn} = V_{out}$; $V_{DSp} = V_{out} - V_{DD}$



@ V_{OL} region   NMOS is in Linear region
and PMOS is in saturation region

$I_{D,P}$ @

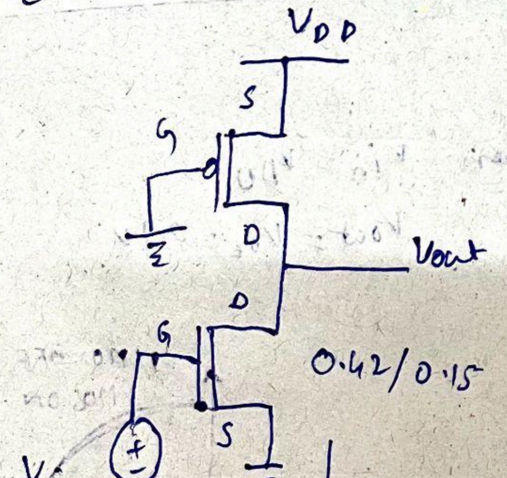


$I_{D,P}$ @ saturation = $I_{D,n}$ @ Linear region.

$$I_{D,P} @ \text{saturation} = \frac{\mu_o C_{ox}}{2} \left(\frac{W}{L}\right)_P \left[(V_{GS_P} - V_{T_P})^2 \right] \left[1 + \lambda_P V_{DS_P} \right]$$

$$I_{D,n} @ \text{Linear} = \frac{\mu_o C_{ox}}{\cancel{2}} \left(\frac{W}{L}\right)_n \left[(V_{GS_n} - V_{T_n}) V_{DS_n} - \frac{V_{DS_n}^2}{2} \right]$$

@ $V_{OL} = 0.1 = V_{out}$



$V_{GS,P} = -1.8V$

$|V_{TP}| = 0.7$

$V_{DS,P} = V_{out} - V_{DD} = 0.1 - 1.8 = -1.7$

$V_{GS,n} = V_{in}$

$V_{Tn} = 0.7$

$V_{DS,n} = V_{out} = 0.1V$

$$I_{D,P} = \frac{(0.009)(0.00816)}{2}\left(\frac{W}{L}\right)_P\left[(-1.8+0.7)^2\right]\left[1+(0.18)(-1.7)\right]$$

$$= (3.672\times10^{-5})\times\left(\frac{W}{L}\right)_P[1.21][0.694]$$

$$\boxed{I_{D,P} = 3.083\times10^{-5}\times\left(\frac{W}{L}\right)_P}$$

$$I_{D,n} = (0.025)(0.00834)\left(\frac{0.42}{0.15}\right)\left[(V_{in}-0.7)0.1-\frac{1}{2}(0.1)^2\right]$$

$$I_{D,n} = (5.838\times10^{-4})\left[0.1V_{in}-0.075\right]$$

if $V_{in} = V_{DD} = 1.8V$; $\boxed{I_{D,n} = 6.1299\times10^{-5}\ A}$

$I_{D,P} = I_{D,n}$

0.45

$\Rightarrow \boxed{\left(\frac{W}{L}\right)_P = 1.988}$ $\Rightarrow W_P = 0.298$ | 0.894

$L_P = 0.15$ | $L = 0.45$

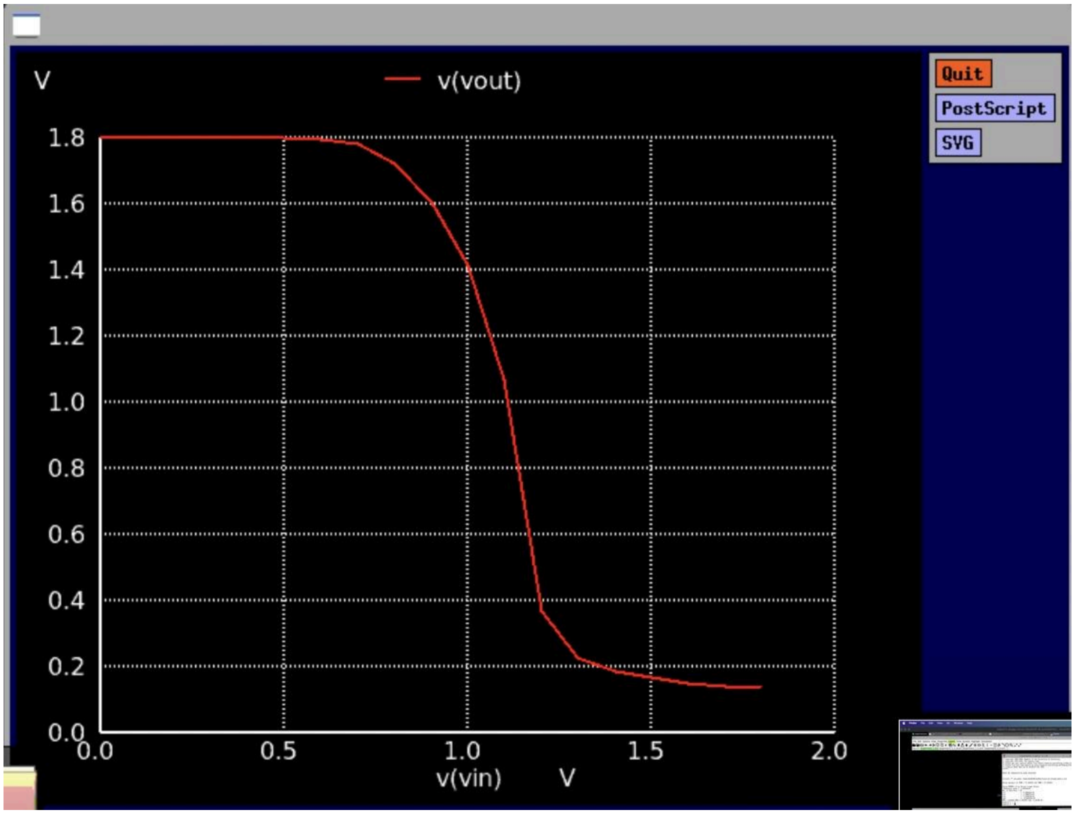
→ inverter threshold voltage from the graph @ 0.9V $= \frac{V_{DD}}{2} = V_{out}$

$\Rightarrow V_{in} = V_{Th} = \boxed{1.12\ V}$

$V_{iL} = 8.166\times10^{-1} = 0.816V$

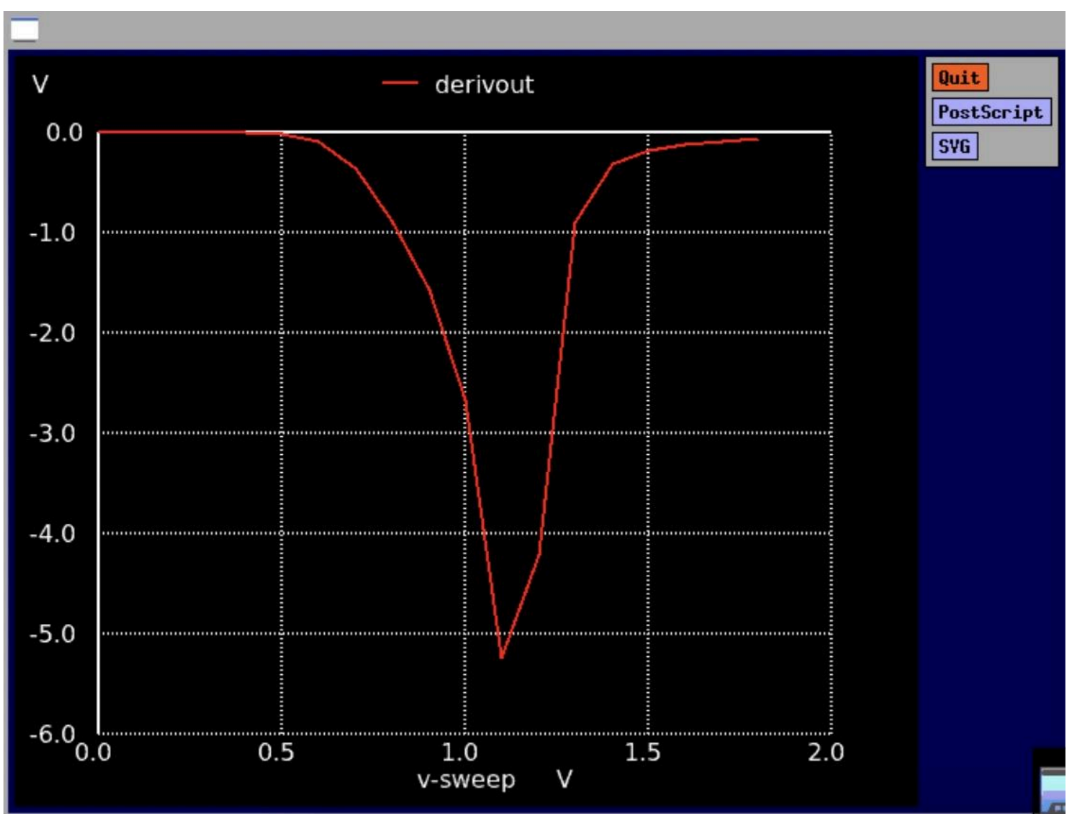
$V_{iH} = 1.296\times10^{0} = 1.296V$

$V_{Th} = 1.12V$



Above figure shows DC characteristics graph for (W/L)p = 1.988

Wp = 0.894 || Lp = 0.45



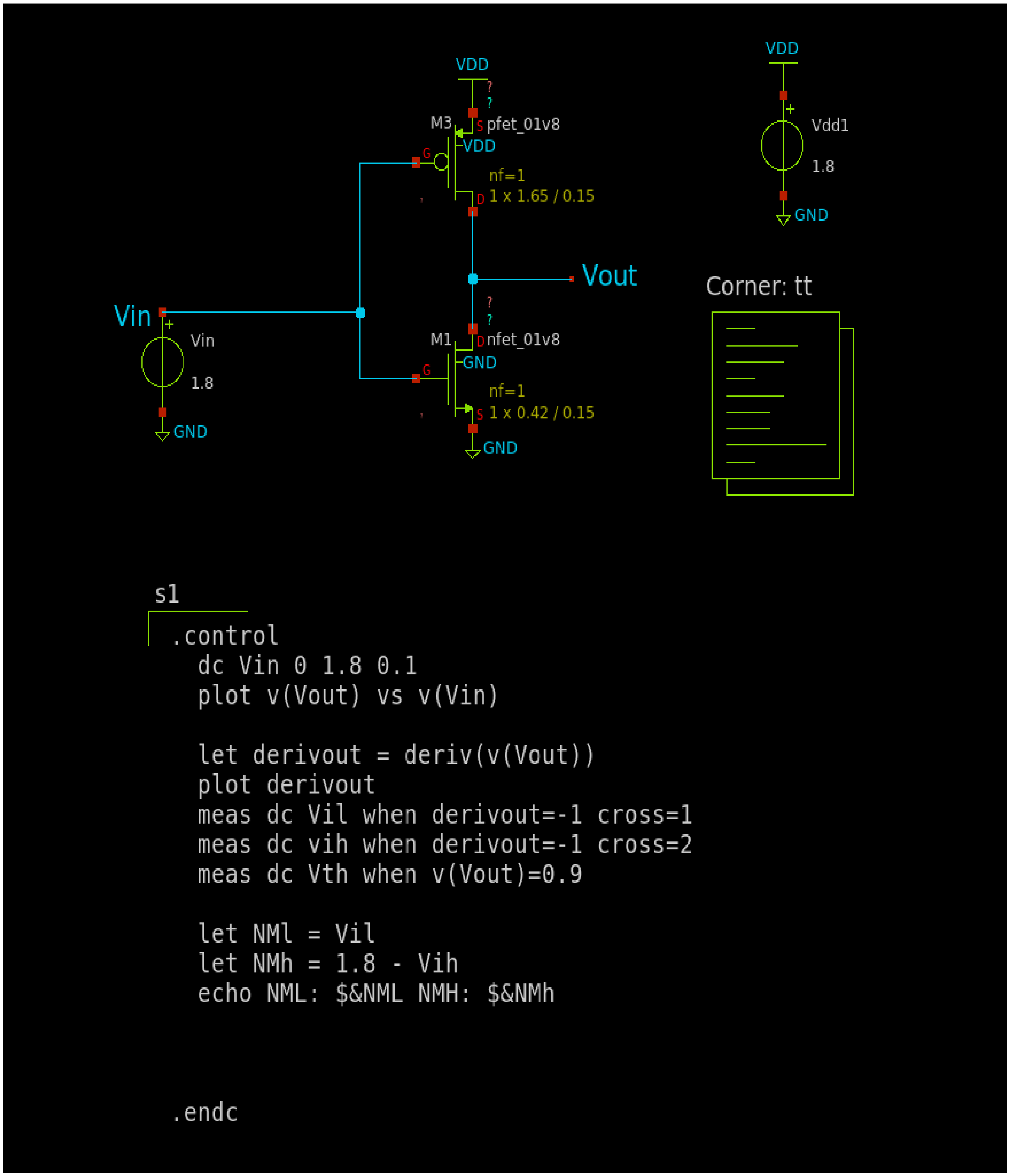
Above Figure shows the Derivative Graph, and The Points hitting "-1" Derivates are noted through the code.

Inverter Threshold Voltage Vth = *1.12V*

Average Power = Idd x Vdd
= 44.976uA x 1.8V = *80uWatt*

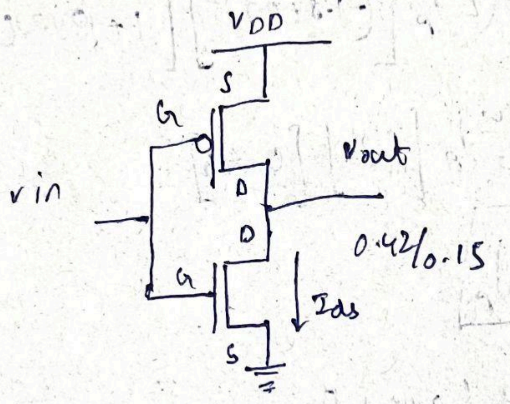
Experiment - 2

Schematic for (A) & (B):



Calculations:

(2)



$V_{GS,p} = V_{in} - V_{DD} = V_{in} - 1.8 = -0.9$

$|V_{Tp}| = 0.7$

$V_{DS,p} = V_{out} - V_{DD} = V_{out} - 1.8 = -0.9$

$V_{GS,n} = V_{in} = 0.9$

$V_{Tn} = 0.7$

$V_{DS,n} = V_{out} = 0.9$

$$I_{D,p} \text{ @ saturation} = \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)_p \left[(V_{GS_p} - V_{Tp})^2\right]\left[1 + \lambda_p V_{DS_p}\right]$$

$$I_{D,n} \text{ @ saturation} = \frac{\mu_0 C_{ox}}{2}\left(\frac{W}{L}\right)_n \left[(V_{GS_n} - V_{Tn})^2\right]\left[1 + \lambda_n V_{DS_n}\right]$$

Condition $V_{inv} = V_{DD}/2$ ie when $V_{\cancel{out}} = \frac{V_{DD}}{2}$

$\cancel{V_{out}}\ V_{Th} = V_{in} = \frac{V_{DD}}{2}$

So; $V_{out} = 0.9 = V_{in}$

$$I_{D,p} = \frac{(0.009)(0.00816)}{2}\left(\frac{W}{L}\right)_p \left[(0.2)^2\right]\left[1 + (0.18)(-0.9)\right]$$

$$\boxed{I_{D,p} = 1.23 \times 10^{-6} A \left(\frac{W}{L}\right)_p}$$

$$I_{D,n} = \frac{(0.025)(0.00834)}{2}\left(\frac{0.42}{0.15}\right)\left[(0.2)^2\right]\left[1 + (0.18)(0.9)\right]$$

$$\boxed{I_{D,n} = 1.356 \times 10^{-5} A}$$

$I_{D,P} = I_{D,N}$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_P = 11.03}$$

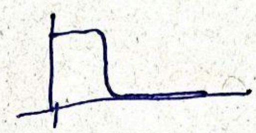
$W_P = 1.65$

$L_P = 0.15$

→ when $\left(\frac{W}{L}\right)_P$ is decreased by a factor of "10"

↳ $V_{Th} = 0.6.6V = 0.66V$

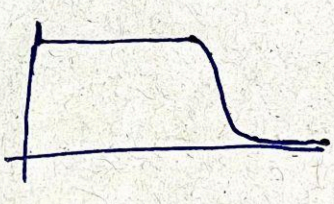
ie ; it decents faster



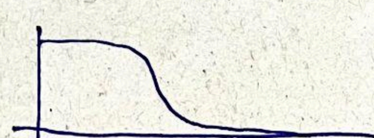
→ when $\left(\frac{W}{L}\right)_P$ is increased by a factor of "10"

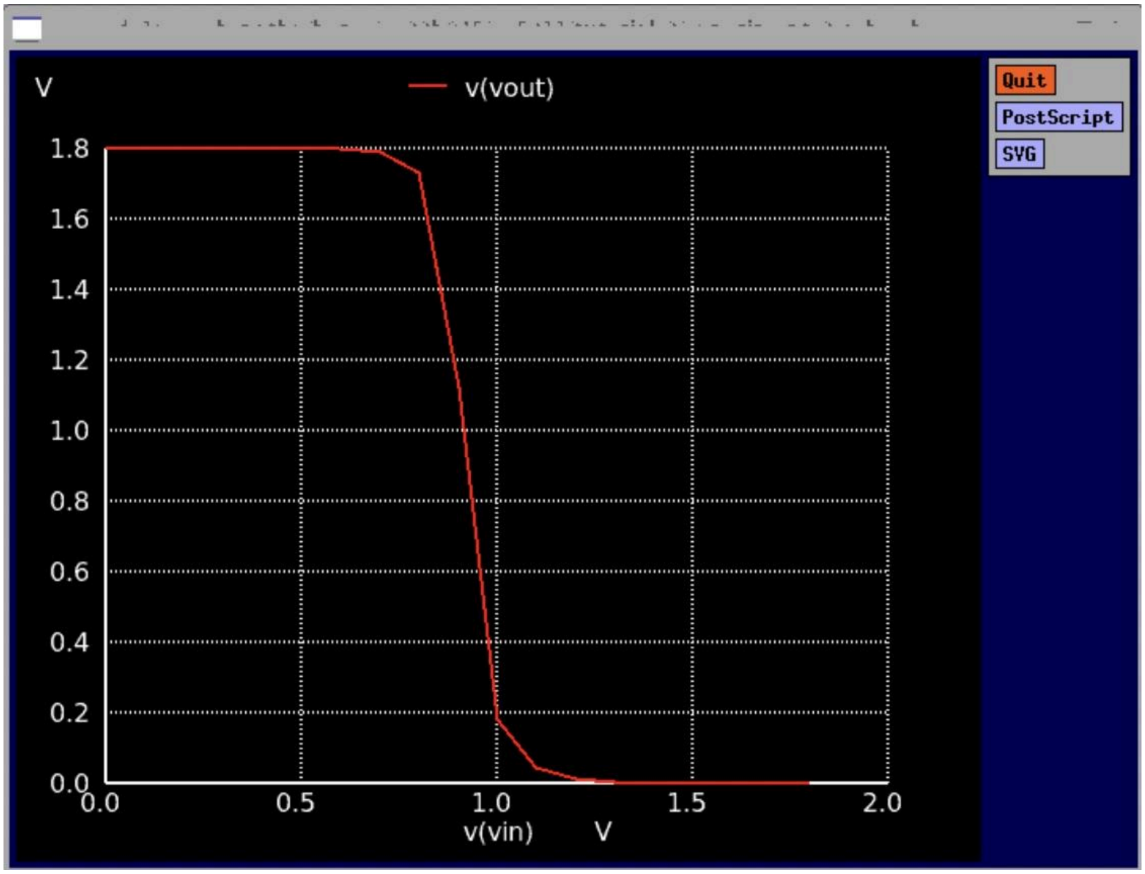
↳ $V_{Th} = 1.04V$

ie; it decents lately.



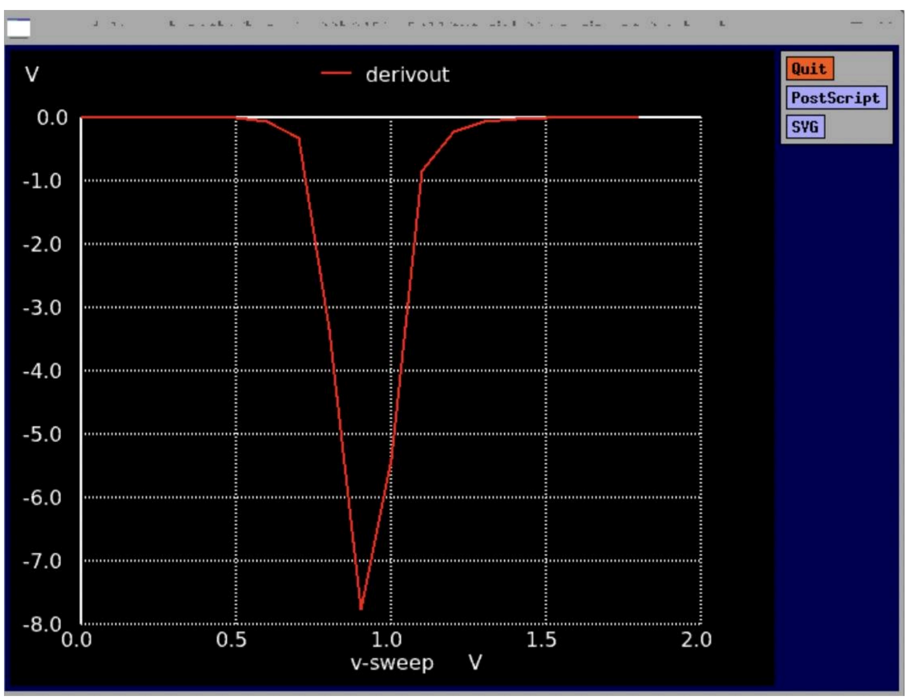
→ ideally when $\left(\frac{W}{L}\right)_P$ $V_{Th} = 0.92V$





Above figure shows DC characteristics graph for (W/L)p = 11.03

Wp = 1.65 || Lp = 0.15



Above Figure shows the Derivative Graph, and The Points hitting "-1" Derivates are noted through the code.

NgSPice Response:

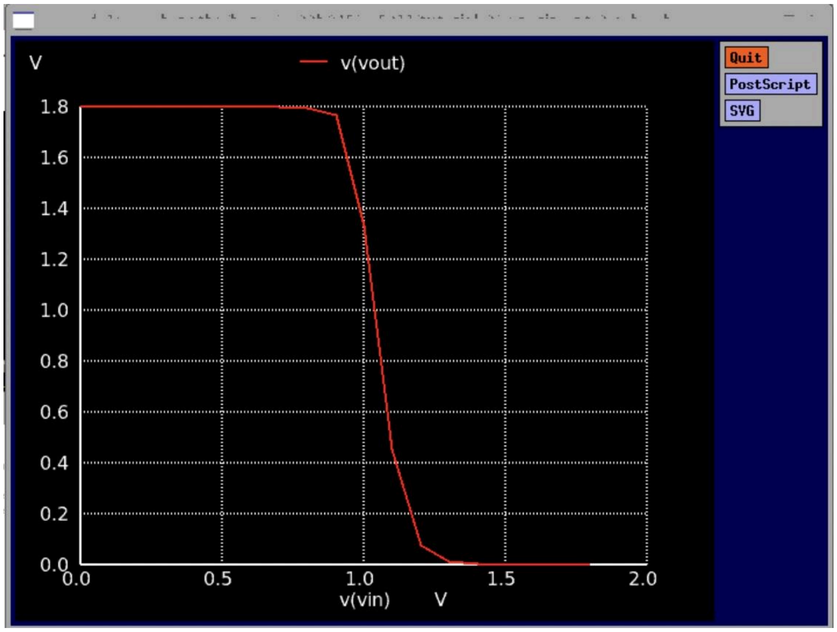
```
Experiment_2_A_B.spice" -a || sh
** Compiled with KLU Direct Linear Solver
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2024, The ngspice team.
** Please get your ngspice manual from https://ngspice.sourceforge.io/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Wed Jan 22 06:35:27 UTC 2025
******

Note: No compatibility mode selected!


Circuit: ** sch_path: /home/ee22b045/ee5311/tutorial_2/experiment_2_a_b.sch

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Using SPARSE 1.3 as Direct Linear Solver
 Reference value :  0.00000e+00
No. of Data Rows : 19
vil                 =  7.223556e-01
vih                 =  1.096542e+00
vth                 =  9.236806e-01
NML: 0.722356 NMH: 0.703458
ngspice 1 ->
```

Noise Margines:

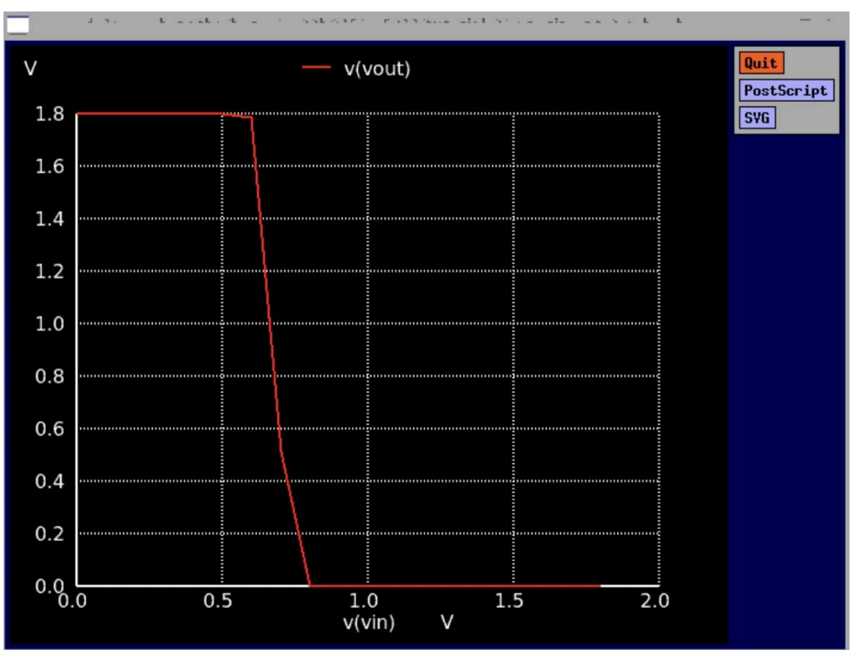
NML = 0.722V

NMH = 0.734V

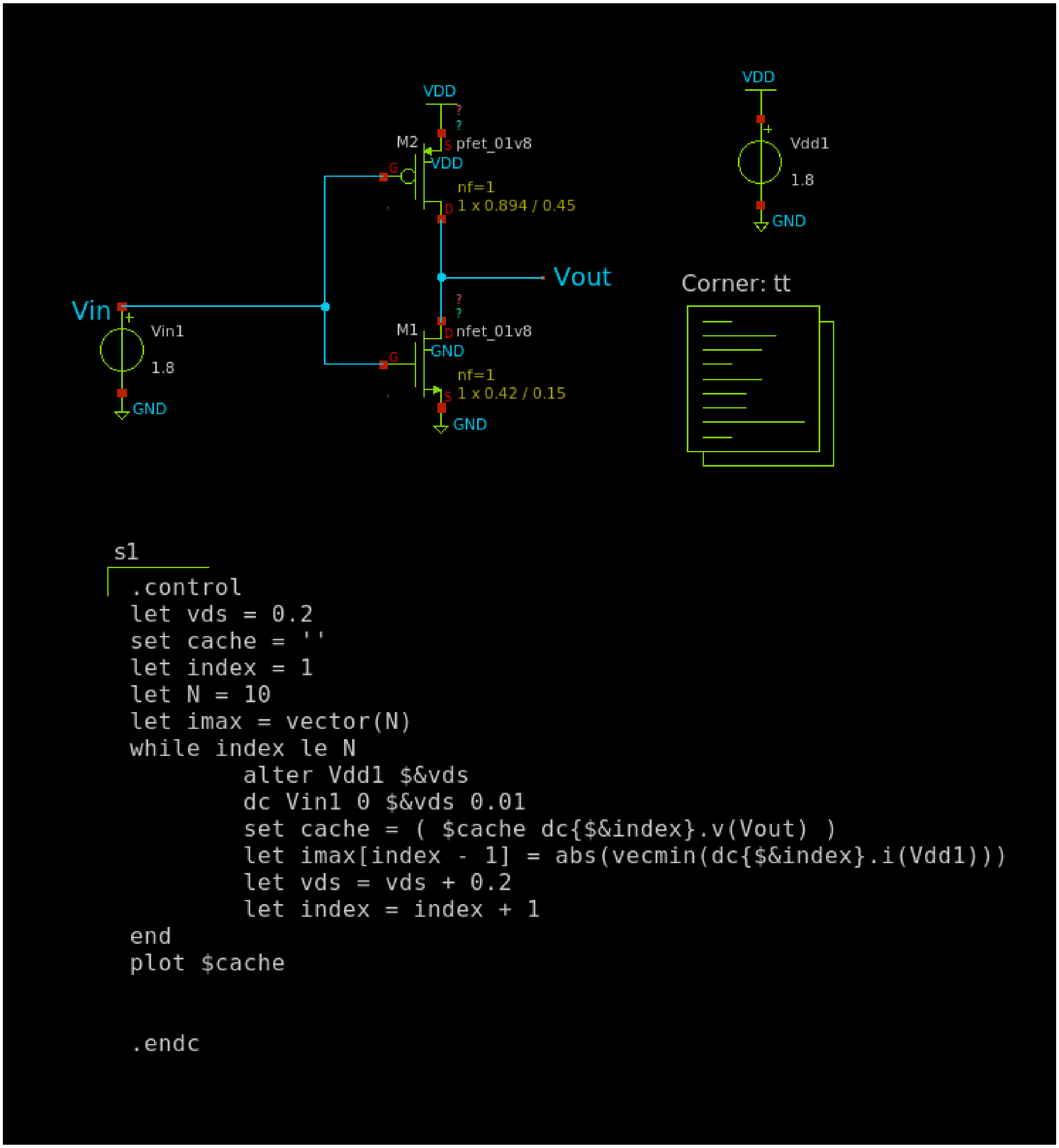
DC Characteristics when W/L ratio is **Increased by 10** times:
NHL: 0.839V
NHM: 0.534V

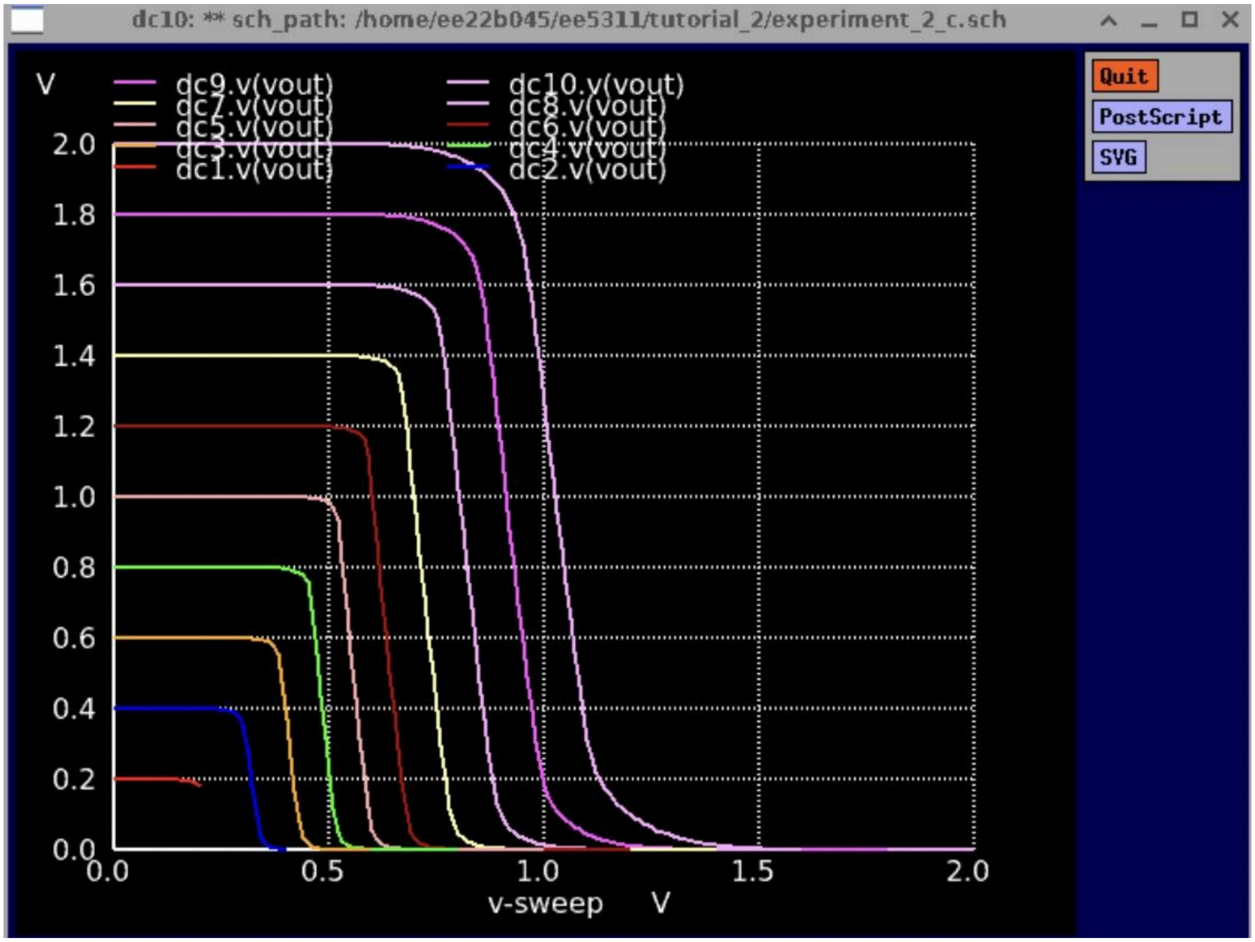


DC Characteristics when W/L ratio is **Decreased by 10** times:
NHL: 0.514V
NHM: 0.938V



<u>Schematic for (C):</u>





For low VDD (e.g., 0.2V, 0.4V):

- The **inverter does not work effectively** because the **MOSFETs are in the subthreshold region**, leading to weak drive currents.
- VthV_{th}Vth deviates from VDD/2V_{DD}/2VDD/2.
- The gain (slope of the transition) is low, causing poor noise margins.

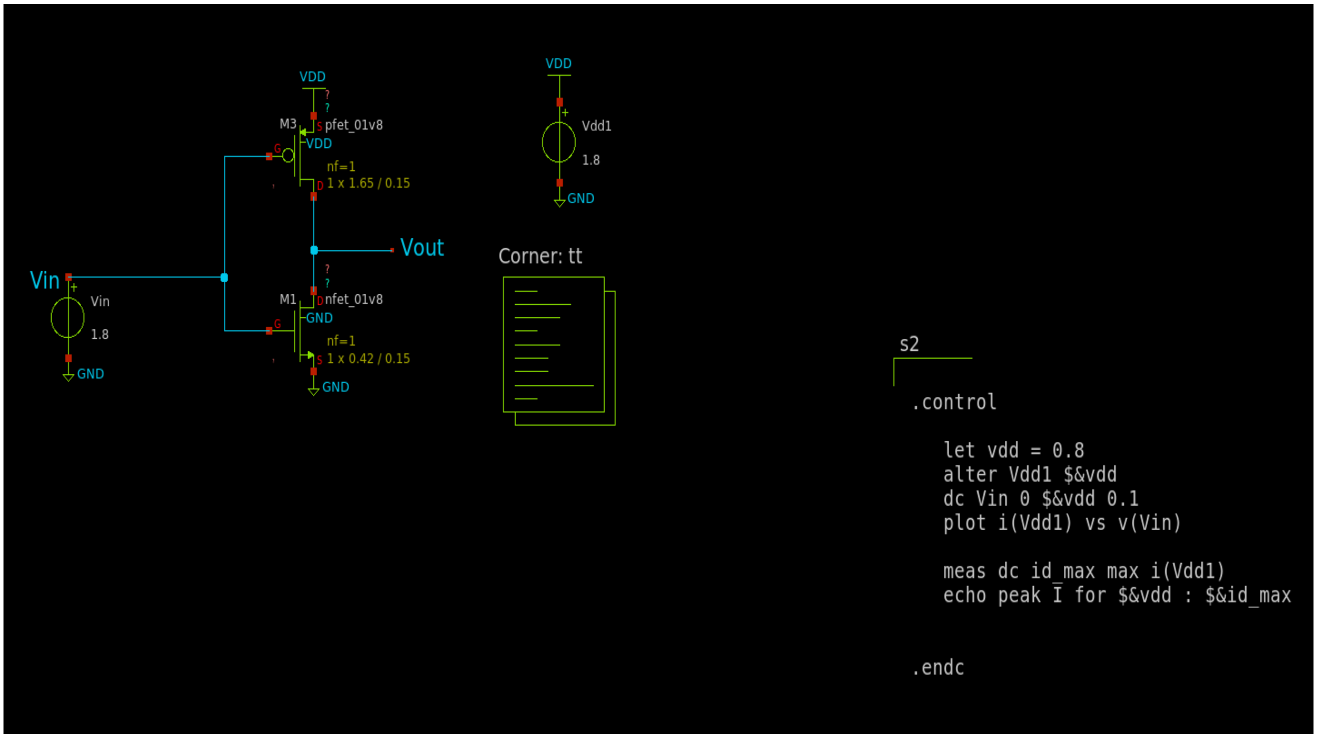
For mid-range VDD (e.g., 0.8V, 1.0V):

- The inverter functions normally.
- Vth≈VDD/2 if (W/L)p is properly sized.
- Noise margins are sufficient for digital logic.

For high VDD (e.g., 1.8V):

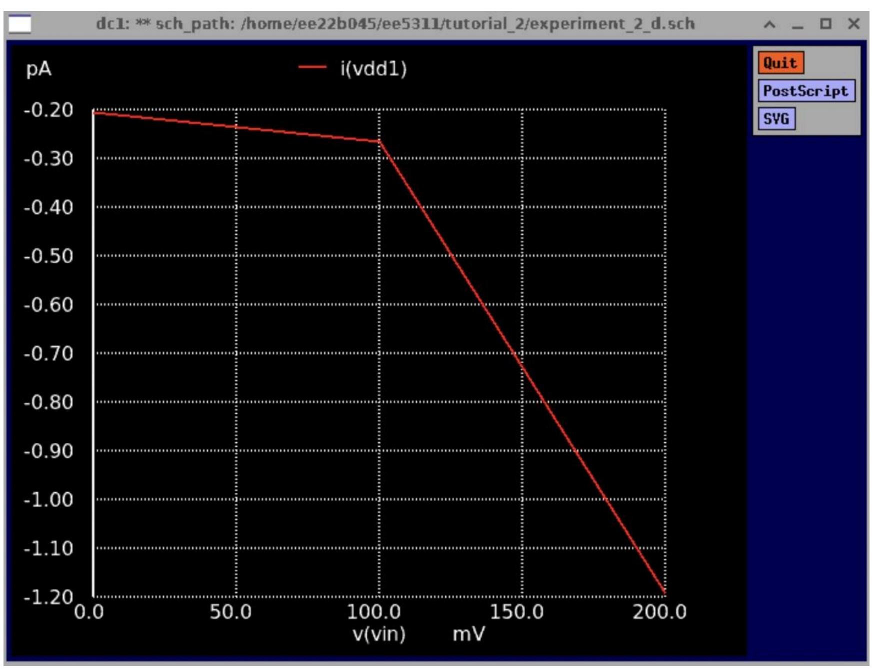
- The transition is sharper.
- **Strong drive currents** improve switching speed.
- Increased noise margins.

Schematic for (D):



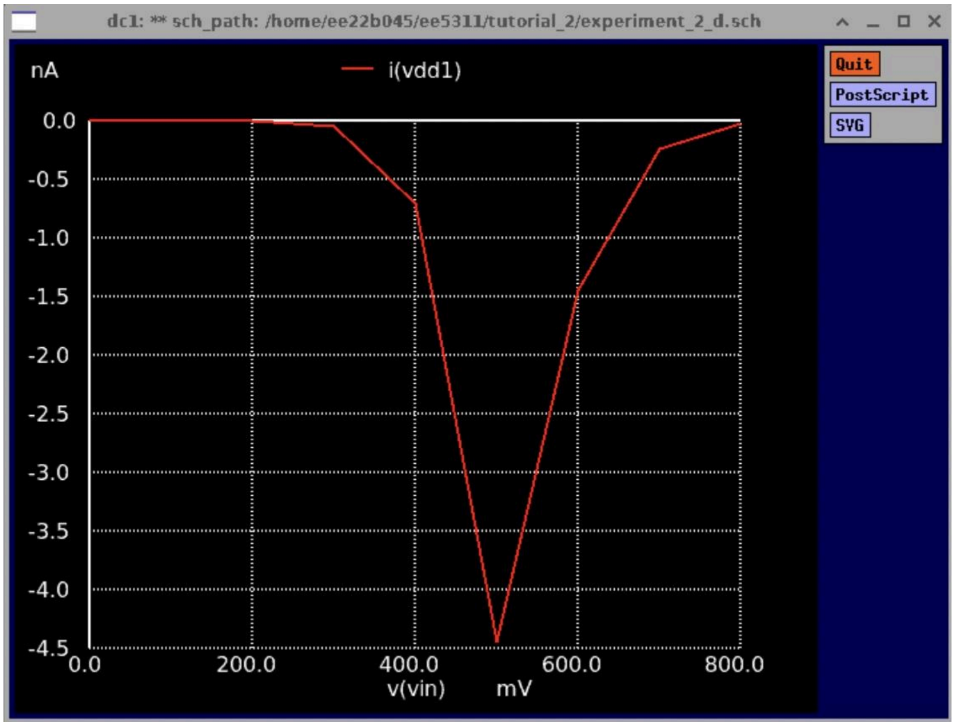
1) Ids vs Vin @Vdd = 0.2V

I_max = -0.204pA (pico Amps)



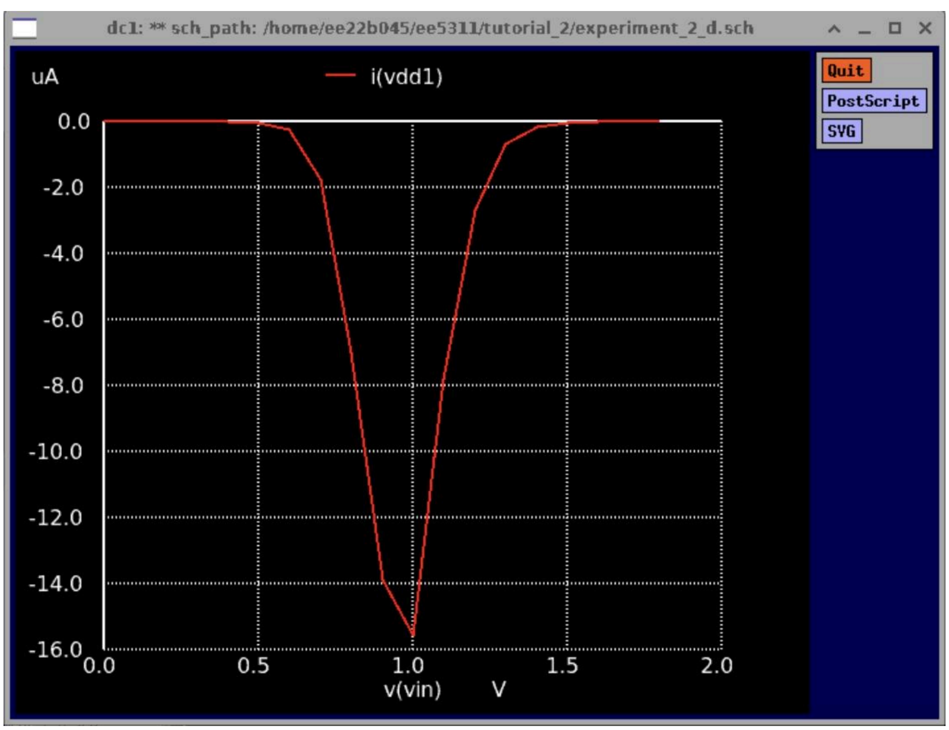
2) Ids vs Vin @Vdd = 0.8V

I_max = -0.812nA (nano Amps)



3) Ids vs Vin @Vdd = 1.8V

I_max = -1.835uA (micro Amps)



- Peak Ids increases as VDD increases.
- For small VDD, transistors operate in the **weak inversion** region, reducing Ids.
- For high VDD, Ids reaches larger values, leading to **faster switching**.

- The End -