Digital IC Design

EE5311

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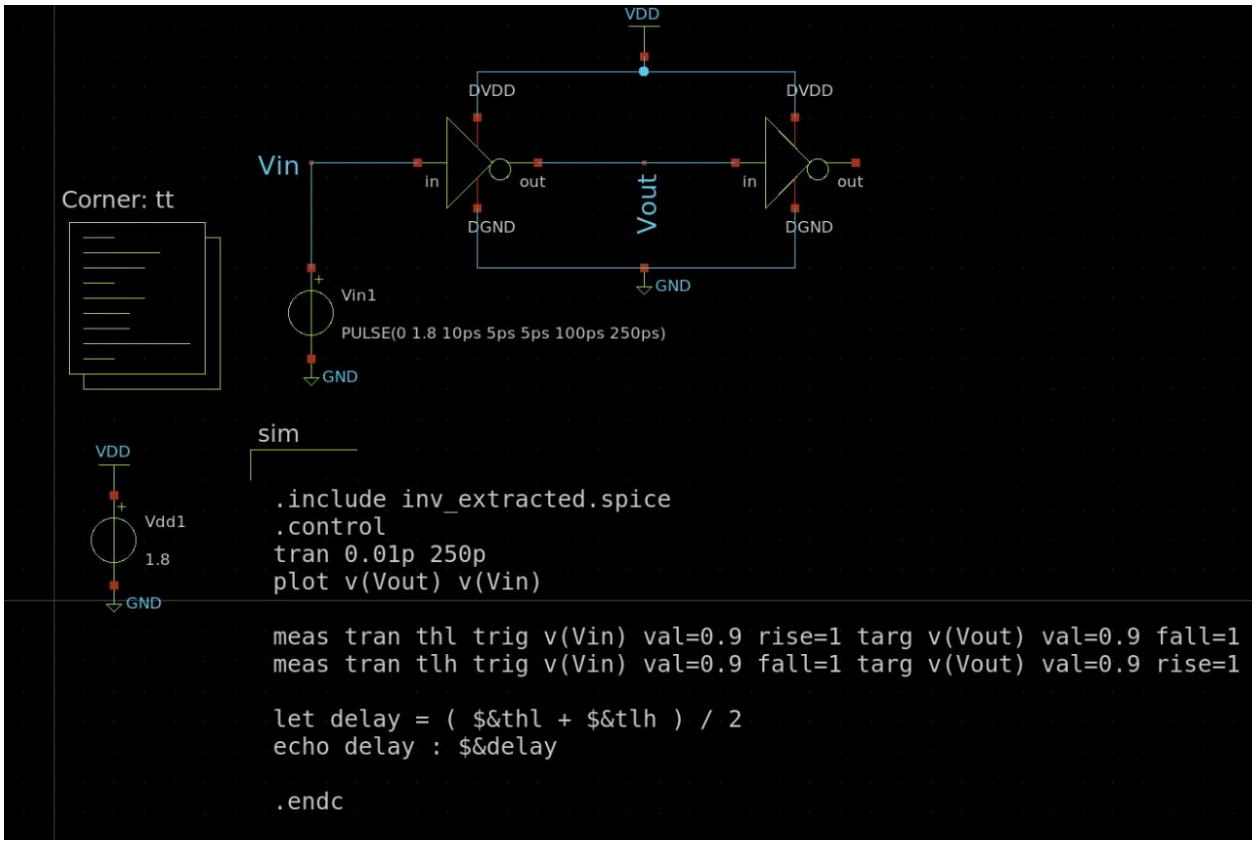
EE22B045

Tutorial - 5

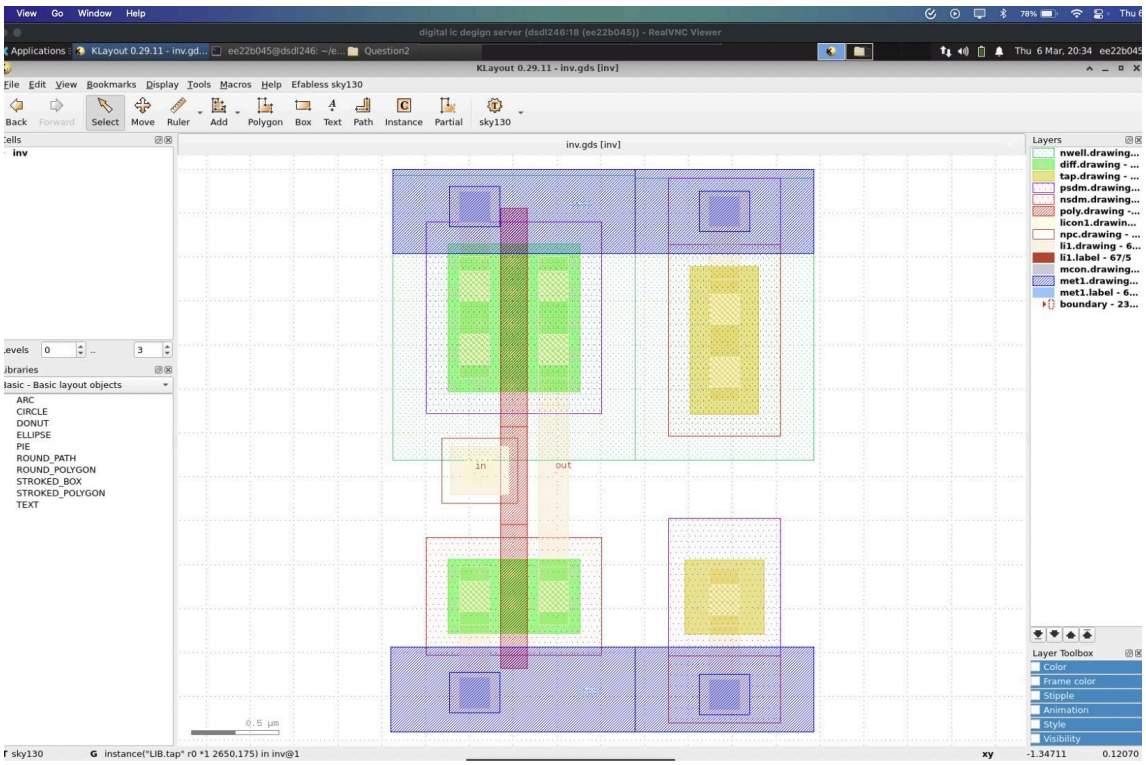
Report

Experiment - 1

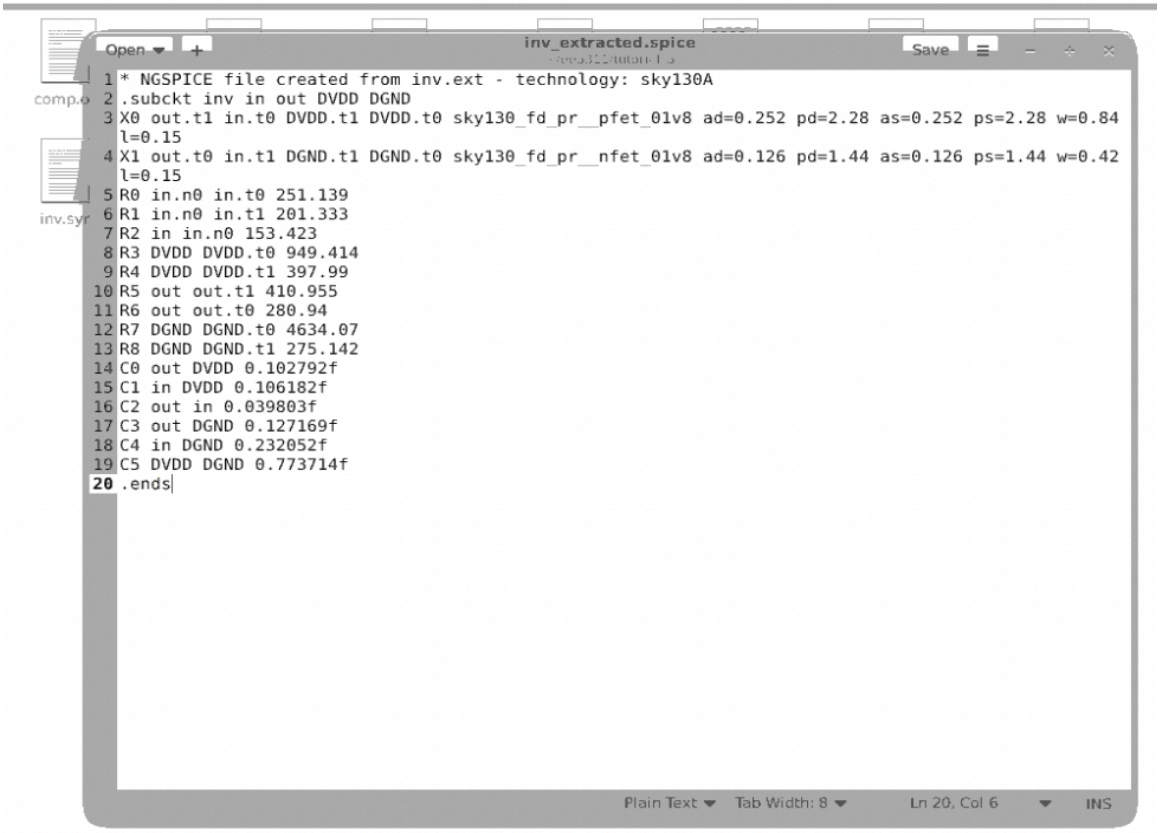
Schematic



KLayout for inverter:



Extracted Parasitics:

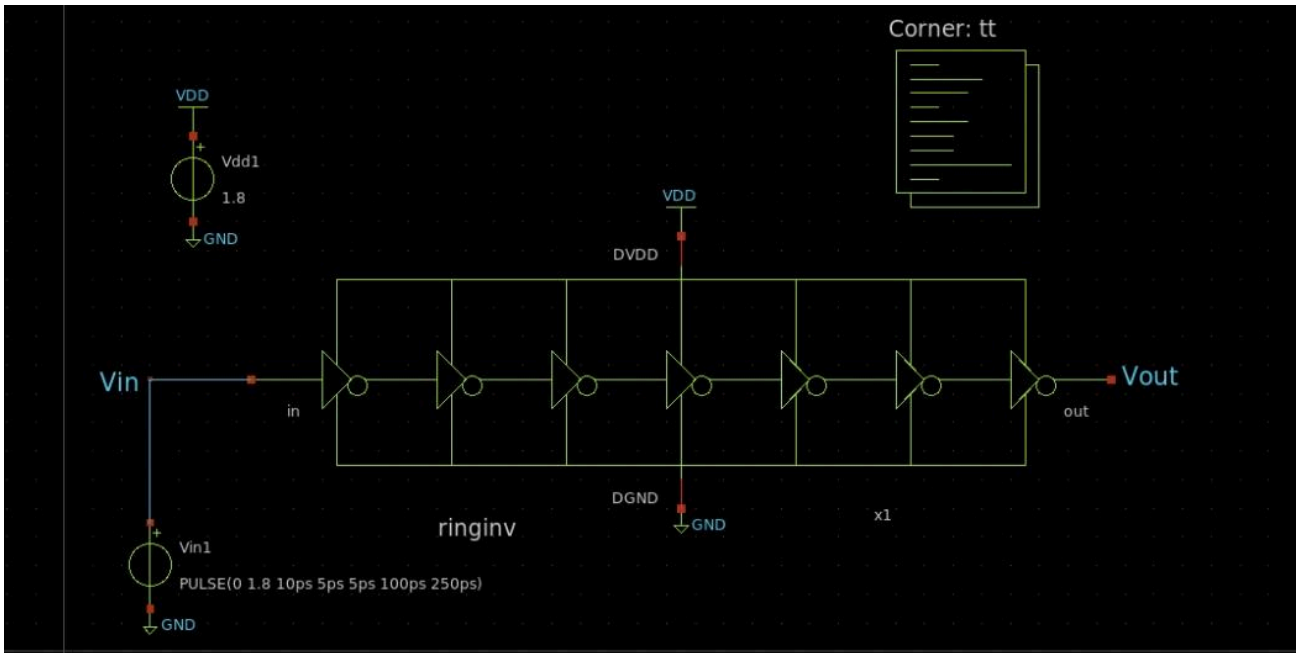


A) The Delay of the Circuit(without the Parasitics) = 2.07 x 10^-11 sec

B) The Delay of the Circuit With Parasitics = 2.52 x 10^-11 sec

Experiment - 2:

Schematic

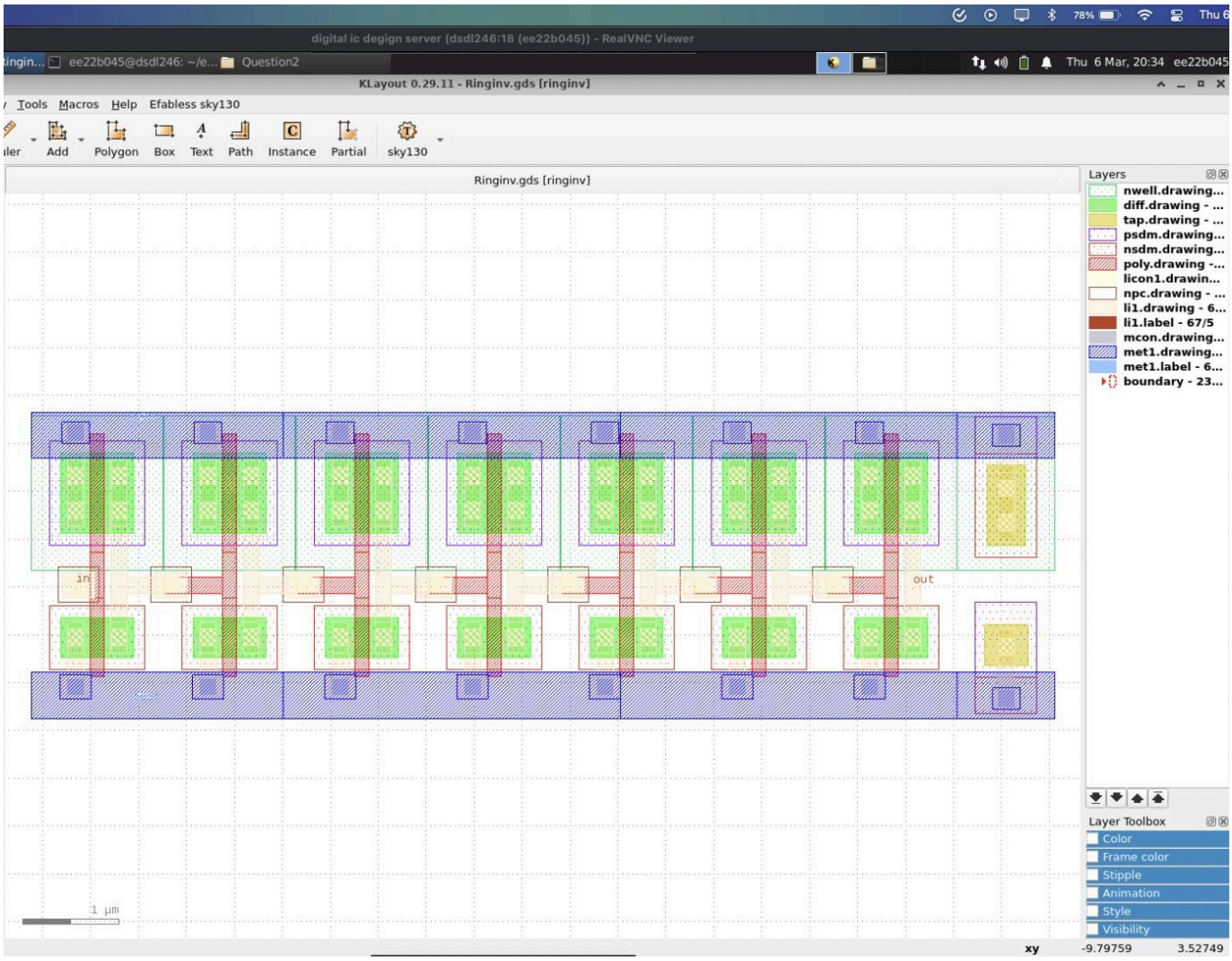


sim

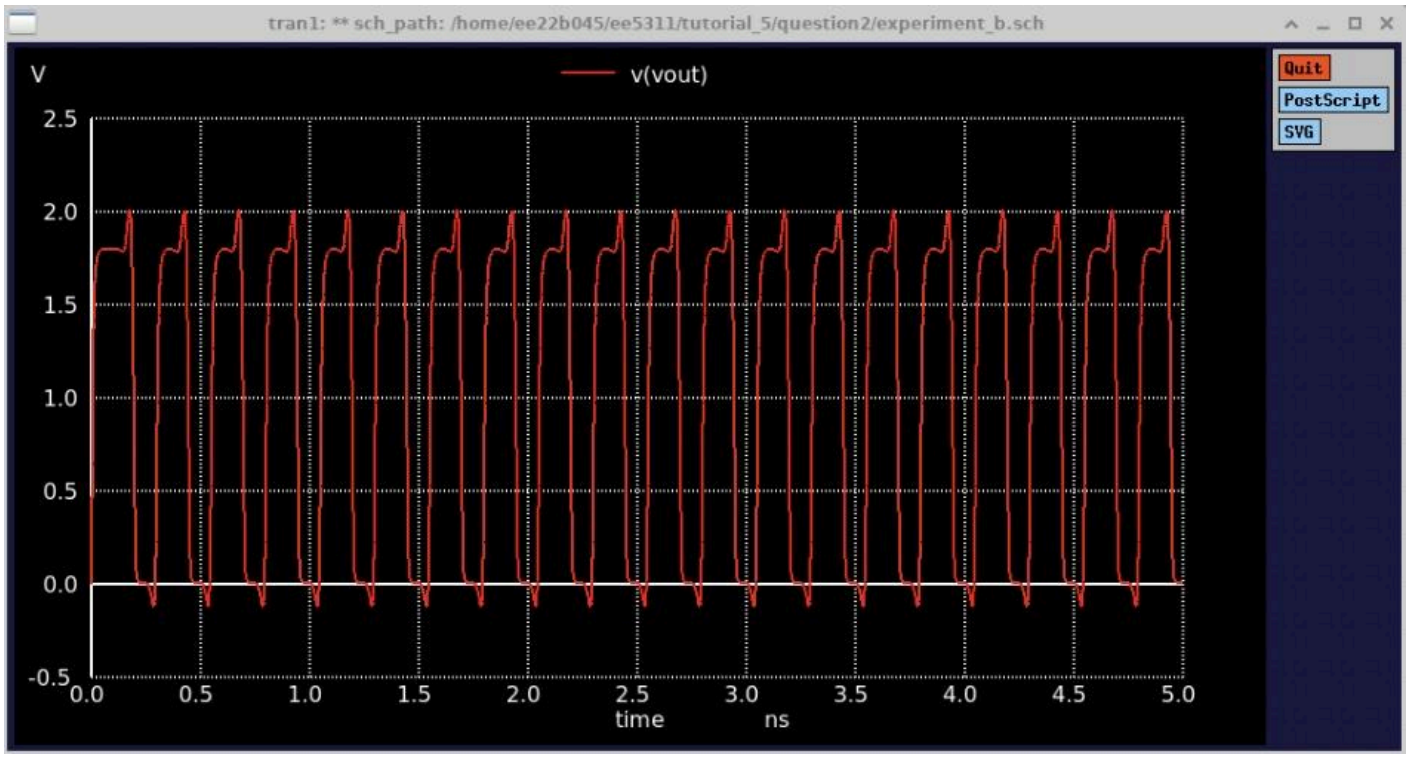
```
.include ringinv_extracted.spice
.param VDD1=1.8
* Set initial condition to start oscillation
.ic v(Vout) = 0
.control
        dc VDD 0 1.8 0.1
        tran 1ps 5ns
        meas tran period trig v(Vout) VAL=0.9 RISE=1 targ v(Vout) VAL=0.9 RISE=2
        let freq = (1/($&period))

        echo Frequency of oscillation: $&freq
        plot v(Vout)
.endc
```

Kayout of Ring Oscillator

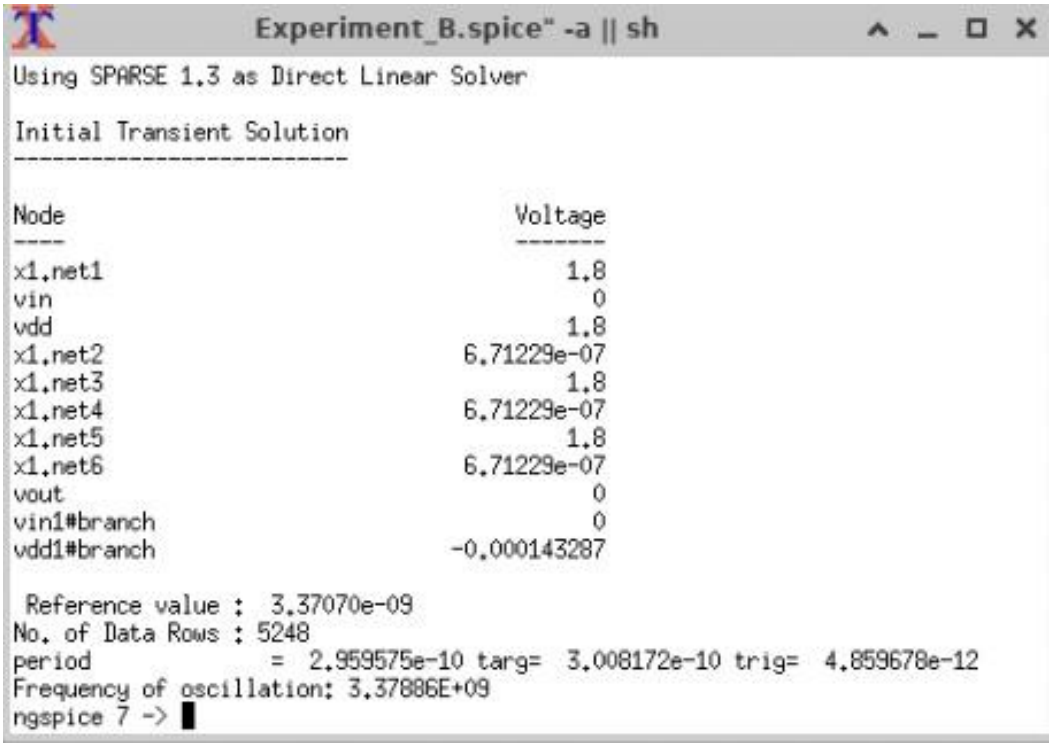


c) When parasitics are not Included in the Schematic:

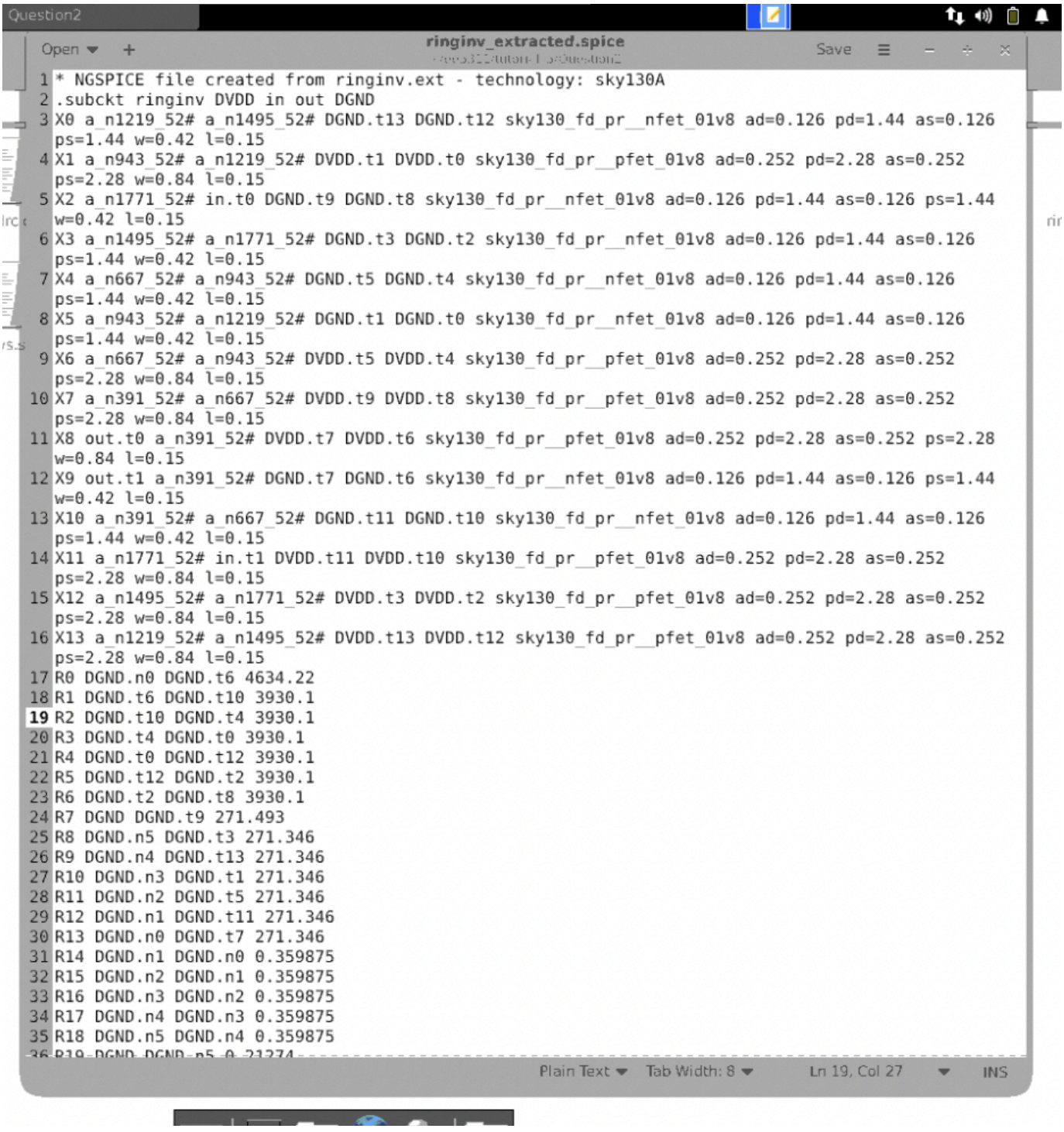


This graph shows the Oscillations without counting for the Parasitics

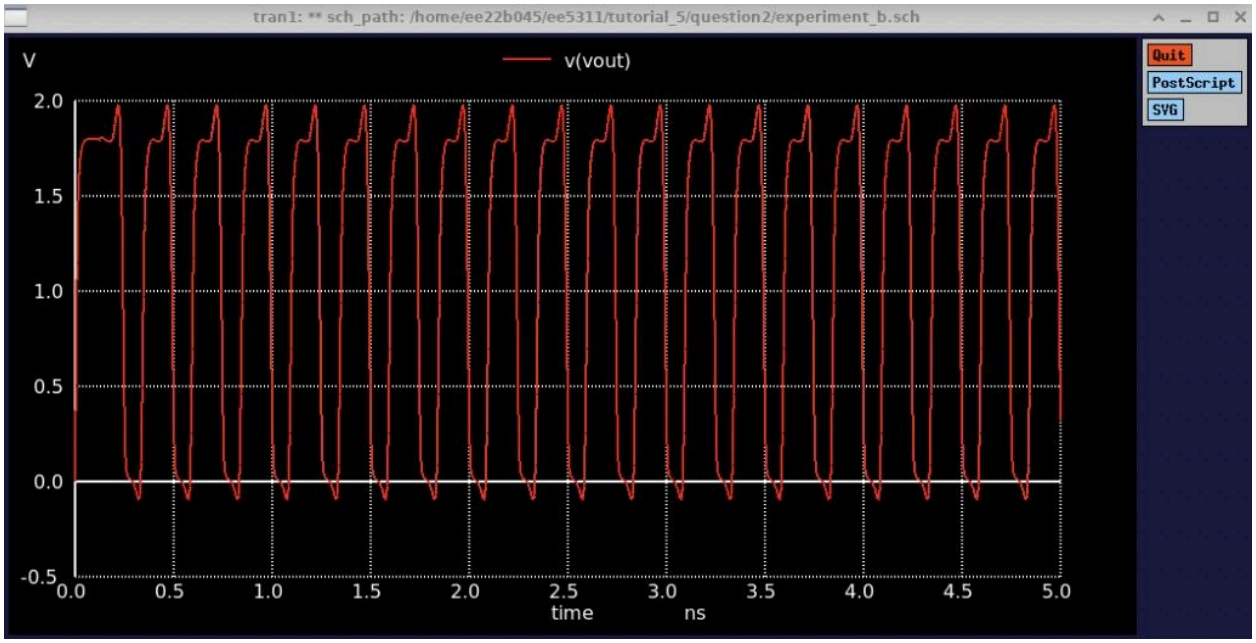
Frequency of oscillation : 3.37 x 10^9Hz or 3.37GHz



Extracted Parasitics:

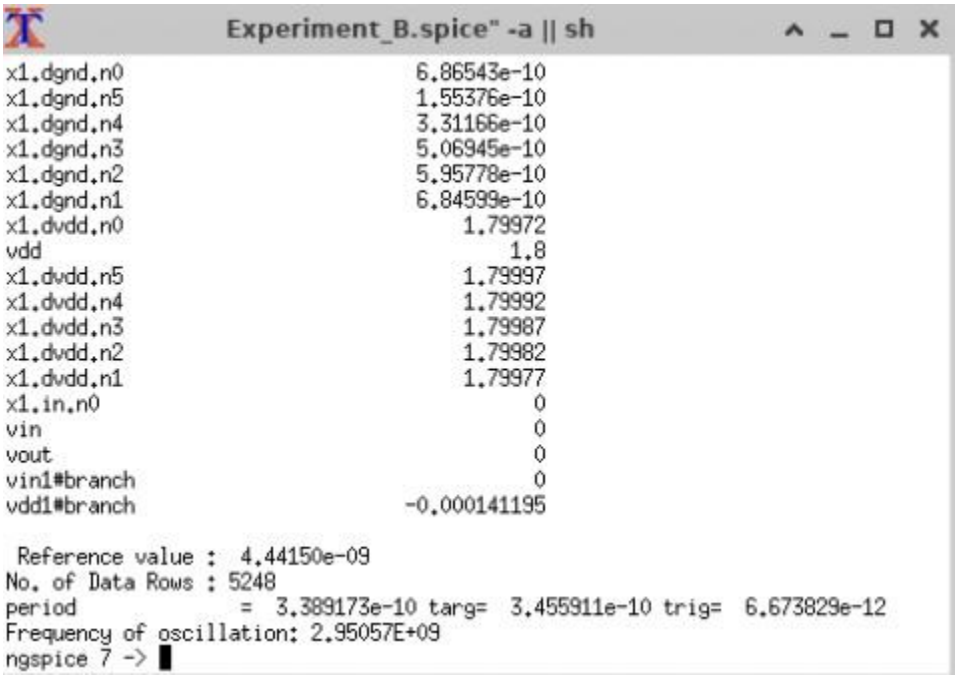


A)When Parasitics are included in the schematic:

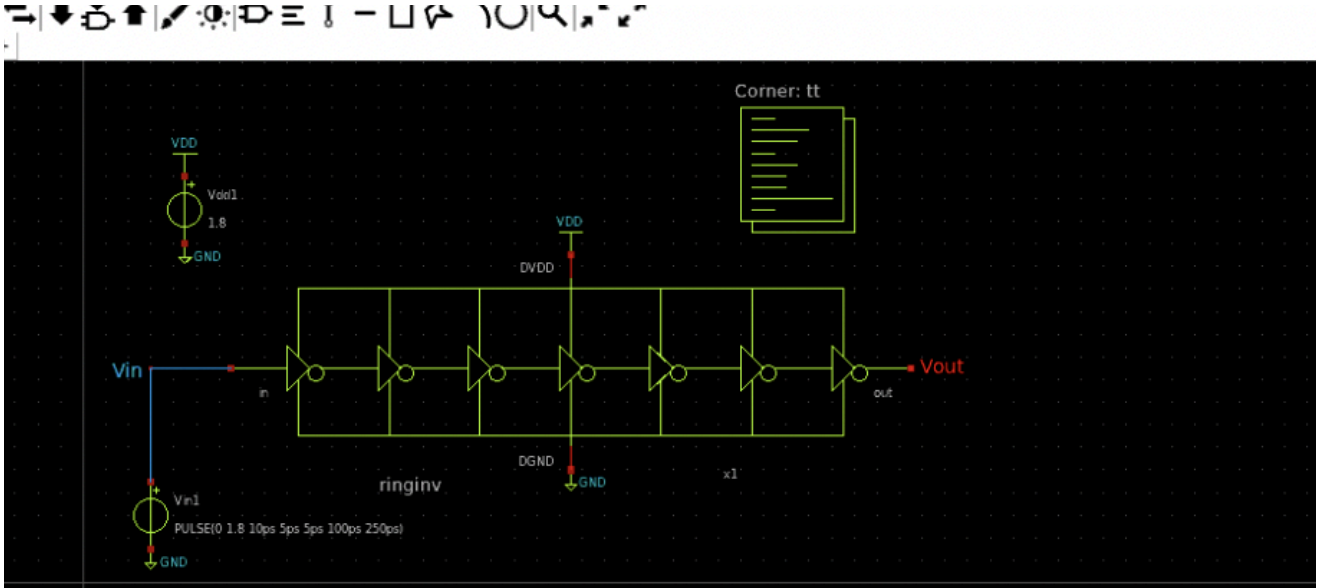


This graph shows the Oscillations without counting for the Parasitics

Frequency of oscillation : 2.97 x 10^9Hz or 2.97GHz



B)Code and Schematic:




```
s2

 .include ringinv_extracted.spice
 .param VDD1 = 1.8
 .ic v(Vout) = 0
 .control
 let Nsim = 9
 let periodvec = vector(Nsim)
 let vddvec = vector(Nsim)
 let freqvec = vector(Nsim)
 let index = 0
 let vdd = 1.0
 while index < Nsim
        let vdd = 1.0 + (index * 0.1)
        alterparam VDD1 = $&vdd
        reset
        tran 1ps 5ns
        meas tran period trig v(Vout) val=0.5 rise=1 targ v(Vout) val=0.5 rise=2
        let freq = 1/$&period
        let periodvec[index] = $&period
        let vddvec[index] = vdd
        let freqvec[index] = freq
        let index = index + 1
        echo  Period = $&period Frequency = $&freq

 end
 plot periodvec vs vddvec
 plot freqvec vs vddvec
 .endc
```

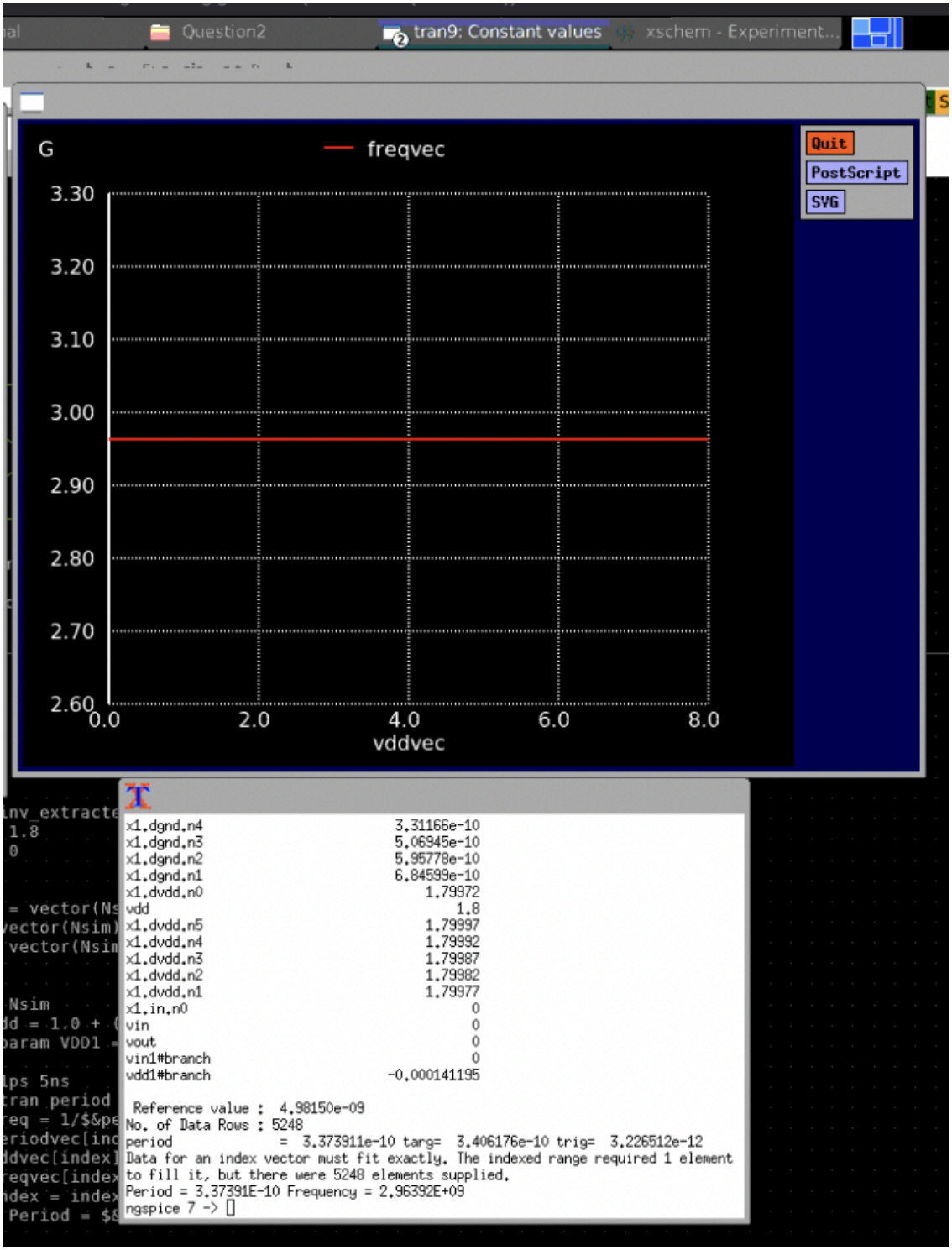
pice Stretch: 0 mouse = -410 70 - selected: 0 path: .

Observation:

Pre-layout frequency (no parasitics): Higher

Post-layout frequency (with parasitics): Lower

Frequency vs VDD response



- The End -