Digital IC Design

EE5311

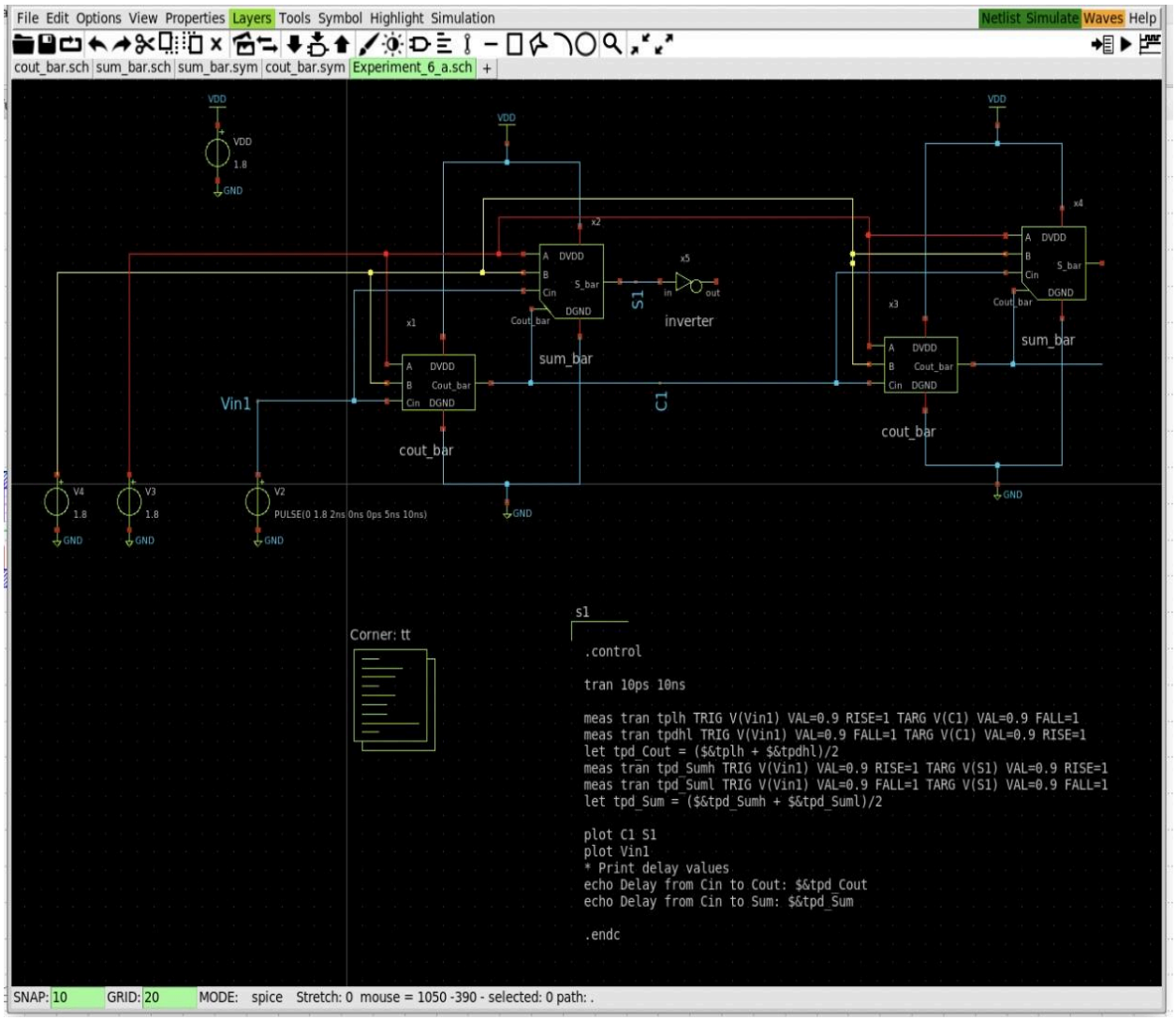
Mourya Sai Sandeep
EE22B045

Tutorial - 6a

Report

Experiment - A

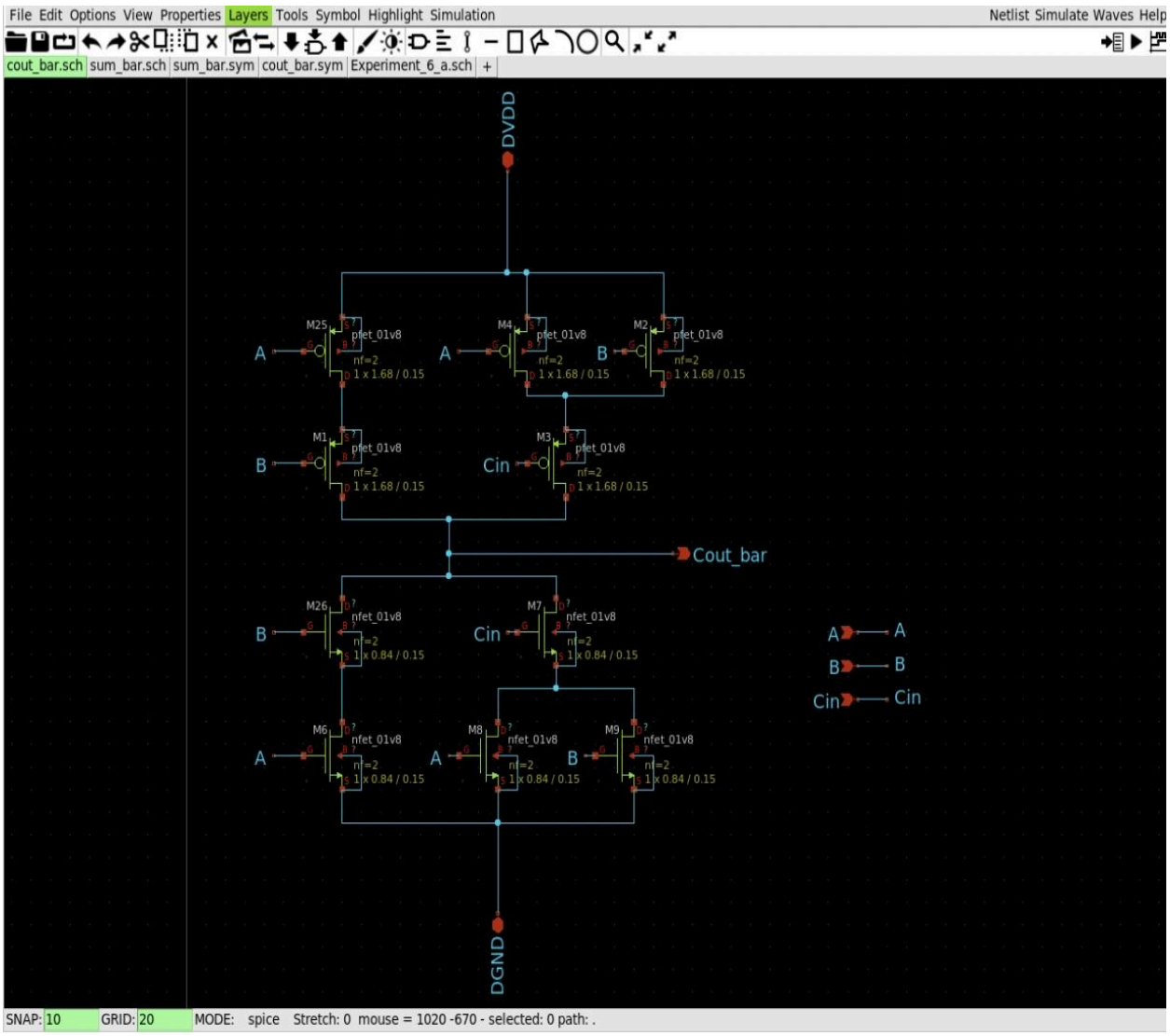
Schematic



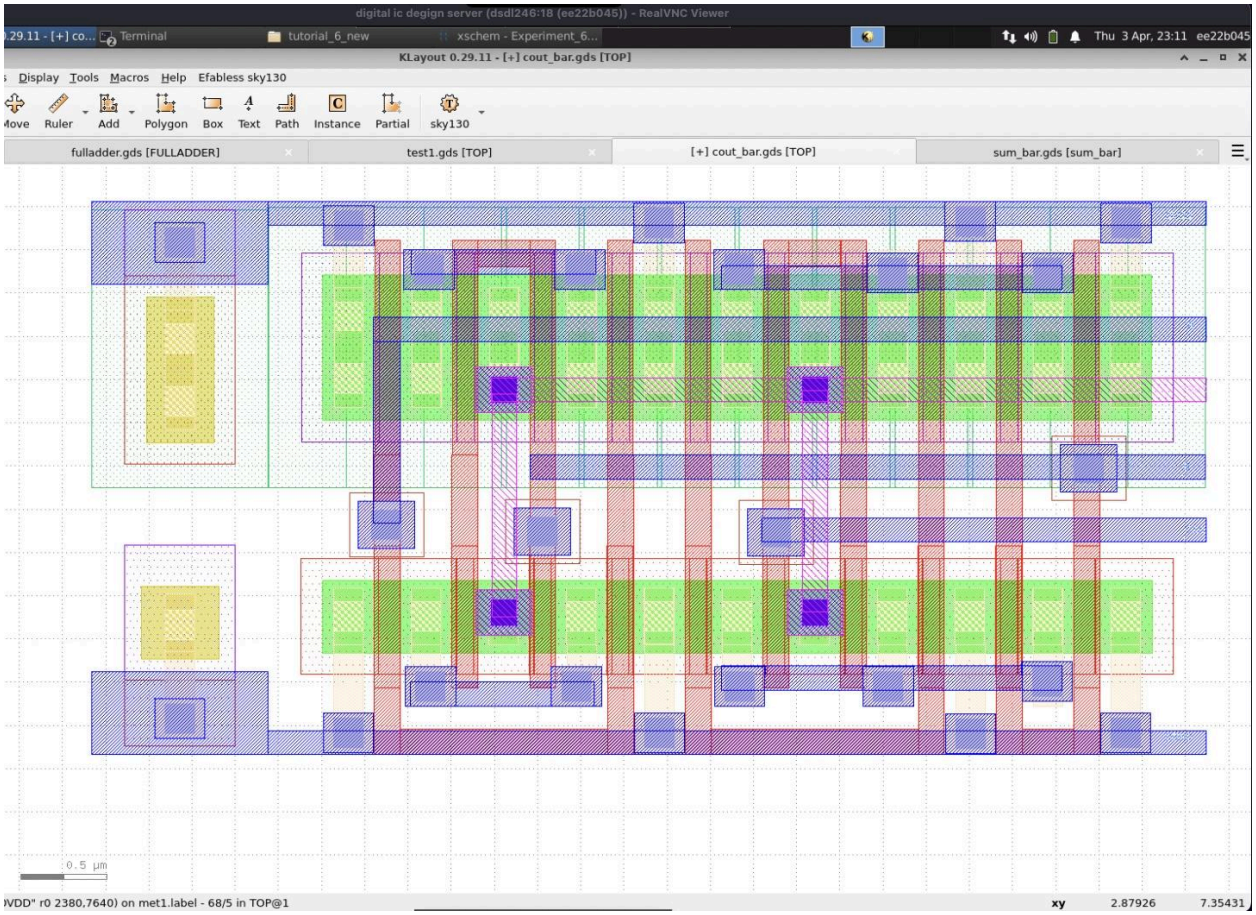
-> This Full adder works through fusion of two blocks

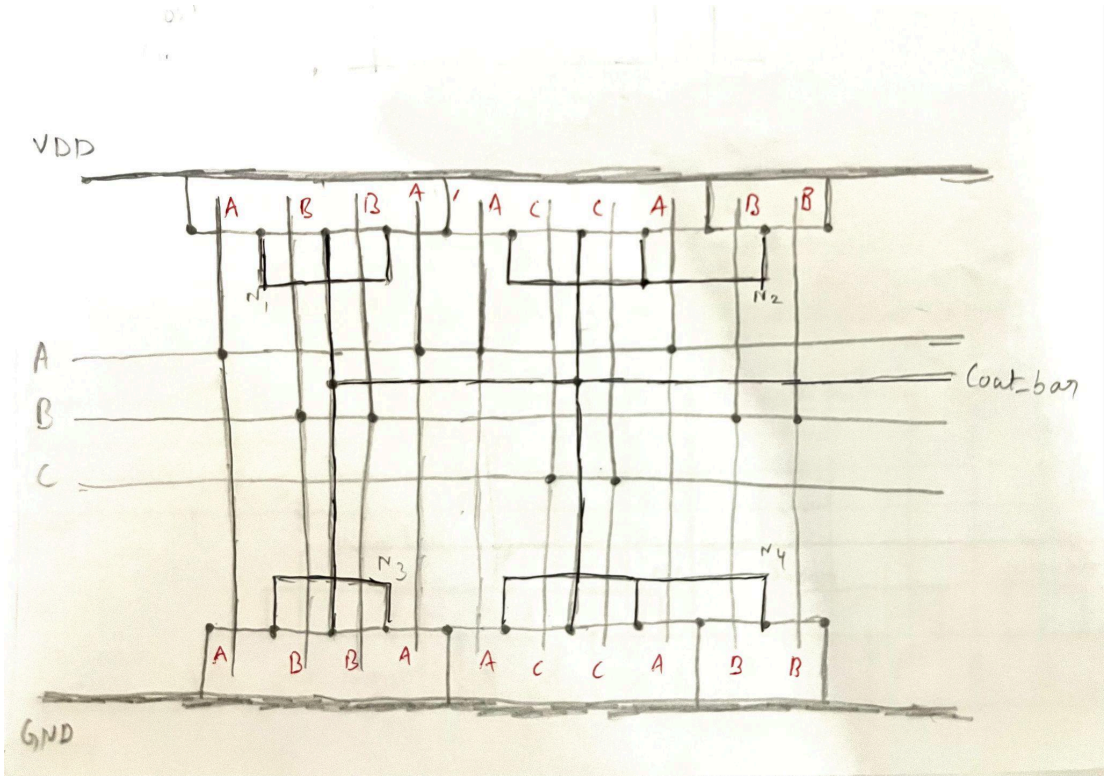
- Cout_bar(A,B,Cin)
- S_bar(A,B,Cin,Cout_bar)

Schematic for cout_bar's symbol:



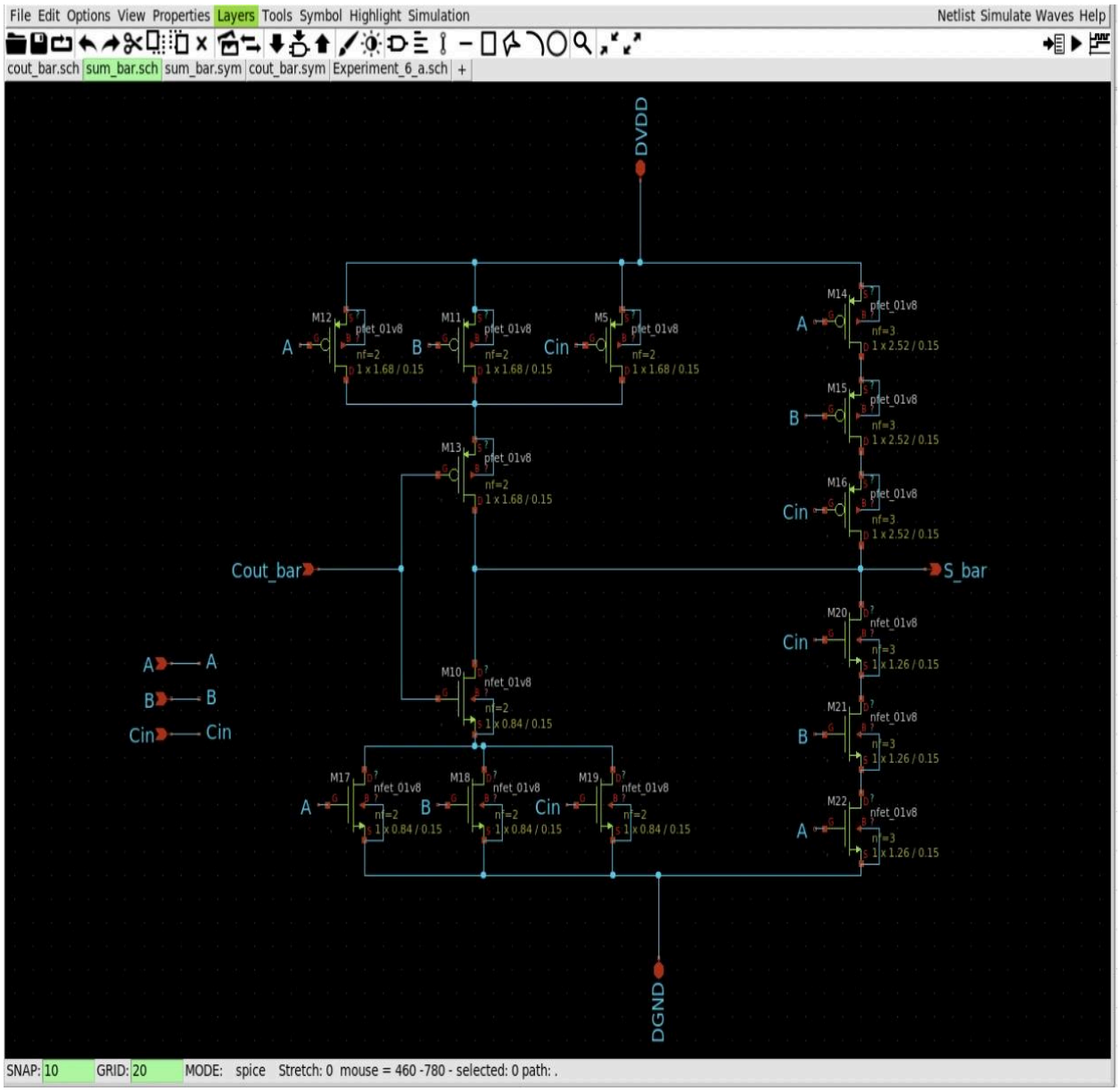
Klayout for cout_bar:



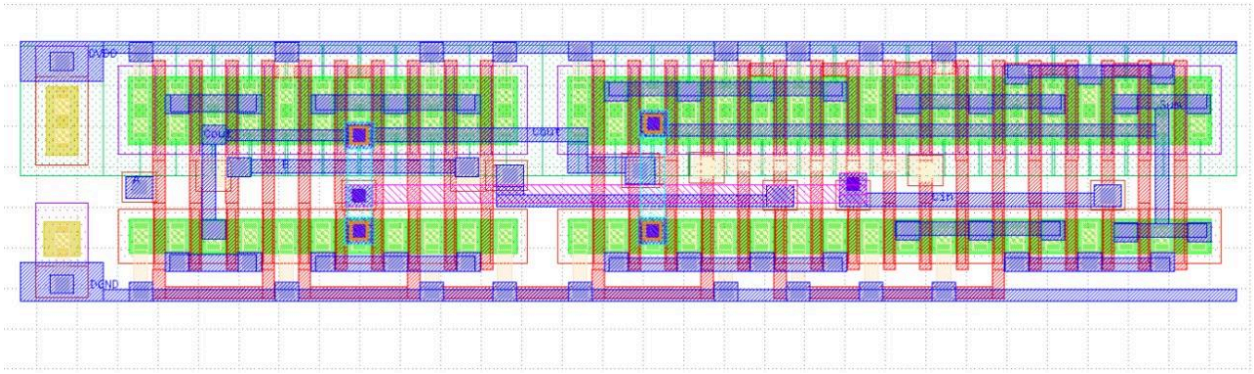


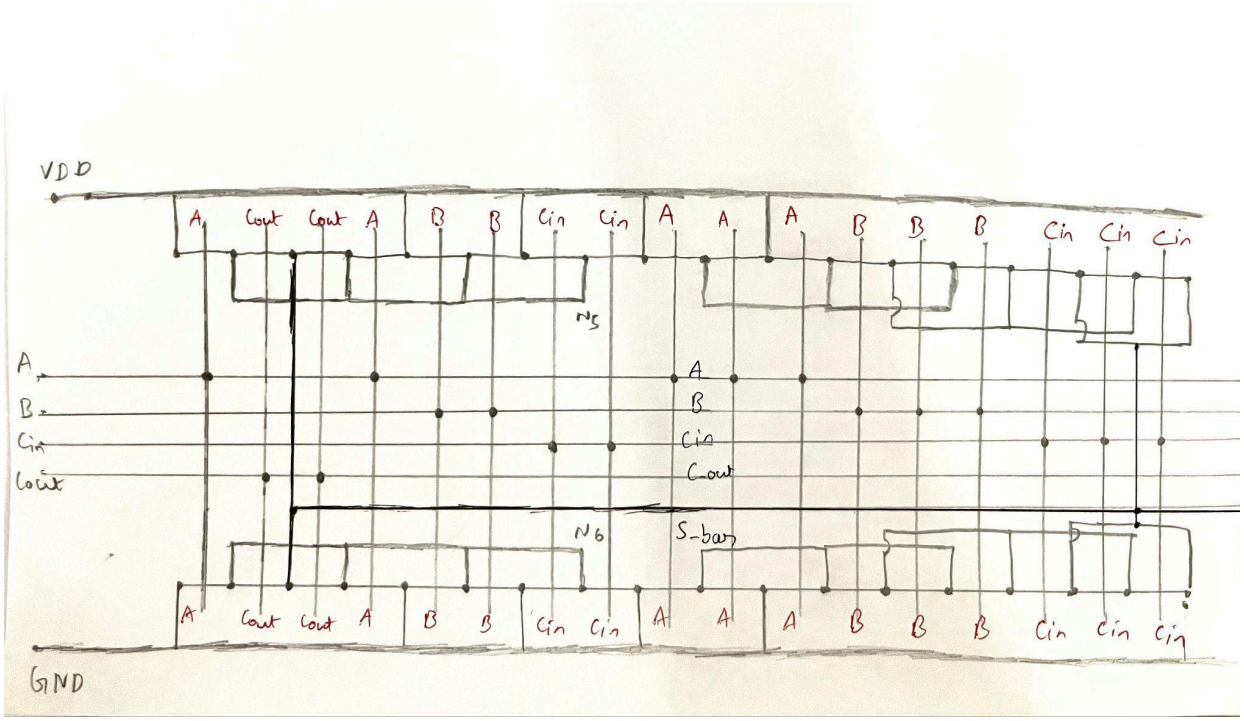
Stick Diagram for cout_bar

Schematic for S_bar's Symbol:



Klayout for S_bar:

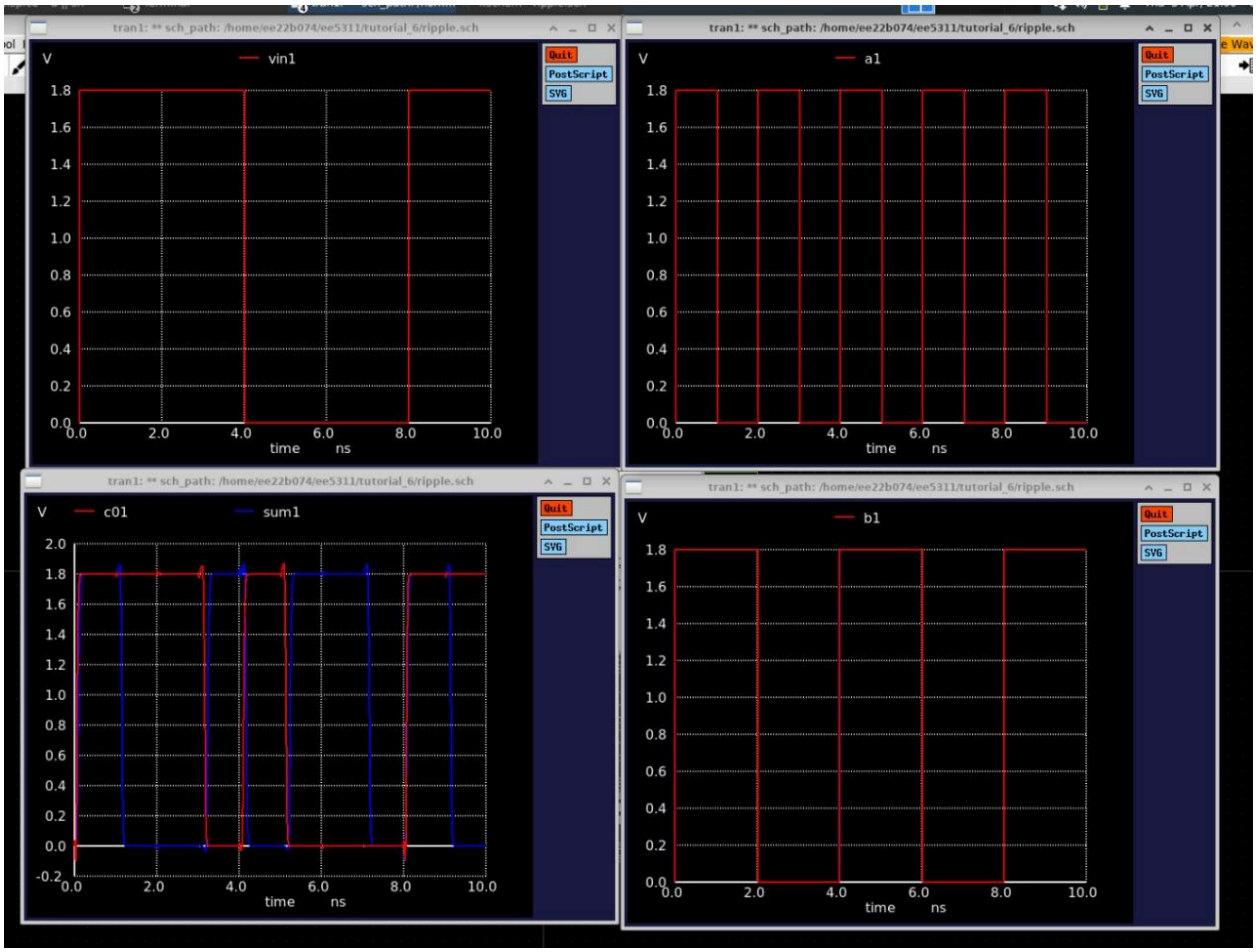




Stick Diagram for S_bar

A) The Delay of the Circuit Cin to Cout = 3.07 x 10^-11 sec

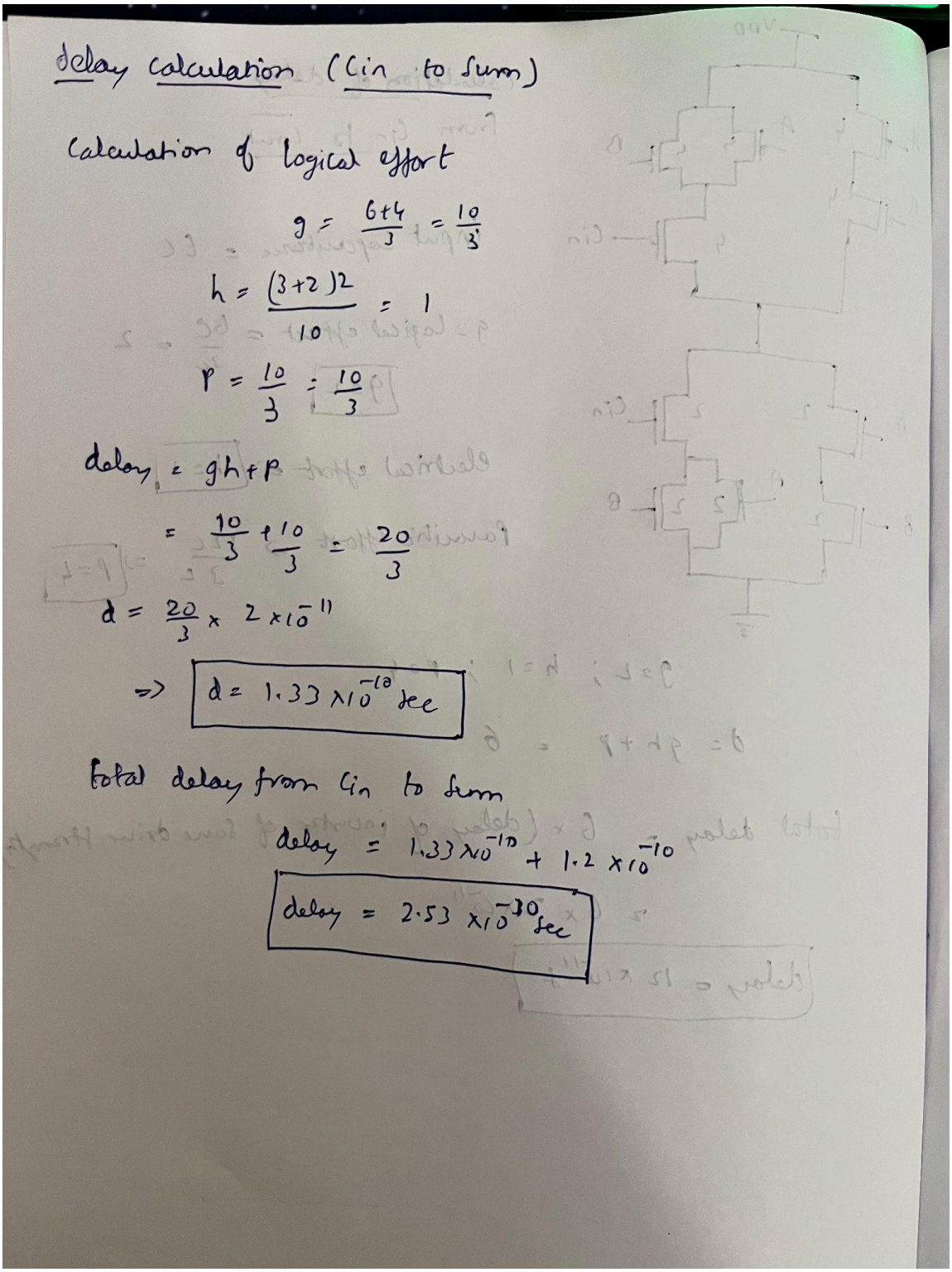
B) The Delay of the Circuit Cin to Sum = 4.92 x 10^-11 sec



Responses of the circuit after the Layout Linkage

Experiment - B:

Calculations:



Delay calculation (Cin to Sum)

Calculation of logical effort

$$g = \frac{6+4}{3} = \frac{10}{3}$$

$$h = \frac{(3+2)2}{10} = 1$$

$$p = \frac{10}{3} = \frac{10}{3}$$

Delay = $gh + p$

$$= \frac{10}{3} + \frac{10}{3} = \frac{20}{3}$$

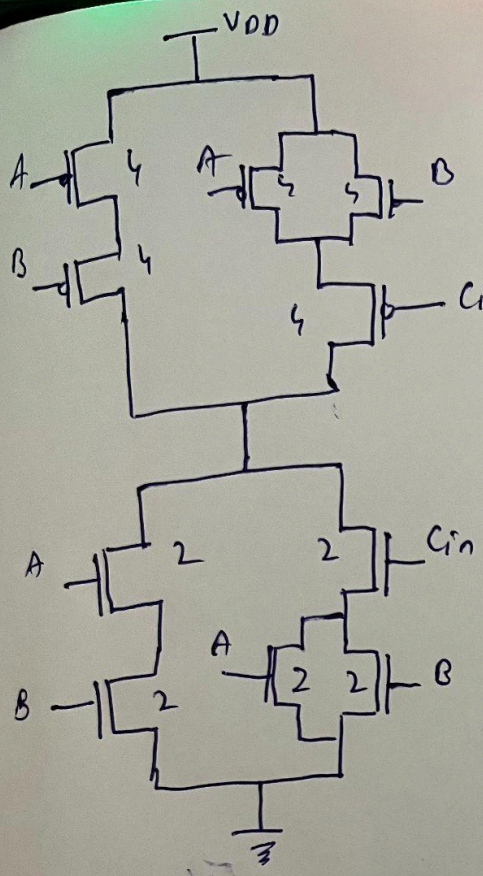
$$d = \frac{20}{3} \times 2 \times 10^{-11}$$

$$\Rightarrow \boxed{d = 1.33 \times 10^{-10} \text{ sec}}$$

Total delay from Cin to Sum

$$\text{delay} = 1.33 \times 10^{-10} + 1.2 \times 10^{-10}$$

$$\boxed{\text{delay} = 2.53 \times 10^{-10} \text{ sec}}$$



Calculation of delay from C_{in} to C_{out}

input capacitance = $6C$

g = logical effect = $\frac{6C}{3C} = 2$

$\boxed{g = 2}$

electrical effort $\Rightarrow \boxed{h = 1}$

Parasitic effort $\Rightarrow \frac{12C}{3C} \Rightarrow \boxed{P = 4}$

$g = 2$; $h = 1$; $P = 4$

$d = gh + P = 6$

total delay = $6 \times$ (delay of inverter of same drive strength

$= 6 \times 2 \times 10^{-11}$

$\boxed{\text{delay} = 12 \times 10^{-11} s}$

- The End -