

Digital IC Design

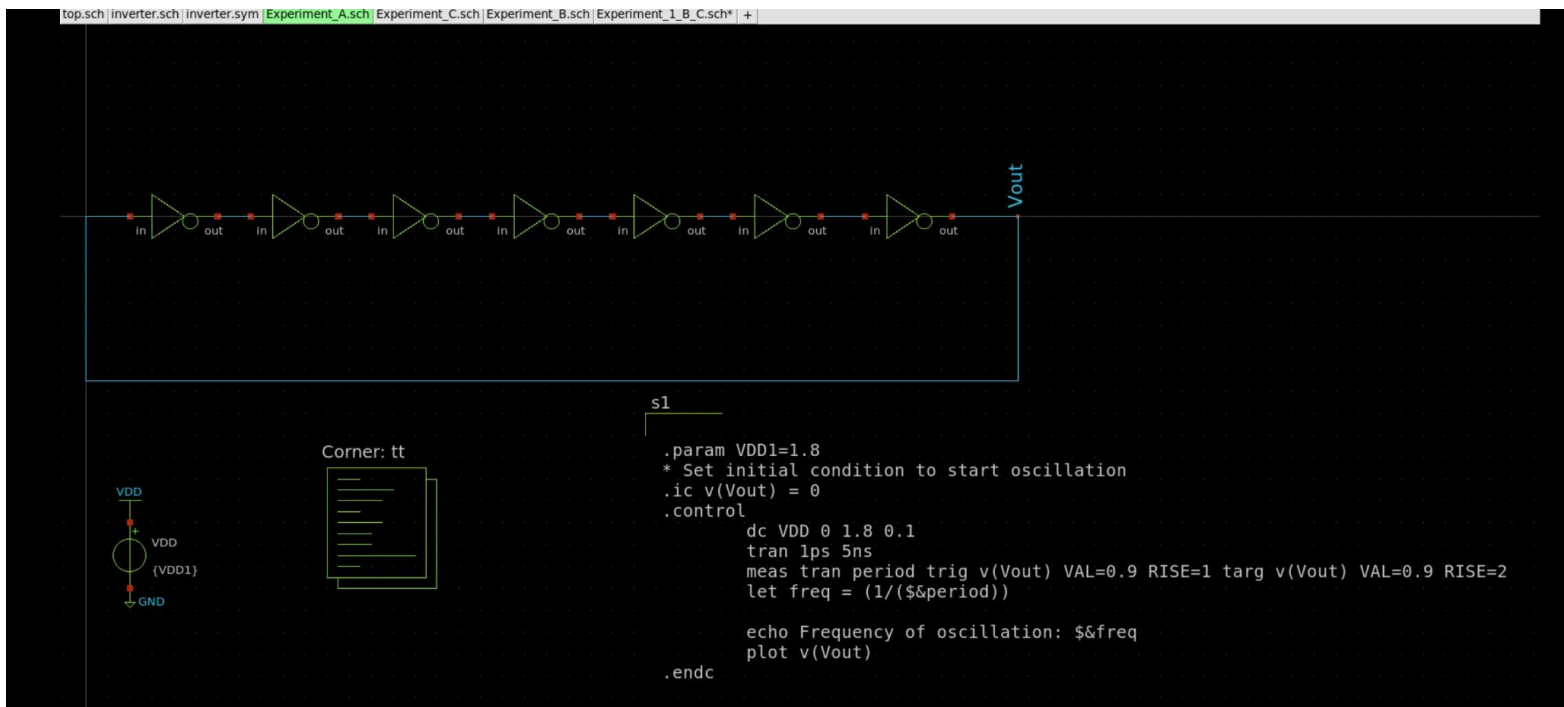
EE5311

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Tutorial - 4
Report

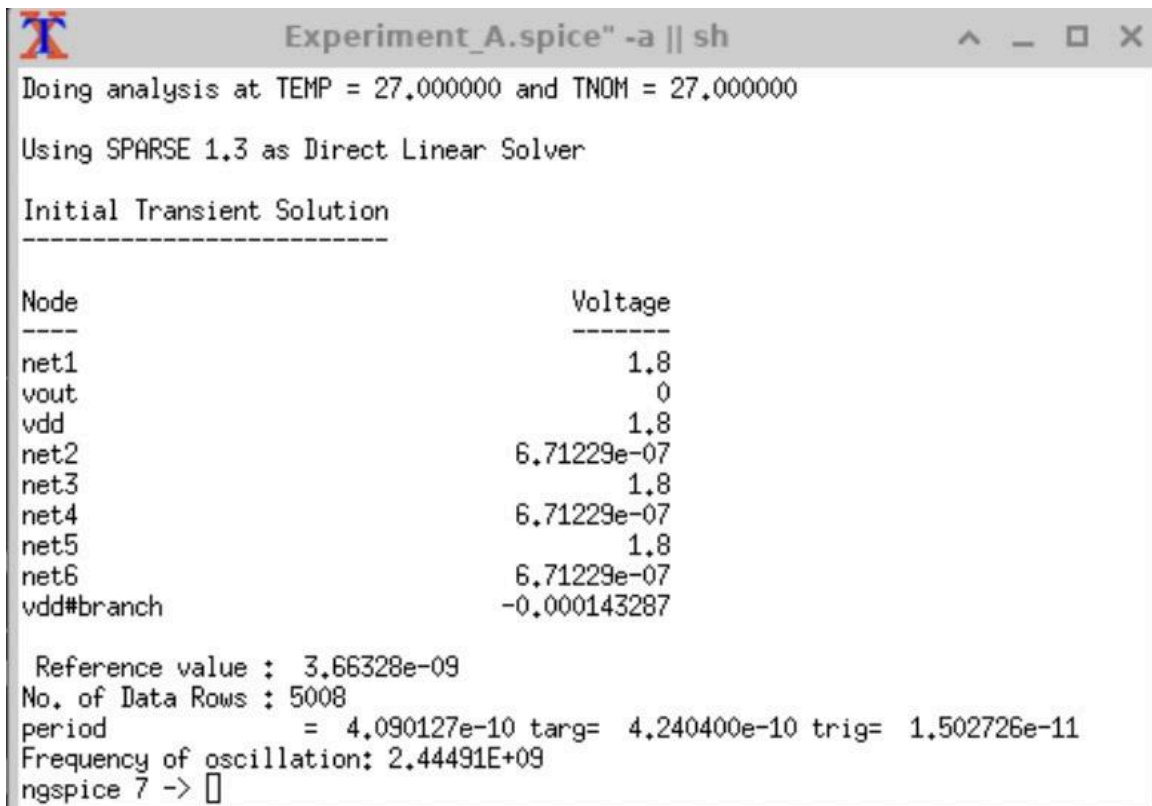
Experiment - 1

Schematic for (A):



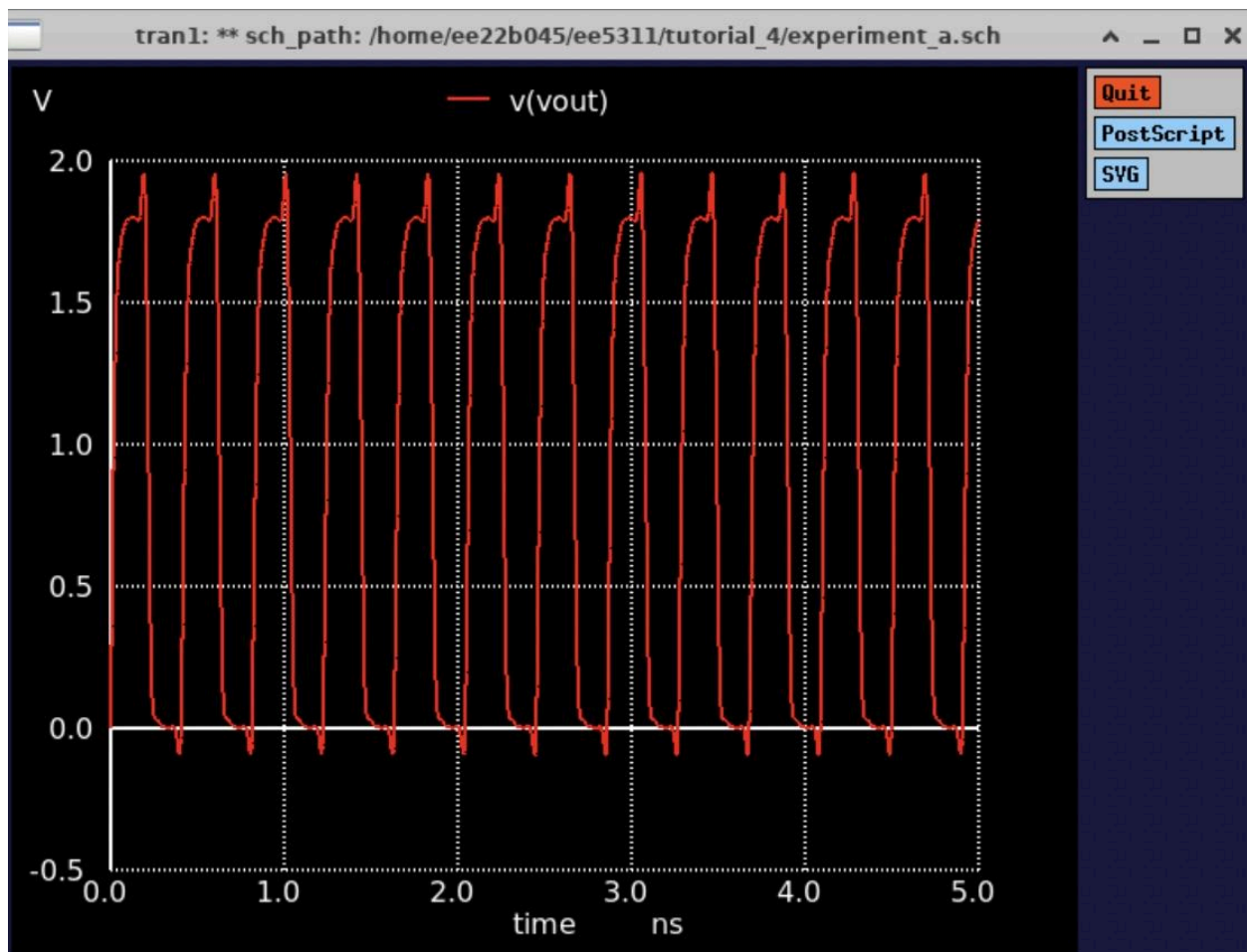
The CMOS inverter with $W_p = 0.84\mu\text{m}$ has the minimum delay

NgSpice response

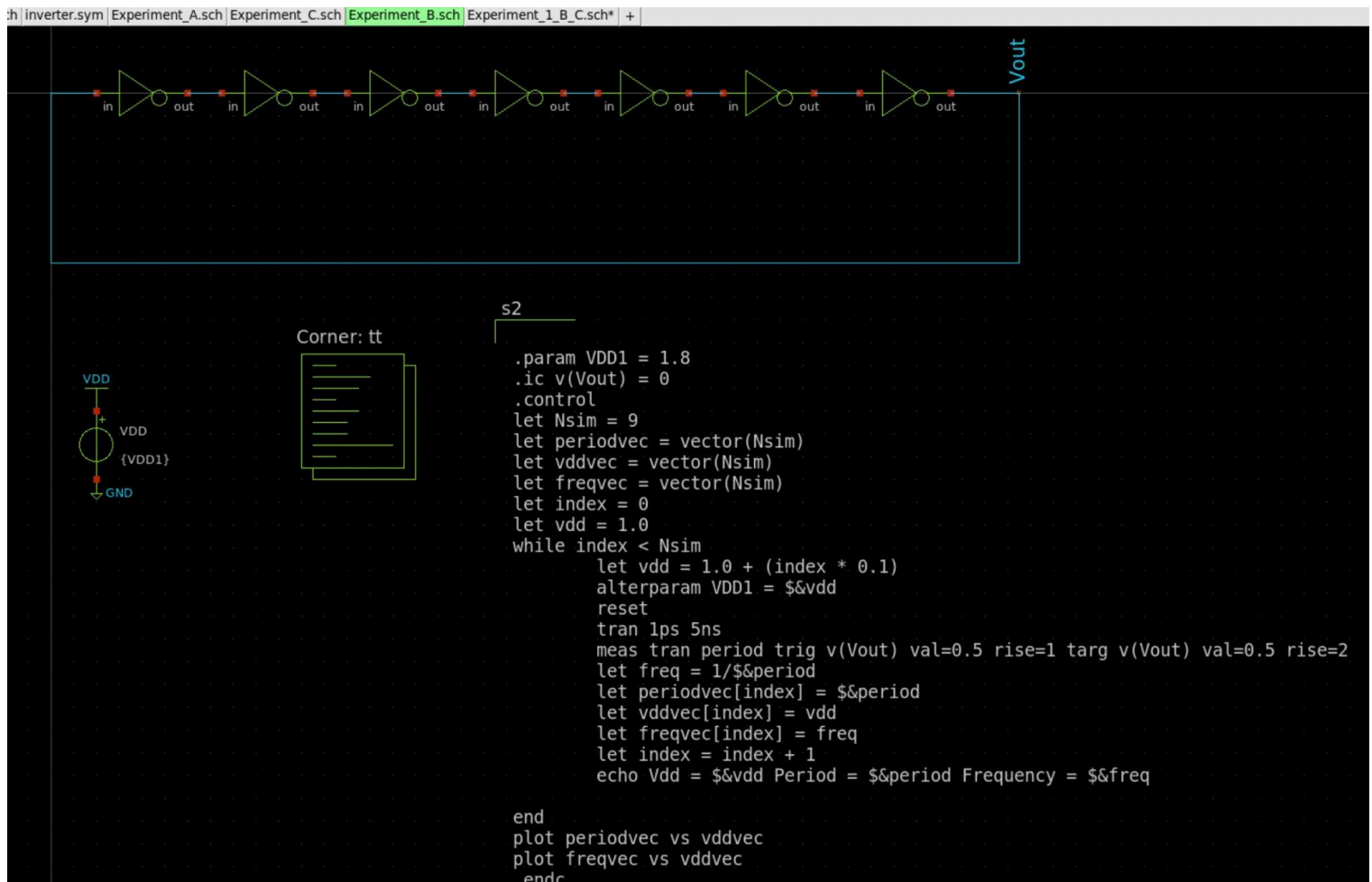


Frequency of Oscillations = 2.449GHz

The below graph Shows the Vout @7th inverter



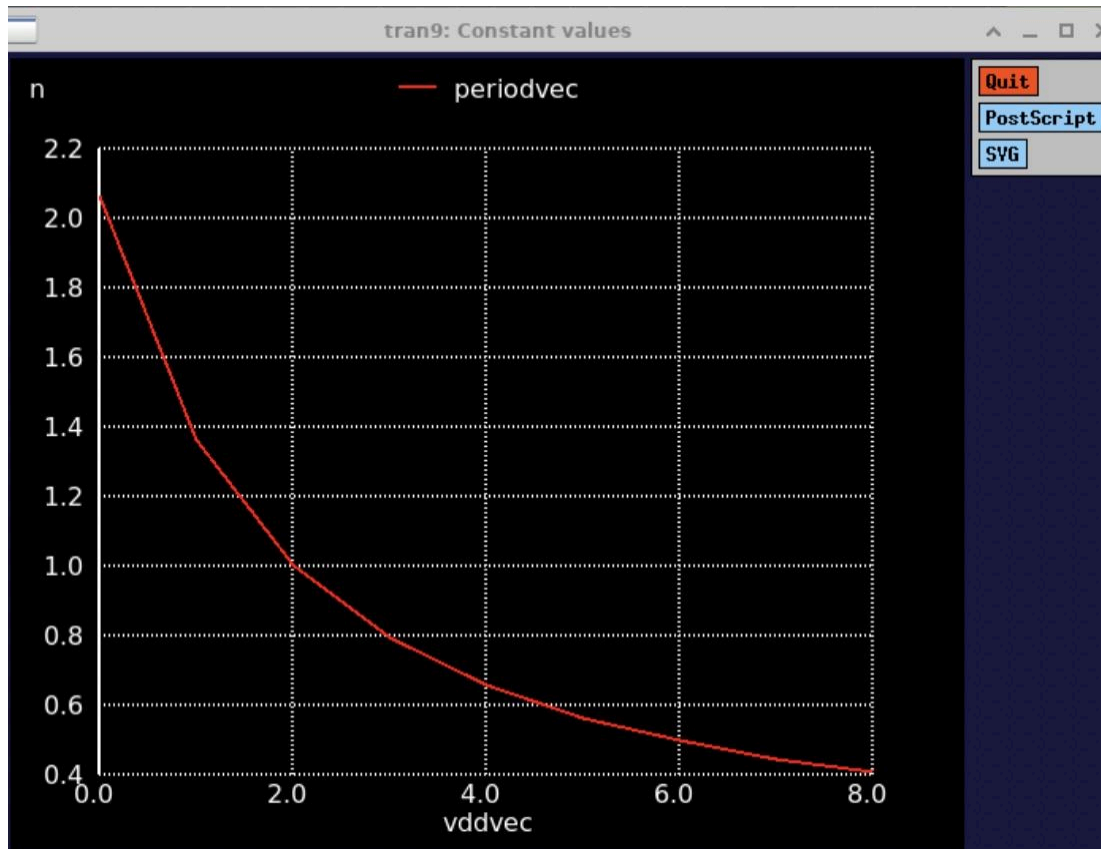
Schematic and code for 7-Inverters(B):



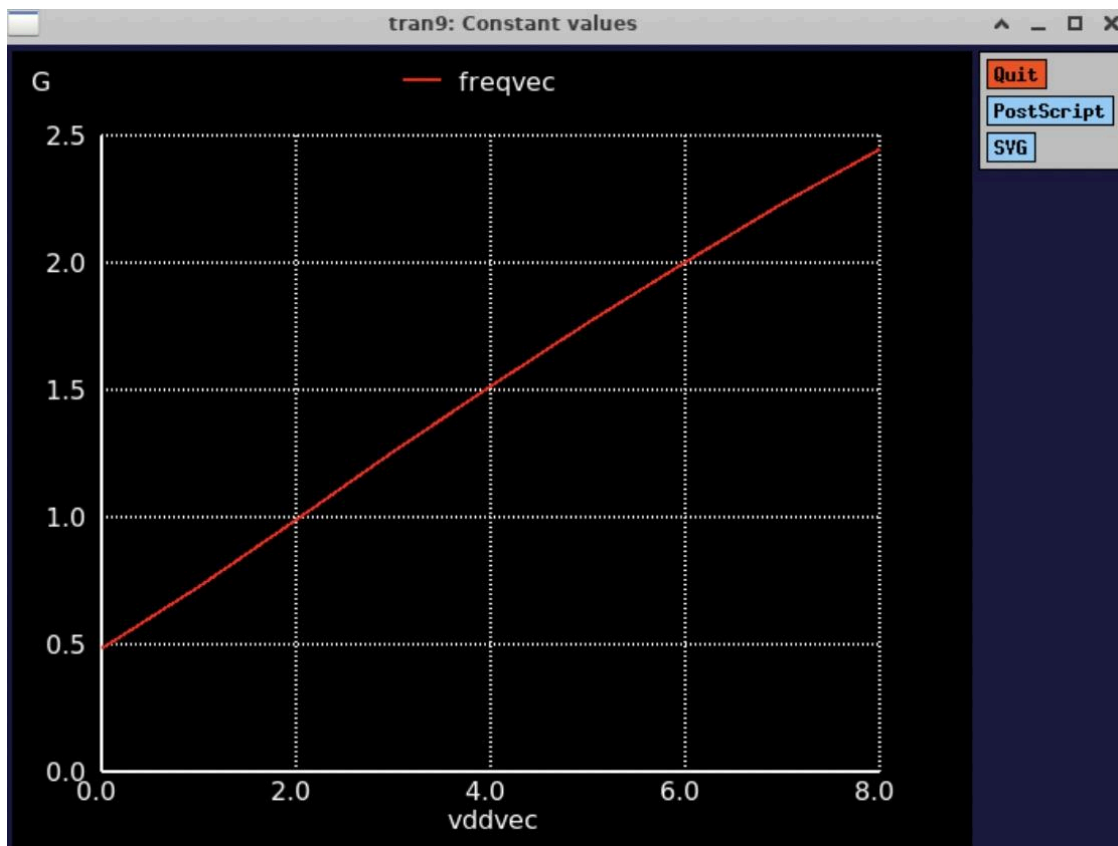
VDD vs Frequency:

1. VDD = 1.0V	;Frequency = 0.484GHz	;Period = 2.064ns
2. VDD = 1.1V	;Frequency = 0.734GHz	;Period = 1.362ns
3. VDD = 1.2V	;Frequency = 0.996GHz	;Period = 1.003ns
4. VDD = 1.3V	;Frequency = 1.259GHz	;Period = 0.793ns
5. VDD = 1.4V	;Frequency = 1.518GHz	;Period = 0.658ns
6. VDD = 1.5V	;Frequency = 1.768GHz	;Period = 0.565ns
7. VDD = 1.6V	;Frequency = 2.008GHz	;Period = 0.498ns
8. VDD = 1.7V	;Frequency = 2.235GHz	;Period = 0.474ns
9. VDD = 1.8V	;Frequency = 2.448GHz	;Period = 0.408ns

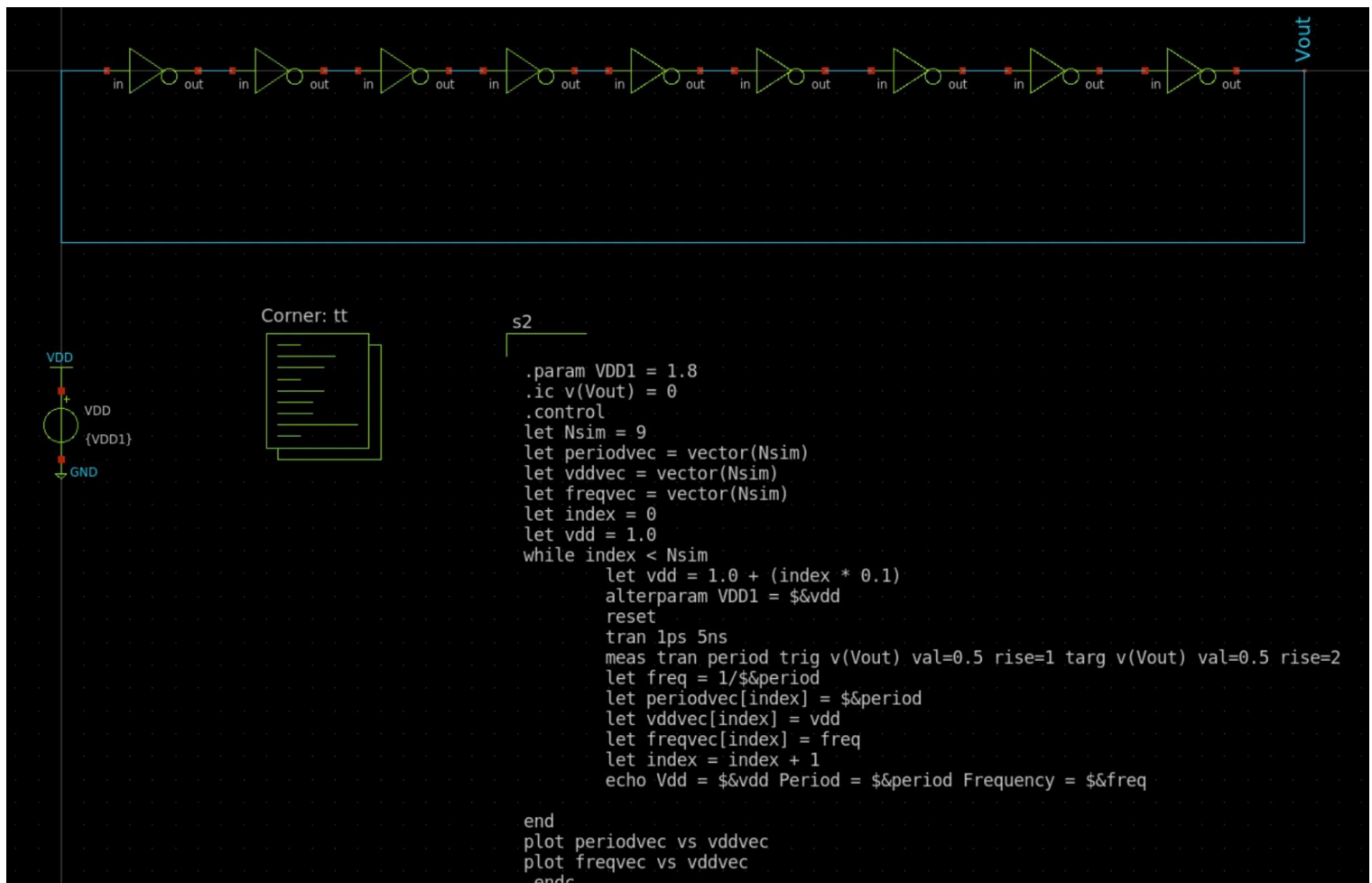
Period vs VDD (from 1.0V to 1.8V)



Frequency vs VDD (from 1.0V to 1.8V)



Schematic and code for 9-Inverters(C):

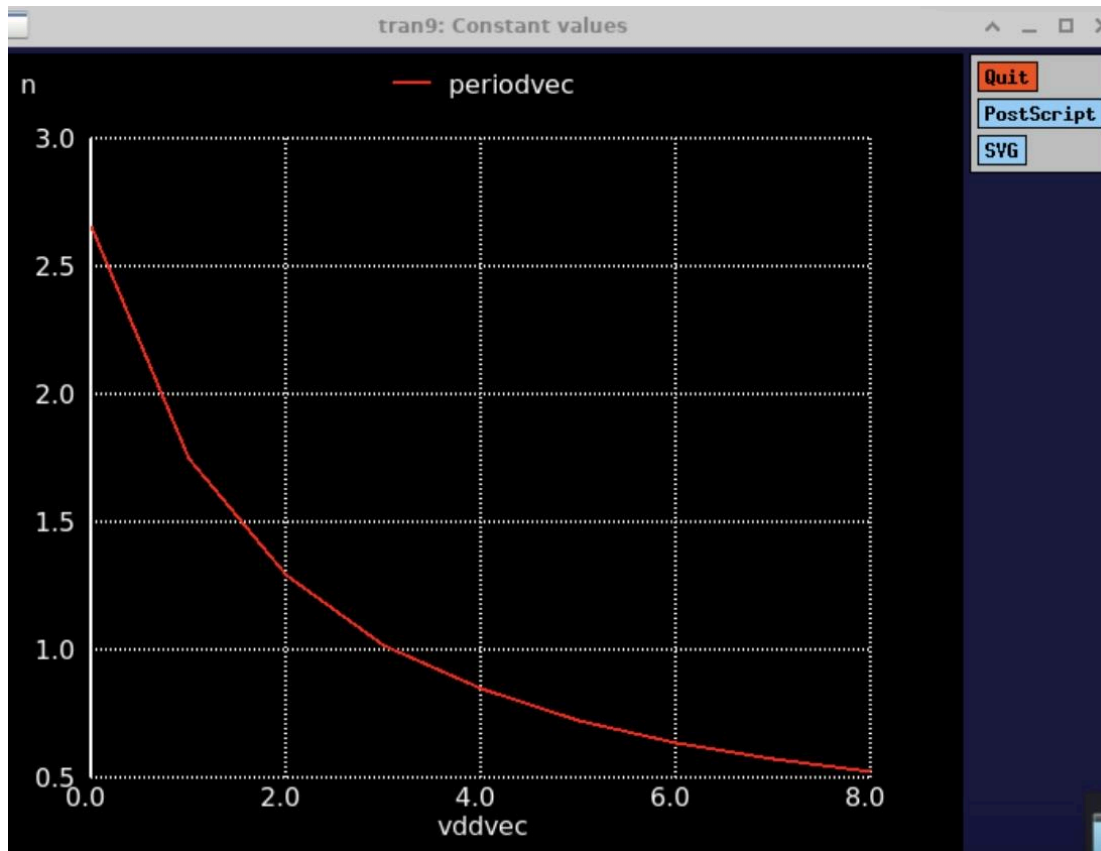


Frequency @VDD = 1.8V is **1.903GHz**

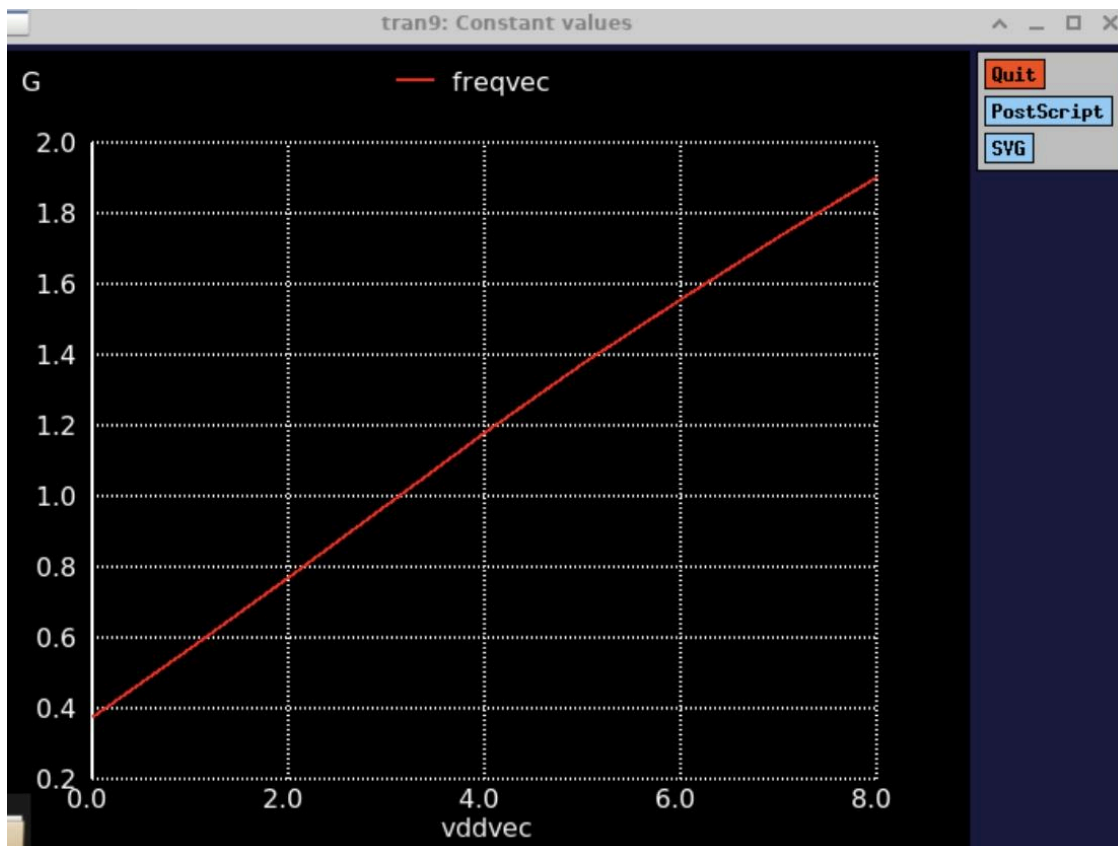
VDD vs Frequency:

- | | | |
|---------------|------------------------------|-------------------|
| 1. VDD = 1.0V | ;Frequency = 0.376GHz | ;Period = 2.654ns |
| 2. VDD = 1.1V | ;Frequency = 0.570GHz | ;Period = 1.751ns |
| 3. VDD = 1.2V | ;Frequency = 0.774GHz | ;Period = 1.290ns |
| 4. VDD = 1.3V | ;Frequency = 0.979GHz | ;Period = 1.020ns |
| 5. VDD = 1.4V | ;Frequency = 1.180GHz | ;Period = 0.846ns |
| 6. VDD = 1.5V | ;Frequency = 1.375GHz | ;Period = 0.727ns |
| 7. VDD = 1.6V | ;Frequency = 1.561GHz | ;Period = 0.640ns |
| 8. VDD = 1.7V | ;Frequency = 1.737GHz | ;Period = 0.575ns |
| 9. VDD = 1.8V | ;Frequency = 1.903GHz | ;Period = 0.525ns |

Period vs VDD (from 1.0V to 1.8V)



Frequency vs VDD (from 1.0V to 1.8V)



- The End -

