Curriculum Vitae

Prof. Rajeev Kumar Ranjan **(Assistant Professor)**
Department of Electronics Engineering
Indian Institute of Technology (ISM), Dhanbad
Dhanbad - 826004, Jharkhand, India
Email: rajeev@iitism.ac.in, rkranjan2k@gmail.com
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Web of Science Researcher ID: F-2448-2019
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Research Interest

Analog and Mixed VLSI Design (CMOS based analog/digital design and different types of challenges and issue of design): Analog Filter, Oscillator, Memristor Circuit, Controllers, Low power temperature Sensor.

Education

Ph.D. (***Specialization*:** Microelectronics and VLSI Design)
Indian Institute of Technology (ISM), Dhanbad India (Oct. 2011 - Nov. 2016)
Thesis title: Design of analog signal processing and generating circuits using current mode building blocks.
Supervisor: Dr. S. K. Paul, Professor, Dept. of ECE, IIT(ISM) Dhanbad

M.Tech. (***Specialization:*** Electronics Design and Technology)
Central University, Tezpur (Assam), India (July 2005 - June 2007)
Thesis title: Full custom IC design to implement cosine function for 2D, DCT targeted to SCL 1.2 µm CMOS foundry
Thesis Place: Central Electronics Engineering Research Institute, Pilani, Rajasthan, India. (July 2006 - June 2007)

B.Tech. (Electronics & Communication Engineering)
Sant Longowal Institute of Engineering and Technology, Longowal, Punjab, India (MHRD Funded Deemed University) (July 2000 - June 2003)

Teaching Experience

1) **North Eastern Regional Institute of Technology, Itanagar, Arunachal Pradesh, India(MHRD Funded Deemed University)**

Designation: Assistant Professor (April, 2007 - July, 2007)

2) **Sant Longowal Institute of Engineering and Technology, Longowal, Punjab, India(MHRD Funded Deemed University)**

Designation: Assistant Professor (Aug, 2008 - Nov, 2010)

3) Indian Institute of Technology (ISM) Dhanbad, India.

Designation: Assistant Professor (Since Nov, 2010 to till date)

Course Taught: Electronics Engineering (Theory and Lab), Analog Integrated Circuit (Theory and Lab), Network Theory and Filter Design (Theory and Lab), Digital Circuit (Theory and Lab), VLSI Design, Current Mode Circuits.

Other Experience

1) Central Electronics Engineering Research Institute, Pilani, Rajasthan, India.

Designation: Project Scientist (July, 2004 – Aug, 2005)

Publications

Types of Research Papers	***Nos.***
International Journals	*23*
International Conferences	*8*
Total Research Papers	*31*

List of International SCI / SCI-Expanded Journals [SELECTED]

International Journals

1. W. Jaikla, F. Khateb, M. Kumngern, T. Kulej, **Rajeev Kumar Ranjan** and P. Suwanjan, "0.5 V Fully Differential Universal Filter Based on Multiple Input OTAs," IEEE Access, DOI: 10.1109/ACCESS.2020.3030239. [Accepted]
2. Pankaj Kumar Sharma, **Rajeev Kumar Ranjan**, F. Khateb and M. Kumngern, "Charged Controlled Mem-Element Emulator and Its Application in a Chaotic System," IEEE Access, vol. 8, pp. 171397-171407, 2020, DOI: 10.1109/ACCESS.2020.3024769.
3. Pushkar Srivastava, R. K. Gupta, R. K. Sharma, and **Rajeev Kumar Ranjan**, "MOS-Only Memristor Emulator," Circuits, Systems, and Signal Processing, vol. 99, no. 1, 2020, DOI: https://doi.org/10.1007/s00034-020-01421-x; Impact Factor: 1.681.
4. Niranjan Raj, **Rajeev Kumar Ranjan,** and Fabian Khateb, "Flux Controlled Memristor Emulator and its Experimental Results," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 4, pp. 1050 – 1061, 2020, DOI: https://doi.org/10.1109/TVLSI.2020.2966292; Impact Factor: 1.946.
5. Vijay Kumar Verma, **Rajeev Kumar Ranjan**, V. Lekshmi, Ankit Kumar Azad, Bhargav Appasani, and Vijay Nath, "A second generation current conveyor based PID controller optimized using a crossover improved genetic algorithm," Microsystem Technologies, vol. 26, pp. 1449–1454, 2020, DOI: https://doi.org/10.1007/s00542-019-04677-9; Impact Factor: 1.737.
6. Fabian Khateb, Tomasz Kulej, Montree Kumngern, Winai Jaikla, and **Rajeev Kumar Ranjan**, "Comparative performance study of multiple-input bulk-driven and multiple-

input bulk-driven quasi-floating-gate DDCCs," International Journal of Electronics and Communication (AEU), Elsevier, vol. 108, pp. 19-28, 2019, DOI: https://doi.org/10.1016/j.aeue.2019.06.003; Impact Factor: 2.924.

7. **Rajeev Kumar Ranjan,** Sagar Surendra, Subrto Raushan, Nishtha Garg, Bharti Kumari, and Fabian Khateb, "High frequency floating memristor emulator and its experimental results," IET Circuits, Devices & Systems, vol. 13, no. 3, pp. 292-302, 2019, DOI: https://doi.org/10.1049/iet-cds.2018.5191; Impact Factor: 1.277.
8. **Rajeev Kumar Ranjan**, Pankaj Kumar Sharma, Sagar, Niranjan Raj, Bharti Kumari, and Fabian Khateb, "Memristor Emulator Circuit Using Multiple-Output OTA and Its Experimental Results," Journal of Circuits, Systems and Computers, vol. 28, no. 10, pp. 1950166, DOI: https://doi.org/10.1142/S0218126619501664; Impact Factor: 0.939.
9. Bhargav Appasani, Pallav Prince, **Rajeev Kumar Ranjan**, Nisha Gupta, and Vijay Kumar Verma, "A Simple Multi-Band Metamaterial Absorber with Combined Polarization Sensitive and Polarization Insensitive Characteristics for Terahertz Applications," Plasmonics, vol. 14, no. 3, pp 737–742, June 2019, DOI: https://doi.org/10.1007/s11468-018-0852-x; Impact Factor: 2.926.
10. Pooja Gupta, Vijay Kumar Verma, **Rajeev Kumar Ranjan**, Bhargav Appasani, Bindu Priyadarshini, and Vijay Nath, "A series expansion method aided design of current mode second-generation current conveyor based active control circuit," Microsystem Technologies, vol. 25, no. 6, pp 2323–2330, June 2019, DOI: https://doi.org/10.1007/s00542-018-4117-6; Impact Factor: 1.513.
11. Prakhar Shrivastava, Sagar Surendra, **Rajeev Kumar Ranjan**, Abhishek Shrivastav, and Bindu Priyadarshini, "PI, PD and PID Controllers Using Single DVCCTA," Iranian Journal of Science and Technology, Transactions of Electrical Engineering, vol. **43**, pp. 673–685, Jan.2019, DOI: https://doi.org/10.1007/s40998-019-00180-z; Impact Factor: 0.657.
12. Pushkar Srivastava, Ravindra Kumar Sharma, and **Rajeev Kumar Ranjan**, "On the realization of current-mode four-quadrant CMOS cuber," Analog Integrated Circuits and Signal Processing, vol. 99, no. 1, pp 47–61, April 2019, DOI: https://doi.org/10.1007/s10470-018-1291-5; Impact Factor: 0.925.
13. Vijay Kumar Verma, **Rajeev Kumar Ranjan**, Pooja Gupta, and Bindu Priyadarshini, "A series expansion method aided design of CCII controller for a TITO system," Microsystem Technologies, vol. 24, no. 9, pp 3843–3849, September 2018, DOI: https://doi.org/10.1007/s00542-018-3869-3; Impact Factor: 1.737.
14. **Rajeev Kumar Ranjan**, and Sajal K. Paul, "Self-generating square/triangular wave and pulse width modulator using a single MO-CCCDTA," Analog Integrated Circuits and Signal Processing, vol. 94, no. 1, pp. 177-193, DOI: https://doi.org/10.1007/s10470-017-1089-x; Impact Factor: 0.925.
15. **Rajeev Kumar Ranjan**, Ankita Sinha, and Sajal K. Paul, "A New Operational Transconductance Amplifier Based Pulse Width Modulator," Proceedings of the National Academy of Sciences, India - Section A, vol. 89, no. 1, pp 51–55, March 2019, DOI: https://doi.org/10.1007/s40010-017-0390-5; Impact Factor: 0.921.
16. **Rajeev Kumar Ranjan**, Nidhi Bhuval, Niranjan Raj, and Fabian Khateb, "Single DVCCTA based high frequency incremental/decremental memristor emulator and its application," International Journal of Electronics and Communication (AEU), Elsevier, vol. 82, pp. 177-192, December 2017, DOI: https://doi.org/10.1016/j.aeue.2017.07.039; Impact Factor: 2.924.
17. **Rajeev Kumar Ranjan**, Kaushik Mazumdar, Ratandeep Pal, and Satish Chandra, "Generation of square and triangular wave with independently controllable frequency and

amplitude using OTAs only and its application in PWM," Analog Integrated Circuit and Signal Processing. Springer, Vol. 91 pp. 1-13, 2017, DOI: https://doi.org/10.1007/s10470-017-0971-x; Impact Factor: 0.925.

18. **Rajeev Kumar Ranjan**, Nishtha Rani, Sajal k. Paul and Gaurav Kanyal, "Single CCTA based high frequency floating and grounded type of incremental/decremental memristor emulator," Microelectronics Journal, Elsevier. vol. 60, pp. 119-128, 2017, DOI: https://doi.org/10.1016/j.mejo.2016.12.004; Impact Factor: 1.405.
19. Kaushik Mazumdar, **Rajeev Kumar Ranjan**, Ravi Shankar, Bindu Priyadarshini, and Aniruddha Ghosal, "Modern comparative approach for carrier transport in InAlN/AlN superlattice device with characteristics and modelling using nitride (^{14}N,^{15}N) isotopes," Superlattices and Microstructures, Elsevier. vol. 103, pp. 190-194, 2017, DOI: https://doi.org/10.1016/j.spmi.2017.01.008; Impact Factor: 2.12.
20. **Rajeev Kumar Ranjan**, Chandan Kumar Choubey, Bal Chander Nagar, and Sajal K. Paul, "Comb Filter for Elimination of Unwanted Power Line Interference in Biomedical Signal," Journal of Circuits, Systems, and Computers (JCSC), vol. 25, no. 6, pp. 1650052-14, 2016, DOI: https://doi.org/10.1142/S0218126616500523; Impact Factor: 1.363.
21. Kaushik Mazumdar, **Rajeev Kumar Ranjan**, Ravi Shankar, Ahna Sharan, Bindu Priyadarshini, Mainak Kundu, and Aniruddha Ghosal, "Analysis of Electron Transport in AlGaN/GaN Superlattice HEMTs for Isotopes ^{14}N and ^{15}N," Superlattices and Microstructures, Elsevier. vol. 100, pp. 983-987, 2016, DOI: https://doi.org/10.1016/j.spmi.2016.10.065; Impact Factor: 2.12.
22. **Rajeev Kumar Ranjan**, Kundan Kumar, Nishtha Rani, Sajal K. Paul, and Shyam Akashe, "A Power Line Filter Circuit Design for Biomedical Applications," Journal of Computational and Theoretical Nanoscience, American Scientific Publishers. vol. 13, no. 5, pp. 3345-3351, 2016, DOI: https://doi.org/10.1166/jctn.2016.4997; Impact Factor: 1.666.
23. **Rajeev Kumar Ranjan**, Surya Prasanna Yalla, Shubham Sorya, and Sajal K. Paul, "Active Comb Filter using Operational Transconductance Amplifier," Active and Passive Electronic Components, Hindawi. vol. 2014, 6 pages, DOI: https://doi.org/10.1155/2014/587932; Impact Factor: 0.72.
24. Mourina Ghosh, Sajal K. Paul, **Rajeev Kumar Ranjan,** and Ashish Ranjan, "Third-order universal filter using single Operational Transresistance Amplifier," Journal of Engineering, Hindawi. vol. 2013, 6 pages, DOI: https://doi.org/10.1155/2013/317296.

International Conferences

1. N. Raj, S. Chandra, B. Priyadarshani, and **Rajeev Kumar Ranjan**, "Multiple output current-controlled current conveyor transconductance amplifier using BiCMOS for analog signal processing," in 4th International Conference on Recent Advances in Information Technology (RAIT), 15-17 March 2018 Dhanbad, India, DOI: https://doi.org/10.1109/RAIT.2018.8388989.
2. Swati Kumari, Pallav Prince,Vijay Kumar Verma, Bhargav Appasani, and **Rajeev Kumar Ranjan**, "GA Based Design of Current Conveyor PLD Controller for the Speed Control of BLDC Motor," in 4th International Conference on Computational Intelligence & Communication Technology (CICT-2018), 9-10 Feb. 2018, Ghaziabad, India, DOI: https://doi.org/10.1109/CIACT.2018.8480149.
3. Sheetal Tewary, Vijay Kumar Verma, Bhargav Appasani, Pooja Guptal, and **Rajeev Kumar Ranjan**, "Design of CCII PID Controller for the Control of Glucose Blood Level Using GA" in 4th International Conference on Computational Intelligence &

Communication Technology (CICT-2018), 9-10 Feb. 2018, Ghaziabad, India, DOI: https://doi.org/10.1109/CIACT.2018.8480402.

4. Vijay Kumar Verma, Bhargav Appasani, Pooja Gupta, and **Rajeev Kumar Ranjan**, "GA based design of CCII PID controller for an inverted pendulum system," in IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-2017), 21-22 Sept. 2017, Chennai, India, DOI: 10.1109/ICPCSI.2017.8392212.
5. Pooja Gupta, Bhargav Appasani, Vijay Verma, and **Rajeev Kumar Ranjan**, "PSO Based CCII PID Controller for a Continuous Stirred Tank Reactor System," in IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-2017), 21-22 Sept. 2017 Chennai, India, DOI: https://doi.org/10.1109/ICPCSI.2017.8392227.
6. Nishtha Rani, **Rajeev Kumar Ranjan**, Ratnadeep Pal, and Sajal K. Paul, "Programmable And Electronically Tunable Voltage-Mode Universal Biquadratic Filter Based On Simple CMOS OTA," in Proceeding of IEEE International Conference on Devices, Circuits and Systems (ICDCS-2016), 3-5 March 2016, Coimbatore, India, DOI: https://doi.org/10.1109/ICDCSyst.2016.7570623.
7. **Rajeev Kumar Ranjan**, Y. S. Prasanna Kumar, S. Sorya, Sajal K. Paul, and M. Ghosh, "Efficient Active Filter for filtering of harmonics in biomedical signal," in International Conference. BEATS-2014, UIET, Chandigarh (India), February, 14-15.
8. Mourina Ghosh, **Rajeev Kumar Ranjan**, and Sajal K. Paul, "Universal filter using OTRA," in Proceeding of IEEE, International Conference CODEC- 2012, December 17-19, Kolkata, India, DOI: https://doi.org/10.1109/CODEC.2012.6509217.

Sponsored Research Project and consultancy

S. No.	*Title of Project*	*Authority*	*Funding Agency & Project No.*	*Amount of Grant (in INR)*	*Month/year of Starting*	*Status*
1.	Design of new low power low voltage and high bandwidth Current Mode Building Block (CMBB) and its application in analog signal processing and signal generating circuits.	Principal Investigator	Minor Research Project, TEQIP-II	2L	20-01-2017	Completed
2.	Quotation for testing of LED Street Light	Principal Investigator	Office of the Dy. Commissioner Dhanbad & CONS/3508/2017-2018	17,400.00	2017-2018	Completed
3.	Auto irrigation and soil monitoring system for COVID-19 migrants Engagement.	Principal Investigator	IEEE/2020-2021/718/ECE	Initial Fund : 3 L	15-07-2020	Ongoing
4.	FIST-2019 Project of Department of Electronics Engineering	Member of project (VLSI implementation group)	Department of Science and Technology (DST), Government of India & TPN-31665	190 L	07/01/2020	Ongoing

5.	Memristor Based Biosensor Design For COVID-19 *{Ministry of Human Resource and Development (Shastri Institutional Collaborative Research Grant)}*	Principal Investigator	MHRD(SICRG)/ 2020-2021/740/ECE	10,0000.00	2020-2022	Ongoing
5.	Determination of 90W street light parameters.	Principal Investigator	Dhanbad Municipal Corporation & TEST/5014/2018-2019	59,322.00	2018-2019	Ongoing
6.	Determination of 120W street light parameters.	Principal Investigator	Dhanbad Municipal Corporation & TEST/5013/2018-2019	84,746.00	2018-2019	Ongoing

Outreach Programme:

S. No.	***Title of Course***	***Authority***	***Department***	***Amount of Grant (in INR)***	***Month/year of Starting***	***Status***
1.	Advanced Analog Signal processing and Generating Circuits.	Co-Consultant	Department of Electronics and Communication IIT(ISM) Dhanbad	0.48 L	2014	Completed
2.	Current mode Analog Circuits	Co-Consultant	Department of Electronics and Communication IIT(ISM) Dhanbad	0.70 L	2013	Completed
3.	Advance Analog Circuits using Current Mode Building Blocks	Co-Consultant	Department of Electronics and Communication IIT(ISM) Dhanbad	1 L	2015	Completed

Ph.D. Student Supervision

1.	Name & Adm. No.	PUSHKAR SRIVASTAVA (17DP000209)
	Date of Registration & Status	2017, Ongoing
	Proposed Thesis Title	Low voltage low power mixed signal circuit design.
2.	Name & Adm. No.	POOJA GUPTA (17DP000214)
	Date of Registration & Status	2017, Ongoing
	Proposed Thesis Title	Realization of some novel active circuit using current mode.
3.	Name & Adm. No.	VIJAY KUMAR VERMA (17DP000215)
	Date of Registration & Status	2016, Ongoing

	Proposed Thesis Title	Realization of novel active control circuits using current mode.
4.	Name & Adm. No.	SOMENATH DUTTA (17DP000255)
	Date of Registration & Status	2016, Ongoing
	Proposed Thesis Title	Design of Analog Signal Processing Circuits using Analog Building Blocks.
5.	Name & Adm. No.	NIRANJAN RAJ (17DR000367)
	Date of Registration & Status	2017, Ongoing
	Proposed Thesis Title	Design of analog signal processing circuits using current mode approach.
6.	Name & Adm. No.	SAGAR(17DR000477)
	Date of Registration & Status	2017, Ongoing
	Proposed Thesis Title	Design of CMOS based low-voltage analog and mixed-signal processing using current mode approach.
7.	Name & Adm. No.	PANKAJ KUMAR SHARMA(17DR000641)
	Date of Registration & Status	2017, Ongoing
	Proposed Thesis Title	CMOS based low power analog and mixed signal-processing circuits: A current mode approach.
8.	Name & Adm. No.	JAGVEER SINGH VERMA (18DP0002)
	Date of Registration & Status	2018, Ongoing
	Proposed Thesis Title	Low Power Analog Integrated Circuits Design.
9.	Name & Adm. No.	SADAF TASNEEM(18DR0119)
	Date of Registration & Status	2018, Ongoing
	Proposed Thesis Title	Design of low-voltage, low-power current mode analog building blocks and application in signal processing circuit.
10.	Name & Adm. No.	PRASHANT KUMAR (19DR0108)
	Date of Registration & Status	2019, Ongoing
	Proposed Thesis Title	Design and development of analog signal processing circuit using current mode building blocks.

Served as a Reviewer

- Microelectronics Journal, Elsevier
- Microsystem Technologies
- Analog Integrated Circuits and Signal Processing
- AEÜ - International Journal of Electronics and Communications
- Circuits, Systems, and Signal Processing
- IET Circuits, Devices & Systems
- Journal of Circuits, Systems and Computers
- Iranian Journal of Science and Technology, Transactions of Electrical Engineering
- IEEE Transactions on Very Large Scale Integration (VLSI) Systems

Membership of Professional Bodies

- Member IEEE. (Sept. 2016- till date)

Administrative Responsibilities at IIT(ISM) Dhanbad

- Member of DFSC of Electrical Engineering, IIT(ISM), (Jan. 2019 – Jan 2020)
- Faculty Advisor of B.Tech ECE, IIT(ISM) Dhanbad (Aug. 2019 - Till Date)
- Member of the review selection Interview Board of IIT(ISM) JRF (Phase - I, 2017-18) of Electrical Engineering Department.
- Member of Centre of Societal Mission (CSM) (May 2017 - Till date)
- Warden. (2017 – Till Date)
- Member of the Selection Interview Board of IIT(ISM) JRF (Phase - I, 2018-19) of Electronics Engineering Department.
- Member of the Selection Interview Board of IIT(ISM) JRF (Phase - I, 2017-18) of Electrical Engineering Department.
- Member of the Selection Interview Board of IIT(ISM) JRF (Phase - II, 2016-17) of Electronics Engineering Department.
- Member of the Selection Interview Board of IIT(ISM) JRF (Phase - I, 2016-17) of Electronics Engineering Department.
- Paper Setter for ISM EE (Entrance Exam) 2016 of M.Tech. for Electronics and Communication Engineering Programme.
- Tabulator of the Semester Examination for 2017-18 session.
- FIC Departmental time-table for 2016-17 session.

Short Term Courses/Workshops/Conferences/Meetings Organized

- Member of Organizing Committee: International Conference of Microwave and Photonics (ICMAP) - 2015.
- Member of Organizing Committee: International Conference of Microwave and Photonics (ICMAP) - 2013.
- Served as a subject expert for the Board of Course Studies (BOCS) meeting of B.Tech Programme held at BIT Sindri. [24-06-2019]
- External examiner for the viva-voce of "VLSI Lab & GP" of B.Tech in Department of Electronics and Communication at BIT Sindri. [22-12-2018]

Conferences/Seminar Attended

1. 4th International Conference on Recent Advances in Information Technology (RAIT), March 15-17, 2018, Dhanbad, India.
2. 4th International Conference on Computational Intelligence & Communication Technology (CICT-2018), 9-10 Feb. 2018, Ghaziabad, India.
3. IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI-2017), 21-22 Sept. 2017, Chennai, India.
4. IEEE International Conference on Devices, Circuits and Systems (ICDCS-2016), 3-5 March 2016, Coimbatore, India.
5. International Conference BEATS-2014, February 14-15, 2014, UIET, Chandigarh (India).
6. IEEE, International Conference CODEC- 2012, December 17-19, Kolkata, India.
7. 1st International Conference on Recent Advances in Information Technology (RAIT), March 15-17, 2012, Dhanbad, India.
8. National Seminar on "Renewable Energy Technology: Issues & Prospects" NIRJULI, Itanagar, India during September 24-25, 2010.

Workshop / Tutorials/STC Attended

1. Workshop on "Advance in Device, Communication and IT" organized by the Department of electronics and Communication Engineering, NERIST, Nirjuli (Itanagar), India. [July 16-18, 2007]
2. Short term course on "Winter School on VLSI Design" at BIT Mesra, Ranchi India. [December 26-30, 2011]
3. Short term training program on "Wireless and Wi-Max Issues: Present Scenario" organized by the Department of Computer Science & Engineering, SLIET, Longowal, Punjab, India. [July 5-16, 2010]
4. Staff Development Programme on "Managerial and Communicative sills in the Era of Globalization" organized by Department of EDP, SLIET, Longowal, Punjab, India. [July 21-31, 2009]
5. Workshop on "Application of Simulators in Photonics, Electronics and Communication Technology (ASPECT 2013)" at Institute of Radio Physics & Electronics, University of Calcutta, Kolkata, India. [March 11-15, 2013]
6. Workshop on "Internet of Things" organized by Department of Electronics and Communication Engineering, BIT Sindri. [October 14-18, 2019]