TEXAS INSTRUMENTS

CSD18531Q5A

SLPS321E – JUNE 2012 – REVISED AUGUST 2015

CSD18531Q5A 60 V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5 mm × 6 mm Plastic Package

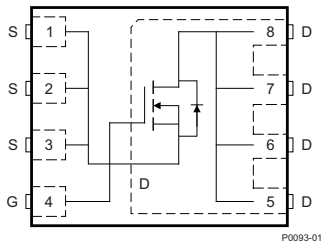
2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Battery Motor Control

3 Description

This 60-V, 3.5-mΩ, 5 mm × 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

TOP VIEW



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-source voltage	60		V
Q_g	Gate charge total (10 V)	36		nC
Q_{gd}	Gate charge gate-to-drain	5.9		nC
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V	4.4	mΩ
		V_{GS} = 10 V	3.5	mΩ
$V_{GS(th)}$	Threshold voltage	1.8		V

Ordering Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18531Q5A	2500	13-Inch Reel	SON 5 mm × 6 mm Plastic Package	Tape and Reel
CSD18531Q5AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

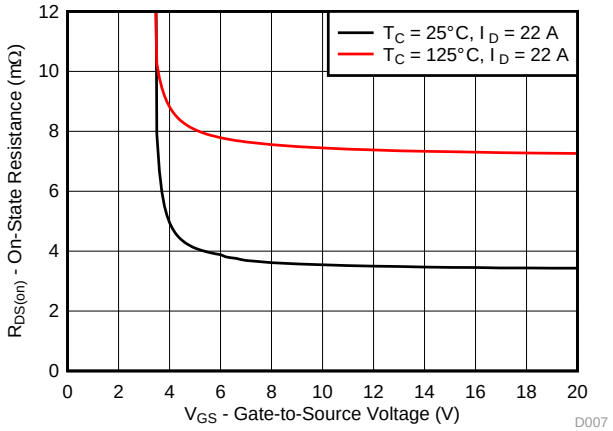
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-source voltage	60	V
V_{GS}	Gate-to-source voltage	±20	V
I_D	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), T_C = 25°C	134	
	Continuous drain current (1)	19	
I_{DM}	Pulsed drain current (2)	370	A
P_D	Power dissipation(1)	3.1	W
	Power dissipation, T_C = 25°C	156	
T_J	Operating junction	–55 to 150	°C
T_{stg}	Storage temperature	–55 to 150	°C
E_{AS}	Avalanche energy, single pulse I_D = 67 A, L = 0.1 mH, R_G = 25 Ω	224	mJ

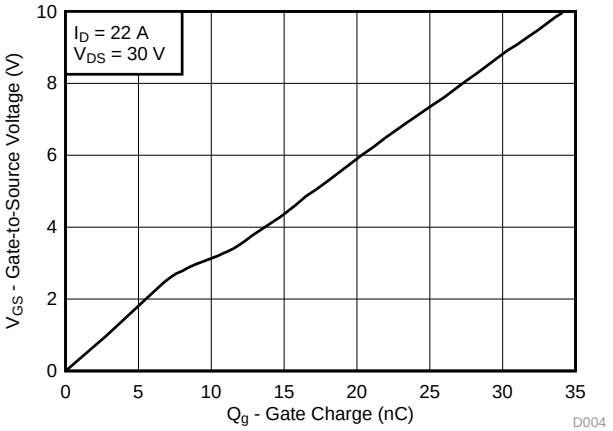
(1) Typical $R_{\theta JA}$ = 40°C/W on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1°C/W, pulse duration ≤100 µs, duty cycle ≤1%

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (May 2015) to Revision E — **Page**

- Corrected device size in description from m to mm. ... 1
- Corrected package type to SON ... 1

Changes from Revision C (March 2015) to Revision D — **Page**

- Added *Community Resources* ... 7

Changes from Revision B (October 2012) to Revision C — **Page**

- Added part number to title ... 1
- Changed Q_g value to 36 nC, measured at 10 V ... 1
- Added 7" reel to Ordering Information ... 1
- Increase max pulsed current to 370 A ... 1
- Added line for max power dissipation with the case temperature held to 25°C ... 1
- Updated pulsed current conditions ... 1
- Updated Figure 1 to show $Z_{\theta JC}$ curves ... 4
- Updated Figure 10 ... 6
- Updated Figure 12 ... 6

Changes from Revision A (June 2012) to Revision B — **Page**

- Changed the Transconductance TYP value From: 177 S To: 128 S. ... 3
- Changed the Turn On and Turn Off Delay Time, Rise and Fall Time Test Conditions From: I_{DS} = 22 A, R_G = 2 Ω To: I_{DS} = 22 A, R_G = 0 Ω ... 3
- Changed the Q_{rr} Reverse Recovery Charge TYP value From: 68 nC To: 100 nC ... 3

Changes from Original (June 2012) to Revision A — **Page**

- Added T_A = 25°C to the Product Summary table ... 1

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

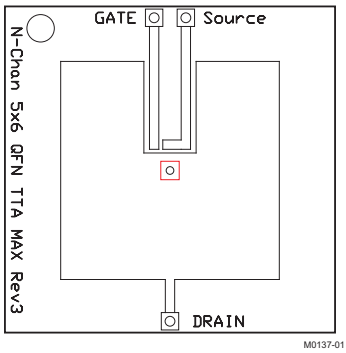
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.5	1.8	2.3	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 4.5 V, I_D = 22 A		4.4	5.8	mΩ
		V_{GS} = 10 V, I_D = 22 A		3.5	4.6	mΩ
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 22 A		128		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		3200	3840	pF
C_{oss}	Output capacitance			380	456	pF
C_{rss}	Reverse transfer capacitance			11	14	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 30 V, I_D = 22 A		18	22	nC
Q_g	Gate charge total (10 V)			36	43	nC
Q_{gd}	Gate charge gate-to-drain			5.9		nC
Q_{gs}	Gate charge gate-to-source			6.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			5.2		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		32		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 22 A, R_G = 0 Ω		4.4		ns
t_r	Rise time			7.8		ns
$t_{d(off)}$	Turn off delay time			20		ns
t_f	Fall time			2.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 22 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 30 V, I_F = 22 A, di/dt = 300 A/µs		100		nC
t_{rr}	Reverse recovery time			40		ns

5.2 Thermal Information

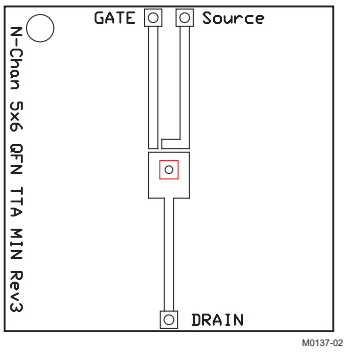
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			1.0	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

5.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

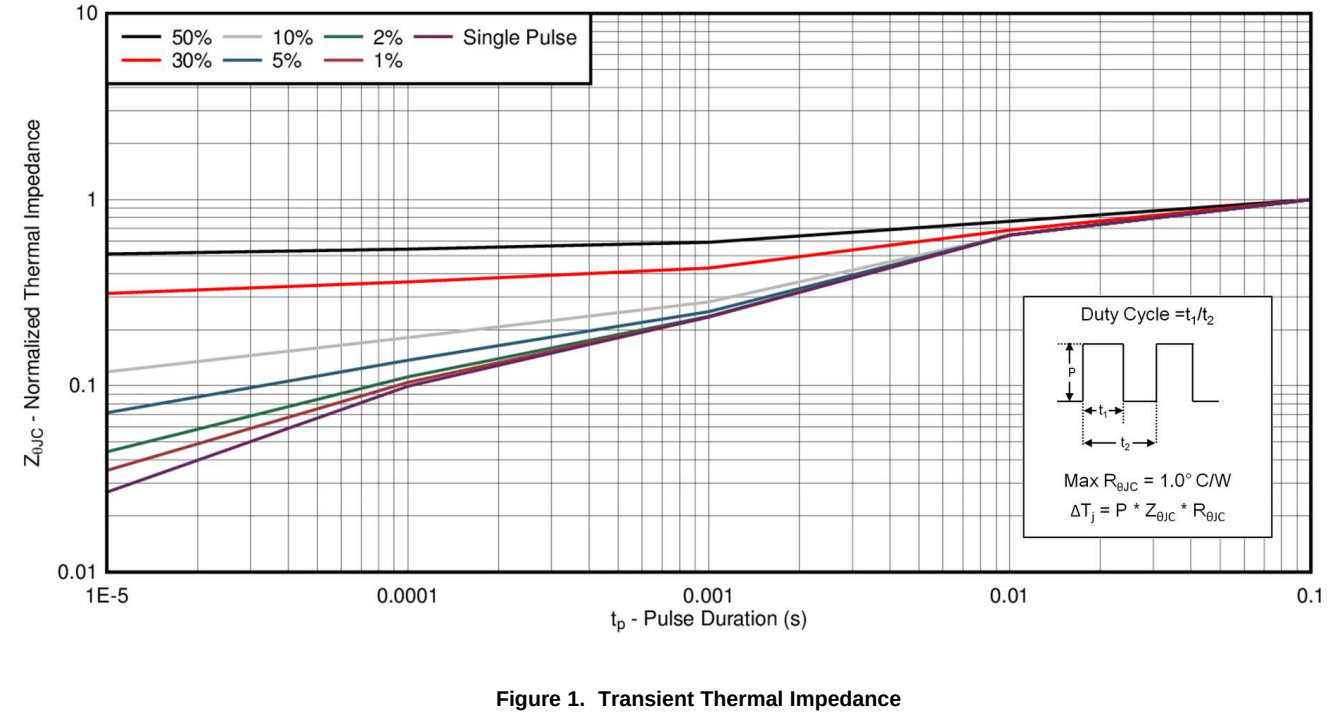


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

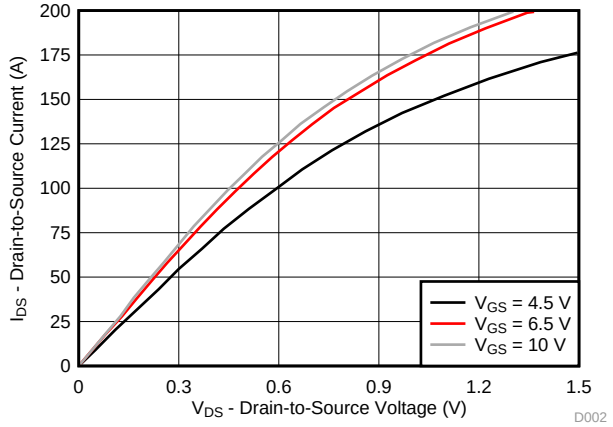


Figure 2. Saturation Characteristics

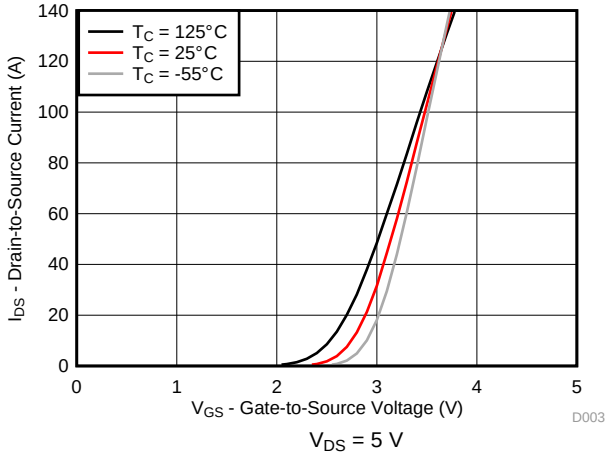


Figure 3. Transfer Characteristics

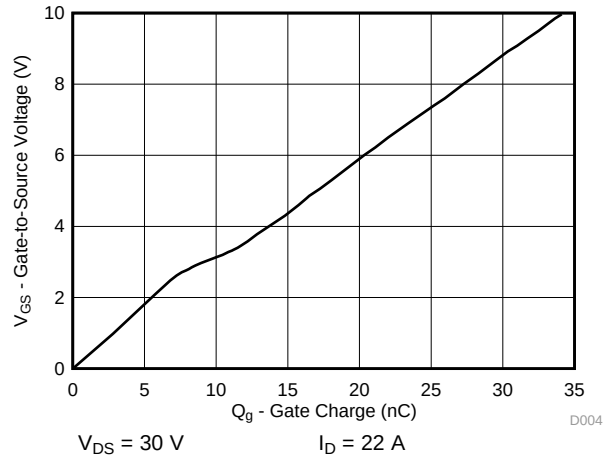


Figure 4. Gate Charge

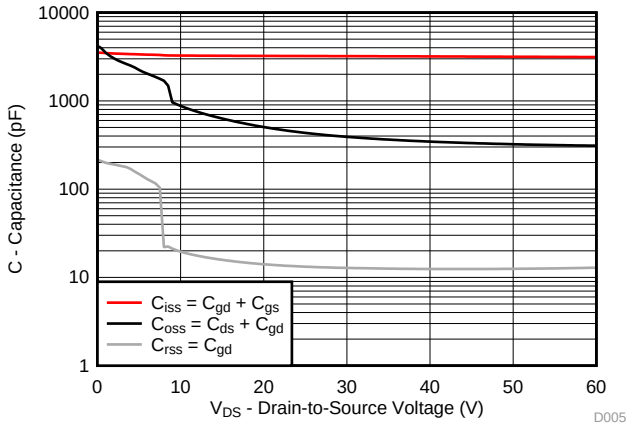


Figure 5. Capacitance

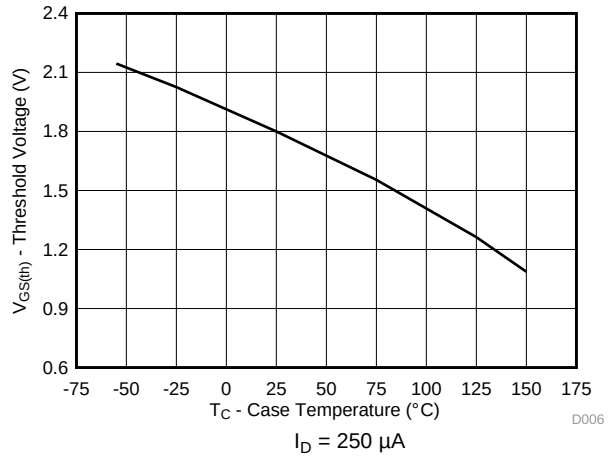


Figure 6. Threshold Voltage vs Temperature

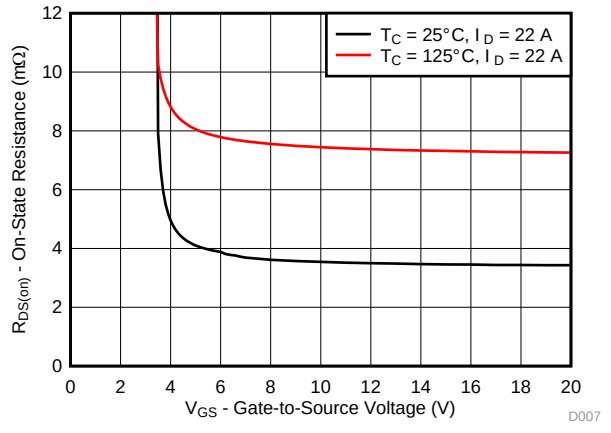


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

(T_A = 25°C unless otherwise stated)

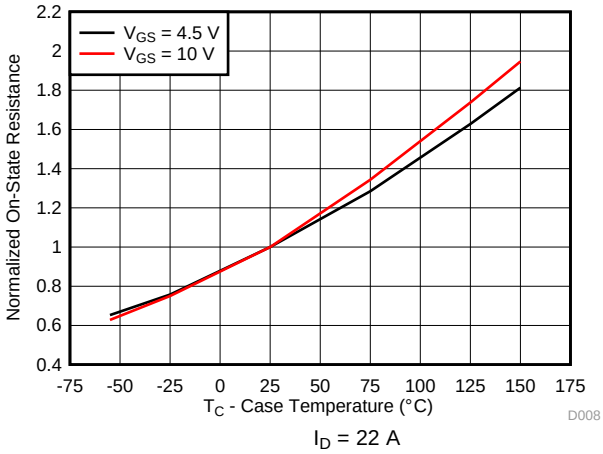


Figure 8. Normalized On-State Resistance vs Temperature

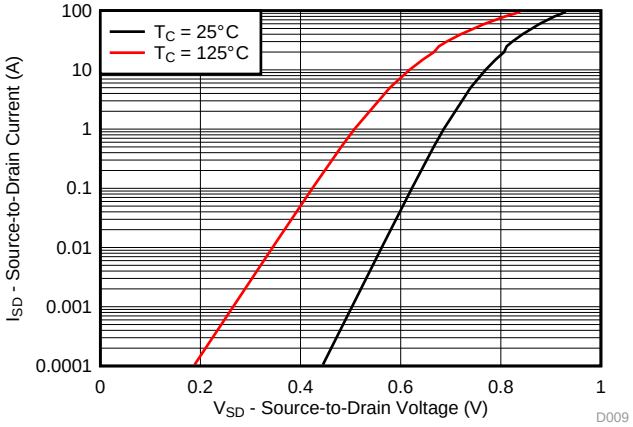


Figure 9. Typical Diode Forward Voltage

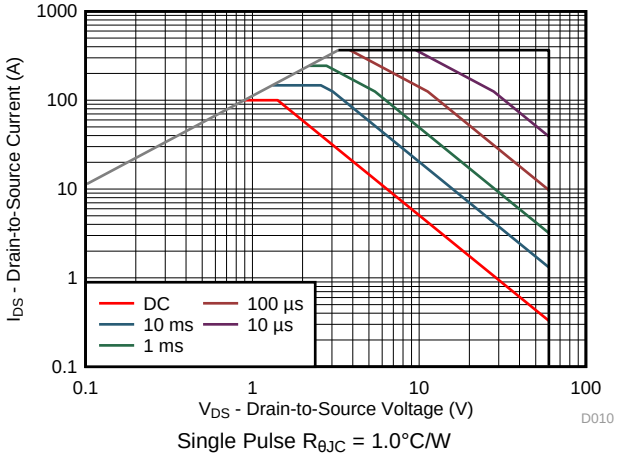


Figure 10. Maximum Safe Operating Area

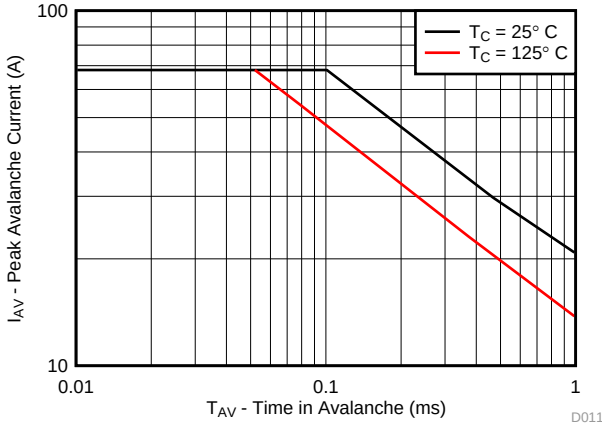


Figure 11. Single Pulse Unclamped Inductive Switching

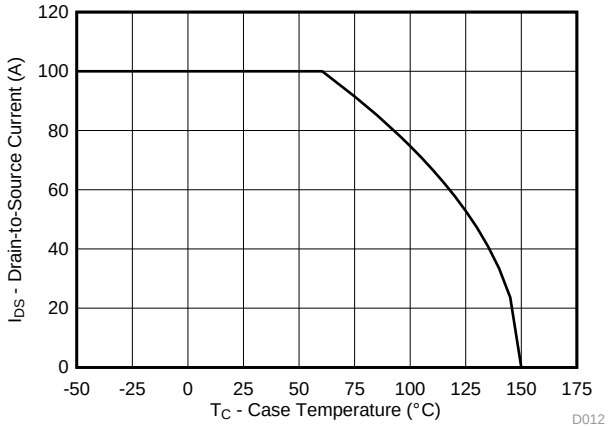


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

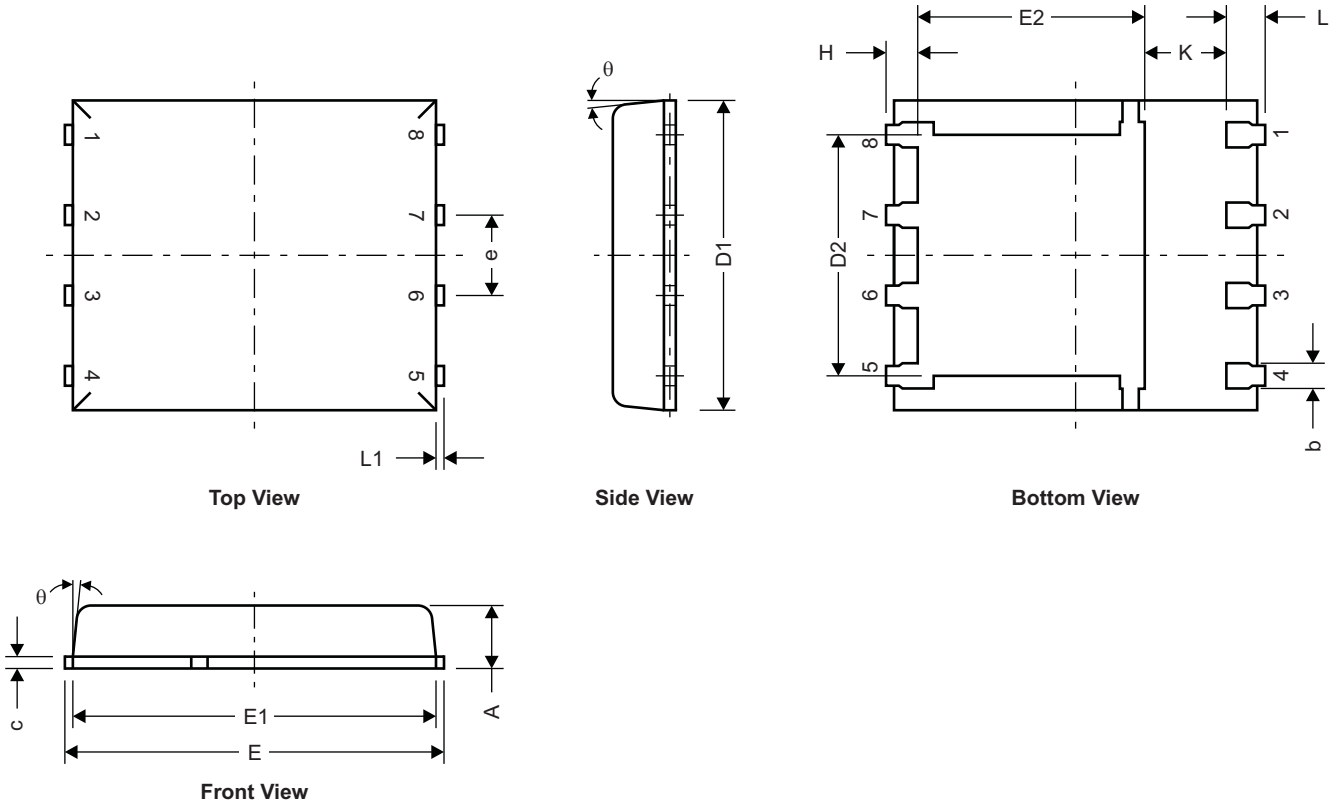
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q5A Package Dimensions



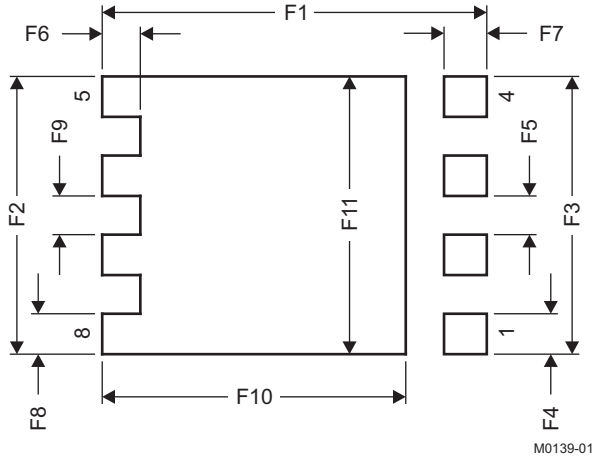
Top View **Side View** **Bottom View**

Front View

M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

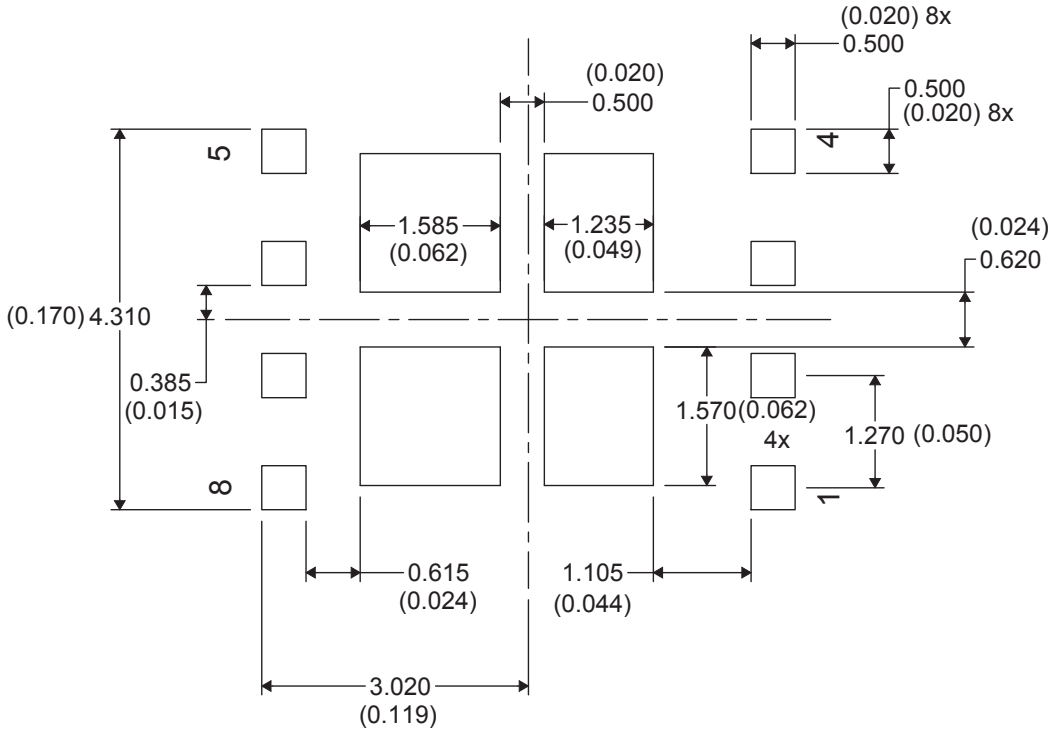
Recommended PCB Pattern



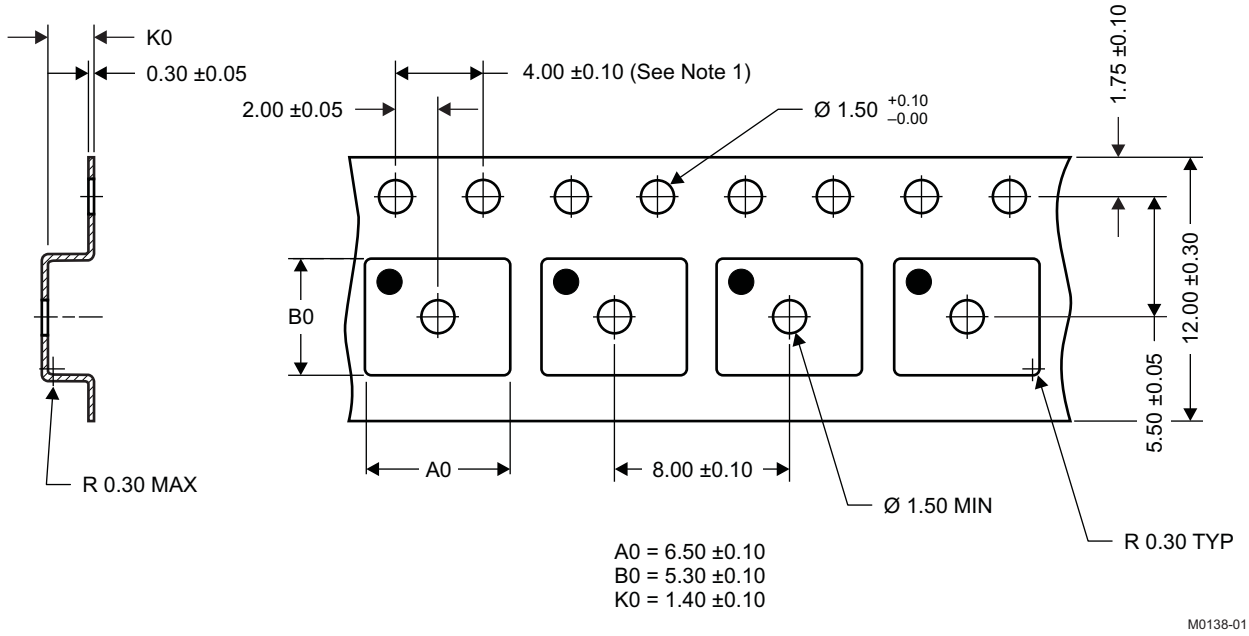
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note *Reducing Ringing Through PCB Layout Techniques*, SLPA005.

7.2 Recommended Stencil Opening



7.3 Q5A Tape and Reel Information



Notes:

1. 10 sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18531Q5A	ACTIVE	VSONP	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18531	Samples
CSD18531Q5AT	ACTIVE	VSONP	DQJ	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM		CSD18531	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

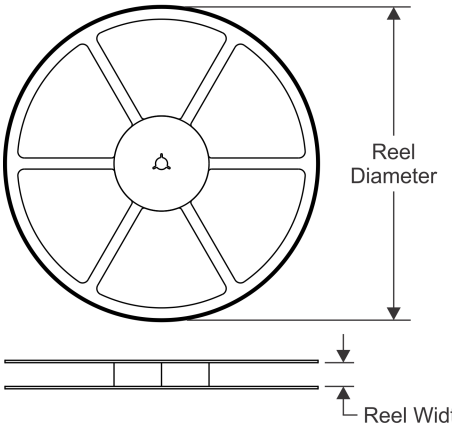
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

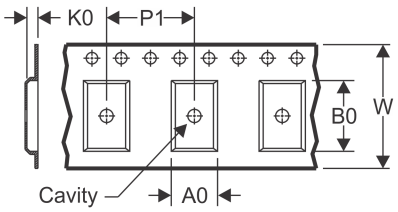
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

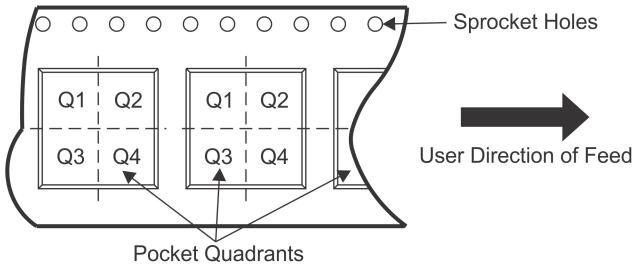


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

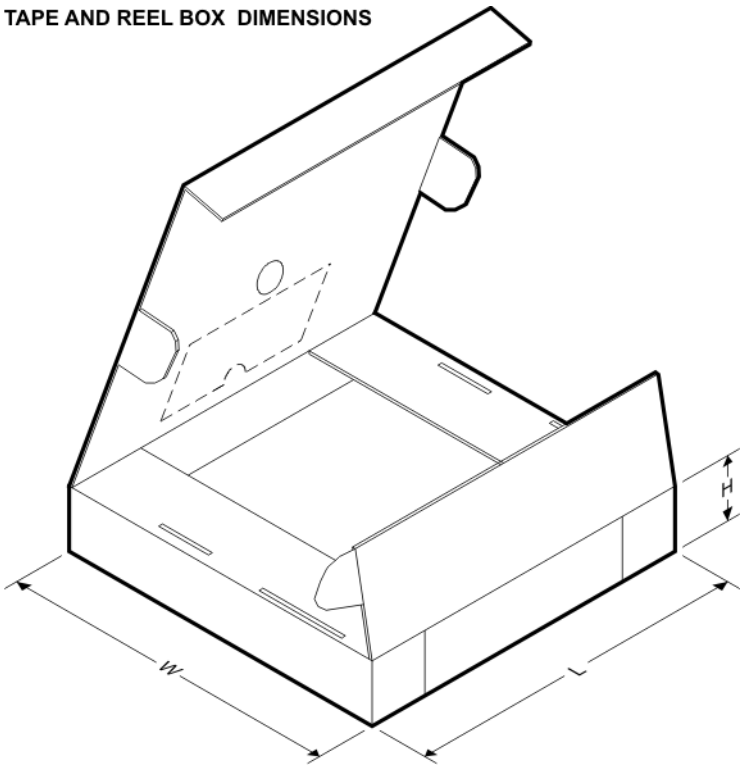
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18531Q5A	VSONP	DQJ	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18531Q5AT	VSONP	DQJ	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18531Q5A	VSONP	DQJ	8	2500	340.0	340.0	38.0
CSD18531Q5AT	VSONP	DQJ	8	250	190.0	190.0	30.0

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