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Jnana Sangama, Belagavi, Karnataka_590014

Project Report

On

" DESIGN AND IMPLEMENTATION OF HIGH SPEED SRAM CELL "

Submitted in partial fulfilment of the requirements for the reward of the degree of

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in
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Submitted by

PAVAN KUMAR S	**1BI20EC088**
SANDESH G NAIK	**1BI20EC127**
SPANDANA N D	**1BI20EC148**
YAMUNA A R	**1BI20EC176**

Under the Guidance of

Dr. VIJAYA PRAKASH A M

Professor

Dept. of ECE, BIT

Department of Electronics & Communication Engineering

BANGALORE INSTITUTE OF TECHNOLOGY

K. R. Road, V.V Puram, Bengaluru - 560004

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BANGALORE INSTITUTE OF TECHNOLOGY

K.R. Road, V. V Puram, Bengaluru -560004
Phone: 26613237/26615865, Fax:22426796
www.bit-bangalore.edu.in

Department of Electronics and Communication Engineering

CERTIFICATE

Certified that the project work entitled "**DESIGN AND IMPLEMENTATION OF HIGH SPEED SRAM CELL**" by **Mr. PAVAN KUMAR S (1BI20EC088)**, **Mr. SANDESH G NAIK (1BI20EC127)**, **Ms. SPANDANA N D (1BI20EC148)**, **Ms. YAMUNA A R (1BI20EC176)** bonafide students of **Bangalore Institute of Technology** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the Visvesvaraya Technological University, Belgaum during the year 2023- 2024. It is certified that all corrections/suggestions indicated for Internal Assessment have been incorporated in the Report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of Project work prescribed for the said Degree.

Signature of Guide	Signature of HOD	Signature of Principal
Dr. VIJAYAPRAKASH A M Professor, Dept. of ECE, BIT.	**Dr. HEMANTH KUMAR A R** Professor & HOD, Dept. of ECE, BIT.	**Dr. ASWATH M U** Principal, BIT.

External Viva

Name of the examiner	**Signature with date**
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PAVAN KUMAR S (1BI20EC088)
SANDESH G NAIK (1BI20EC127)
SPANDANA N D (1BI20EC148)
YAMUNA A R (1BI20EC176)

ABSTRACT

Static Random Access Memory (SRAM) has been an important memory device in VLSI design. This proposed work presents design and implementation of 1kb SRAM cell using single bit six transistor SRAM memory using CMOS technologies by EDA tool. The 6T SRAM cell is a popular type of SRAM cell, which is widely used in various electronic devices. In this proposed work SRAM cell is operated with voltage of 1V. Proposed high speed 6T SRAM cell decreases read and write delay by 29.4ps & 15ps respectively and improved overall read and write stability by 70 mV & 595 mV respectively compared to previously published ([7] [11]). In the proposed work static power is 36.6uW which is very less and dynamic power is 82.2uW.

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Semiconductor memories have a significant role has most fundamental units in VLSI layout. It is the most important unit in SOC and contain memories inclusive of flash memory, read only memory (ROM), static random access memory (SRAM) and dynamic random access memory (DRAM). SRAM which is kind of memory used in computer that keeps its information stored as long as power is supplied. It is described as "static" because unlike dynamic RAM which require frequent refreshing to maintain its information. SRAM is commonly utilized as a memory for input/output operations in computer systems and as high-speed cache memory in CPU. Compared to DRAM, it is more costly and faster and also more dependable, uses less power and has a higher access time. This makes SRAM cells a fundamental building block of modern computing systems and a key technology for achieving high-speed data processing.

SRAM is made of flip flops which are electrical circuits storing a bit of information. Four to six transistors make up each flip-flop, allowing them to maintain their value until power is turned off. SRAM is used in variety of computer systems and electronics including routers, phone switches and other networking equipment, as a result of its many benefits. SRAM is typically found in cache memory in microprocessors and other types of memory in devices. SRAM can be designed using BJT's however, power loss in switching is larger. SRAM is now created utilizing MOSFET's which reduces power loss in switching. In this nanoscale era, the static or leaky power usage of CMOS devices predominate over the dynamic power dissipation. Whenever power is consumed in device it generates heat that heat has to get out of the device and that can create problems for small form factor device.

Transistor switching characteristics are to blame for dynamic power loss. For the extension of battery life manufacturers should regulate both static and dynamic power. SRAM is used in the high-speed, low-capacity levels of the memory hierarchy due to its fast access times. As we move down the hierarchy, capacity increases significantly (DRAM), but speed decreases. Other memory technologies like DRAM offer better cost-effectiveness for larger capacity needs, while SRAM excels in speed-critical applications. SRAM is used as Cache memory which is very fast

and used to speed up the task of processor and memory interface. In this proposed work 1Kb SRAM is designed using 90nm CMOS technology. All peripherals like pre-charge, Row Decoder, Word line driver, Sense amplifier, Column Decoder/MUX and write driver are designed. In this proposed work we have concentrated on the design of high speed 6T SRAM which can be used as high speed. SRAM is used as Cache memory which is very fast and used to speed up the task of processor and memory interface. With the recent improvements in VLSI technology, processor speeds have increased intensely. To take the advantage of high speed processors, i.e. high clock rates, need to provide instructions and data to the processor with little or no delay. Therefore, the very high frequency is required for instructions and data.

With improvements in VLSI technology, the speed of the logic gates has increased significantly, but memory speed is not improved equivalently because memory densities have increased simultaneously. Therefore, for high speed computers, SRAM memories are very important to improve speed and can be used with processors to do so. In this work we have concentrated on the design of high speed SRAM which can be used as high speed memory for high speed computers. Thus, for high speed PCs SRAM memories are critical to enhance operating speed and DRAM are utilized as a part of Main Memory where Density has more significance than Speed.

CHAPTER-2

LITERATURE SURVEY

In order to get a foothold and basic understanding of the idea of our proposed project, we need to review and analyze previously published technical papers in the design and implantation of SRAM for high speed. The list below presents the details about the major such papers.

2.1 REVIEW ON LITERATURE SURVEY

Six transistor SRAM memory design of 16-bit storage, in different nodes is presented in [1]. The performance evaluation of all 3 designs was carried out. The performance criteria were total power dissipation & average delay. It was observed that reduction in technology results in reduced power dissipation & average delay. The comparison of the results is done at 180nm, 90nm, 45nm technology nodes. It shows that power dissipation and average delay is improved as the channel length is reduced.

Inference

There is a lack of specific details regarding the methodology employed in the design and implementation process.

V. Panduranga Vemula, S. Priyanka, A. Sairam [2] proposed many processors and SoC devices now employ SRAM and CMOS technology, which necessitates new SRAM design innovations. SRAM bit cells are formed of lowest geometry devices in order to achieve high density and stay up with CMOS technology scaling as a consequence. To deal with the nano-regime issues, numerous SRAM bit cell topologies and array layouts have recently been suggested. Different SRAM bit cell topologies and their benefits and drawbacks are also discussed in which we have considered the design architecture which shows speed improvements along with scaling of technology and delay time also decrease.

Inference

Fail to overcome primary issues like poor stability, process variation tolerance in SRAM designs.

The read, write, operations were performed for the 6T SRAM. Also, DC response for temperature and power is simulated in [3]. Another major factor that is the Static Noise Margin has been done and the noise responses obtained for both read and write operations. Here we have designed the Read and Write Operations for 6T SRAM Cells. The analysis of 6T Static Random-Access Memory is done in

[3]. In the future, we can upgrade the Static Random-Access Memory cell and make it dependable and robust to the noise present in the environment.

The SRAM cell design and its operational aspects, there's limited discussion on design trade-offs or optimizations made to achieve specific performance goals. So, to overcome this we provide Elaborating on design decisions and their impact on performance would enrich the circuit analysis.

Designing of 32*32 Memory Array SRAM is done in [4]. 1Kb SRAM array in bit orientation with a 6T SRAM cell in CMOS technology was designed and analyzed. It features a 1024-bit capacity for storage. The power consumption for read and write operations was 48.22 µW and 385 µW, respectively, and used for the write driver circuit for low-power applications. The performance attributes of the CMOS based SRAM arrays, such as the power dissipation for the read and write operations, were contrasted with those of previous works. This paper was validated using the Cadence Virtuoso tool in CMOS 22 nm technology.

The paper does not discuss security aspects such as susceptibility to side-channel attacks, which can be crucial in memory designs, especially for applications dealing with sensitive data. So, to overcome this addressing security concerns is essential in modern memory design which is incorporated in our design.

16- bit SRAM cell using different configurations is designed and analyzed in180nm CMOS technology in [5]. Based on the simulated results, Low power SRAM cells have the lowest power consumption as compared to 6T and 8T SRAM and read and write operation is performed. Low power SRAM shows the reduction in power consumption for the read cycle and write cycle. In comparison with 6T SRAM, the low-power SRAM is 20% faster. The only drawback is area overhead due to an increase in the number of transistors.

The paper mentions improved charging and discharging times for higher operating frequencies but does not provide specific details about the read and write access times. So, to overcome this optimized access time is a critical parameter in memory design which is incorporated in our design.

Govind Prasad, Bipin Chandra Mandi, Megha Jain [6] proposed the basic 6T Static random access memory (SRAM) cell experience relatively high static and total power loss problem, to solve this 8T, NC cells were designed. But this all consume more area as well as delay. Hence in this paper, 5T SRAM cell proposed and checked by Monte Carlo Simulation. In this we have Considered the speed of read and write operation.

Stability is decreased which needed to be increased for the high speed processer. This consumes more

area as well as delay.

Vibhash Choudhary, Dharmendra Singh Yadav [7] proposed 6T and 8T SRAM cells have been compared on 180nm technology using an industry-standard Cadence Virtuoso Tool. It's challenging to make an SRAM cell with low power consumption and stay in a small space. The consumption of power on both the SRAM cells are compared. The parameters of SRAM Static Noise Margin (SNM), Write Delay, Read Delay and average power consumption are examined and discussed thoroughly. Results illustrate that Read delay and Write delay will decrease of 8T as differentiate to 6T SRAM. In this we have considered the variation of average power consumption and delay has been observed as an operation of the supply voltage.
Results can vary depending on the chosen CMOS process technology (e.g., 45nm vs. 130nm).

Debasis Mukherjee, Hemanta Kr.Mondal [8] proposed the different types of analysis such as noise, voltage, read margin and write margin of SRAM cell for high-speed application. The design is based upon the 0.18 µm CMOS process technology. Static Noise Margin (SNM) is the most important parameter for memory design. For demand of the high-speed application of the SRAM cell operation, supply voltage scaling is often used that is why we have done Data Retention Voltage. We took different types of curve by which straight forwardly we could analyses the size of the transistor of the SRAM cell for high-speed application, In this we have considered the butterfly method to calculate static noise margin, write noise margin and read noise margin of a 6T SRAM cell.
Primary issues like poor stability, process variation tolerance in SRAM design.

T. Wada, S. Rajan, and S. Przybylski [9] considered configuration, organization, and process parameters for formulation of the access time of on chip cache.
It doesn't consider interconnect delays and tag paths, for each delay stage it assumes a step input waveform, and overgeneralized delay models and circuit models.

Hansraj, Ajay Rana [10] proposed the power dissipation of the projected new SRAM cell is sort of stable for top speed operations. Since the number of transistors and therefore the space has exaggerated compared to the standard SRAM 6T cell, this disadvantage will simply be overcome by low power dissipation even at terribly high frequencies. This new style approaches the voltage mode methodology to scale back voltage swing around writing switch activity. Within the standard SRAM cell thanks to method variation, the hold on knowledge is also destroyed throughout the read operation. As a result, the outpouring current thanks to bigger power dissipation is reduced. Dynamic

power is calculated for various frequencies and compared to the standard SRAM 6T cell.
Fails to provide specific details about the read and write access times and area overhead due to an increase in the number of transistors.

Designing a basic 6T SRAM cell in which READ and WRITE operations are observed one after the other. Each operation is done using the Tanner tool in the SEDIT in [11]. There is no need to refresh the circuit each time because the power supply is given as the bits are already stored in the memory. Also, the circuit operates at low power that is READ operation power is about 1.028720e-007 watts and WRITE operation power is about 2.483478e-004 watts. In ideal conditions, it consumes very less amount or negligible amounts of power in the circuit.
The paper doesn't provide information about the fabrication process or technology node used for the design.

2.2 OVERVIEW OF LITERATURE SURVEY

From the above referred research paper there are few observations associated with Read and Write Stability, Read and Write Speeds, Design Complexity, Power Consumption, and Cost. In the research paper we have found that read, write, hold, operations were performed for the 6T & 8T SRAM and the performance criteria were total stability & average delay. The various design techniques are used to overcome factors like power dissipation, read and write delay, and stability. After analyzing the required research papers, we found that the fast access time and low latency need to be upgraded so our main aim of this proposed work is to enhance the throughput with read and write speeds. We have about to minimize access times to improve memory bandwidth and system performance by multi-threshold voltage (Vt) design techniques using advanced EDA tool. Since in current day world speed seems to be a prominent while designing the integrated circuits with memories, if this not met slower SRAM can lead to reduced responsiveness in computing systems

2.3 PROBLEM STATEMENT

This proposed work focuses on designing and implementation of 1kb SRAM memory with operating voltage of 1V using CMOS technology. By enhancing the speed and efficiency of SRAM cells through CMOS technology, the project seeks to overcome existing limitations in access times and power dissipation, thereby enhancing overall system performance in integrated circuits.

2.4 OBJECTIVES

- Design and implementation of Six Transistor SRAM memory cell.
- Design and Implementation of peripherals like sense amplifier, pre-charge circuit, 32X32 cell array, row decoder and column decoder.
- Implementation of 1Kb SRAM memory cell using those peripherals.
- Stability analysis of SRAM cell SNM using Butterfly Curve.
- Analyzing the Waveform of 1 bit SRAM cell for delay calculation

CHAPTER – 3

METHODOLOGY

3.1 INTRODUCTION TO SIX TRANSISTOR SRAM CELL

1-bit 6T SRAM is designed by placing two CMOS cross coupled inverters which works as a latch. These two inverters are used to latch the data to be saved. Latch perform different operations, i.e. Read, Write & Hold. This latch is operated by internal pulse provided to it. Additionally, to its two access transistors are also used to provide access to BL and BLB (both BL & BLB works according to WL). The basic structure of a 6T SRAM memory cell is shown in Fig. 3.1

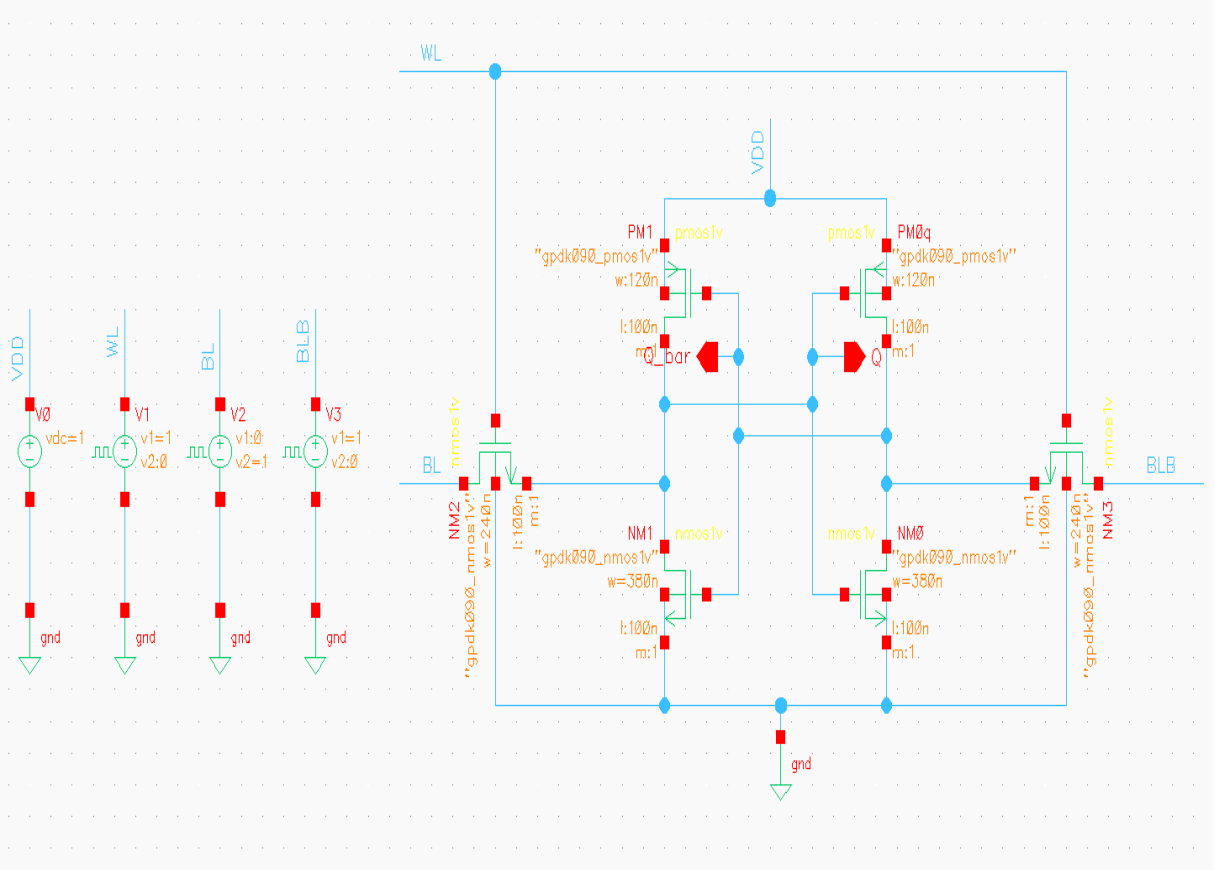

Fig 3.1. Schematic of 1-bit 6T SRAM cell

- The act of saving data is known as a write operation.
- The process of recovering data is known as a read operation.
- The process of carrying previous data is known as hold operation.

The Write operation updates the contents of an SRAM cell, whereas the Read operation fetches the contents of SRAM cell.

Fig. 3.1 shows a schematic diagram of a 6T SRAM cell. 6 MOSFETs make up a typical SRAM cell. Each bit in an SRAM is stored on two cross-coupled inverters made up of four transistors (PM1, PM0, NM1 and NM0).

PM0 and PM1: Pull-up Transistors

NM0 and NM1: Pull-down Transistors

NM2 and NM3: Access Transistors

WL: Word Line

BL: Bit Line

BLB: Bit Line Bar

The digits 0 and 1 reflect the two stable states of this secondary cell. Two more access transistors control the cell's entrance during read and write operations. The word line WL governs whether the cell is linked to the bit lines BL and BLB, providing access to the cell. The bit lines BL and BLB were utilised to transfer data in both read and write operations. Inverters in the SRAM cell move the bit lines high and low when the cell is being read. Simulation result for 1-bit SRAM cell is shown in fig 3.1.1.

The SRAM cell has three modes:

1. Write Mode
2. Read Mode
3. Stand-by Mode

A. Write Mode

The term "write mode" refers to the process of changing data. To write anything in SRAM, either BLB or BL are discharged to ground. When logic 1 must be written, charge BL to VDD and discharge BLB to ground. When writing logic 0, BLB is connected to VDD and BL to ground. If data is to be written into the cell, WL is turned on. Assume a 0 is stored at NM1-PM1(node A) and 1 must be written; 1 logic is applied to the BL line, which begins charging node A through the NM2 transistor. As a result, PM0 is activated, and the output of inverter NM0-PM0 (node B) begins to discharge, causing MM1 to activate. As a result, the value 1 is now written on node A.

B. Read Mode

Read Mode can be defined as fetching data from memory. The two access transistors NM2 and NM3, which are coupled to the bit lines, are enabled when WL is set to read mode. The data from nodes A and B is now transmitted to the bit lines. Assuming 0 is stored at node A, BL will discharge through NM2 and PM1 transistors, and the BL BAR will be brought up to VDD through NM0. In this mode of operation, the NM1 and PM0 transistors are turned off, but the PM1 and NM0 transistors function in linear mode. To Read data from memory we need a sense amplifier circuit.

C. Hold Mode (Stand-by Mode)

Hold Mode can be defined as no operation to be held on memory, memory is in hold state. When the two access transistors NM2 and NM3 are off and the SRAM cell cannot be accessed in standby mode, WL is 0, and the contents of connected transistors stay unaltered if supply voltage is present.

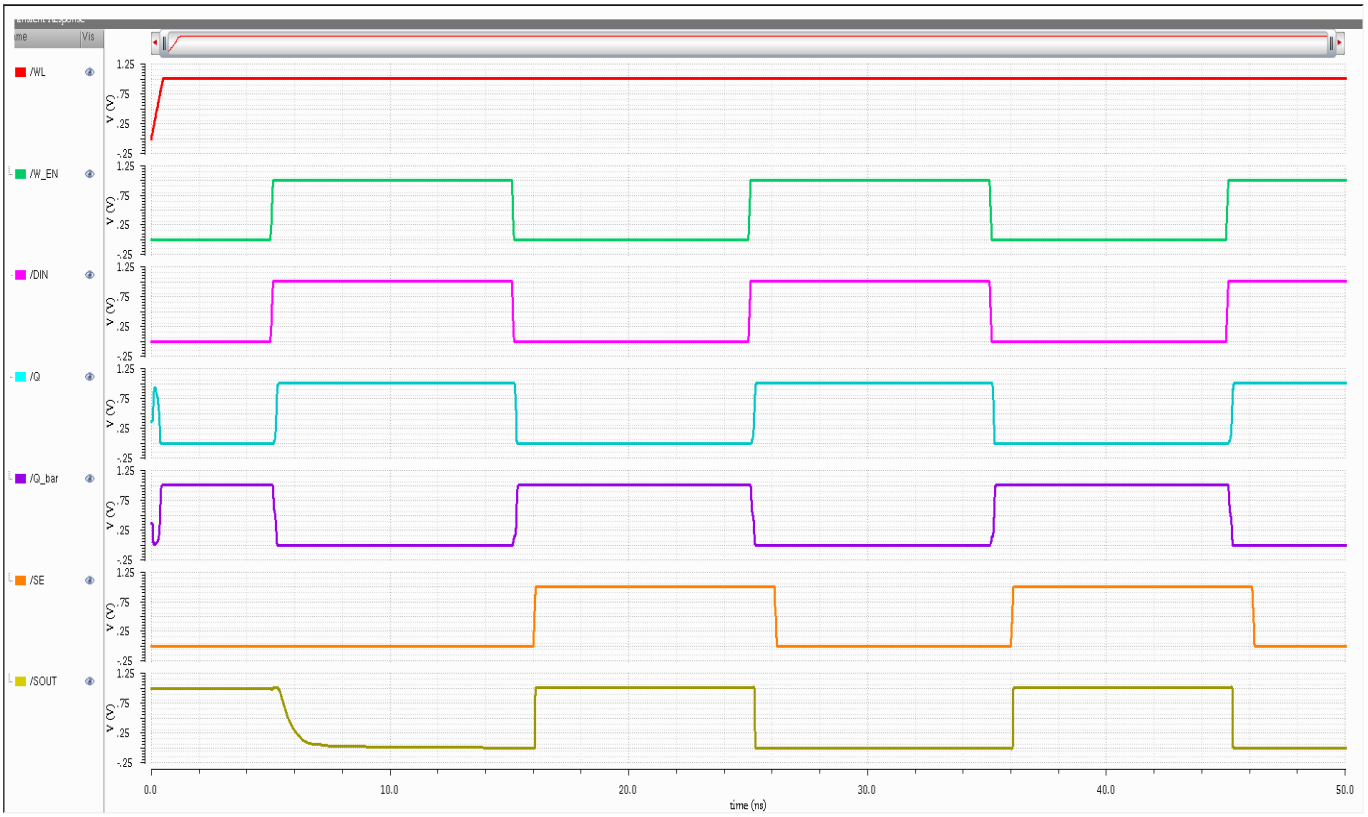

Fig 3.1.1. Simulation results of 1-bit 6T SRAM

3.2 DESIGN AND IMPLEMENTATION OF 1 BIT SRAM CELL

The One-Bit 6T SRAM schematic with peripheral components. The signals used in the simulation results: ‘pre-charge’ from the pre-charge circuit, ‘word-line’ from 6T SRAM circuit, ‘write_en’ corresponds to write enable signal from the write driver circuits, ‘bit-line’ and ‘bit-line bar’ acts as input or output based on write/read operation, ‘q’ and ‘qb’ corresponds to the storage nodes Q and QB of 6T SRAM during write operation.‘read_en’ corresponds to the read enable signal given to the sense amplifier circuits and ‘out’ signal gives the output of reading operation from sense amplifier circuit.

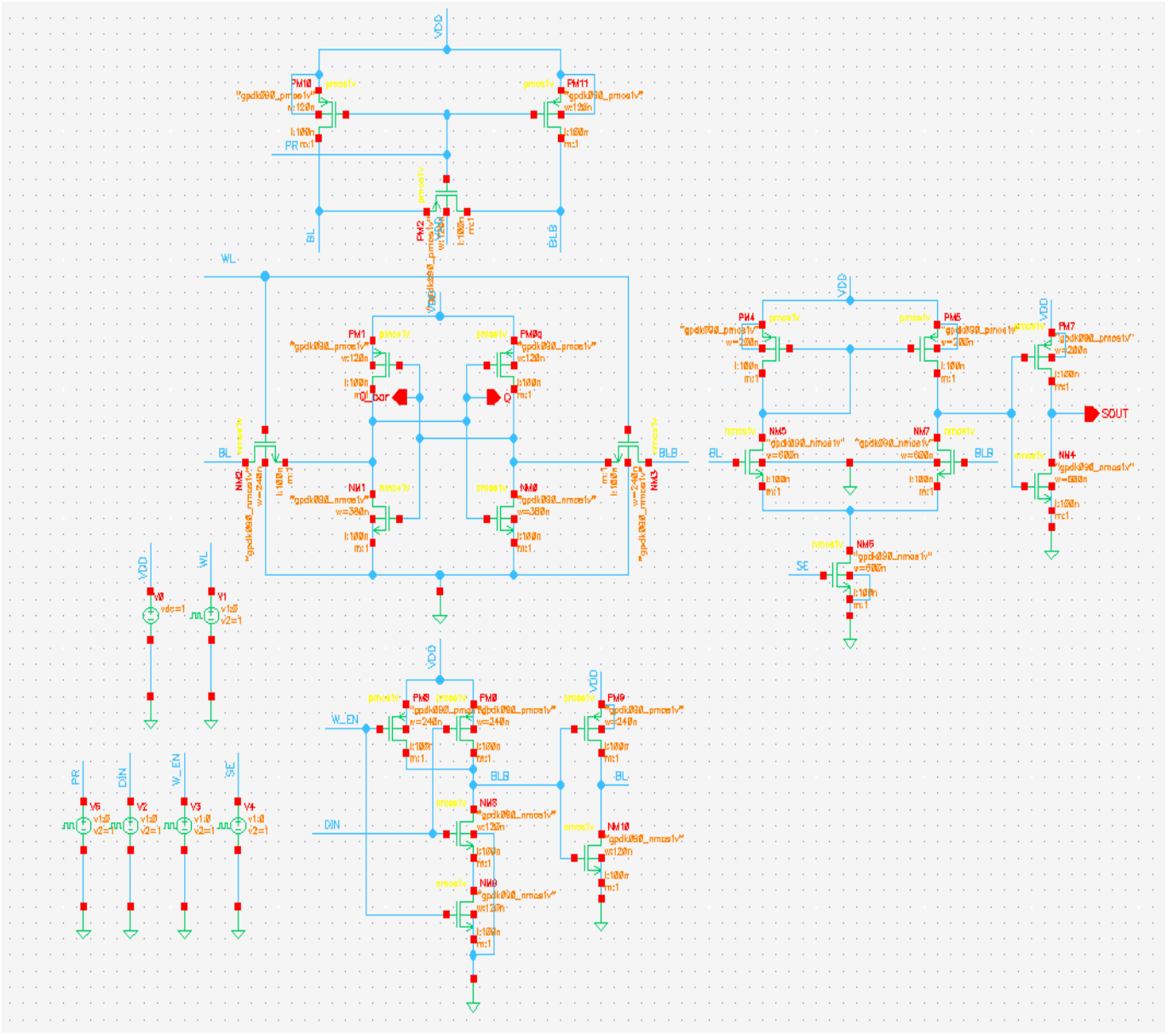

Fig 3.2. Design and implementation of 1-bit 6T SRAM cell

3.3 BLOCK DIAGRAM OF 1KB SRAM CELL

Fig. 3.3 shows 1-kb SRAM block structure which includes Cell Array, decoder, sense amplifier, write driver, column mux, precharge circuitry, address latch and read and write control as the peripheral circuit to the SRAM cell array. Since the memory core trade performance and reliability in reduction area, memory design relies exceedingly on the peripheral circuitry to recover both speed and electrical integrity. While the design of the core is dominated by technological consideration and is largely beyond the scope of the circuit designer, it is in the design of the periphery where a good designer can make an important difference. Generally, for smaller memory designs monolithic architectures are preferred, but in the Design of bigger memories monolithic architecture will not give efficient performance. The frequency of operation of the circuit is reduced by a factor of two as the number of rows doubles. Similarly, the frequency of memory, reduced by a factor of four as the number of 42 columns doubles, hence in bigger memory designs memory portioning technique is used which is known as memory banking.

- Write Circuit: This block is responsible for storing data in the memory cells. It involves generating and controlling signals to write information into the selected memory cell.
- Precharge Circuit: The precharge circuit prepares the bitlines in the memory array for read and write operations. It sets the initial conditions for proper sensing and writing.
- Row and Column Decoder: Row and column decoders are crucial for selecting the specific memory cell in the array. The row decoder activates the desired row, while the column decoder selects the appropriate column.
- Sense Amplifier: The sense amplifier is used during read operations to detect and amplify the small signals from the memory cells. It helps in accurate reading of the stored data.

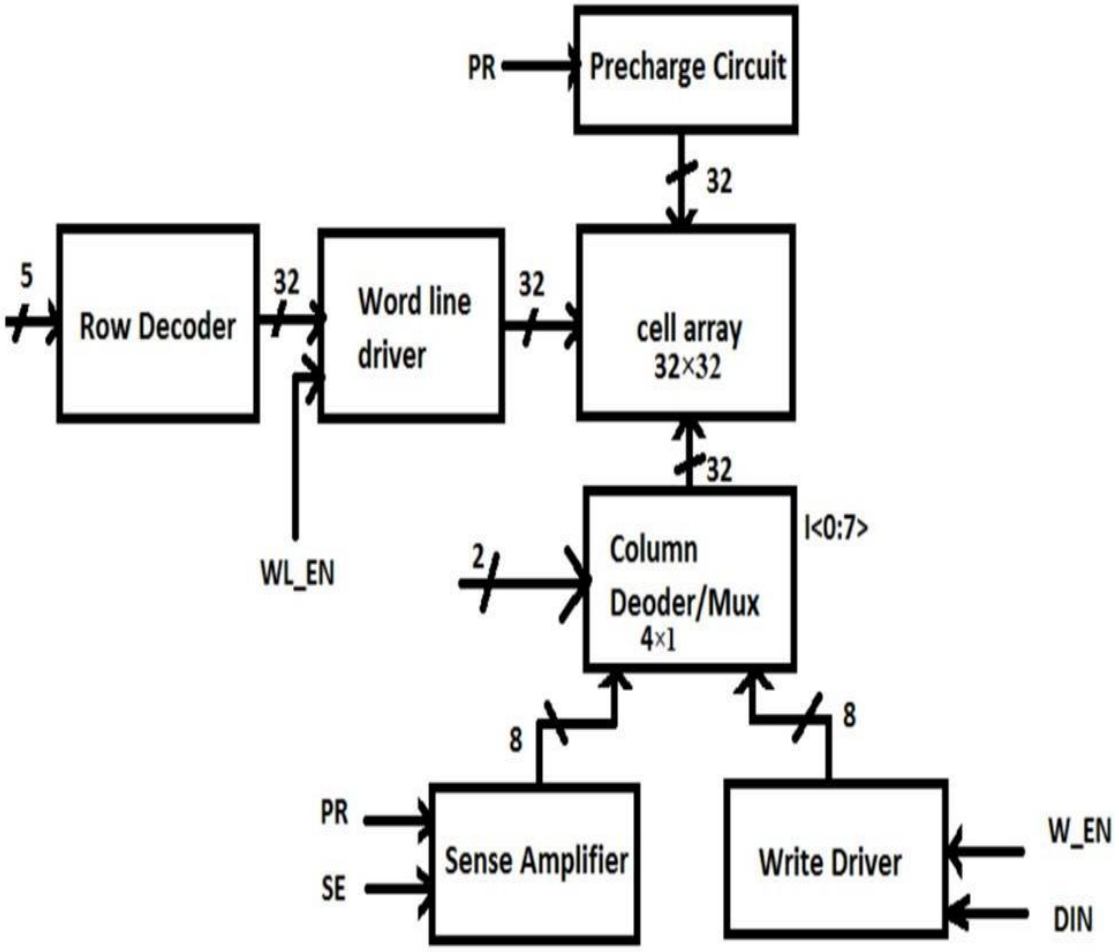

Fig 3.3. 1-kb SRAM Based Memory Block Diagram.

3.4 DESIGNING OF PRECHARGE CIRCUIT

Precharge circuit is used to pre-charging the both bit lines voltages to supply voltage and pre-charging operation should perform before every write and read operation. Figure 3.4 shows the pre-charge circuit which consists of pull up PMOS transistors and an equalizer which is used to equalize the voltage on both bit lines. The pull up PMOS transistors are controlled by PR signal i.e. The Transistor M3 shown in the schematic of Pre-charge is an equalizer which is used to equalize the voltage on both bit lines. Pre-charge circuit should provide large driving current to drive the bit lines which are having large parasitic capacitances, so the transistor sizes of pre-charge circuit need to be increased. Therefore, size of transistors used in precharge circuit is large. When the precharge signal is low bit lines get charged and when it goes high bit lines becomes floating. Test Circuit for the precharge circuit is shown in fig 3.4.1.

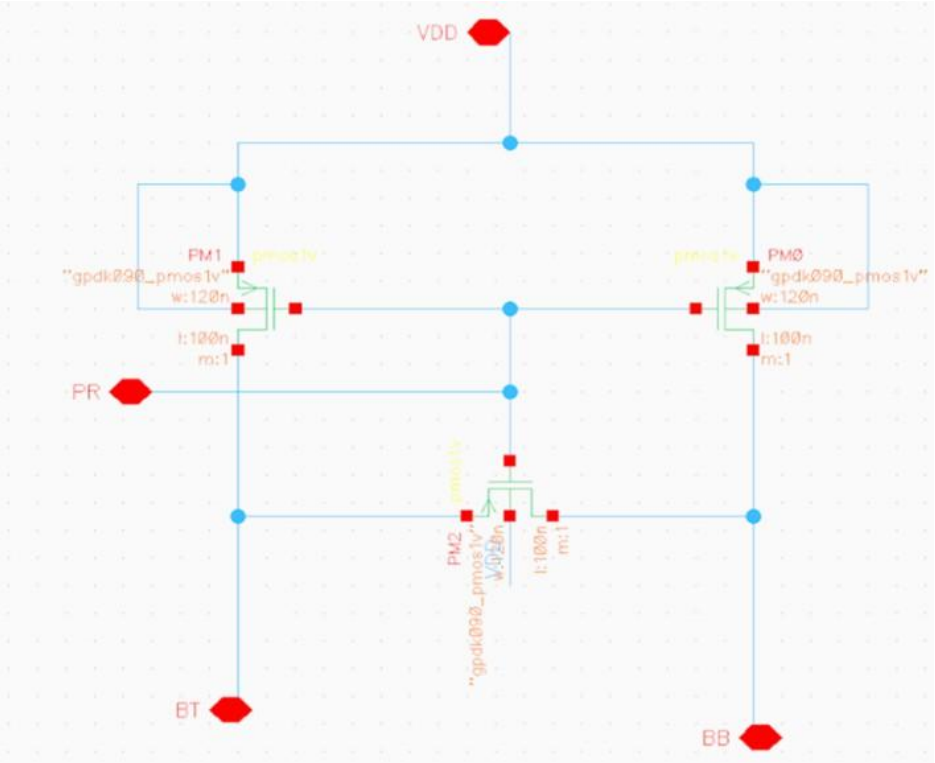

Fig 3.4. Schematic of Precharge Circuit

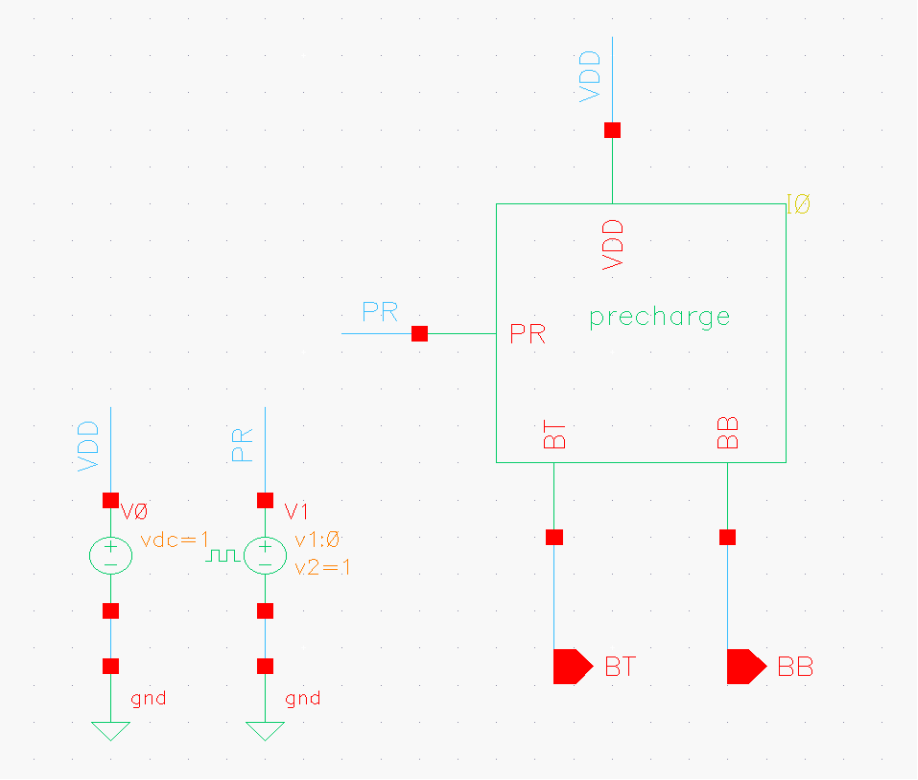

Fig 3.4.1. Test Circuit of Precharge circuit

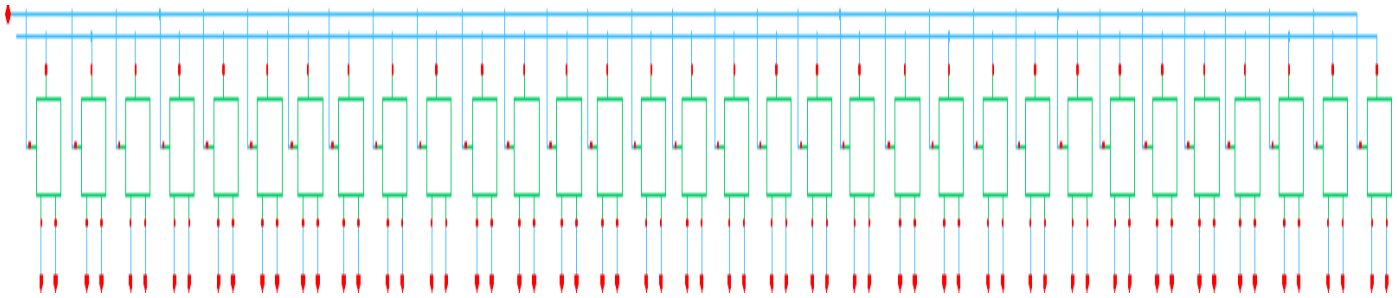

Fig 3.4.2. Test Circuit of 32-bit Precharge Circuit

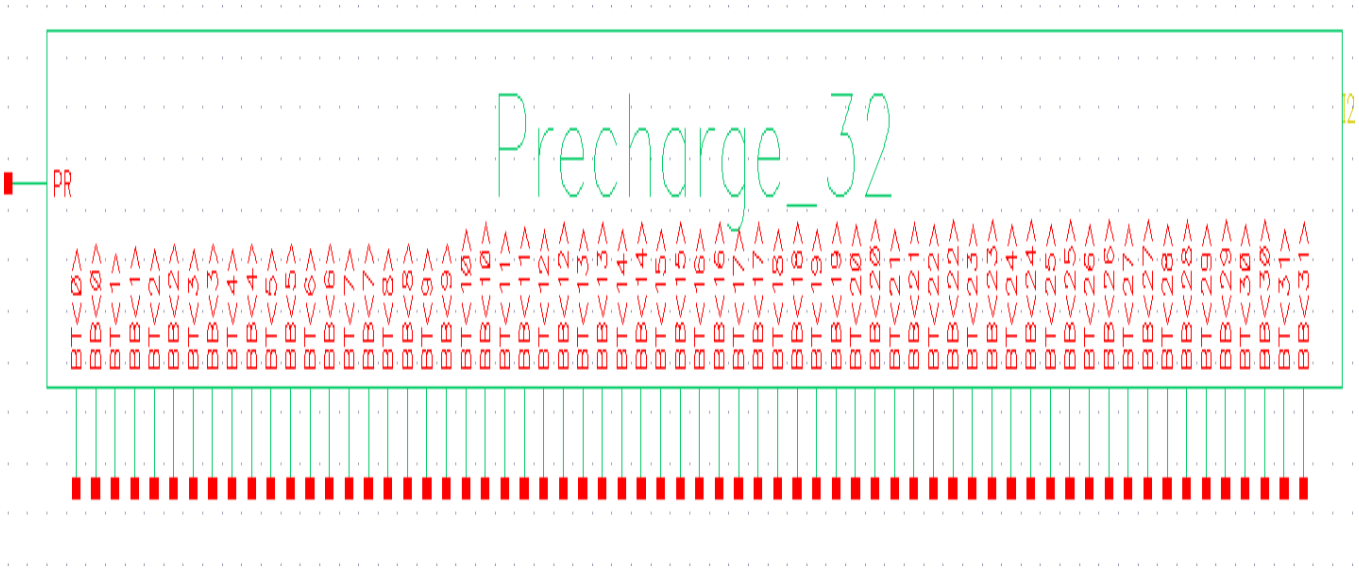

Fig 3.4.3 Symbol for 32-bit Precharge Circuit

In this work, we have designed precharge circuit for 32-bits which is required to operate in 1kb SRAM memory. Test circuit for 32-bit precharge circuit is shown in fig 3.4.2 and the symbol is shown in fig 3.4.2. Simulation result for 1-bit precharge circuit is shown in fig 3.4.4.

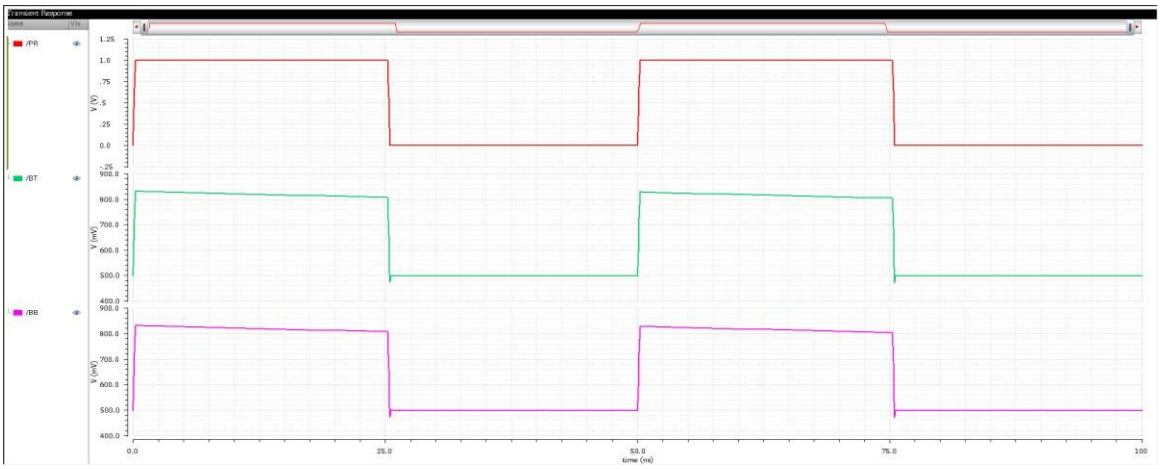

Fig 3.4.4. Simulation result of Precharge Circuit

3.5 DESIGN OF SENSE AMPLIFIER CIRCUIT

Sense Amplifiers plays a crucial role in the design of memories to achieve performance, reliability and functionality of memory circuits. Figure 3.5 shows the design of sense amplifier circuit. Normally sense amplifiers perform various operations like voltage amplification, reduction in delay, power reduction and restoration of original signal. Generally, sense amplifiers are used in the memories to speed up the read operation. Sense amplifier takes the small signal difference bit line voltage as input and gives full swing single ended output. Access time and power consumption of memory is affected by the sense amplifier hence the performance of memory is improved by reducing both sensing delay and power dissipation.

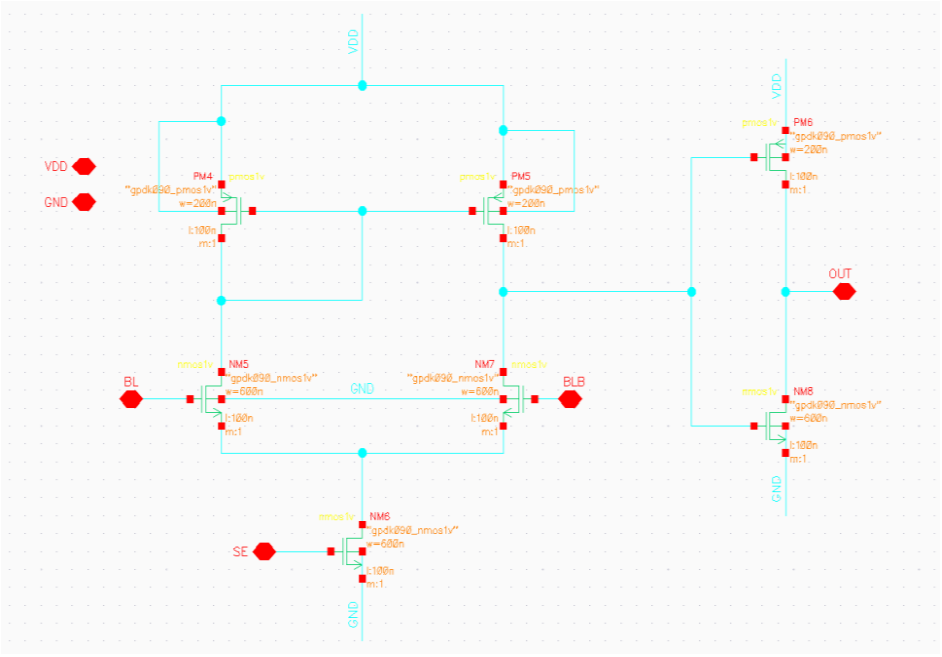

Fig 3.5. Schematic of Sense Amplifier

Bit line and bit line bar is the input to the sense amplifier, these are highly capacitive bit lines and are driven by SRAM cell. NM5 and NM7 are the differential input devices and inputs are given to them, whereas transistors PM4 and PM5 act as an active current mirror load. The sense enable SE signal is used to turn on and off the sense amplifier.

Test Circuit of the Sense Amplifier is shown in Fig 3.5.1.

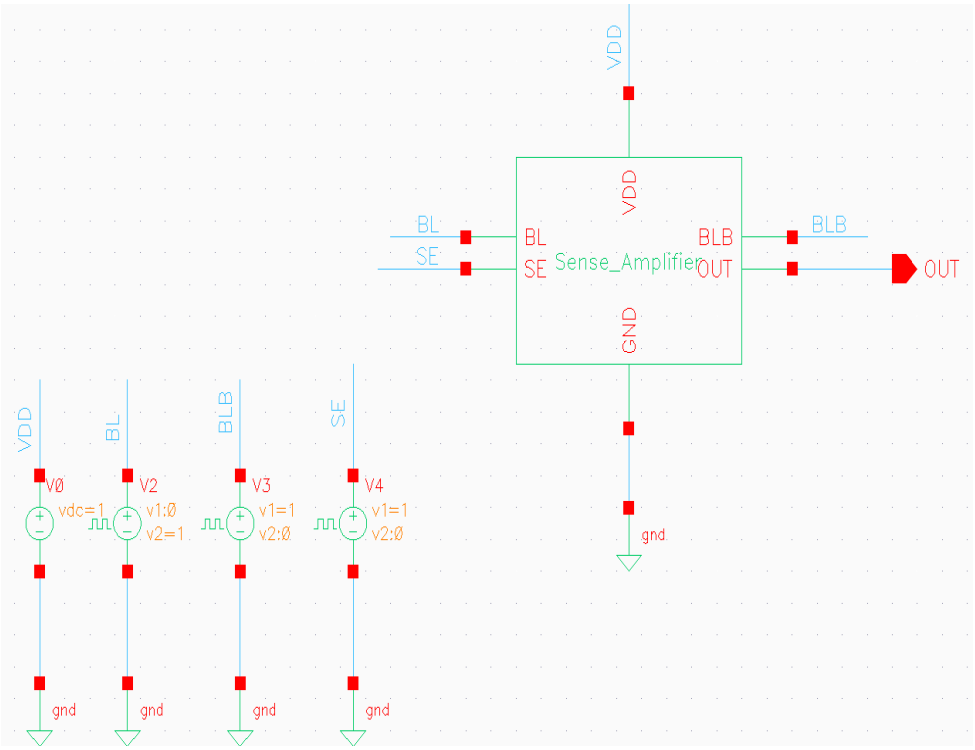

Fig 3.5.1 Test Circuit of the Sense Amplifier

Similarly, we have designed schematic and test circuit for 8-bit sense amplifier, required to operate in 1kb SRAM memory. Test circuit for 8-bit sense amplifier is show in Fig 3.5.2. Symbol of 8-bit sense amplifier is shown in Fig 3.5.3.

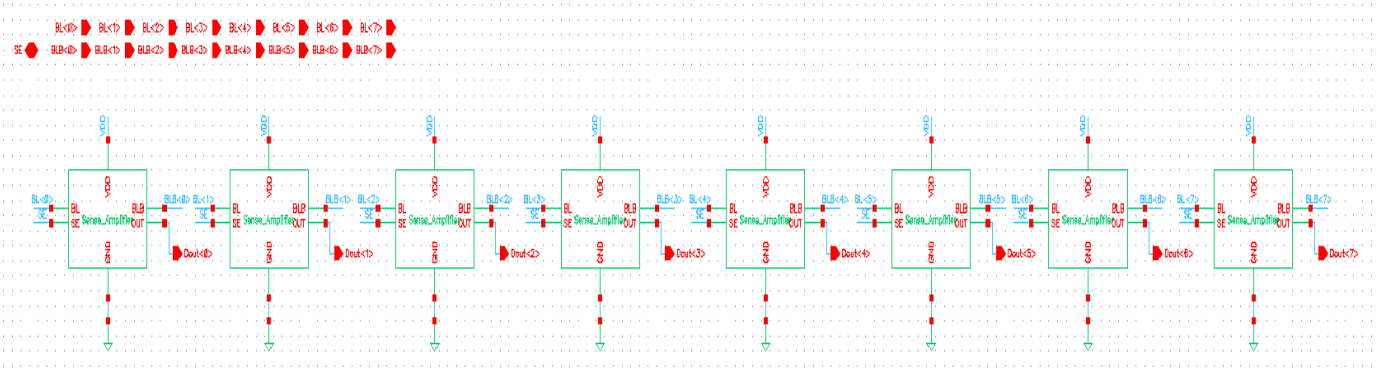

Fig 3.5.2 Test Circuit of 8-bit Sense Amplifier.

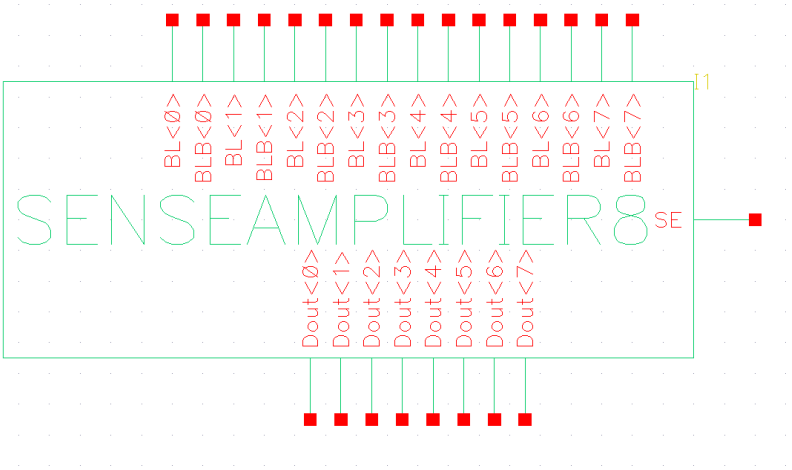

Fig 3.5.3 Symbol for 8-bit Sense Amplifier

When SE is logic low then both bit line voltages are charges to supply voltage, when SE is logic high then sense amplifier is getting ON and one of the bit line voltage discharges to ground via pull down transistor. It takes BL and BLB voltages as an input and generates single ended output. When BL voltage is greater than the BLB voltage then current through is increases and simultaneously current through decreases to maintain as a constant, then the drop across is decreases hence output voltage increases, which interprets output as the logic 1. Similarly, when BL voltage is less than BLB voltage then it indicates output as the logic 0. In this way, Sense amplifier plays a crucial role in the memory read operation. Simulation result is shown in fig 3.5.4.

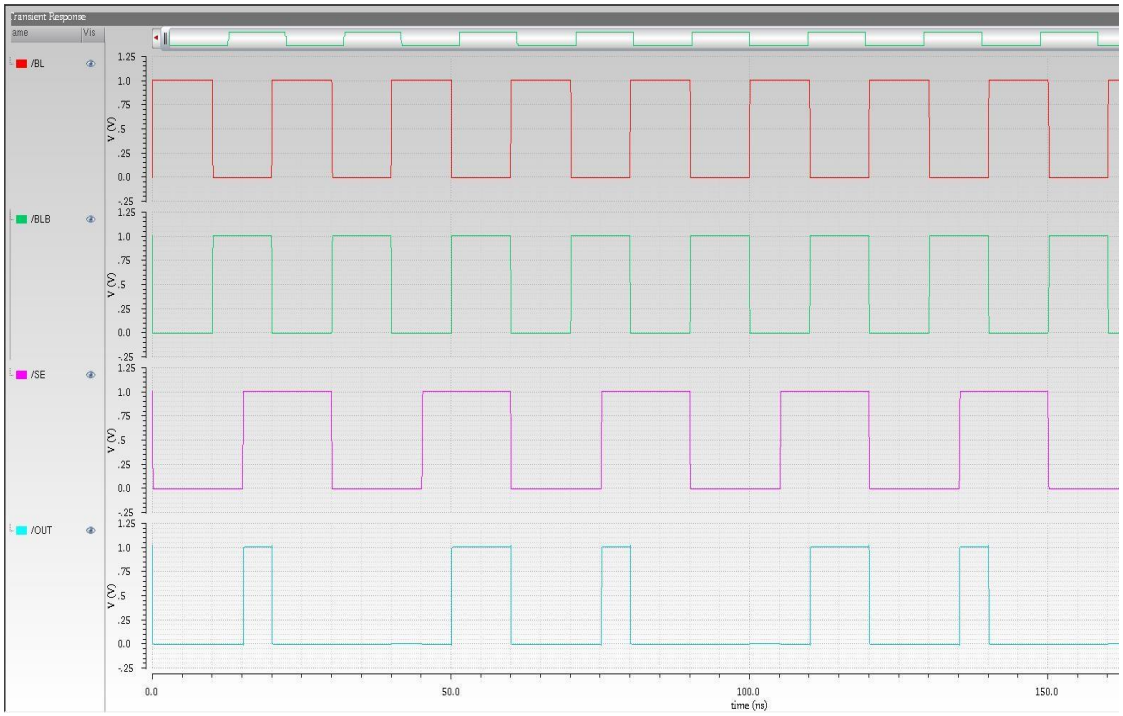

Fig 3.5.4. Simulation result of Sense Amplifier.

3.6 DESIGN OF 2:4 DECODER

Whenever a memory allows for random address based access, address decoders must be present. The design of these decoders has a substantial impact on the speed and power consumption of the memory. Since only one transition determines the decoder speed, it is interesting to evaluate other circuit implementation. Dynamic logic offers a better alternative. A first solution is presented in Fig. 3.6, where the transistor diagram of decoder is depicted. Notice that this structure is identical to the NOR ROM array, differing only in the data patterns. The same structure can be used to build 5:32 decoder for 32x32 memory array. Test circuit for 2:4 decoder is shown in fig 3.6.1 and the simulation results in fig 3.6.2.

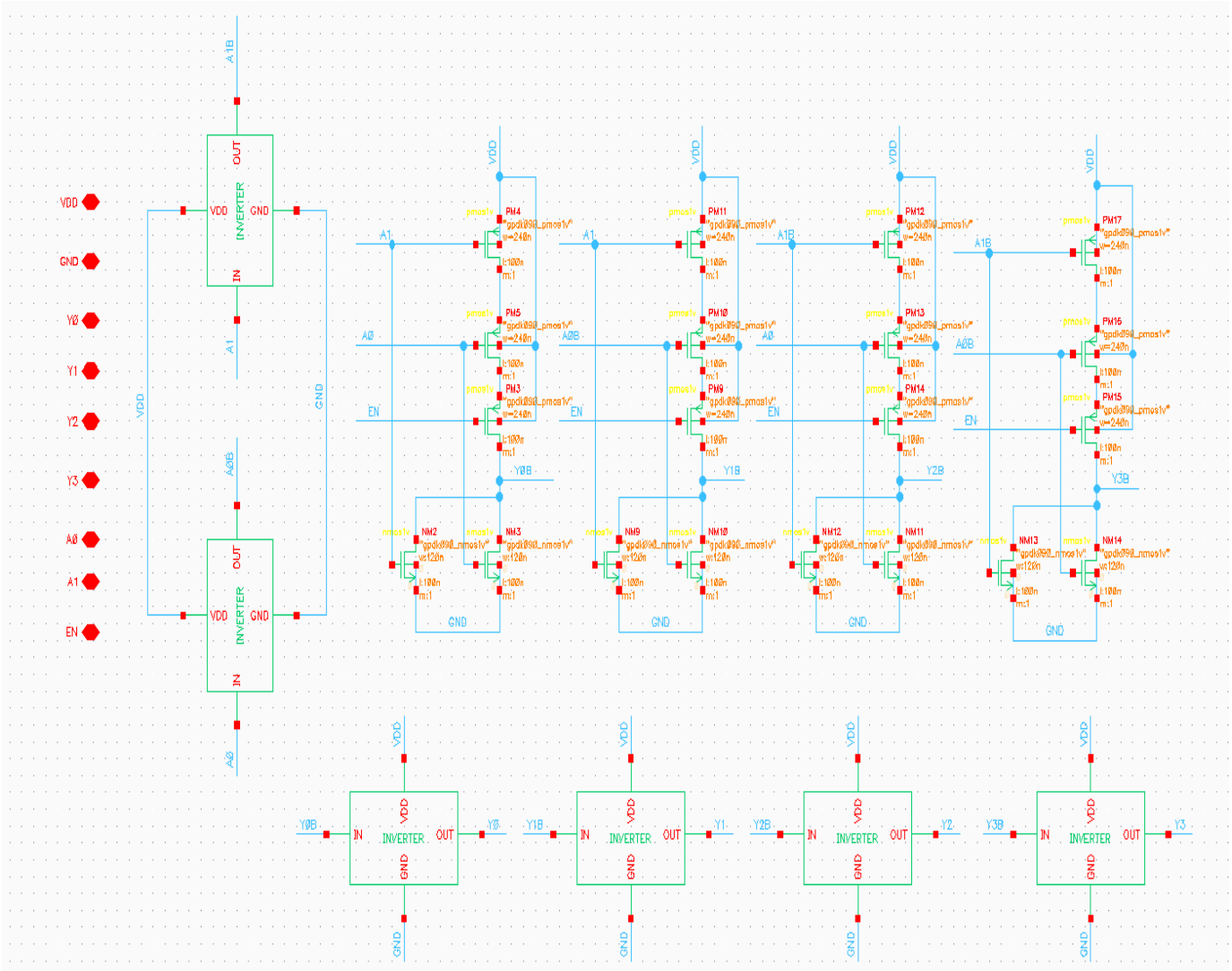

Fig 3.6 Schematic of 2:4 Decoder

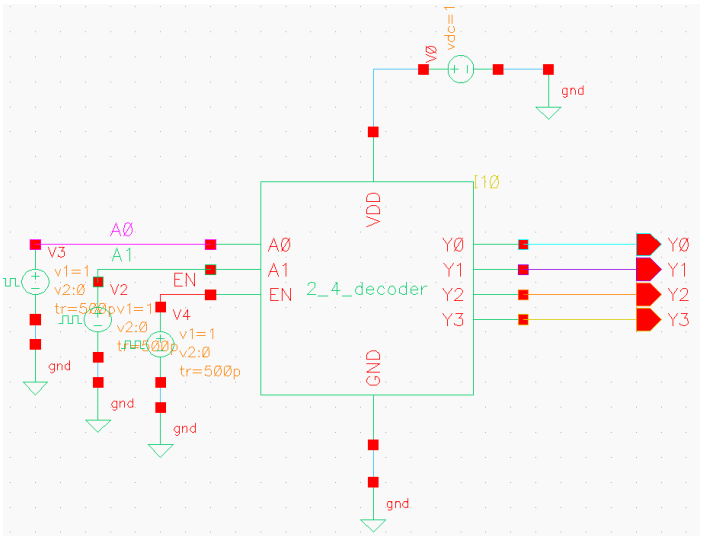

Fig 3.6.1 Test Circuit of 2:4 Decoder

Below given fig 3.6.2 represents the simulation result of 2:4 decoder. A 2:4 decoder typically has five output lines: two inputs (enable, A, and B) and four outputs (Y0, Y1, Y2, Y3). The enable line controls the overall activation of the decoder. When enabled, the specific combination of A and B determines which output line (Y0 to Y3) goes high (typically logic 1) and the others go low (logic 0).

The waveform for a 2:4 decoder would show the voltage levels on the enable, input, and output lines over time. During transitions, there might be short spikes or glitches as the outputs switch states.

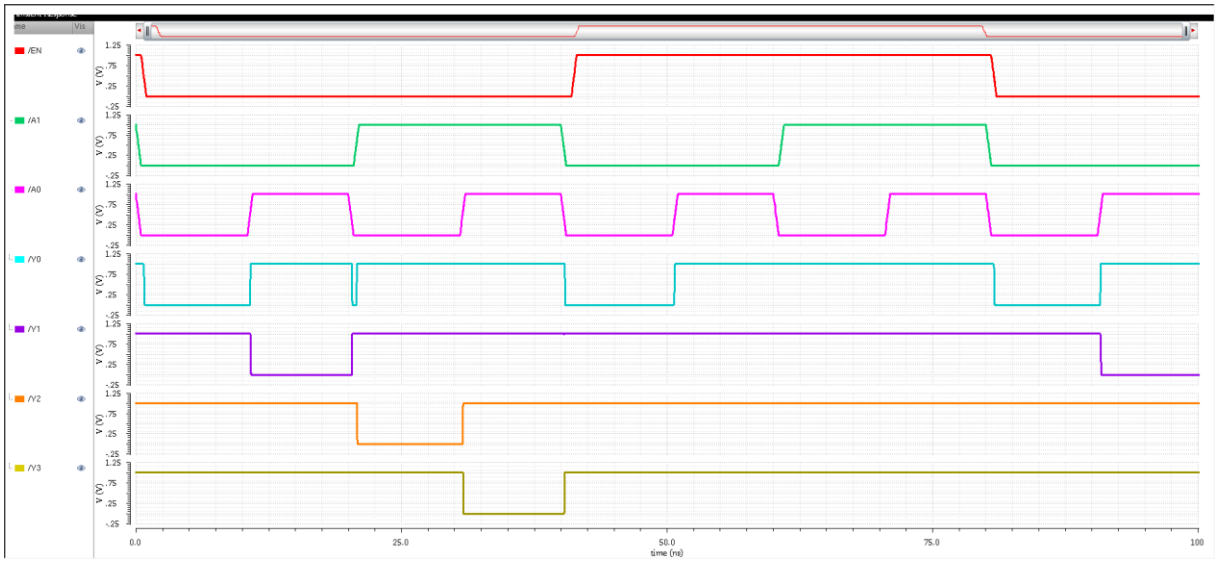

Fig 3.6.2 Simulation result of 2:4 Decoder

3.7 DESIGN OF 5:32 ROW DECODER

Row decoder, whose task is to empower one memory row out of 2^M, where M is the width of particular fields in address word. When the number of inputs is more than or equal to four then the speed of operation of the decoder is affected so pre-decoders are to be used which reduces the large fan-in. The structure of 2:4 decoder is used to build 5:32 decoder. Fig 3.7 shows the schematic, Fig 3.7.1 shows the test circuit of the row decoder and the simulation result is shown in the fig 3.7.2.

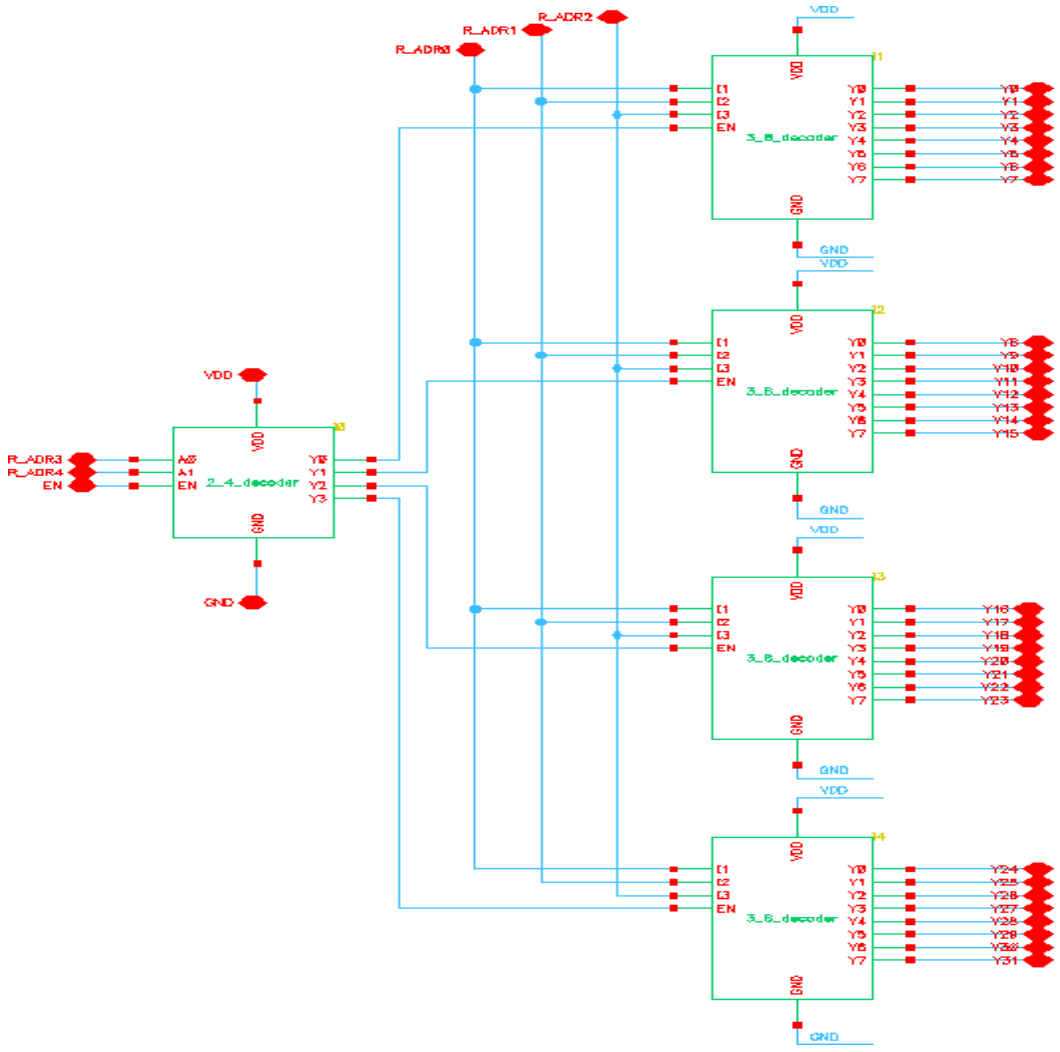

Fig 3.7 Schematic of 5:32 Row Decoder

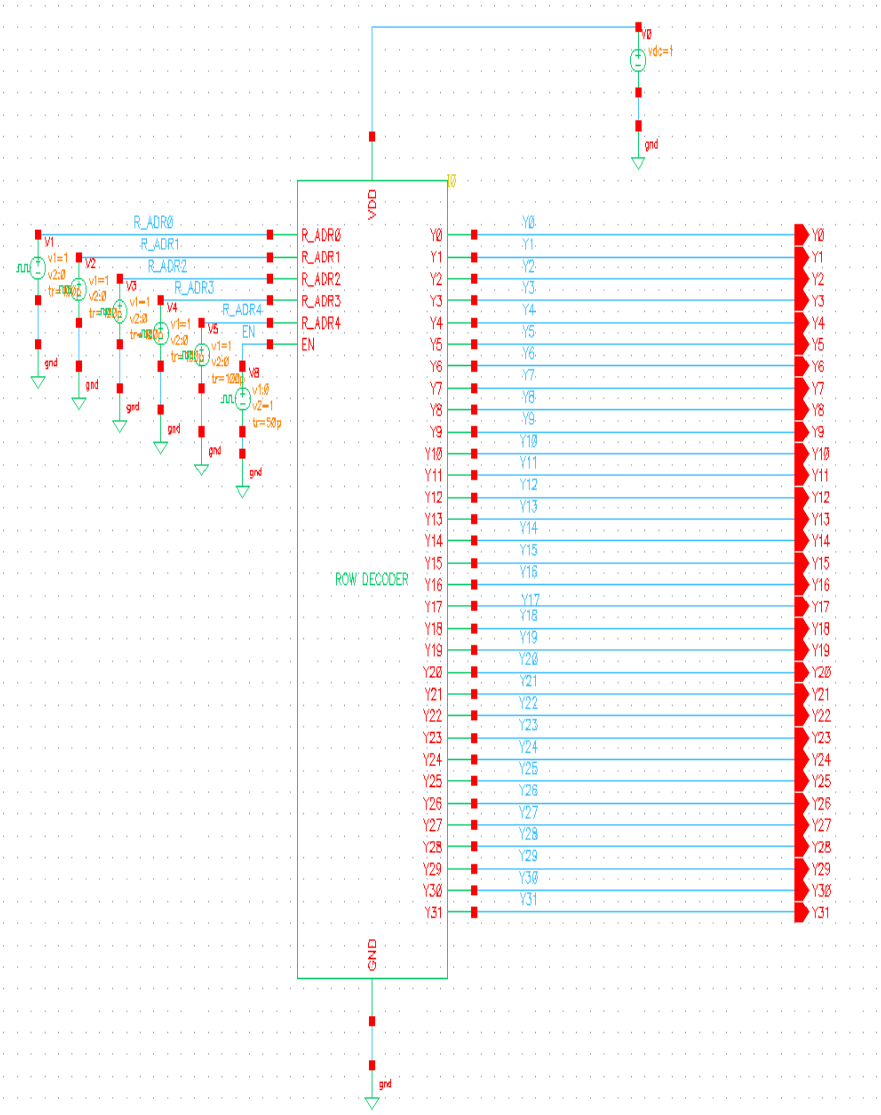

Fig 3.7.1 Test Circuit for 5:32 Row Decoder

While considering these decoders, it is imperative to keep the complete memory floor plan in context. When the number of inputs is more than or equal to four then the speed of operation of the decoder is effected so pre-decoders are to be used which reduces the large fan-in such that the speed of the decoder is improved. The principal level is the pre decoder where two groups of address inputs and their complements are first decoded to initiate one of the pre-decoder yield wires separately to obtain the partially decoded outputs. The pre-decoder yields are consolidated at the following level to enable the word line. The decoder delay comprises of word line wire delay, interconnect delay of pre-decoder and gate delays in the critical path. As the wire RC delay develops as the square of the wire length, the wire delays inside the decoder structure, particularly of the word line, gets to be critical in extensive SRAMs. From delay analysis, it was observed that the NOR based decoder is quicker than the NAND based decoder.

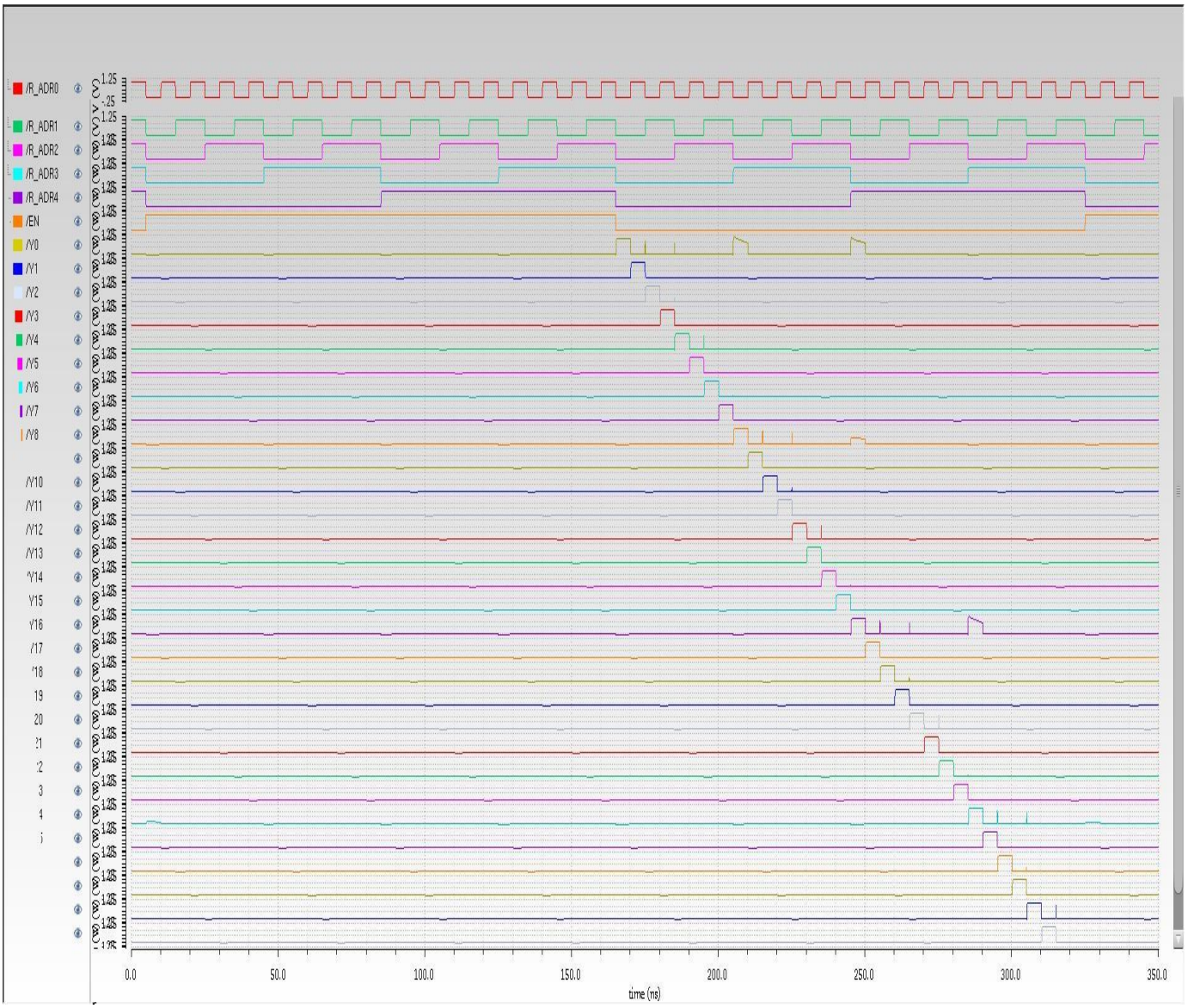

Fig 3.7.2 Simulation Result of 5:32 Row Decoder

3.8 DESIGN OF COLOUMN MULTIPLEXER

For 1-kb 8-bit SRAM block, Array is of size 32x32 and we have to select 8 out of 32 bit lines for that 4:1 column mux is used. 2:4 decoder is needed to select one of the select lines of column mux. It is better to design 4:1 mux using transmission gate logic. NMOS pass transistor logic mux works very well during write cycle as one of the bit line need to discharge to ground and NMOS is good to transfer zero logic. Fig 3.8 shows the schematic of column mux for write operation and the waveform shown in fig 3.8.1.

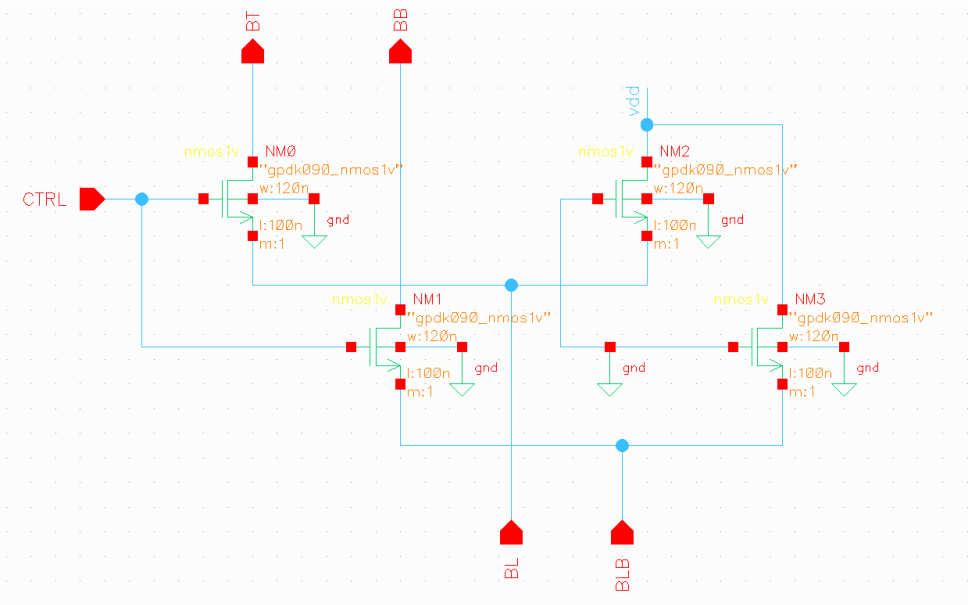

Fig 3.8. Schematic of Column mux for write operation.

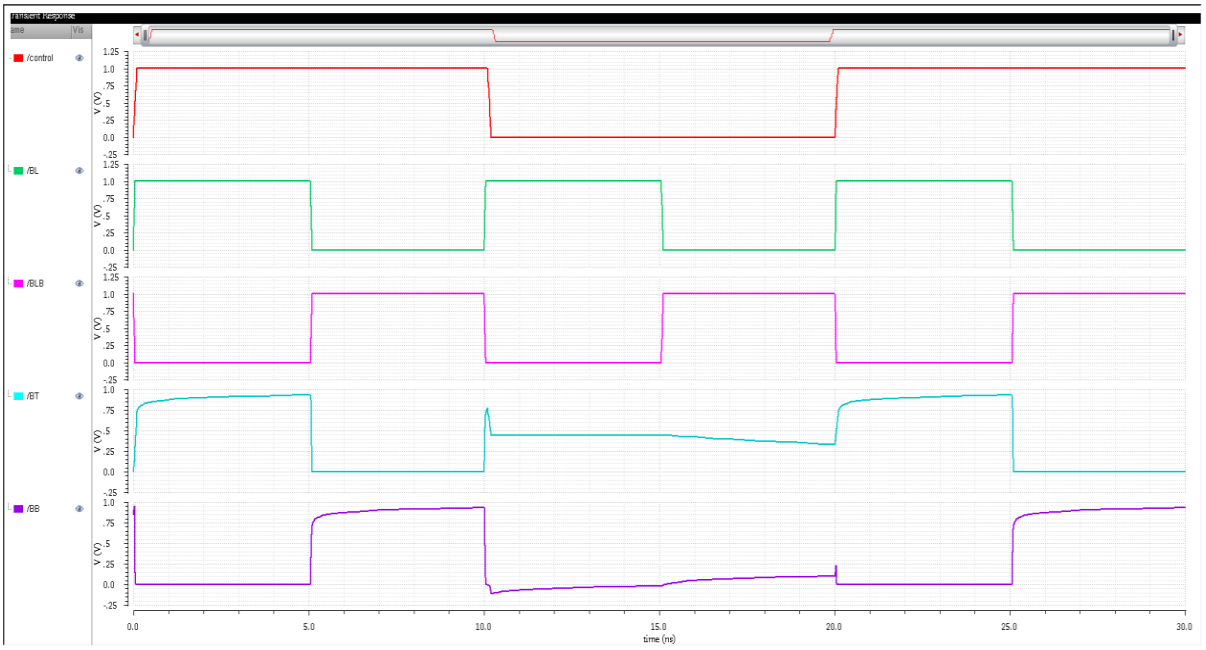

Fig 3.8.1 Simulation Result of Column mux for write operation.

During read cycle sense amplifier is connected after mux and due to bad logic 1 transfer of NMOS sense amplifier can't detect the difference in BT and BB until it goes above threshold voltage and thus increases the delay in operation so we have used transmission gate logic mux to improve the performance. Fig 3.8.2 shows the schematic of column mux for read operation and the waveform is shown in fig 3.8.3.

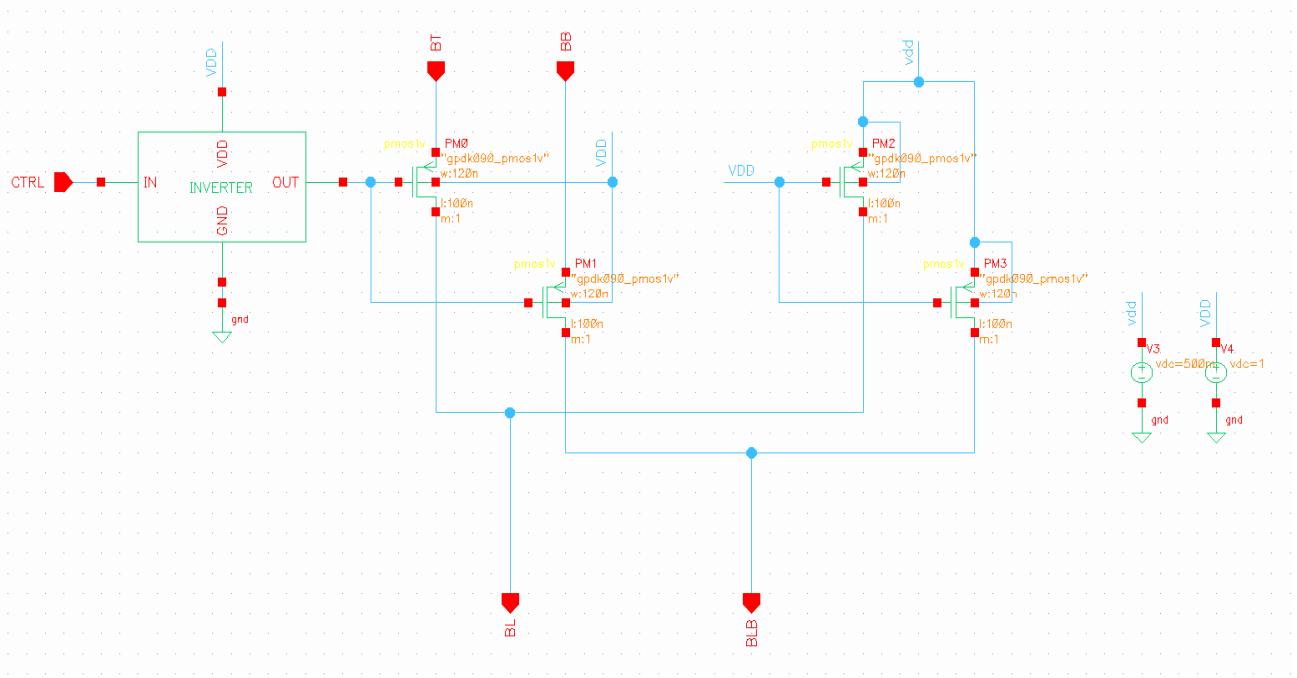

Fig 3.8.2 Schematic of Column mux for read operation.

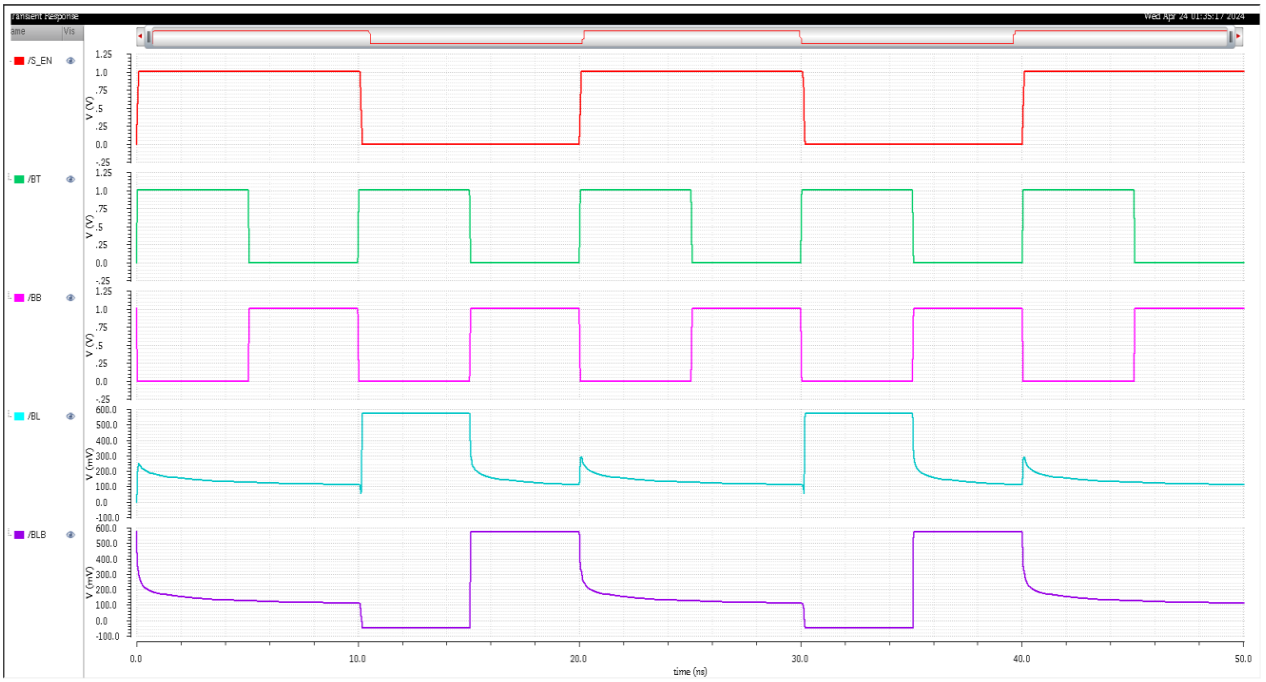

Fig 3.8.3. Simulation Result of Column mux for read operation.

A multiplexer (MUX) has been designed using transmission gates because they require fewer transistors, resulting in a smaller chip area. Additionally, the transmission gate MUX provides a full swing in the output, reducing static leakage. Both PMOS and NMOS transistors used in the design are of 90nm technology.

In this proposed work, we have designed 8-bit column multiplexer using 8 single bit column multiplexer which is shown in the Fig 3.8.2. Consider the design of 1Kb array, there is totally 32 numbers of SRAM cells present in a cell row and these 32 cells are divided into 4 portions such that the output of SRAM memory is having a size of 8 bits. So, 4 to1 multiplexer is used to select one of the portions out of 4 portions.

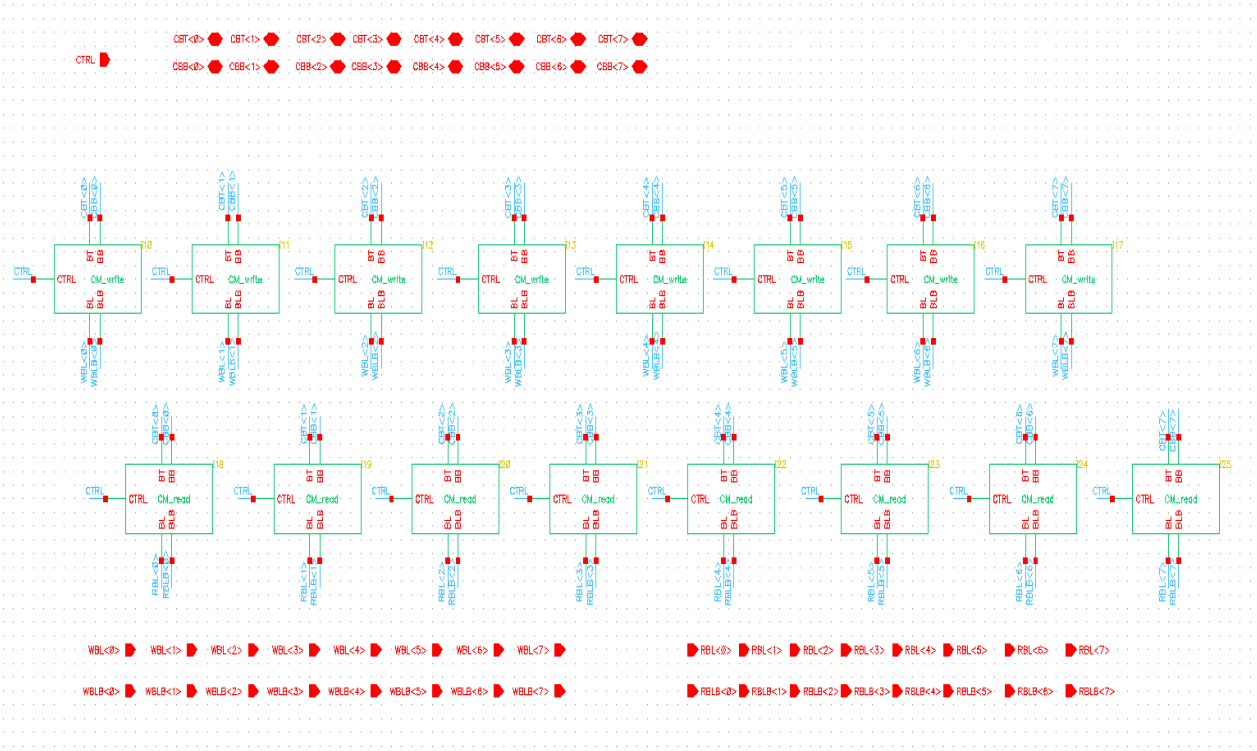

Fig 3.8.4 Schematic of 8-bit Column Multiplexer.

3.9 DESIGN OF WRITE DRIVER

In write cycle, initially both bit line BT and bit line bar BB are charged to VDD. After that, according to the data on data lines which is to be written in memory, either BT or BB is selected to discharge to ground. If logic 1 need to write in a cell the BT is charged to VDD while BB gets discharged ground and if logic 0 has to write then vice versa. Then the word line goes active and data gets written in the cell. Now, after recharging BT and BB to VDD to discharge it to ground it takes time, to minimize this we have designed a write driver for 1-bit as in Fig. 3.9, the test circuit is shown in fig 3.9.1 and the waveform is shown in 3.9.2, which makes bit lines down to the ground depends on input data. Size of transistors is more as it has to handle large current.

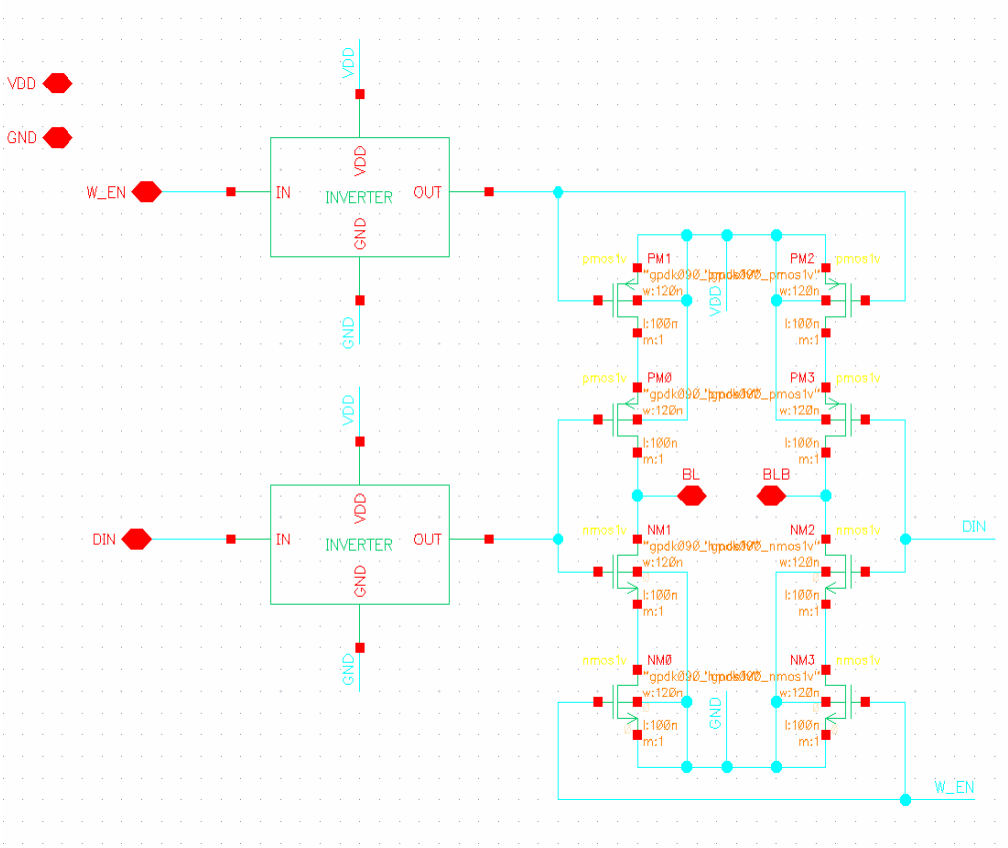

Fig 3.9 Schematic of 1-bit Write Driver

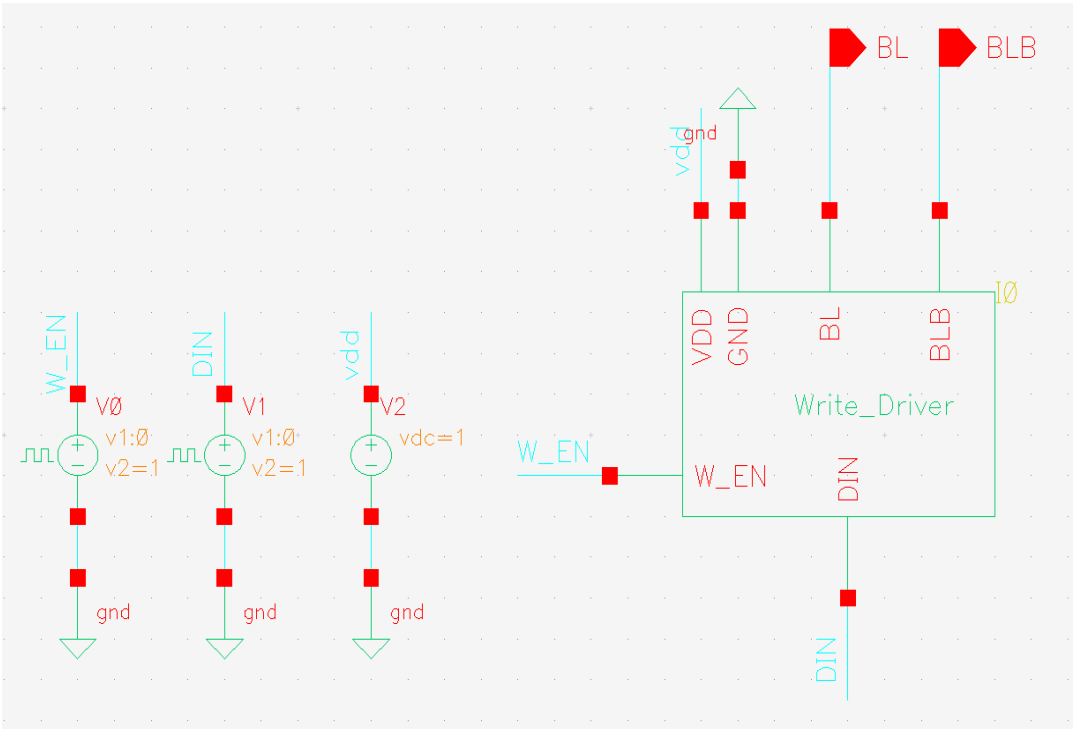

Fig 3.9.1 Test Circuit of 1-bit Write Driver

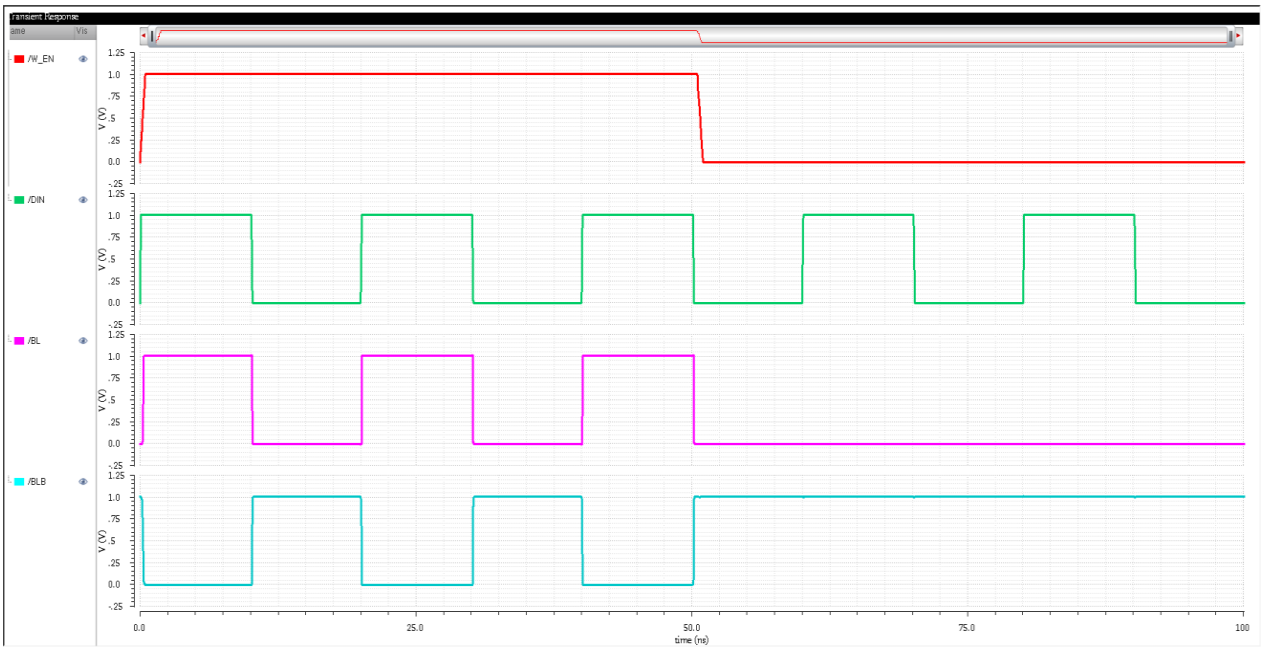

Fig 3.9.2 Simulation Result of 1-bit Write Driver

Before write operation both bit line voltages are charging to supply voltage and the write operation is performed by enabling W_EN signal. Suppose if we want to write logic 0 in to the memory cell, then the BB line voltage charges to supply voltage VDD and BT line voltage is discharges to lower potential i.e. ground. The data stored in bit line, BT and bit line bar, BB is accessed by enabling word line.

Similarly, we have designed 8-bit Write Driver to operate in 1Kb SRAM memory. Fig 3.9.3 shows the schematics of 8-bit Write Driver and the symbol for 8-bit Write Driver is shown in Fig 3.9.4.

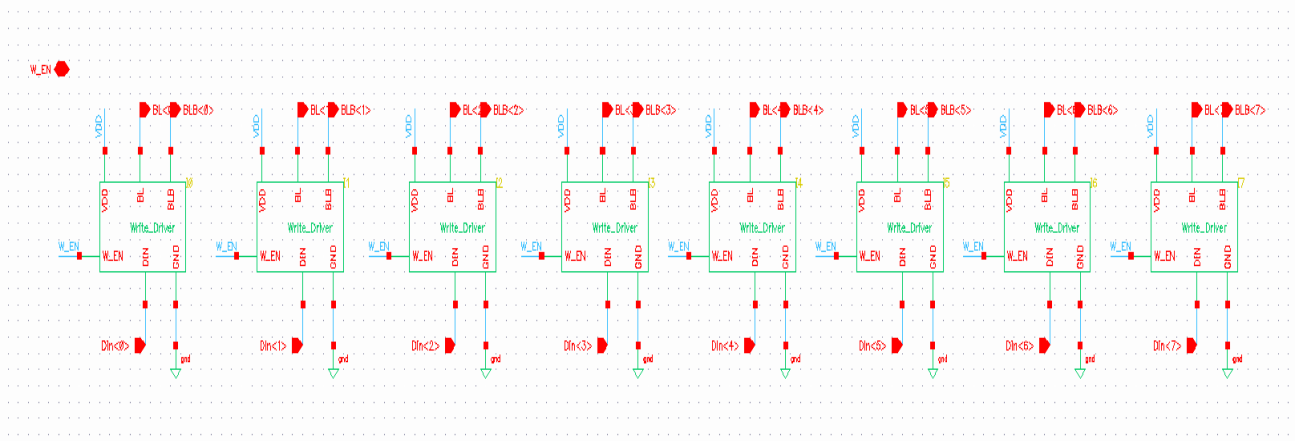

Fig 3.9.3 Schematic of 8-bit Write Driver

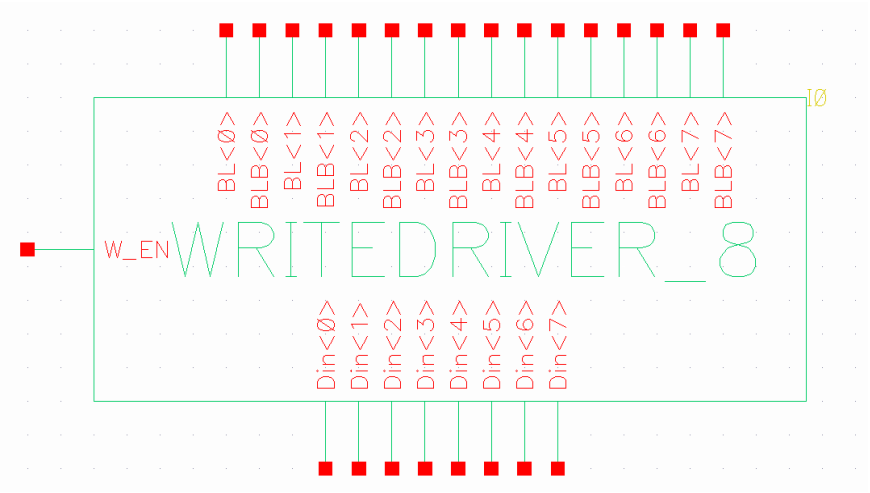

Fig 3.9.4 Symbol for 8-bit Write Driver

3.10 DESIGN OF 32*32 CELL ARRAY

SRAM cell array size and its orientation are most important to consider before the start of circuit design. For the design of bigger memories with particular operating frequency, we need to design the small blocks of memory which satisfy the frequency requirement and multiple use of such small blocks will give the bigger memories. Array size that is the number of rows and column of SRAM array will work for some maximum frequency, if we want to increase the speed, array size will go on reducing so that delay will be less. Not only has the speed that decides the number of row and column in the SRAM array, but aspect ratio also needed to be considered. 1:1 is the perfect aspect ratio of no. of rows to column. Suppose, for 1-Mb 8-bit SRAM memory, 1-kb is block we

are using so that operating frequency will be very high. Therefore, for 1kb SRAM the memory array should have an aspect ratio as 128x8. It is not practically good to go with such aspect ratio and also bit line capacitance increases with increase in bit line length. So, we have divided the 128 rows into 4 portions and used a 4:1 Mux to select one out of these. Now the memory array is perfectly square that is aspect ratio of 32x32 and is shown in fig 3.10. Enlarged view of cells in 32*32 cell array is shown in the fig 3.10.1.

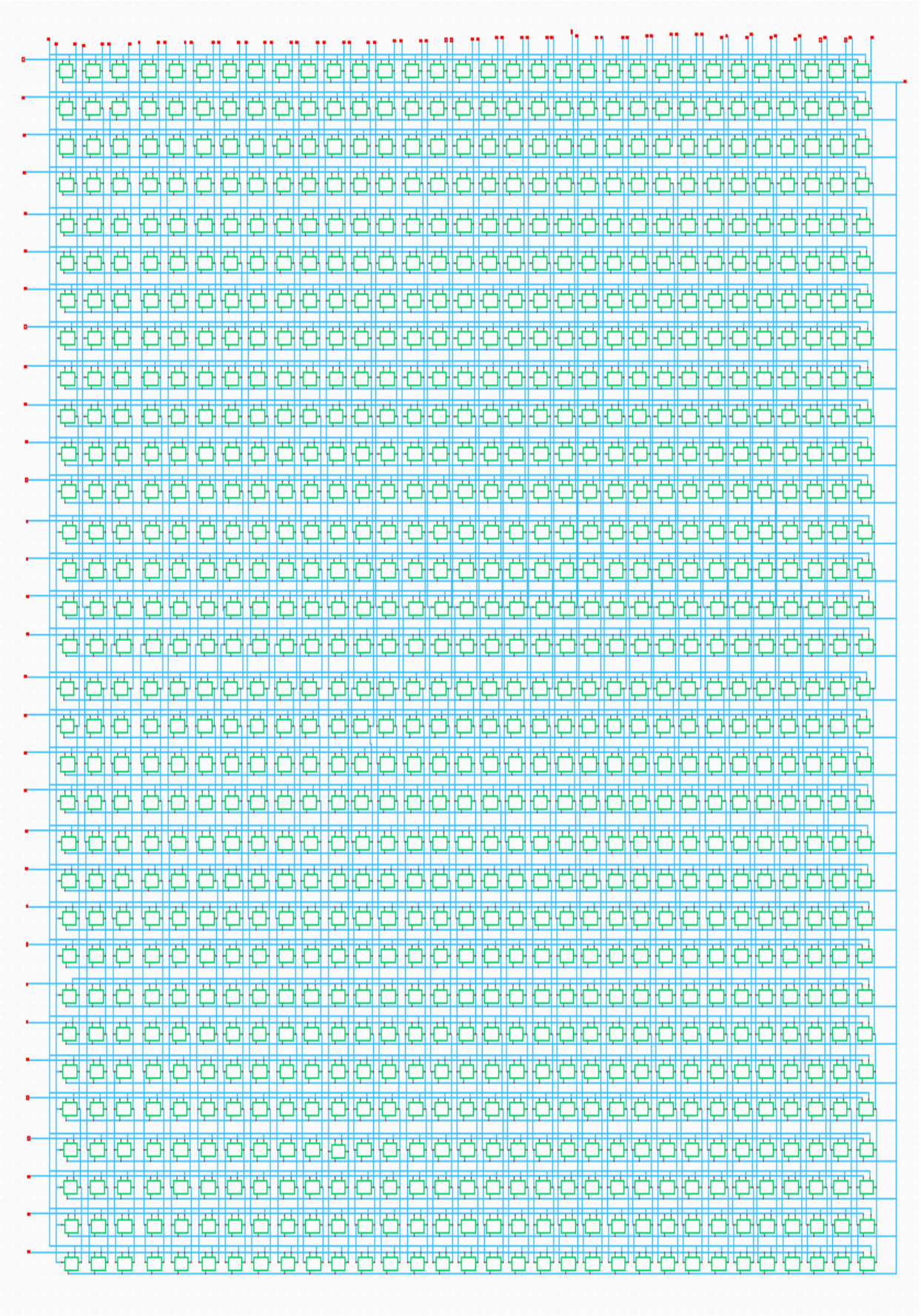

Fig 3.10 Design of 32*32 Cell Array

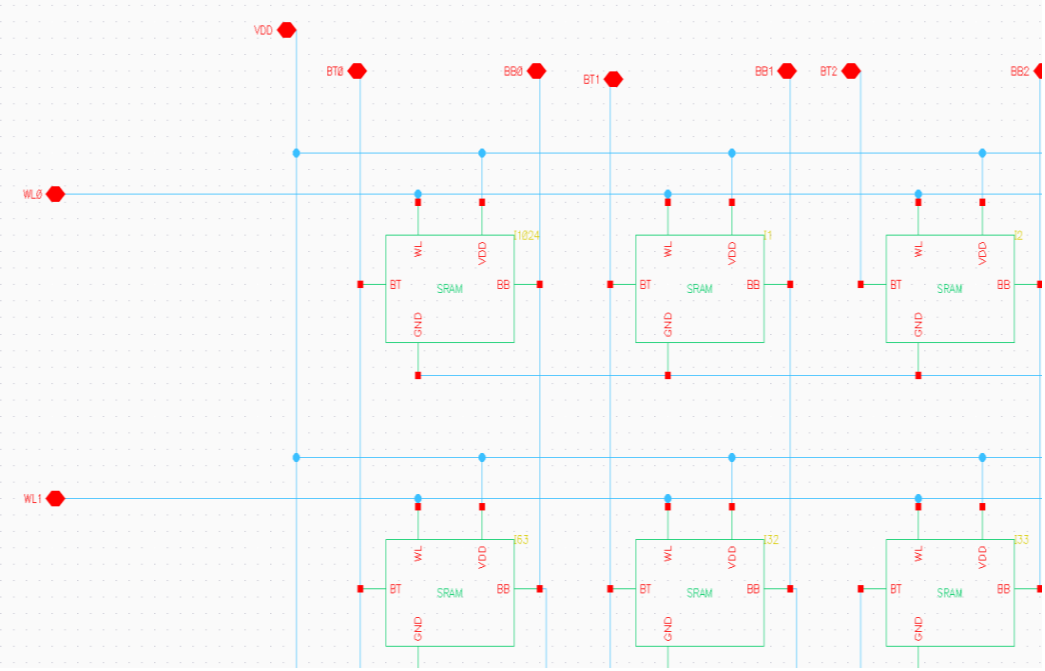

Fig 3.10.1 Enlarged View of cells in 32*32 Cell array

3.11 DESIGN OF 1Kb SRAM MEMORY

1-kb SRAM memory contain blocks like precharge circuit, row decoder, cell array, column mux, sense amplifier, write driver. Complete schematic of 1-kb SRAM is shown in fig. 3.11. For 1-kb SRAM the memory array should have an aspect ratio as 128x8. It is not practically good to go with such aspect ratio and also bit line capacitance increases with increase in bit line length. So, we have divided the 128 rows into 4 portions and used a 4:1 Mux to select one out of these. Now the memory array is perfectly square that is aspect ratio of 32x32.

The SRAM can perform read and write operations at the granularity of a single bit. The row and column decoders enable efficient access to any memory location within the 1kb SRAM. Sense amplifiers are essential for reliable data reading due to the small voltage differences within the SRAM cells. Precharging bit lines helps maintain a stable starting point for read operations.

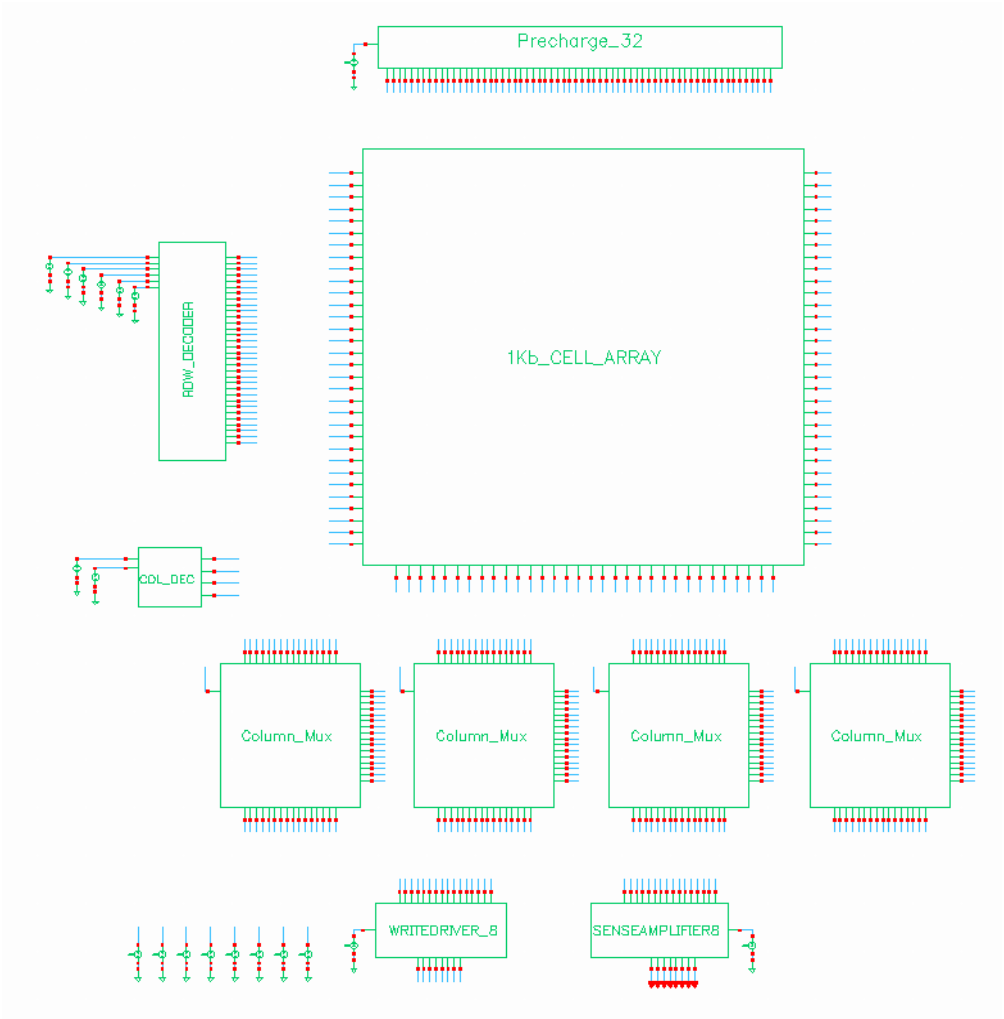

Fig 3.11 Schematic of 1Kb SRAM Memory

The sense amplifier plays an important role in the functionality, performance and reliability of the memory circuits. Precharge circuit is used to charge both bit lines to VDD. It is to be performed before every read and write operation. As bit lines have high capacitance, precharge circuit needs to provide large current to bit lines to get charged quickly. In write cycle, initially both bit line BT and bit line bar BB are charged to VDD. After that, according to the data on data lines which is to be written in memory, either BT or BB is selected to discharge to ground. If logic 1 need to write in a cell the BT is charged to VDD while BB gets discharged ground and if logic 0 has to write then vice versa. Then the word line goes active and data gets written in the cell. Now, after precharging BT and BB to VDD to discharge it to ground it takes time, to minimize this we have designed a write driver which makes bit lines down to the ground depends on input data. For 1-kb 8-bit SRAM block, Array is of size 32x32 and we have to select 8 out of 32-bit lines for that 4:1 column mux is used. The simulation result for 1kb SRAM memory is shown in fig 3.11.1.

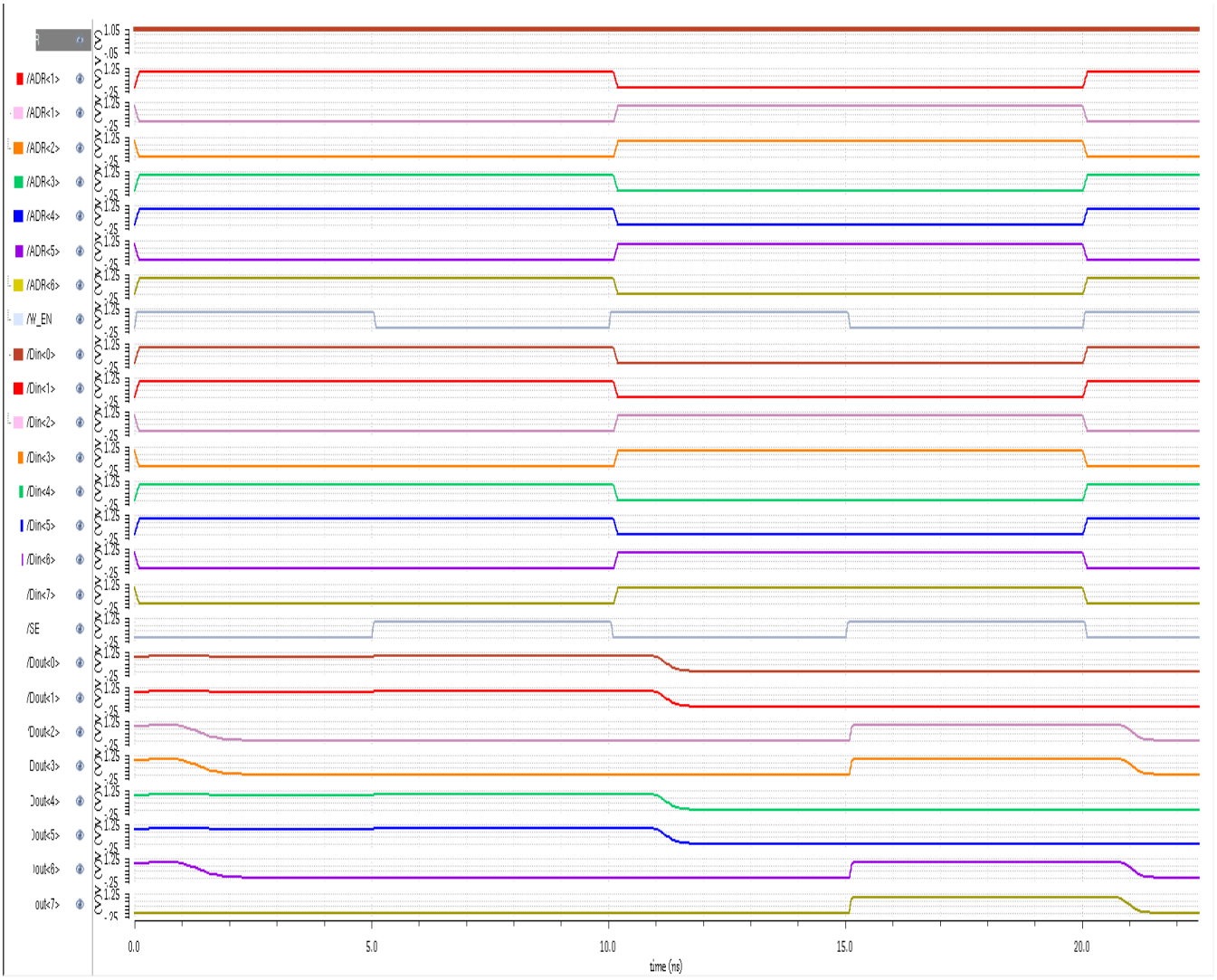

Fig 3.11.1 Simulation result of 1kb SRAM memory

CHAPTER-4

RESULTS AND DISCUSSION

4.1 Delay calculation using simulation result of 1 bit SRAM cell

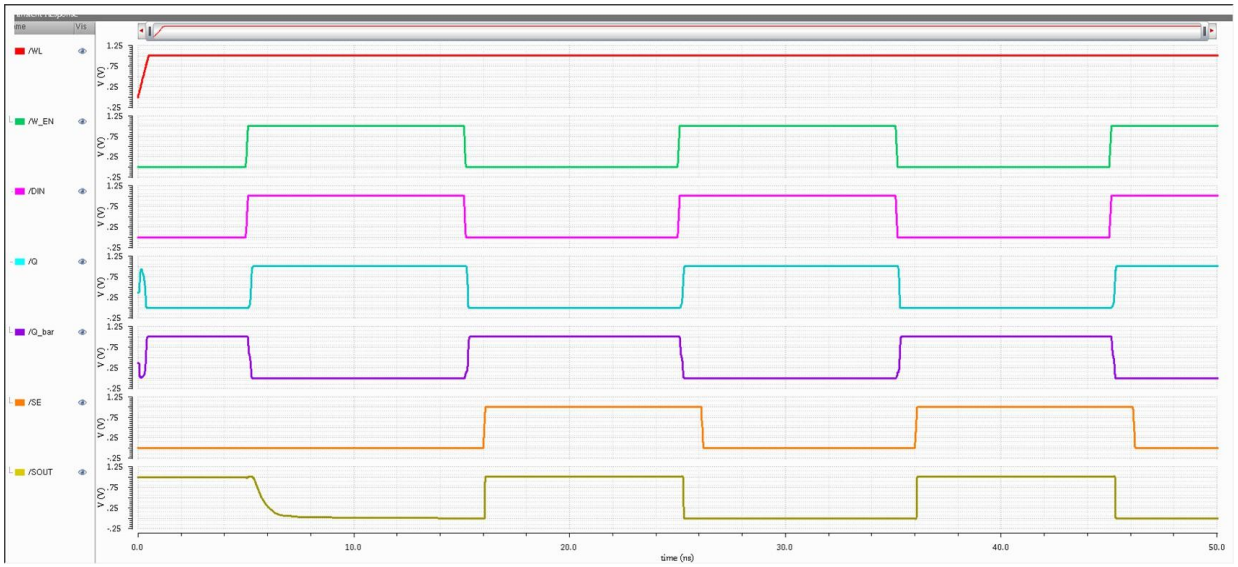

Fig 4.1: Simulation of Single bit SRAM cell

The above figure 4.1 shows the simulation result of single bit SRAM cell which is used for read delay and write delay calculation. Read delay is calculated by knowing how much time DIN will take to give input for Q and write delay is calculated by knowing how much time SE will take to give output to SOUT. Delay is calculated using above Fig 4.1 and values od delay is compared with already existing recent research paper which is shown in below comparison table.

Table 4.1: Comparison Of Delays.

Delay	Proposed design	Ref [11]	Ref [7]
Read Delay (ps)	29.4	170	267.3
Write Delay (ps)	15	180	156.3

4.2 Stability analysis of 6T SRAM cell

The stability of SRAM cell can be decided by mostly three parameters i.e. Static Noise Margin (SNM), Read Margin (RM) and Write Margin (WM).cell ratio (CR) and pull-up ratio(PR) are two parameters which effects the above three parameters.

Static Noise Margin:

SNM (Static noise margin) is a parameter which measures the stability of the SRAM cell to hold its data compared to the noise. At the storing nodes, the minimum amount of noise voltage present, which needs to be there to change the state of SRAM cell, is called SNM.

There exist two methods to measure the static noise margin of the SRAM cell.

- The first method is the graphical approach in which SNM can be obtained by mirroring the CMOS inverter characteristics and then obtaining the maximum possible square between them.
- The second approach involves the use of noise source voltages at the nodes.

SNM Dependences includes cell ratio, pull up ratio and supply voltage. The SNM of SRAM cell can be calculated by using Butter fly method which is shown in the below figure 4.2 & 4.3. Cell ratio, pull up ratio and power supply are the three important parameters which affects the noise margin of the memory cell. Around seventy per cent of noise margin value is responsible by the driver transistors.

During the reading of the data, ratio of driver to load transistors is Cell ratio, whereas pull up ratio is defined as the ratio between the sizes of the load transistor to the access transistor while writing of the data into the SRAM cell. In this proposed work cell ratio is 3.16 and pull up ratio is 2. Here Static Noise Margin is found out to be 70.578 mV and 595 mV for read and write operation respectively.

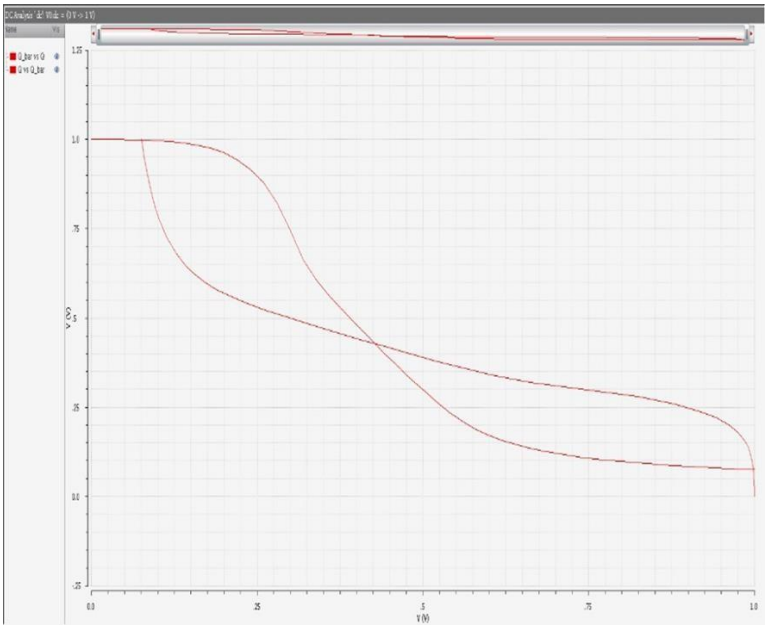

Fig 4.2: Butterfly Curve Analysis for Read Operation.

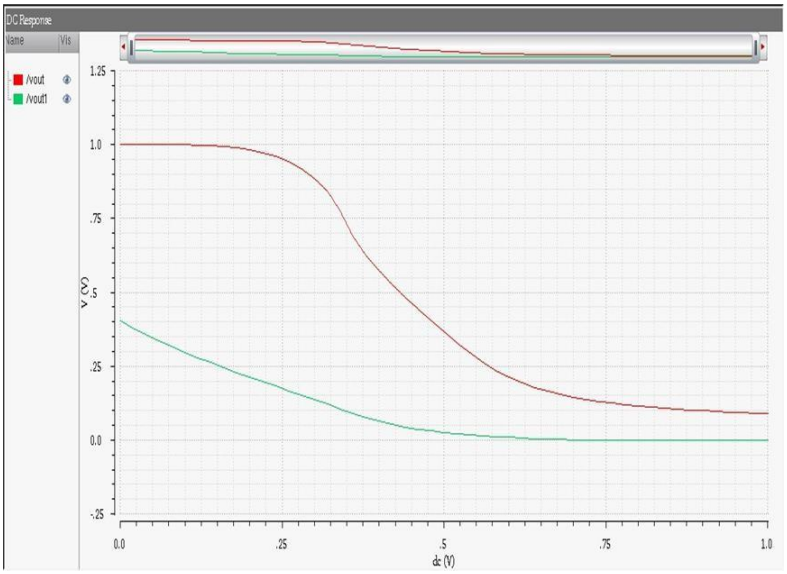

Fig 4.2.1: Butterfly Curve Analysis for Write Operation.

4.3 Power Analysis

SRAM (Static Random-Access Memory) consumes power in two main ways:

- **Dynamic Power:** This is the dominant power consumption during read and write operations. It occurs when transistors in the SRAM cell switch states. In this proposed work 82.23uW dynamic power is consumed.

- **Static Power:** This is the leakage current that flows even when the SRAM is not actively reading or writing data. It's a continuous power drain. In this proposed work 36.617nW dynamic power is consumed.

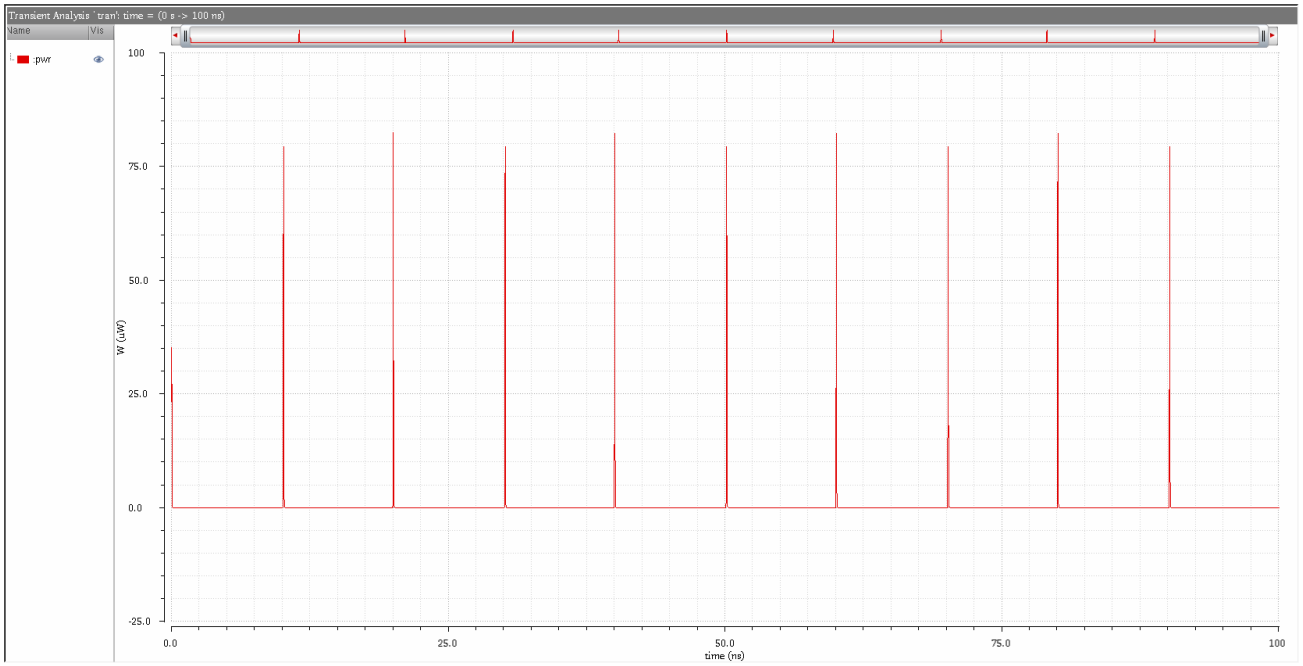

Fig 4.3. Power graph for SRAM memory

Power analysis in SRAM cells typically involves analysing the current flowing through the cell during read and write operations to understand the cell's power consumption. This analysis can be done through Simulation and Measurement. From the Fig 4.3, Simulating the SRAM cell circuit to estimate the dynamic and static power consumption under various operating conditions. Measurement can be done by using power analyzers to measure the actual power consumption during read/write operations.

CHAPTER-5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The proposed work involves the performance analysis of a 1kb Static Random-Access Memory (SRAM) using 1-bit 6T SRAM cells. The simulations were conducted using Spectre, a popular tool for circuit simulation, and the memory is designed using a 90nm CMOS technology node. The primary focus of the project is on achieving high speed, and thus, attention is given to analyzing the delay to ensure that the memory array operates within specified speed requirements. In this proposed work successfully achieved its objectives, focusing on the development of a high-speed 1kb SRAM using single bit 6T SRAM cells in a 90nm CMOS technology node.

The proposed work placed significant emphasis on achieving high-speed operation. Various design techniques, including transistor sizing, topology optimization, and circuit-level innovations, were employed to minimize access time and enhance overall speed. In the stability analysis of a single 6T SRAM cell, the design achieves a Read Noise Margin of 70.578 mV and a Write Noise Margin of 595 mV for a supply voltage of 1V. These parameters are crucial indicators of the stability and reliability of the memory cell. The Read Noise Margin ensures reliable read operations by providing a sufficient voltage difference between the stable states, while the Write Noise Margin ensures robust write operations by allowing for sufficient voltage margins to write data reliably into the memory cell.

Overall, the analysis demonstrates that the designed 6T SRAM cell meets the stability requirements for reliable memory operations. By achieving adequate noise margins and ensuring stability, the memory array can operate effectively within the specified speed requirements, thereby enhancing its performance and reliability in practical applications.

5.2 Future scope

The future works that can be conducted for manufacturing of 2kb ,1MB chip using designed 1-kb block. For that 1MB memory need to design using 1-kb block so that operating frequency will be near to 1kb design. Whereas the design of bigger memories beyond the range of Mb such as Gb can be designed by using scripting languages like Perl and SKILL because the layout design of such a bigger memory could not be drawn with the hands of a man. Hence in industries the bigger memory designs can be automated by using scripting languages to achieve better performance. By carefully considering these strategies, challenges, and future trends, which create a roadmap for designing larger memories using smaller building blocks while striving to maintain performance characteristics comparable to the original 1kb design. The optimal approach will depend on specific application requirements, technology limitations, and cost constraints.

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