Design of High Speed 9T SRAM Cell at 16 nm Technology with Simultaneous Read-Write Feature

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***Abstract*— This study presents a new 9 transistor (9T) static random access memory (SRAM) architecture with effortless and stable read operation. The proposed topology is implemented in predictive technology model (PTM) 16nm technology using LTspice software. Delay and power consumption of read and write operations, and power delay product (PDP) have been investigated and compared to traditional 6T, 8T, 9T, and 10T SRAM cells. The simulation results demonstrate that the proposed design provides fastest read operation and optimized overall PDP. The noise margin is also improved compared to existing 6T and 9T topologies.**

Keywords—SRAM, CMOS, noise margin, PDP.

I. INTRODUCTION

Many applications, such as wireless sensor networks, microprocessor and microcontroller chips, and memory cells, demand ultra-low power circuits in today's modern design techniques [1,2]. Moore's law has dramatically improved VLSI design over the previous four decades due to CMOS technology scaling, which has significantly reduced power dissipation [3,4]. The consequence of supply voltage scaling on dynamic and static power is profound. To maintain the driving current, the threshold voltage V_{TH} must be decreased in the same proportion as the supply voltage [5].

Thanks to recent advancements in CMOS technology, chips with higher integrated densities, faster performance, and reduced power consumption can now be designed. To fulfill these goals, deep-sub micron transistors have been used in CMOS devices, ranging from the 7nm node today to the 3nm node in the near future [6]. Static random access memory, or SRAM, is a type of static memory cell that is commonly used in electrical systems. Electrical systems frequently use static memory cells known as static random access memory, or SRAM. In comparison to other memory cells, it is faster and consumes less electricity [7]. Due to its lack of a recurring refresh requirement, it is the most preferred memory cell among VLSI designers.

The bit lines (BL and BLbar) in existing 6T, 8T, 9T, and 10T must be pre-charged to read the data already written to the cell for read operations. Pre-charging the read bit line (RBL) and read line (RL) to V_{dd} is also recommended [5, 8–11]. During the read process, the bit lines are discharged. As a result, which bit line will discharge is unknown because it is dependent on "Q" and "Qbar.". Scaling of V_{dd} reduces the cell's stability since pre-charged bit lines during read operation have the potential to flip the contents of storage nodes (particularly when the cell works at very low supply voltages) [8].

A redesigned 9T SRAM cell with better read operation is shown in this paper. The remainder of the paper is structured as follows: A few prevalent SRAM topologies are covered in Section III, where the suggested circuit is displayed. Section IV presents the simulation findings. Section V concludes the essay by describing the subject of more investigation.

II. DIFFERENT SRAM CELL TOPOLOGIES

Conventional 6T SRAM cell

A typical 6T memory cell, as depicted in Figure 1, is made up of two CMOS invertors that are cross-linked with two pass transistors that are connected to complimentary bit lines. Data can be written to the memory cell when the gate of access transistors M3 and M4 is connected to the WL (word line) during write and read operations [9,10]. Pre-charge both bit lines to "1" before WL is permitted to read the cell's stored data. If the stored data is "1," M1 is off and M5 is on. The value of "1" persists since node Q, where the pre-charged BL line is, prevents it from connecting to ground, and the pre-charged BLB is discharged through M4 and M5 to ground. Therefore, reads the value '0' from node QB. If the saved

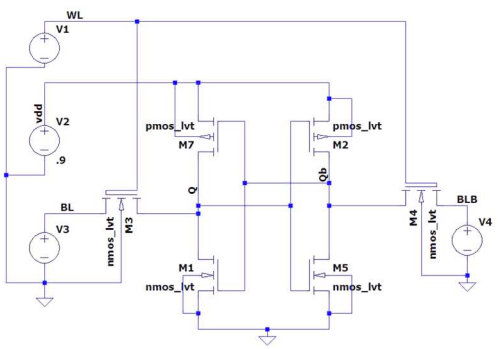

Fig. 1. Conventional 6T SRAM Cell.

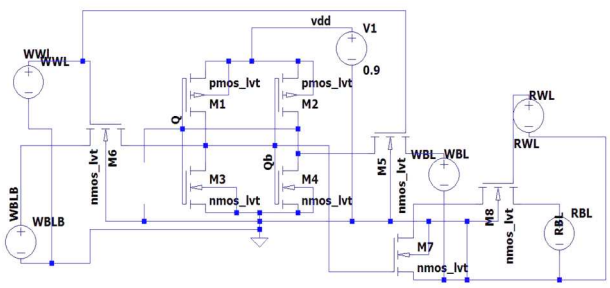

Fig. 2. 8T SRAM Cell.

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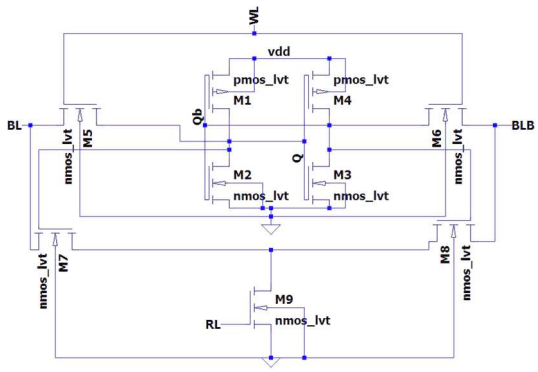

Fig. 3. 9T SRAM Cell.

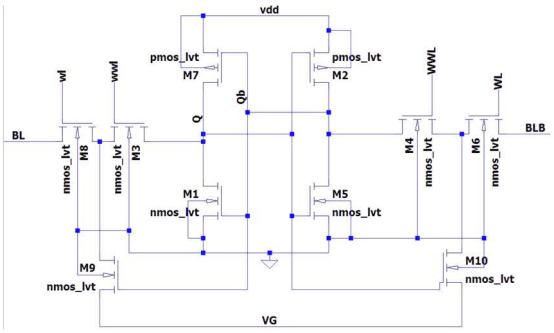

Fig. 4. 10T SRAM Cell.

data is '0', M1 is turned on, whereas M5 is turned off. BL was discharged via node Q reads '0' because M3 and M1 are connected to ground [8]. The bit lines serve as I/O buses, transporting information from the memory cell to the sense amplifier. Although they are not required, two bit lines are sometimes used to increase noise margins by supplying both the signal and its inverse. SRAM cells conduct all of the read, write, and hold operations [9,10].

enabled in read mode, and VGND is set to 0 V, but WL is disabled. During read access, the disabled makes data nodes ('Q' and 'QB') disconnected from bitline. The read SNM of 10T cell is nearly identical to the hold SNM of a normal 6T cell as a result of this isolation. After WL is enabled, one of the bitlines starts discharging depending on the cell data value. Because the read value in 10T cell is created as an inverted signal of cell data, we swap the positions of BL and BLB, as illustrated in. Both WL and are enabled to send write data from bitlines to cell nodes during write mode.

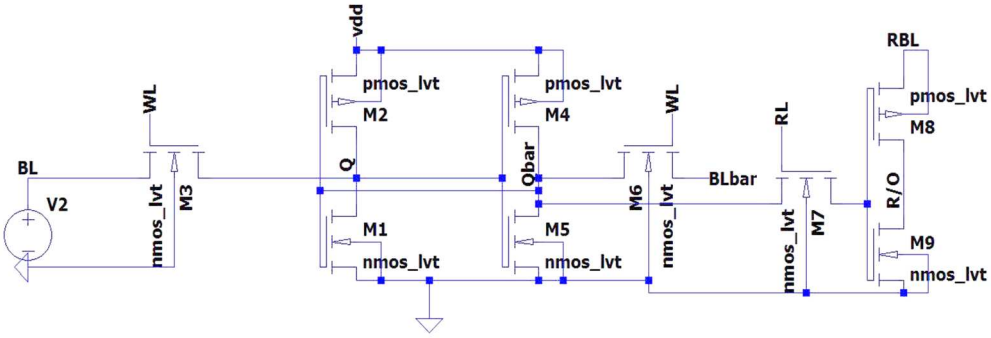

Fig. 5. Proposed 9T SRAM Cell.

8T SRAM cell

In Figure 2, we can see an 8T SRAM cell. Prior to the read cycle starting, the read bit line is pre-charged to Vdd. The read operation only takes place when both the read bit line (RBL) and read word line (RWL), depending on whether the Q is "1" or "0," are logic "0" or "1. Similar to a 6T SRAM cell, the write cycle will be the same [5].

9T SRAM cell

The upper sub-circuit of the 9T memory circuit is basically a 6T SRAM cell with the addition of the M7-M9 components, as shown in Fig. 3. The write signal (WL) controls the two write access transistors (M5 and M6). In this higher memory sub-circuit, the data is kept. The bit-line access transistors (M7 and M8) and the read access transistor are the components of the new cell's lower subcircuit (M9). The information in the cell regulates M7 and M8. A unique read signal (RD) is used to operate M9 [7]. During a read operation, the 9T SRAM cell entirely separates the data from the bit lines [11].

10T SRAM cell

10T SRAM cell [8] is shown in Fig. 4. The operating principle of our 10T SRAM can be stated as follows: WL is

III. PROPOSED 9T SRAM CELL DESIGN

Figure 5 illustrates the new 9T SRAM cell model. One most important characteristic of this circuit is that it does not need any pre-charge condition to read the data. It can also read and write data simultaneously as the read port is isolated from write operation. Two storage nodes Q and Qbar stores the data. Source of M2, M4, M8 is connected to RBL while the source of M1, M5 & M9 is connected to ground. During read operation RBL needs to be high. Data write and read commands i.e. RL & WL are given through the gate of M3 & M7 respectively. BL is given through the source of M3. Transistors M7, M8 & M9 are used to read the data. Read output (R/O) is taken from the common drain of M8 & M9. Node Qbar drives the CMOS inverter read circuit through the pass transistor M7.

A. Write Operation

Write '1': while writing '1' data is carried through M3 transistor if a write signal is given to WL & BL is provided with the input which is to be written. It is directly fed to the storage node Q which will turn on M5 and store '0' at Qbar. Qbar will activate M2 and maintaining the stored value of "1" in storage node Q.

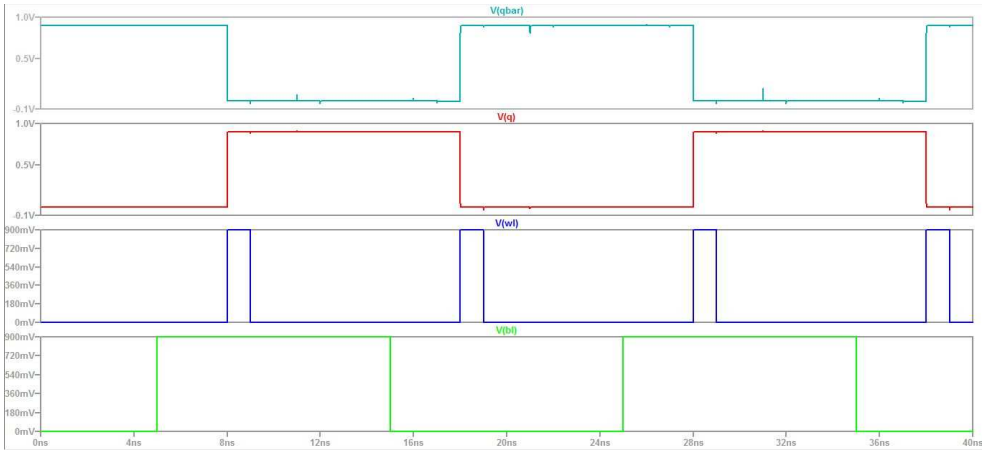

Fig. 6. Write operation of proposed 9T SRAM.

Write ‘0’: If a write signal is sent, BL supplies the data at the moment of writing "0," and M3 then processes it. Storage node Q will get the data and turn on M4 in return. M4 is connected to vdd. So, Qbar node will store ‘1’ & turn on M1. So, the data stored in Q will not change and it will store ‘0’.

B. Read Operation

Read ‘0’: Storage node Qbar stores "1" when storage node Q stores "0," and transistor M7 receives that value at its source from storage node Qbar. The logic '1' stored in Qbar and transferred through M7 activates M9, sending the read output node R/O to VSS, and the data read is '0' if RL sends a read signal.

Read ‘1’: To read data ‘1’, storage node Q needs to store ‘1’ and Qbar ‘0’. If a read signal is transported through RL, transistor M7 passes the signal at Qbar to the gate of inverter read circuit. As a result, transistor M8 will turn on and pulls up R/O node to the supply rail V_{DD} and logic ‘1’ is read.

C. Simultaneous Read-Write

Simultaneous read-write operation can be achieved in two ways. While reading the previous data, RL remains LOW and RBL remains HIGH. Data can be overwritten in the storage nodes by pulsing WL to logic ‘1’ without destroying the previous read value. On the other hand, real time data can be read with RL = 1. If data is overwritten in this case, it will be reflected at the R/O output.

IV. Simulation Results and Analysis

Proposed and existing SRAM cells are simulated in PTM 16 nm technology using LTspice platform. Read and write latency (both "0" and "1"), read and write power consumptions (both "0" and "1"), PDP, and noise margin are used to assess the performance of the topologies. All the simulations have been performed at 0.9 V supply voltage.

Transient analysis of the proposed SRAM cell is shown in Fig. 6. Hold and Write 1/0 operations are presented. Both data are successfully written with perfect voltage levels. Data is also overwritten successfully without any distortions.

Reading data is much more challenging than writing data in SRAM. Due to stability issue the read data disappears after read cycle end. To hold exact data for a bit long makes the SRAM cell much efficient. Fig. 7 also makes it clear that the voltage stays constant throughout subsequent read operations. After one read operation, the output will not be delayed for reading the same data. It shows constant and stable values. We can even write data during the read operation. In that case, the read output does not change until providing a read signal. While doing the write operation, we can read the data from the write operation at any time. This is called a "simultaneous operation."

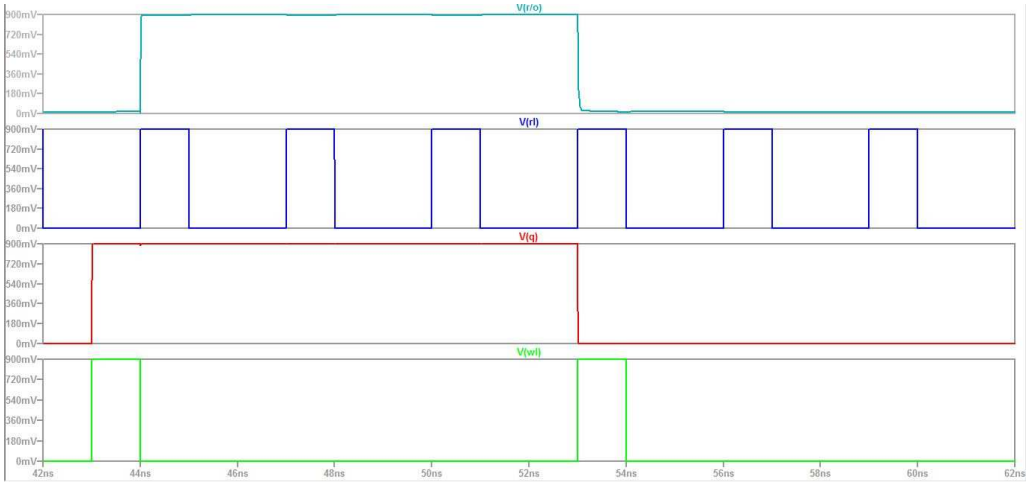

Fig. 7. Successive Read operations of proposed 9T SRAM.

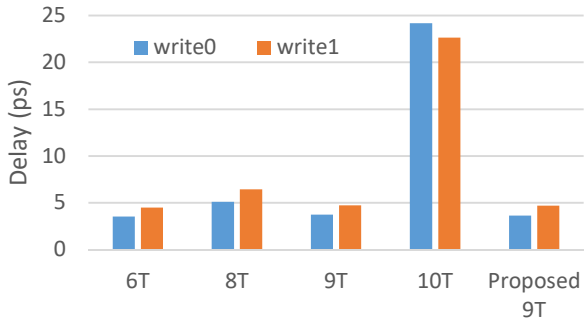

Fig. 8. Calculated write delay comparison.

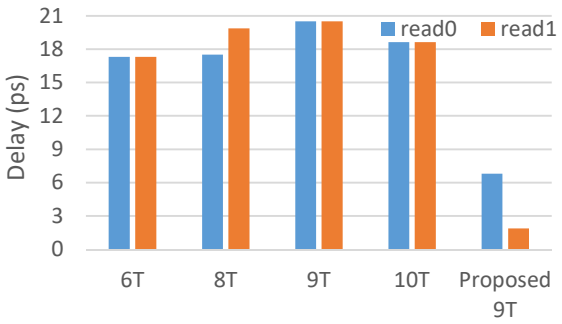

Fig. 9. Calculated read delay comparison.

Compared to existing architectures, the proposed cell provides the option of simultaneous read and write operations with no pre-charge requirement. The read operation does not hamper the write operation. Successive read operation is achieved by keeping RBL node HIGH. When read operation is not required, RBL can be kept LOW, reducing the power consumption of the circuit.

Fig. 8 shows the comparison of write 0 and write 1 delay for all the studied SRAM cells at supply voltage of 0.9 V. The proposed 9T SRAM cell has lower write 0 and write 1 delay than 8T, 9T and 10T SRAM cell but slightly greater than 6T SRAM cell.

TABLE I. COMPARISON OF WRITE AND READ POWER OF DIFFERENT SRAM CELLS

Cell	*Power (uW)*			
	Write 0	*Write 1*	*Read 0*	*Read 1*
6T	2.88	3.24	0.93	0.92
8T	11.41	10.63	0.22	0.34
9T	9.61	9.40	1.40	1.40
10T	6.67	6.19	0.14	0.14
Proposed	10.27	9.29	1.29	0.35

Fig. 9 shows the comparison of the read 0 and read 1 delay for all the studied SRAM cell. The suggested 9T SRAM cell has the lowest read delay, according to the results. The read 0 delay is reduced by 34.32 percent, 35.03 percent, 44.54 percent, and 38.97 percent when compared to 6T, 8T, 9T, and 10T cells, respectively. Meanwhile, read 1 latency is reduced by 89.08 percent, 90.48 percent, 90.78 percent, and 89.85 percent, respectively, as compared to 6T, 8T, 9T, and 10T cells.

The write and read power consumptions of the examined cells are compared in Table I. In comparison to the 8T and 9T SRAM cells, the proposed 9T SRAM cell has a lower

TABLE II. POWER DELAY PRODUCT OF READ AND WRITE OPERATIONS OF DIFFERENT SRAM TOPOLOGIES

Topology	*PDP (aJ)*			
	(write 0)	*(write 1)*	*(read 0)*	*(read 1)*
6T	*10.20*	*14.50*	*16.17*	*15.94*
8T	*58.42*	*68.46*	*3.92*	*6.75*
9T	*35.85*	*44.37*	*28.70*	*28.70*
10T	*161.21*	*140.14*	*2.61*	*2.61*
Proposed	*37.41*	*43.67*	*8.74*	*0.66*

TABLE III. COMPARISON OF READ NOISE MARGIN OF PROPOSED CELL WITH THE CONVENTIONAL 6T AND 9T SRAM.

Cell	*Read Noise Margin (RNM) (mV)*
6T	*59*
9T	*150*
Proposed	*189*

write power, but a greater write power than the 6T and 10T SRAM cells. The suggested 9T SRAM cell's read 0 power is lower than that of a 9T SRAM cell and closer to that of a 6T SRAM cell. The read '1' power of the proposed 9T SRAM cell is lower than that of the 6T, 8T, and 9T SRAM cells, but slightly higher than that of the 10T SRAM cell. Result shows that for the proposed 9T SRAM cell the read 0 Power is 7.8% and read 1 Power is 75% better than the 9T SRAM cell.

Table II presents the comparison of PDP of different SRAM topologies. Moreover, for the proposed 9T SRAM cell the read 0 PDP is 69.5% and read 1 PDP is 97.7% greater than 9T SRAM cell. Our proposed 9T SRAM cell has reduced PDP than 8T, 9T and 10T SRAM cell. In Table III, the suggested cell's read noise margin is contrasted with that of existing 9T and 6T topologies. Results shows that the proposed read circuit provides improved noise margin.

V. CONCLUSION

This study compares a modified SRAM cell with 9 transistors to previously reported standard cells, including 6T, 8T, 9T, and 10T. The focus of this paper is to make read operation faster and easier. The proposed SRAM cell circumvents the need of bit lines pre-charging and isolates read operation from write circuit. Hence, simultaneous read and write operations can be achieve with effortless and stable read operation. The read delay of the suggested circuit is reduced by at least 34.32% and 89.98% for reads of "0" and "1," respectively, compared to published studies in literature, along with enhanced noise margin and low PDP. The unsymmetrical operation, which may be addressed along with power consumption in future development, is indicated by the difference in time between reads "0" and "1".

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