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Design and Analysis of Area and Power Optimised SRAM Cell for High-speed Processor

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***Abstract*—The basic 6T Static random access memory (SRAM) cell experience from relatively high static and total power loss problem, to solve this 8T, NC cells were designed. But this all consume more area as well as delay. Hence in this paper, 5T SRAM cell proposed and checked by Monte Carlo Simulation. The area reduced by 20.3%, 20.42%, and 7.82% compared to NC, 8T, and 6T cell respectively. The total power is reduced by 95.05%, 94.2%, and 96.6% compared to NC,8T, and 6T. Similarly, static power is diminished by 57.8%,75.8%, and 79.9% compared to NC, 8T, and 6T. Speed of proposed cell improved by 52.3%, 47.6%, and 53.9% compared to NC, 8T, and 6T respectively with acceptable stability. Finally, all the cells are also checked by Monte Carlo Simulation under 45 nm CMOS Technology.**

***Index Terms*—Bit Line, Signal Noise Margin, SRAM, Word Line, Write Trip Voltage.**

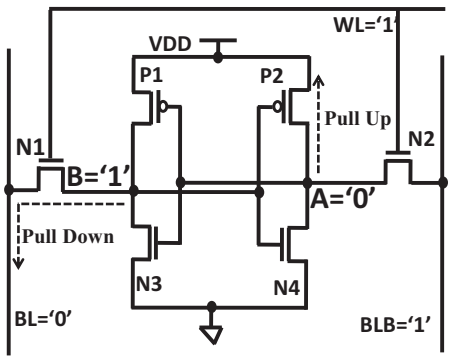

Fig. 1. Architectural diagram of the 6T cell.

I. Introduction

The SRAM is uses bistable locking equipment for securing bits [1]. A few qualities, for example, data transfer capacity, control effectiveness make SRAMs perfect for the electronic machines, for example, PDAs, computerized cameras and hardware. A portion of the general employments of SRAMs are workstations, PCs, switches and other fringe types of gear, for example, CPU register records, switch cushions and hard circle supports, among others. Printers and LCD screens likewise use SRAM to spare the see of the picture printed or showed. Neural systems and adaptable hardware are developing open doors in SRAM advertise [2], [3]. The market for cell RAM is expanding at developing quickly and use and utilization of SRAM in cell gadgets is relied upon to support the market in coming time. The gadgets where SRAMs are utilized need it for either its rapid or its low power utilization [4], [5]. The SRAMs can hold rapid execution while lessening power utilization in a little bundle will offer a critical incentive in IoT applications [6], [7].

There are two wide classes of SRAM based on application: Low Power (LP) is worked in low spillage forms and utilized for battery worked gadgets. These are generally moderate and no power utilization when inert [8], [9]. At that point there are SRAM worked for elite stores, the spillage present and reserve power is entirely high and the transistors are quick, so they have high power utilization when inactive and considerably higher when working quick [10]- [15]. The other one is radiation hardened SRAM cell under high radiation environment with optimized performance of parameters.

Association of this paper is as beneath portrayed way: Section II includes the review of the fundamental SRAM cells, for example, 6T, NC and 8T cell. Section III displays the point by point structure and working standard of the proposed cell. Section IV gives the insidious incredible comparison of the power, deferral, area and reliable nature of various SRAM cells. Section V concludes the paper.

II. Basics SRAM cells

A. 6T SRAM cell

The 6T cell utilizes bistable locking hardware to store each piece [6]. The Architectural diagram of 6T cell is given in Fig. 1. The basic 6T cell pulls down through N1 and its pulls up through N2 as declined in Fig. 1. As it consume more static and total power loss, many SRAM cells had been design to overcome this problem. Few SAM cells is explained in sub sections B and C.

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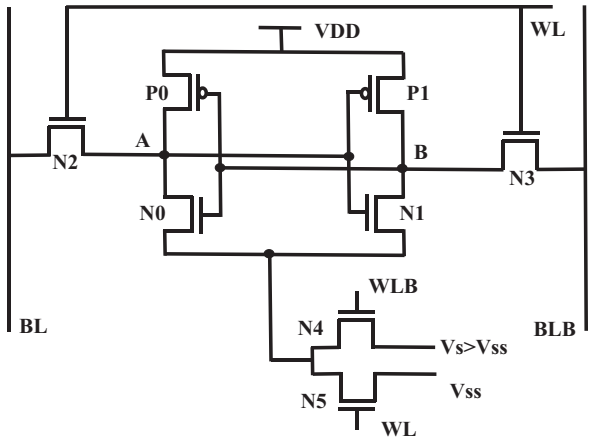

Fig. 2. Architectural diagram of the NC cell.

B. NC SRAM cell

The NC cell [12] is planned for most prominent spillage decline for possible later use and embedded memories without impacting the show basically as shown in Fig. 2. The data set away in the retention unit are held despite when the memory is working in reserve mode in this way not impacting the read/make access times during the run of the typical task. Two-fold breaking point voltage process advancement grants planning transistors with two particular edge voltages in a comparative circuit. The real job of including these two pass transistors is to give the different ground supply voltages during the various method of activity of NC-SRAM cell. The N4 and N5 give a positive and ground voltage out of apparatus and dynamic mode independently.

C. 8T SRAM cell

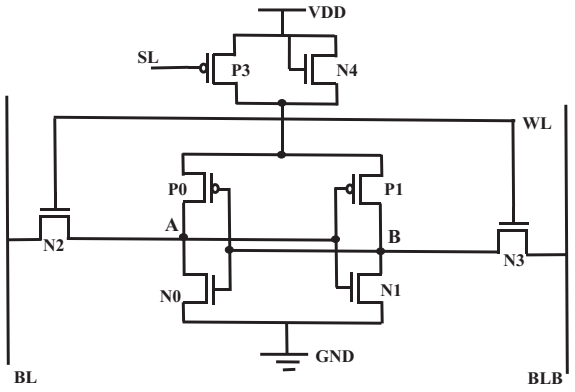

Fig. 3. Architectural diagram of 8T cell.

An 8T cell [9] contains eight transistors, as appeared in Fig. 3. The P3, N4, is utilized to give exceptional voltage levels. In active mode, the full supply voltage appeared across latch through P3 to perform a perfect read-write operation. But in hold mode, less supply voltage (VDD-threshold of N4) appeared across latch through N4. This reduces static power loss and stability.

III. Proposed SRAM Cell

A. Cell structure

The proposed cell (5T) as delineated in Fig. 4 looks alike a basic 6T cell but only difference is lack of an access transistor. Peruse and compose tasks are indistinguishable to 6T SRAM cell. Since for proposed SRAM, we require fewer transistors i.e., only five so we can save area this is the main advantage of 5T SRAM cell. Power dissipation and delay is also less when compared with other SRAM cells with acceptable stability (noise margin).

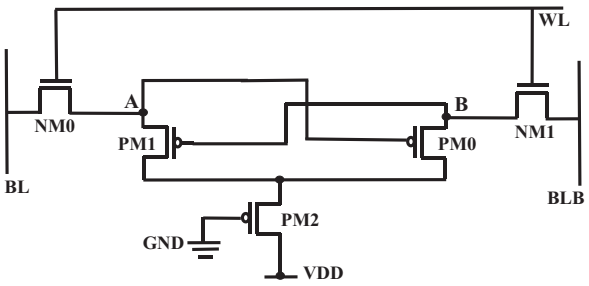

Fig. 4. Architectural diagram of the proposed cell.

B. Working principle of proposed cell

1) Write mode: The WL is given logic 1 for a write operation. As a result, NM0 and NM1 are turned "ON". The output nodes "A" and "B" are connected to gate of PM0 and PM1 respectively to form the latch. To write logic '0' on cell. The BL and BLB should be set at logic '0' and '1' respectively. As PM2 is "ON" and when "A" is logic '0', it switches "ON" the PM0 and output node "B" takes the value from supply VDD (logic '1') through PM2 (strong passer of logic '1').

2) Read mode: In read mode of the proposed cell (different from 6T) logic, '0' is applied instead of logic 1 to the bit-lines and logic '1' is applied to WL. After applying WL to logic '1', it's "ON" the access transistors NM0 and NM1. The node (assume "A"='1') which was holding logic '1' will charge the bit-line BL to '1' (weak '1' due to NM1), and the node (assume "B"='0') which was holding '0' will be pulled to logic '0'. The sense amplifier will detect the difference voltage across bit-lines (BL greater than BLB), and it gives logic '1'. Similarly, when '0' at node A and '1' at node B, then BL voltage will be less than the BLB, and sense amplifier output will be logic '0'.

3) Hold mode: In hold mode of the proposed cell, logic '0' is applied on WL; before hold mode, during write mode of cell, while writing the logic '1' on the node "A" it stores weak '1' due to access transistor NM0 (weak passer of 1). Now the WL is set to logic '0'; it will "OFF" the both NM0 and NM1. As the node "A" and "B" was holding weak '1' and strong '0' respectively. Now the node"B" will switch ON the PM1 and node B pulled up to strong '1' from supply voltage through ON PM2 (strong passer of 1). The simulated response of the proposed cell when WL is logic 1 (read write mode) and when WL logic 0 (hold) appears in Fig. 5 with all the

transistors are same size. From Fig. 5, it proved the validation of proposed cell.

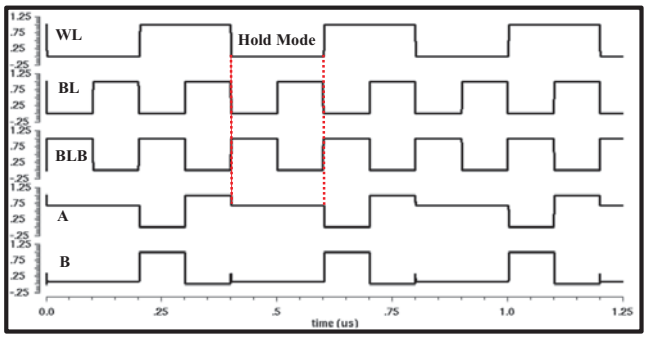

Fig. 5. Proposed cell shows perfect simulated response under same size of all the transistors.

IV. Comparison among Different SRAM Cells

A. The Write, Read Delay, and Area Comparison

The proposed cell gives better speed and area overhead compared to NC, 8T, and 6T under 45 nm Technology reported in Table I. As in proposed cell, only five transistors used, so for writing and reading the data it requires less time compared to other SRAM cells. Also due to proper size and less number of transistors its area is less compared to other cells.

TABLE I
Write, Read Delay, and Area Comparison of Cells

SRAM Cells	6T	NC [12]	8T [9]	Proposed
Write Delay(ps)	338.9	327.5	298.6	156.3
Read Delay(ps)	410.1	432.2	421.2	267.3
Area(μm^2)	1.725	1.995	1.998	1.59

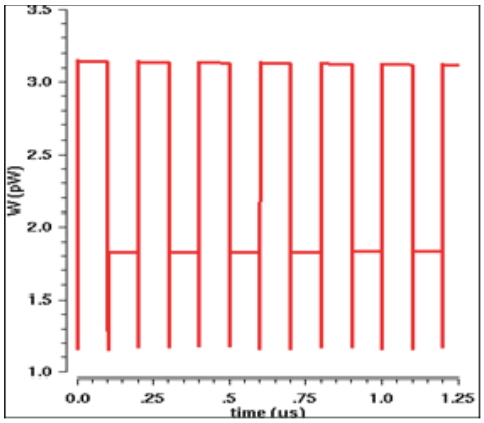

Fig. 6. Static Power loss of the proposed cell.

B. Power loss Comparison

The less transistors and optimized size of transistors in the proposed cell, reduces the total and static power loss with high write read speed and less area. Leakage power consumption give maximum contribution on total power loss and in future it may increase [16]- [**?**]. Fig 6 and 7 shows the static and total power loss responses respectively. The static power loss of novel cell is decreased by 79.9% contrasted with that of the customary 6T basic cell, 57.8% contrast with NC cell, and 75.8% contrast with 8T cell. The total power loss of the novel cell is decreased by 96.6% contrasted with that of the customary 6T basic cell, 94.2% contrast with NC cell, and 95.05% contrast with 8T cell. The power loss comparison of cells shown in Table II.

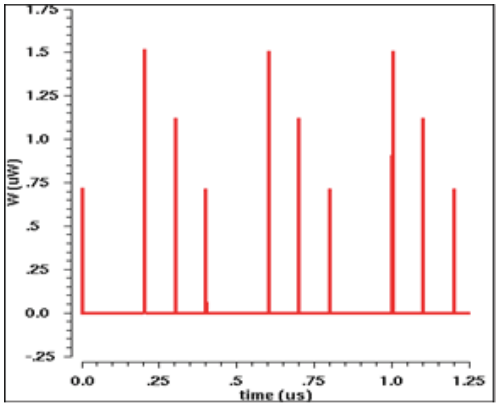

Fig. 7. Total Power loss of the proposed cell.

TABLE II
Comparison of Power Dissipation of Cells

SRAM Cells	6T	NC [12]	8T [9]	Proposed
Static power Dissention	12.47pw	5.93pw	10.35pw	2.5pw
Total power dissention	44.34nw	30.36nw	26.11nw	1.5nw

TABLE III
Stability Comparison of SRAM Cells

SRAM Cells	6T	NC [12]	8T [9]	Proposed
SVNM (mV)	354.7	319.4	321.2	212.1
SINM (uA)	35.15	17.02	10.44	8.46
WTV (mV)	491.6	440.2	432.2	292.6
WTI (uA)	-8.67	-5.04	-6.25	-3.35

C. Stability Comparison

For the SRAM based memory, noise margin is a significant parameter [6]. The disservice of estimating SNM utilizing butterfly bends is the breakdown to compute the SNM with programmed inline analyzers. The N curve method gives both voltage and current noise margin and permits to mount portrayed for the SNM [7]. N-curve for proposed cell shown in Fig. 8

The noise margin of cell during read mode is more important than write mode due to the critical path of the proposed cell. The butterfly method (same for 6T) used to calculate

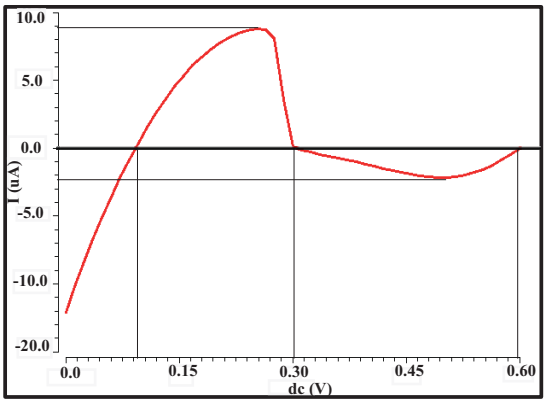

Fig. 8. N curve of the proposed cell.

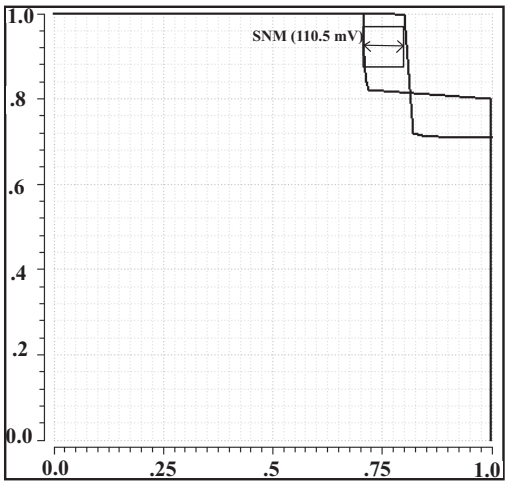

Fig. 9. Butterfly curve of proposed cell during read operation.

the stability (noise margin) while BL, BLB, and WL at logic high [6]. Two noise source is inserted between two output nodes of the proposed cell, and slowly the noise voltage has been increased. Initially, the output remains stable, but as noise voltage rises, the output difference reduces — the voltage at which output nodes flip gives noise margin. The butterfly curve of proposed cell shown in Fig. 9. Table III shows the stability comparison of cells. Stability of proposed SRAM is less and acceptable compared to other cells. From the simulation result, it is observed that the 6T cell is more stable than the novel 5T cell for the low value of cell ratio (CR). To match the noise margin of the novel cell with 6T cell, the CR value has to be high. Table IV shows the stability (RSNM) comparisons at various cell ratio.

TABLE IV
COMPARISON OF SNM (READ) FOR VARIOUS CELL RATIO

Cell Ratio	2	3	4	5
6T Cell (mV)	195.2	203.2	214.2	221.5
Proposed Cell (mV)	96.5	110.5	121.2	129.3

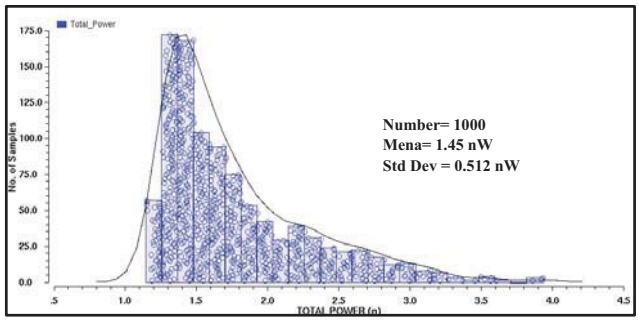

Fig. 10. Total Power loss Distribution using 1000 MC Simulation of the proposed Cell

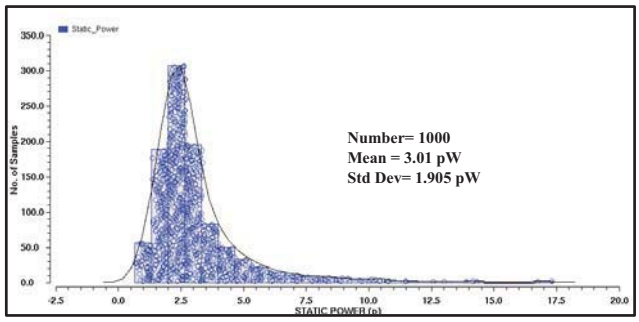

Fig. 11. Static Power loss Distribution using 1000 MC Simulation of the proposed SRAM Cell

V. STATISTICAL ANALYSIS OF SRAM CELLS

The process variation may affect the output of circuit. So it is necessary to know the variation of output due process and temperature variations. The analysis of variation during manufacturing of components can be done by using statistical analysis. The foundry company gives model file for sub-nano technology to check the variations of output under process variations. In this paper, we performed the statistical analysis to know the mean and standard deviation of total and static power is shown in Fig. 10 and 11 respectively. The statistical analysis of cells for total and static power is reported in Table V. Also the total, static power, and stability checked under different process corners are reported in Table VI, VII, and VIII respectively.

VI. CONCLUSION

In this paper, we have presented point by point recreation derive for the SRAM cells. Here, we have shown the delay, area, and power investment funds acquired in the proposed cell configuration when contrasted with the regular 6T, 8T, and NC cell. The rate reserve funds in static power loss of proposed cell, when contrasted with the ordinary 6T cell is 79.9%, 8T cell is 75.8%, and contrasted with NC SRAM it is 57.8%. Similarly the total power dissemination of proposed SRAM when contrasted with a basic 6T cell is 96.6%, 8T cell is 94.2%, and with NC cell it is 95.05%. The area-overhead is reduced by 7.82%, 20.42%, and 20.32% compared to 6T, 8T, and NC cell. The speed during write mode of proposed

TABLE V
POWER DISSIPATION DISTRIBUTION USING 1000 MC SIMULATION OF THE SRAM CELLS

SRAM Cells	Number of Samples	Total Power		Static Power	
		Mean (nW)	Standard Deviation (nW)	Mean (pW)	Standard Deviation (pW)
Proposed	1000	1.45	0.512	3.01	1.02
NC[12]	1000	30.65	1.63	6.24	2.12
8T [9]	1000	26.63	1.23	13.23	4.34
6T	1000	44.96	2.82	14.32	3.01

TABLE VI
TOTAL POWER LOSS (nW) OF CELLS AT VARIOUS PROCESS CORNERS

SRAM Cells	6T	NC [12]	8T [9]	Proposed
FF	66.8	39.1	28.9	2.11
SF	42.3	26.2	25.3	1.42
SS	28.3	21.4	34.4	1.25
TT	44.3	30.4	26.1	1.51
FS	45.3	35.2	27.9	1.91

TABLE VII
STATIC POWER LOSS (pW) OF CELLS AT VARIOUS PROCESS CORNERS

SRAM Cells	6T	NC [12]	8T [9]	Proposed
FF	142.1	93.2	131.1	47.2
SF	13.4	6.41	11.4	3.61
SS	5.51	3.32	3.5	1.1
TT	12.5	5.9	10.41	2.5
FS	28.7	21.7	26.7	7.8

cell is improved by 53.9%, 47.6%, and 53.9% compared to 6T, 8T, and NC cell. Similarly the read speed of proposed cell is improved by 34.8%, 36.54%, and 38.15% compared to 6T, 8T, and NC cell. Stability of novel cell is decreased and comparable, it can be improve by up-sizing the driving and access transistors. Overall the proposed cell is giving perfect balance among all the parameters.

TABLE VIII
STABILITY COMPARISON UNDER VARIOUS PROCESS CORNERS OF PROPOSED CELL

Process Corners	TT	FF	SS	SF	FS
SVNM (mV)	212.1	201.3	221	181.1	232.1
SINM (uA)	8.46	10.46	5.56	9.76	7.06
WTV (mV)	292.6	299	255	310.6	260.6
WTI (uA)	-3.35	-3.74	-0.435	-3.62	-0.892

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