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Low-Power and High Speed SRAM for Ultra Low Power Applications

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***Abstract*—The rapid development of battery-powered gadgets has made low-power design a priority in recent years. In addition, integrated SRAM units in contemporary soCs have become an essential component. The increased number of transistors in SRAM units and the increased leakage in scaled technology of the MOS transistors have turned the SRAM unit into a power block from dynamic and static perspectives. This memory circuitry consumes many chips and determines the system's overall power consumption. Typically, the primary 6T SRAM cell gives more power loss and delay. In this paper, various SRAM transistor cells have been built and analyzed from different topologies. A proposed low-power 9T SRAM cell area has improved reading and writing access time. As anticipated from the modeling findings, experimental results show a significant overall power decrease compared to traditional and previously published.**

***Index Terms*—Dynamic Power, high speed, process analysis, SRAM, stability, static power.**

I. Introduction

SRAM is intended to work in close collaboration with the central processor unit (CPU) and consumes less power to conserve battery life due to the fast proliferation of portable devices [1]- [5]. The speed and power parameters are critical in boosting the capabilities of electronic devices used in research and commercial facilities. With the growing need for low-power SRAMs, low-power design methodologies are concentrating their efforts on a few specific sources of power consumption [6]-[8]. Low-power methods of decreasing the SRAM cell's leakage current are necessary because of the increased leakage current associated with scaled technology. The high capacitance of the long interconnecting wires also contributes to the SRAM unit's large dynamic power consumption. Thus, the electronic industry's need for tiny and portable electronic gadgets with low power consumption and fast speed has developed significantly [9]-[13]. Therefore, designing an SRAM-based memory with optimum power and stability without sacrificing performance is tricky.

The traditional 6T cell design is relatively simple in various applications [14]-[18]. It has excellent conduction and performs well in terms of delay and power. The power dissipation of 6T, Comparatively high. The numerous types of SRAM cells, such as 7T SRAM [26], 8T SRAM, and 9T SRAM [26], are overviewed to the power consumption problem of the 6T SRAM. High static power is provided by the 6T SRAM cell [19]-[22]. An 8T is chosen and implemented to achieve low static power. The 8T SRAM cell is more stable and uses less power than the 6T SRAM cell. A new 9T SRAM cell has been proposed to overcome these limitations. The suggested SRAM has a lower power usage than a 6T SRAM [20]. Compared to a standard 6T cell, the proposed cell includes less outgoing current. Several techniques are discussed for reducing the SRAM cell's outgoing currents [23]-[25]. The power dissipation of the SRAM cell is particularly targeted.

The rest of the paper is structured as follows: The conventional SRAM cells are explained in Section II. Section III describes the proposed SRAM cell. Section IV presents and discusses the experimental results using the Cadence tool. The paper concludes with Section V.

II. Standard SRAM Cells

SRAM is made up of two cross-coupled inverters in such a fashion that it store data and provide positive feedback. When powered, it functions as a volatile memory, storing data. It accelerates 'read' and 'write' operation using BL and BLB bit lines.

A. 6T SRAM Cell

The CMOS standard 6T SRAM cell has two PMOSs, two NMOSs, and two NMOSs as access transistors. Two data-storage inverters are manufactured and cross-coupled so that positive feedback is generated. The two inverters are P0, N0, and P1, N1. It also has vertically aligned Bit Lines

(BL and BLB) and a horizontally oriented Word Line (WL) [20]. SRAM has three modes of operation: standby, read, and write. Vdd is provided to BL during standby mode, and WL is switched off, causing the transistors connected to it to turn off as well.

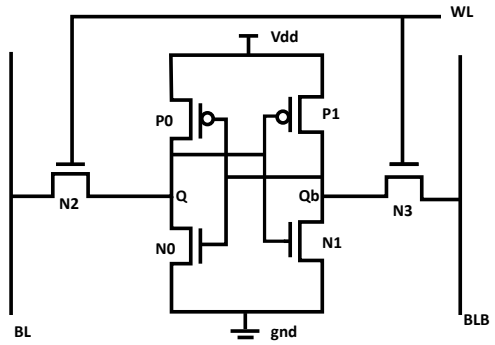

Fig. 1: Schematic diagram of 6T SRAM cell.

The two cross-coupled inverters provide positive feedback since BL=Vdd, allowing data storage while power is supplied. Only read and write operations are permitted on the WL line, which controls the state of the access transistors.

Sense Amplifier: A sense amplifier is required for memory circuits to attain high performance, endurance, and usefulness. It is a part of the read circuitry responsible for reading data from memory. Its purpose is to monitor low-power signals from a bit line and convert the tiny voltage difference to full logic voltage, representing the data bit stored in a memory cell, thus significantly reducing read time. It includes voltage sensing, low-voltage amplification, delay reduction, power consumption [4] reduction, and signal restoration capabilities. They are mainly used to amplify the differential voltage across complementary bit lines during 'read' operations without flipping the stored cell data, enabling the data to be adequately handled by the memory's output circuitry. To function correctly, the SRAM cell must have a Static noise margin (SNM) since this determines the dependability of sensing data from the chosen cell [5]. Since the driving transistors do not need to discharge the bit lines completely, the inclusion of a sensing amplifier reduces the size of the memory cell. The sensing amplifier's design significantly impacts the read speed and power consumption.

It has seven transistors, two of which serve as differential input devices (N0 and N1). They function as driver transistors and accept inputs, while transistors P0 and P1 work as active current mirror loads, transistors N3 are current sources, and transistors P2 and N4 are inverter transistors (amplifier). The control circuit generates a sense enable

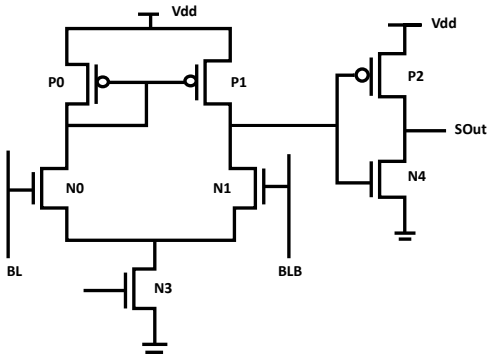

Fig. 2: Schematic diagram of Sense Amplifier.

signal (SE) to activate the sense amplifier. When this enabled signal is high, the sensing amplifier increases the differential voltage of the bit lines (active). Amplification of differential voltage results in a single-ended digital output reflecting one bit read from the SRAM array.

Pre-charge circuits: It is used to quickly and painlessly charge both bit-lines voltages to VDD before each read and write operation. The pre-charge circuit is shown. It comprises two pull-up PMOS transistors and an equalization that balances the voltages on both bit lines [4]. The pull-up transistors are controlled by the PR signal, which controls the transistor P3, an equalization signal that balances the voltage on both bit lines. The term "Vdd pre-charge" refers to the pre-charge. PMOS transistors are utilized in the pre-charge circuit because they are the most efficient at transmitting the Vdd level voltage to the bit lines.

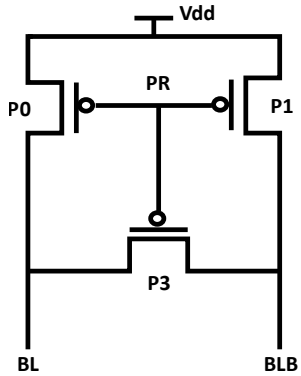

Fig. 3: Schematic diagram of Pre-charge circuit.

When the word lines are activated, the memory cell nodes must raise the voltage on the bit lines to a level adequate to read the correct data value from memory during a read operation. Due to the high load capacitance of the bit lines in large memory arrays, charging and discharging them takes

a lengthy time. Waiting for the bit-line capacitance to drain before performing the next read operation may be an issue since it adds time to the 'read' process. Additionally, an error may result if the subsequent read operation occurs before the bit lines have been discharged. Consequently, a pre-charge circuit is required to provide a high current to bit lines to charge them fast. To do this, a pre-charge circuit is used to charge both bit-lines to a steady voltage Vdd. Since the voltage on both bit lines is known and steady, the voltage difference may be easily detected.

Write access time: The time interval between the positive edge of the word line reaching 50% Vdd and the junction of the two storage nodes Q and Qb are defined as the memory cell's write access time.

Read access time: The period between the positive edge of the word line hitting 100% Vdd and the sensing amplifier output reaching 100% of the stored value is the read access time of a memory cell.

B. 7T SRAM Cell

Before write operation, The 7T SRAM cell disables the feedback link between the two inverters inv1 and inv2. An additional NMOS transistor N5 handles feedback connection and disconnection, and the cell is completely reliant on the BL bar for a write operation.

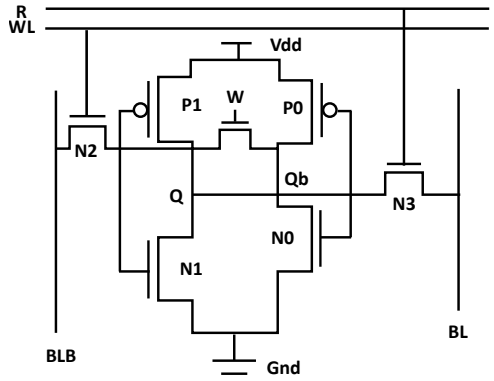

Fig. 4: Schematic diagram of 7T SRAM cell.

C. 8T SRAM Cell

The architecture of the 8T SRAM cell is depicted in the figure. It features two extra transistors N4 and N5 as compared to a standard 6T SRAM cell. Precharging BL is the first step in the read process. The reading is then initiated by setting RD to Vdd [3]. If bit 1 is stored in the cell, Q is at Vdd and Qb is at the ground. During the read process, the precharged BL begins to discharge via N4 and N5. Discharging should be fast enough to keep up with the rate at which BL leaks through all of the unaccessed SRAM cells connected to it. As a consequence, the read circuit can correctly identify the data.

If bit 0 is stored in the cell, BL should not discharge and should stay at or near Vdd. In this case, the read circuit should calculate the value of BL before leakage reduces it considerably. To assist retain the value one in the bit line, we connected a weak pull-up to the read circuit. Because short bit lines have low capacitance, they facilitate the charging and discharging of SRAM cells and peripheral circuits [10]. As a consequence, transistor sizes are reduced, leakage is reduced, and reliability is enhanced.

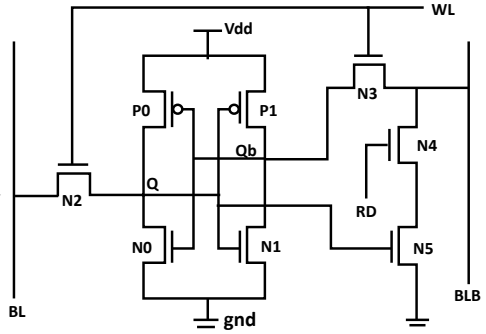

Fig. 5: Schematic diagram of 8T SRAM cell.

D. 9T SRAM Cell

The 9T SRAM's top circuit is identical to the 6T SRAM's but with fewer transistors. The two access transistors are controlled by the word line (W), and the data is stored in this subcircuit. A separate read signal (R) controls the bottom circuit, which consists of a single read access transistor [26].

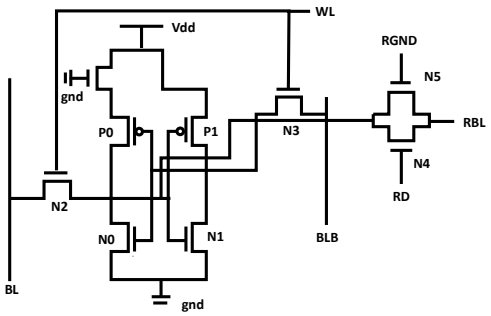

Fig. 6: Schematic diagram of 9T SRAM cell.

III. THE PROPOSED 9T SRAM CELL

A new 9T SRAM cell is being developed. Compared to a standard 6T SRAM cell, it has three more transistors, N4, N5, and N6. Figure 7 shows a single-sided read circuit. It

takes up less space and does not rely on the perfect timing of control signals, as the differential read of a typical sense amplifier circuit does. Figure 7 depicts the write circuit. One of these circuits is for BL, and the other receives the data bit and its inversion as input. Because PMOS transistors are larger than NMOS transistors, their pullup and pulldown currents are symmetrical, allowing the write circuit to drive both 0 and 1 to the bit lines. The reliability and static power

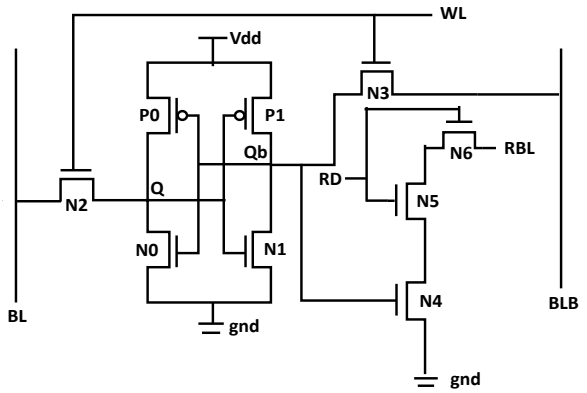

Fig. 7: Schematic diagram of Proposed 9T SRAM cell.

consumption of transistors are the primary determinants of transistor size. The dimensions used are listed in Table I. P0 and P1 have the narrowest widths allowed by the technology. Vdd leak currents are reduced as a result. In 6T SRAM, the pull-down NMOS transistors N0 and N1 are wider than the access transistors N2 and N3. This improves cell stability during read operations when 6T SRAM is most susceptible to undesirable state change. Because N2 and N3 are not used during read operations, the widths of the pull-down and access transistors in the proposed 9T SRAM have been flipped, making write operations faster and more reliable. The width of the N4, N5, and N6 of 9T SRAM decrease leakage.

IV. Simulation and Result

The proposed 9T and other comparative SRAM cells are simulated at a 45-nm technology node in this work. The cadence virtuoso simulation tool is used for simulations.

A. Transient Response and Power Consumption

Power savings are significant in the proposed 9T cell structure, regardless of the stored value, i.e., whether the SRAM cell stores 0 or 1. When a bit cell in the 7T structure stores a 1, the PMOS is enabled, leading to significant power consumption in standby mode. When the bit cell stores a 0, the voltage difference between the drain and source raises the sub-threshold leakage via the PMOS. This grows

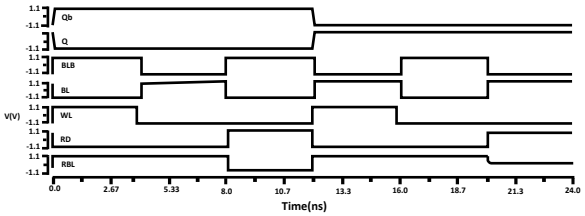

Fig. 8: Transient Responses of the proposed 9T SRAM cell.

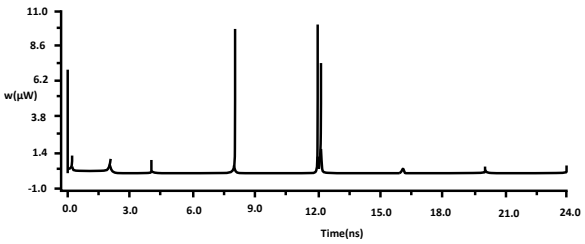

Fig. 9: Power consumption of the Proposed 9T SRAM cell.

exponentially as the threshold voltage decreases, indicating a significant leakage current component in the off-state. The average standby power consumption of the 7T structure in Figure 4, the 8T structure in Figure 5, and the 9T structure in Figure 6, the proposed 9T structure in Figure 7 when the SRAM cell stores a 0 is shown in Figure for various power supply voltages, the proposed 9T cell achieve minimum power savings in each bit cell without sacrificing performance.

B. Analysis of Stability Using the N-Curve Method

The static noise margin (SNM) is a metric for the SRAM cell's stability. The read, write and hold modes of this SNM are used to get the read SNM, write SNM, and hold SNM, respectively. Generally, the butterfly method is employed to determine the SNM in various modes [26]. However, the disadvantage of the butterfly technique is that it only provides information about SNM; deriving SINM (Static Current Noise margin) requires mathematical calculations. Two distinct circuits must be examined to achieve read and write SNM. Another technique for determining SNM is the N-curve method, which provides both voltage and current information concurrently. The cell's read stability and write capabilities are also determined directly from the N-curve. The N-curves for all SRAM and planned SRAM cells are shown in fig. below. The values for SVNM, SINM, WTV, and WTI are as given in Table I.

C. Analysis of Stability Using the Butterfly Method

The SRAM cell's ability to store data against noise is measured in SNM. The SNM of SRAM is defined as

TABLE I: Comparative Analysis of SRAM cells

Parameters	**Proposed 9T**	6T [3]	7T [6]	8T [8]	9T [25]
Total Power Dissipation (μW)	**0.09041**	25.48	25.26	6.101	0.1154
Read Time Access (ns)	**68.938**	191.74	141.85	155.177	69
Write Time Access (ns)	**78**	92.562	70.5028	79.058	78
Static Voltage Noise Margin (mV)	**423.32**	369.094	371.581	359.41	393.51
Static Current Noise Margin (μA)	**74**	36.094	33.394	55.535	51.650
Write Trip Voltage (mV)	**513.79**	522.57	540.86	496.99	511.96
Write Trip Current (μA)	**-12.208**	-8.6711	-9.1072	-9.4437	-8.6705
Static Power Noise Margin (μW)	**31.308**	13.35	12.40	19.9598	20.325
Write Trip Power (μW)	**-6.2723**	-4.531	-4.9257	-4.6934	-4.439

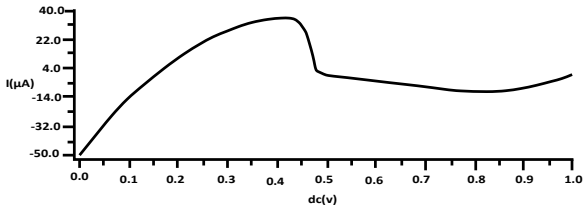

Fig. 10: N-curve Analysis of Proposed 9T SRAM.

the minimum amount of noise voltage required to flip the state of a cell on the SRAM's storing nodes. The static voltage transfer characteristics of the SRAM cell inverters are used in the graphical technique to determine the SNM. It multiplies one cell inverter's voltage transfer characteristic (VTC) by the inverse VTC of the other inverter [14].

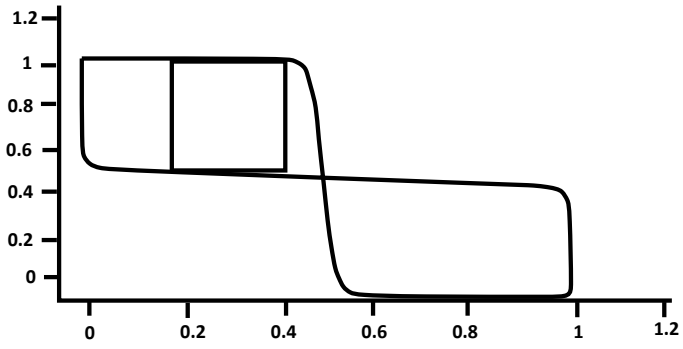

Fig. 11: Butterfly Curve Analysis of Proposed 9T SRAM cell.

The greater the SNM value, the better the read stability of the SRAM cell. The read stability of a cell with a lower RSNM is poor.

V. Conclusion

The performance of three SRAM cell topologies in terms of stability has been demonstrated. SRAM speeds will increase as process technologies advance, but devices will be more prone to mismatches, reducing the static noise margin of SRAM cells. The 6T SRAM's RNM is relatively low. The width of the pull-down transistor must be raised to get a larger RSNM in 6T SRAM cells. However, this increases the area of the SRAM, which increases leakage currents. The read noise margin of an 8T SRAM cell is significantly higher. An 8T SRAM cell may fail during a write operation due to the asymmetric cell structure. Compared to 6T and 8T SRAM cells, 9T SRAM cells have stronger RSNM and WSNM, resulting in improved stability performance.

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