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Analysis of Power in SRAM Cell with Various Pull up, Pull down and Pass Gate Transistors

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Abstract: SRAM cell plays major role in many microelectronic and nano electronic devices. Low power consumption or low leakage power, high speed operations to match the recent trends are the challenges in SRAM designs. In this work, we have designed a 6T SRAM which has 6 transistors with 2 pull up, 2 pull down and 2 transistors acting as pass gate transistors, cross coupling between the pull up and pull down vertical connections helps in maintaining the sleep mode leakage power in SRAM cell. Threshold conditions can be introduced for high speed operations in SRAM. 6T SRAM is designed in cadence with 90nm technology, further the layout is drawn for 90nm technology and the output waveforms from SRAM cell layout are presented.

Keywords: *6T SRAM Cell, threshold effect, leakage power, cadence 90nm*

1. INTRODUCTION

To prevent for power leakage in 6T- SRAM cell power in SRAM are 60.7, 65.22 and 59.57 times less than 1:1:1 configuration [1]. To modified power and static noise margins of single port 6T- SRAM to 8T-SRAM [2]. To improve CMOS 6T SRAM scalability in the decananomete regime SNM and WNM cell ratio follow opposite trends [3].

Design of 10nm TFET base 6T-SRAM circuital reduced supply voltage of 0.5V [7]. CNFET CMOS SRAM array demonstrate 1kbit (1024) 6 transistor 6T-SRAM fabrication [8]. Three ways to mechanisms that are responsible for soft error at terrestrial altitudes [10]. To prevent a single bit up set and multiple bit upset on a 45nm SOI SRAM [11]. To measure the SET if inverters chain based on 65nm CMOS technology [12]. SRAM analysis of write static noise marge for both 45nm and 65nm to compact analytic has been developed in WSNM in subthreshold region [13].

The 9T CMOS SRAM developed for improve stability, power dissipation and delay [14] [15]. Low power and noise reduction in 16x16 SRAM array incensed in power consumption [17]. Analyzed for power consumption, write delay and write power delay [18]. They use 90 nm technology to reduce the power efficiency and fast the memory transfer [19] [21].

2. RELATED WORK

Leakage power of T-SRAM are 60.7, 65.22 and 59.57 times less than 1:1:1, 1:5:2 and 2:5:2 configuration it will prevent from power leakage in 6T SRAM cell [1]. In paper for every device has lowest energies the error in every relactionship to use common simulation of every type of devices data manipulation efficiency and performance [4]. They perform many new techniques for all devices by design a new technique for logic circuits and interconnected for memory, clock and power distribution [5].

In this CNFET CMOS SRAM cell takes voltage supply of 300mV CNFET CMOS SRAM array demonstrate 1kbit (1024) 6 transistor 6T-SRAM fabrication [8]. The area of SRAM cell is reduced to 25% when the cell ratio is 1 and pull up ratio is 1 to under going with area reduction by pull-up, pull-down ratio [9]. Three times chip area and reduces maximum operating frequencies with Higher energy cosmic and lower energy cosmic [10] [22].

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Table1. SRAM Cell- Literature survey

Author Name, Year	Algorithm	Steps for / Technique	Performance Metrics	Application
Mahmood Uddin et al., 2018 [1]	To prevent from power leakage in 6T SRAM cell.	By using pull up, pull down and pass gate ratio	Leakage power of T-SRAM are 60.7, 65.22 and 59.57 times less than 1:1:1, 1:5:2 and 2:5:2 configuration	SRAM
B.Cheng et al., 2007 [3]	To improve CMOS and TSRAM scalability in the decananometer regime	By using WNM and SNM performance	SNM, WNM cell ratio. WNM is 2times better than SNM	SRAM
Jaeyoonkim et al., 2013 [4]	robustness, data manipulation	To use common simulation of every type of devices	In paper for every device has lowest energies the error in every relationship	Nano electronic
Benton H. Calhoun et al., 2007 [5]	new logic circuits and interconnected for clock, memory, power distribution	Device level modeling	They perform many new techniques for all devices	SRAM
Chanh-Hung Yu et al., 2016 [6]	cell stability, write ability - voltage SRAM	By using WFV	Delta V, IDS and superior subthreshold slope.	SRAM
Nahib Hossain et al., 2017 [7]	Design of 10nm TFET base 6T-SRAM circuital reduced supply voltage of 0.5V	read power and energy, write power and energy	TFET base SRAM write 11% faster thenFinFET base SRAM TFET base SRAM read 21% slower than FinFET based SRAM	SRAM
PritpalS.Kanhaiya et al., 2019 [8]	CNFET CMOS SRAM array demonstrate 1kbit (1024) 6 transistor 6T-SRAM fabrication	Fabrication of CNFET	CNFET SRAM cell takes voltage supply of 300mV	SRAM
G.Torrens et al., 2017 [9]	decreasing cell ratio from 1.5-2.5 to 1	Under going with area reduction by pull-up, pull-down ratio	The area of SRAM cell is reduced to 25% when the cell ratio is 1 and pull up ratio is 1	SRAM
Robert Baumann, 2002 [10]	Three ways to mechanisms that are responsible for soft error at terrestrial altitudes	Higher energy cosmic and lower energy cosmic	Three times chip area and reduces maximum operating fequencies	SRAM

The compact analytic has been developed in WSNM in subthreshold region, power and energy by using subthreshold, leakage power and access energy [13]. SRAM has actives 33% power saving in the 9T SARM in 32nm 9T CMOS SRAM developed for improve stability, power dissipation and delay [14]. The 4:16 decoder and 16x16 memory array low power and noise reduction in 16x16 SRAM array incensed in power consumption [16] [17]. It use 38.1% less power SRAM is 18.18.% faster by analyzed for power consumption, write delay and write power delay [18]. 500MHz power dissipation in 6T SRAM is 4.890uw

and in SRAM is 606.519nm they use 90 nm technology to reduce the power efficiency and fast the memory transfer [19].

Table2. Types in SRAM Cell- Literature survey

Author Name, Year	Algorithm	Steps for / Technique	Performance Metrics	Application
Guillaume Hubert et al., 2013 [12]	To measure the SET	Single event transient	cross section, pulse width	CMOS
Ruchi et al., 2018 [13]	SRAM analysis of write static noise marge for both 45nm and 65nm	By using subthreshold, leakage power and access energy	The compact analytic has been developed in WSNM in subthreshold region, power and energy	SRAM
Sheng Lin et al., 2010 [14]	The 9T CMOS SRAM developed for improve stability, power dissipation and delay	By using HSPICE	SRAM has actives 33% power saving in the 9T SARM in 32nm	SRAM
Akshay Bhaskar, 2017 [18]	write delay, power delay	CMOS SRAM technology	It use 38.1% less power SRAM is 18.18.% faster	SRAM
Hansraj et al., 2020 [19]	They use 90 nm technology to reduce the power efficiency and fast the memory transfer	Low power for power reduction	500MHz power dissipation in 6T SRAM is 4.890uw and in SRAM is 606.519nm	SRAM
Ching-Wei Wu et al., 2014 [20]	SRAM - pseudo two port, single port SRAM function compiler	2 in 1 SRAM	Test chip fabricated in 16nm FinFET 0.0907um2 6T memory cell is used	SRAM

3. Architecture of 6T SRAM Cell

Now a days, high bandwidth and large capacity in memories are in demand for which SRAM cell plays major role. In SRAM cell, leakage power during standby mode of operation is a challenge. In this work, we have proposed SRAM cell with 6T as shown in figure [1] for low power consumption. 6T stands for 6 transistors in which 2 are pull up PMOS transistors, 2 are pull down NMOS transistors and 2 are pass gate transistors. BL and BLB are the bit line and bit line bar which operates based on WL and the vn1, vn2 voltages. WL is the write line. Vn1 and vn2 are the voltages connected as cross coupling between gate and the opposite side vertical connection between drain and source of NMOS pull down and PMOS pull transistors. Threshold is another strategy where we can reduce the delay or increase the speed of SRAM transistors.

$$C_{thres} = \frac{W}{L}\mu_o D_O (N-1)\frac{KT^2}{Q}\exp\left[q\frac{1}{nKT}(V_{GS}-V_T)\left[1-\exp\left(-\frac{qV_{cs}}{KT}\right)\right]\right]$$

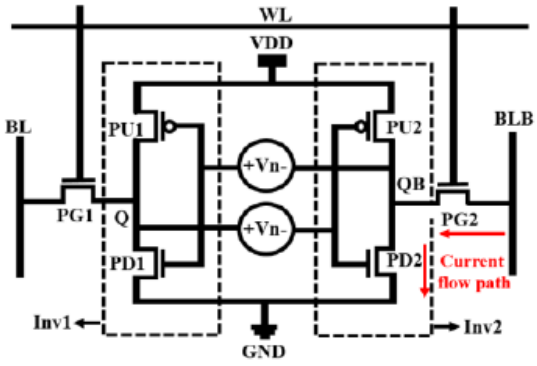

Fig1. SRAM Cell with 6T [1]

The threshold voltage strategy for reducing or monitoring the leakage power in SRAM cell operates based on the formula shown. Leakage power in standby mode of a sleep transistor is analyzed using multiple threshold strategies in SRAM cell. Power consumption in SRAM cell varies for different temperatures and the voltages for read operation, write operation are different at any particular node in SRAM cell. Noise margin is a basic parameter to analyze the performance of SRAM cell. There are 3 types of noise margins namely static

noise margin in hold mode (SHNM), static noise margin in write mode (SWNM) and static noise margin in read mode (SRNM) in a SRAM cell. If the number of transistors in SRAM cell design is increased from 6T to 7T and then from 7T to 8T, 13T there is more possibility for fixing threshold values to desired levels and thereby reducing the leakage power in standby mode of sleep transistors in SRAM cell.

4. Results

SRAM cell is designed in cadence 90nm technology as shown in figure 2. Power consumption and high speed operation are the challenges in SRAM cell. It can be designed using 6T which means 6 transistors. Similarly, SRAM can be designed using 7T or 8T which has 7 transistors, 8 transistors respectively. These designs are to obtain high speed or low power consumption in SRAM cell memory unit. Sleep transistors can be introduced to achieve less power leakages in SRAM and thereby reducing power consumption in SRAM cell. On the other hand, threshold strategies in a multiple levels can be applied to increase the speed of operation in SRAM cell.

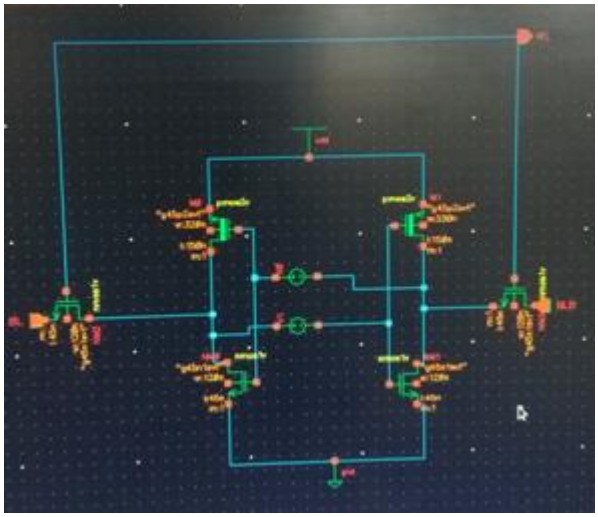

Fig2. SRAM Cell in cadence tool 90nm technology

Figure 3 shows the layout of 6T SRAM cell in which 4 NMOS transistors, 2 PMOS transistors are used. N-well is present in PMOS transistors in which vdd are connected to avoid floating effect. These PMOS transistors are the pull up transistors; the other 4 NMOS transistors are used for acting as pull down transistors and pass gate transistors. Connections in layout are done using metal for source and drain terminal connections. Polysilicon is used to connect the gate terminals of PMOS and NMOS transistors. Vss are connected to the 2 pull down NMOS transistors in the SRAM cell. BL bit line and BLB bit line bar are connected on pass gate transistors which are present on either extremes.

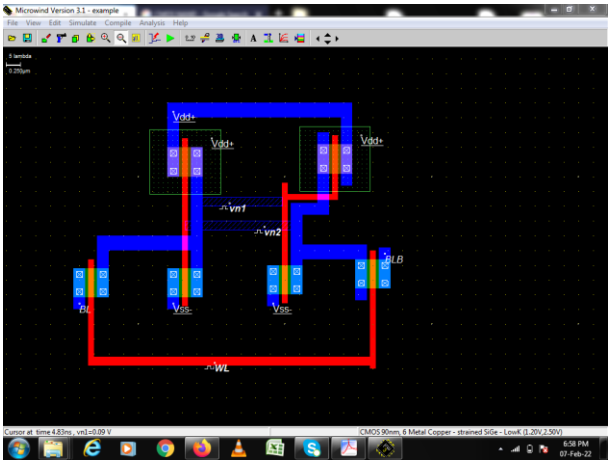

Fig3. Layout of SRAM cell- 90nm technology

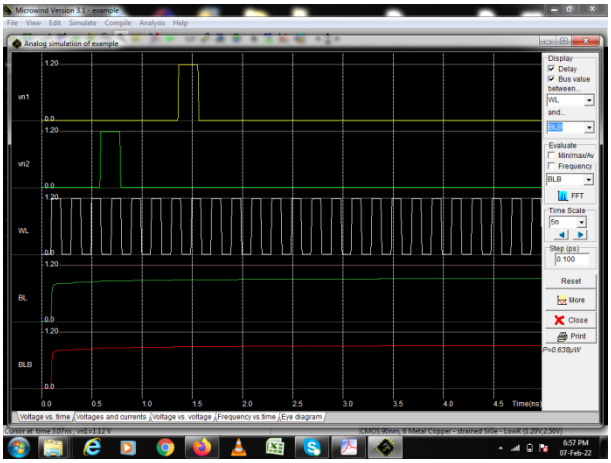

Fig4. Output of SRAM cell from layout

In the layout in figure 3, gates of pass transistors are connected together in which the WL write line visible output node is connected in layout. Gate terminals of one pull up PMOS and respective pull down NMOS transistors are connected using polysilicon material. The drains of 2 pull up transistors are connected using metal. At last the cross coupling is done with another metal between drain and gate of the vertical connections between pull up and pull down transistors. Visible nodes vn1 and vn2 are connected on these cross couplings in the layout.

Figure 4 shows the output waveform obtained from layout. Vn1 and vn2 are activated at 1.3 nano seconds and 0.6 nano seconds respectively, the WL write line gets data and it is passed onto BL bit line and BLB bit line bar respectively based on the working of vn1 and vn2, their cross coupling working procedure. The power consumption in the SRAM cell is 0.638 microwatts.

5. Conclusion

In this paper, we have designed 6T SRAM cell for low power micro devices and nano devices. Leakage power during sleep and standby mode of transistors are balanced in the 6T SRAM using cross coupling connections. Threshold levels are maintained to increase the speed of SRAM operation. SRAM is designed in cadence 90nm technology, layout is drawn and waveform for the 6T SRAM layout are presented which shown the power consumption is 0.638 micro watts.

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