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Design and Analysis of SRAM cell using Body Bias Controller for Low Power Applications

Jitendra Kumar Mishra[1] · Bharat Bhushan Upadhyay[1] · Prasanna Kumar Misra[1] · Manish Goswami[1]

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Abstract

Low power consumption of electronic devices has become one of the most desirable factors in the present day's technology. Static random access memory (SRAM) being an integral part of most of the electronic gadget suffers from leakage current which results in static power dissipation and subsequently affects its performance particularly during standby or hold mode. This becomes crucial especially for those systems which are portable and have limited power supply. This work therefore proposes a body bias controller implemented with a 7T SRAM cell at 28 nm CMOS technology node which lowers the static power consumption and increases the hold static noise margin (HSNM) of SRAM during standby mode by changing the threshold voltage. Moreover, it also reduces write delay due to reduction in threshold voltage of proposed design without having a significant effect on write static noise margin and read static noise margin. It has been noticed that there is a reduction of 40%, 28%, 41.9% and 30% in static power dissipation whereas there is an enhancement of 19%, 14.2%, 6.6% and 5.2% in HSNM of the proposed design when compared to 6T SRAM cell, 7T SRAM cell, WRE8T SRAM cell and 9T SRAM cell, respectively. The proposed design can thus be a suitable alternative for low power SRAMs.

Keywords Body bias controller · 7T SRAM cell · Static power dissipation · Stability · Delay

✉ Manish Goswami
manishgoswami@iiita.ac.in

Jitendra Kumar Mishra
Jithin.mishra@gmail.com

Bharat Bhushan Upadhyay
imi2017006@iiita.ac.in

Prasanna Kumar Misra
prasanna@iiita.ac.in

[1] Department of Electronics and Communication Engineering, Indian Institute of Information Technology, Allahabad (Prayagraj), India

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1 Introduction

Today's technologies of electronic devices are the result of "More Moore" which has made the life handy, easy and durable. The main impetus of this is, however, on scaling which was initially proposed by Dennard et al. [6] and whose seed had now cultivated into a fruit. The reduction in dimensions had enabled the designers to place millions of transistors on a single chip. (Surprisingly, the number of transistors in the chip was only 32 when G Moore predicted the law.) However with the scaling of technology node, static power consumption and behavior of transistor as an ideal switch are some of the issues which often become critical and poses problem to the designers.

Particularly in memory-based system, power dissipation is a major issues as high density chips have more number of transistors which contribute in overall power dissipation [4]. Moreover, high density of transistors in static random access memory (SRAM) increases the temperature which eventually increases the leakage current and results in increasing the overall power dissipation [21, 23, 26]. The static power dissipation in an SRAM cell arises out of several leakage currents which flow in transistors. For a non-conducting transistor sub-threshold leakage, depletion punch through leakage and gate-induced drain leakage (GIDL) are the prominent sources of leakage while for a conducting transistor, the leakage current contributors are mainly gate tunneling and reverse bias p–n junction current [9]. Most of them are, however, uncontrollable at the circuit level, but sub-threshold leakage can be controllable to a certain extent by the circuit designers. The sub-threshold leakage current which contributed in the static power dissipation is mainly dependent on threshold voltage (V_{TH}) which can be varied by controlling source-to-substrate (body) connection. It is pertinent here to mention that high V_{TH} transistors have low sub-threshold leakage current with lesser driving speed and vice versa [14].

The demand to design the memory cell at lower technological node comes with various issues, some of which are stability, power dissipation, speed, etc. [22]. The sub-threshold leakages occur in the SRAM cell through access transistors (bit-line leakage) as well as through pull-up and pull-down transistors (cell leakage) with the latter being dominant. The sub-threshold leakage can result in data sensing error by significantly discharging pre-charged bit-lines. Nobakht and Niaraki [17] although had proposed 7T SRAM cell using multi-threshold voltage technique to reduce static power dissipation but it eventually suffered from the write and hold stability. The reduction in read static noise margin (RSNM) with decreasing feature size too had created stability issue in conventional 6T SRAM cells. However to address this issue, read port was decoupled from the write port and a separate read and write port had eventually lead to the significant improvement in read stability of 8T cell as proposed by Chang et al. [5]. A single-ended read port which had reduced the impact of large bit-line capacitance was also proposed by Pasandi and Fakhraie [20]; however, it had resulted in a larger write delay. Agawa et al. [1] had proposed a bit-line compensation technique to equalize the bit-line leakage current, but detection of leakage current and injection of compensation current were a challenging task in such a technique. The calibration of bit-line differential technique was, however, attempted by Lai and Huang [11] but it too suffered from the stability issues. Later Lorenzo and Chaudhury [12] had proposed a body bias controller implemented in 9T SRAM cell which subsequently

reduced the power dissipation and delay, but controller circuit does not self-generate the required voltage and also posed problem in write operation due to single-ended structure. Differential 8T SRAM cell by Pal and Islam [19], supply voltage reduction in bit-line and storage cell by Ye et al. [25], a single-ended 7T SRAM in sub-threshold regime by Kushwah et al. [10], to equalize leakage currents and stability issues for different SRAM cell by Naghizadeh and Gholami [16], using preferential state and modified read access circuitry by Calhoun and Chandrakasan [3], 9T SRAM using feedback power gating method by Moghaddam, et al. [15], a body bias controller using switched capacitor voltage follower by Kamae et al. [7] and other body bias controller circuit [2, 18, 24] were also attempted by different researchers in the past. However, the impact of body bias controllers in threshold voltage to improve the performance of the cell had not been extensively studied. This paper therefore proposes a novel body bias controllers (BBC) implemented with 7T SRAM cell to address power dissipation and stability issue in SRAM. The main highlights of this paper are as:

- This paper proposes a novel body bias controller circuit which generates a positive and negative voltage.
- This body bias controller circuit implemented with proposed 7T SRAM cell. The body of access and pull-down transistor connect to the output of controller circuit.
- The controller circuit changes the body voltage of transistors resulting in decrementing and incrementing the threshold voltage of transistors in the write and read or hold mode, respectively. Moreover, the increment in the threshold voltage of transistors had reduced the sub-threshold leakage current leading to the significant reduction in static power dissipation during hold mode as well as increasing the stability.

The proposed work had therefore resulted in saving the power as well as increasing the stability of SRAM. Rest of the paper has been framed as follows. Section 2 describes the design and working of proposed body bias controller, while Sect. 3 describes the implementation of the proposed body bias controller with 7T SRAM cell. The results and discussion of proposed work and conclusion are presented in Sects 4 and 5, respectively.

2 Proposed Body Bias Controller (BBC)

Figure 1 shows the design of the proposed body bias controller, consisted of three NMOS diode loads M_1, M_2 and M_3 to generate the voltage drop approximately equal to three times threshold voltage of each NMOS transistors. (Three load devices had been taken to obtain body voltage between the desirable limits, and any other number had resulted in drop of voltage swing.) The OR gate has two inputs W_{en} and C_{ntrl}. When W_{en} signal is high, a write operation is performed while it kept low during read and hold operation. The C_{ntrl} signal is used to periodically refresh the capacitor so that it does not lose its charge due to leakage. W_{en} and C_{ntrl} signals do not occur simultaneously. The C_{ntrl} signal is applied only after certain clock cycles for refreshing the capacitor. Thus, the controller retains its voltage even during hold mode if it persists for a longer time. Transistor M_4 has been used to disconnect the MOS diode loads

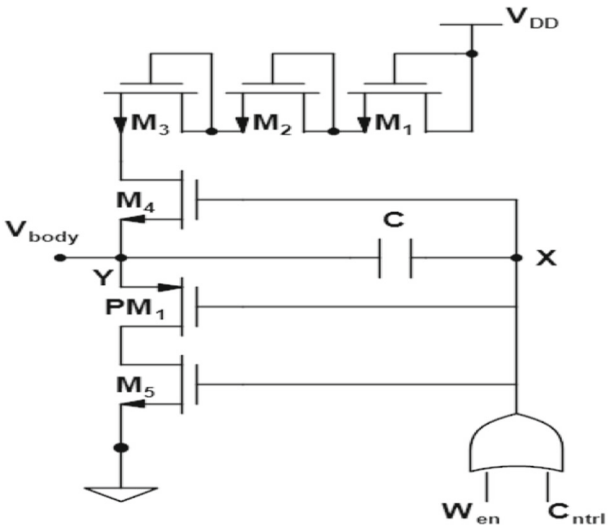

Fig. 1 Proposed body bias controller

from node Y when W_{en} signal is low, i.e., when a read or hold operation is performed. Transistor PM_1 has been used to cut down the direct path between V_{DD} and ground when the W_{en} signal is high, i.e., when a write operation is performed. Transistor M_5 has been employed to prevent the capacitor to discharge when W_{en} goes low during read and hold operation. This helps in the generation of negative voltage. The principle behind the generation of the negative voltage is that a capacitor does not allow sudden change of voltage across its terminals. Thus to maintain the voltage across it, if the potential of one plate of the capacitor goes low, the potential of the other plate also goes down by the same amount to maintain the same potential across its terminals.

The output (V_{body}) of the controller depends mainly on W_{en} signal. When the W_{en} signal is high (write operation is performed), the right plate (node X) of capacitor is at potential V_{DD} while the left plate (node Y) comes at potential $V_{\text{DD}} - 3V_{\text{TH}}$ where V_{TH} is the threshold voltage of NMOS transistor used as an active load. Hence, the charge stored by the capacitor is $Q = C \times 3V_{\text{TH}}$, where C is the capacitor used in the controller. The capacitor C is obtained from the 28 nm CMOS technology node. The value of capacitor C is 6 fF, whereas the area occupied by the capacitor is 1.53 μm^2. The right plate of the capacitor is positively charged, while the left plate holds an equal but negative charge.

When read or hold operation is performed, W_{en} signal goes low thereby making upper and lower driver transistor M_4 and M_5 to operate in cutoff mode while PM_1 in triode mode. Thus in such case, the node Y is disconnected from V_{DD} and ground. Since capacitor does not allow sudden change of voltage, hence to conserve the law of charge, as the right plate (node X) of the capacitor goes to zero potential then according to the expression, i.e., $Q = C \times V$, the potential on the left plate (node Y) changes to $-3V_{\text{TH}}$, thereby generating a negative voltage. In this way, a negative potential has been obtained at node Y. Even when node Y is a float, it is not much sensitive

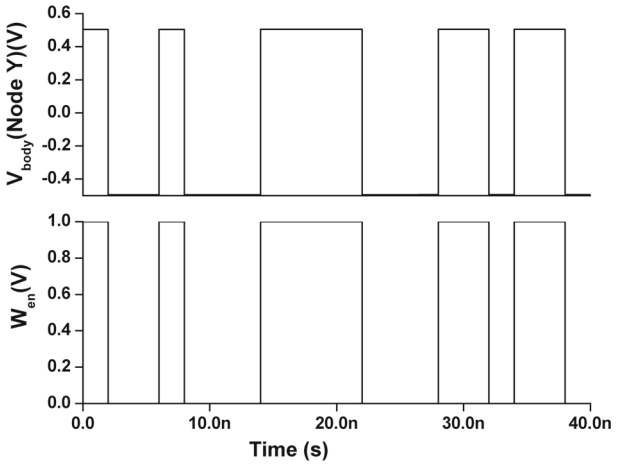

Fig. 2 Controller input and output waveform

to noise because change in the potential at node Y is controlled by the potential of node X which is pulled down to ground. Hence due to law of conservation of charge, the potential of node Y remains constant. Thus, the robustness of the proposed design does not decrease.

Figure 2 illustrates the waveform of input and output of the proposed controller. The input to the controller is random bits of 2 ns duration where the input (W_{en}) '1' represents $W_{\text{en}} = 1$ and a '0' represents $W_{\text{en}} = 0$. The controller provides a positive voltage for $W_{\text{en}} = 1$ (for a write operation) and a negative voltage for $W_{\text{en}} = 0$ (for read and hold operation) which is shown in the output waveform of the controller in Fig. 2. This generates the forward body bias (FBB) voltage of the controller as 0.5 V and reverse body bias (RBB) voltage of the controller as − 0.5 V. These limits on FBB and RBB voltages of the controller have been imposed by implementing the controller on the SRAM cell when the output of controller was applied to the body of NMOS of the SRAM cell and on simulating the design for different output voltages of the controller. The voltage at which the abrupt change in parameters occurs defines the limits of the output voltage of the controller to be applied to the body of NMOS of the SRAM cell. However, in the proposed design it is kept well within the exact limits obtained by simulations results such that the design does not behave abnormally even if there are significant changes in the power supply voltage, temperature, etc.

The minimum value of V_{DD} for proposed BBC is 1 V which is required to achieve ± 0.5 V at the output of BBC circuit. The minimum value of V_{DD} must be greater than $3V_{\text{THn}} + V_{\text{THp}}$ in such case. However, this minimum value of V_{DD} can further be reduced by reducing the number of active loads but with reduction in V_{DD} the output voltage also reduces. Moreover, the minimum V_{DD} requirement is not only governed by the controller but also by the SRAM cell.

There are some advantages of proposed controller as follows.

- The output voltage levels can be adjusted by increasing or decreasing the number of NMOS diode loads. Thus, it can be used for various applications.

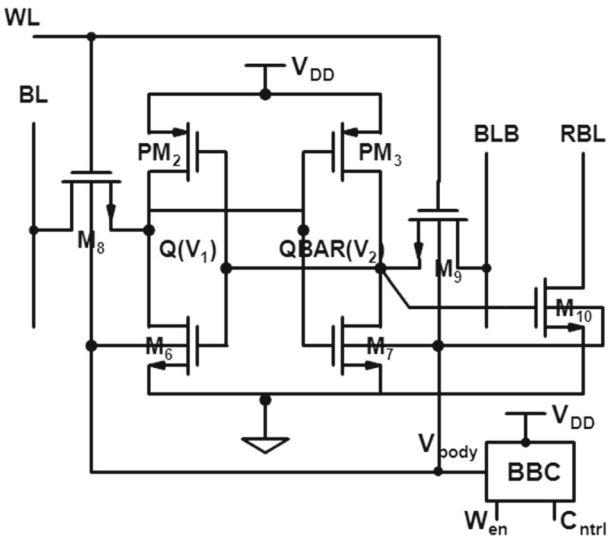

Fig. 3 Proposed design

- This controller eliminates the need of negative power supply for reverse biasing the body of the pull-down and access transistors in hold or read mode of the SRAM cell.
- This controller can be used to any design of SRAM cell like 6T, 7T, 8T, 9T and 10T, since all the SRAM design consists of pull-down and access transistor. Hence, this controller connects to the bodies of these transistors of any design of SRAM cells.

3 Proposed Design (PD)

Figure 3 shows the proposed design which comprises of proposed body bias controller implemented in 7T SRAM cell with separate bit-lines for read and write operation. The transistors M_6, M_7, PM_2 and PM_3 form the internal latch, while the transistors M_8, M_9 and M_{10} act as an access transistor for write and read operation, respectively. The Q and QBAR are the storing nodes whereas bit-line (BL) and bit-line bar (BLB) are inputs during write operation and read bit-line (RBL) as input or output line for read operation. The access transistors are driven by word-line (WL) signal. The pull-up and cell ratio of 7T SRAM is kept as 0.8 and 1.3, respectively. The operations of the proposed design in different modes are discussed below.

3.1 Write Mode of Operation

In write mode, the data to be written into a cell (0 or 1) are applied to bit-lines (BL and BLB). When the WL signal become high (WL = 1), the access transistors M_8 and M_9 switch to ON mode and start to charging and discharging of storing nodes according to the data available at bit-lines. Since the W_{en} signal is kept high (W_{en} =

1), it results in a positive potential at the output of the BBC (refer Fig. 2). The body of the pull-down and access transistors comes now at a potential higher than the potential at their source (i.e., forward body bias) which in turn reduces the threshold voltage and eventually reduces the write delay (as per Eq. 1) and also increases the write ability of the proposed design (due to reduction in the threshold voltage). However, the data holding capability (write stability) after write operation is slightly degraded due to reduced threshold voltage. (The chance of the flipping of data had increased due to low threshold voltage.) The dependence of propagation delay (T_{pd}) on the threshold voltage is given in Eq. (1) [13].

$$T_{pd} = \frac{C_L * V_{DD}}{A(V_{DD} - V_{TH})^2} \tag{1}$$

where T_{pd} is propagation delay, V_{DD} is the supply voltage, V_{TH} is the threshold voltage, C_L is load capacitor and A is constant. From Eq. (1), it can be inferred that the delay would be decreased by reducing threshold voltage.

3.2 Read Mode of Operation

In read operation, RBL is initially forced to V_{DD} and a WL signal is asserted (WL = 1). Since W_{en} signal is kept low ($W_{en} = 0$), it results in a negative potential at the output of the BBC (reverse body bias as illustrated in Fig. 2). The body of access and pull-down transistors of SRAM cell is now at a potential lower than the potential at their source which in turn increases the threshold voltage that eventually increases the read stability with slight increases in the read delay due to high threshold voltage as per Eq. (1). Moreover at the high threshold voltage, the chance of data degradation at storing nodes had also reduced. To confirm the valid read operation, let us assume that node Q and QBAR are at logic '0' and '1', respectively. This in turn makes transistor M_{10} as ON which then forms a conducting path between RBL and ground. Subsequently, RBL starts to discharge to zero potential thereby confirming the validity of read '0' operation.

3.3 Hold Mode of Operation

In hold operation, the cell should retain or hold the data which is stored in it. Hence, the cell is isolated from bit-lines by keeping the WL signal low (WL = 0). This eventually turns off the access transistors M_8 and M_9. The W_{en} signal is also kept low ($W_{en} = 0$) which results in a negative potential at the output of BBC (reverse body bias as demonstrated in Fig. 2). Thus, the body of the pull-down and access transistors of proposed design are now at a potential lower than the potential of their source which in turn increases their threshold voltage. This increment in the threshold voltage of these transistors weakens the leakage current flowing from V_{DD} and bit-line pairs to the

ground leading to the significant reduction in static power dissipation. The dependence of sub-threshold leakage current on a threshold voltage is as per Eq. (2) [13].

$$I_{\mathrm{SUB}} = I_{\mathrm{S}} \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_{\mathrm{T}}}\right)\left\{1 - \exp\left(\frac{-V_{\mathrm{DS}}}{V_{\mathrm{T}}}\right)\right\} \tag{2}$$

$$P_{\mathrm{St}} = I_{\mathrm{SUB}} \times V_{\mathrm{DD}} \tag{3}$$

where I_{SUB} is a drain to source sub-threshold leakage current, I_{S} reverse saturation current, η is the sub-threshold factor, V_{GS} is a gate to source voltage, V_{TH} is the threshold voltage, V_{T} is the thermal voltage, V_{DS} is a drain to source voltage, V_{DD} is the supply voltage and P_{St} is the static power dissipation [14].

Thus, it can be observed from Eqs. (2) and (3) that the sub-threshold leakage current and static power dissipation can be decreased by raising threshold voltage. The threshold voltage, however, is given as:

$$V_{\mathrm{TH}} = V_{\mathrm{TH0}} + \Upsilon\left(\sqrt{|-2\emptyset_{\mathrm{F}} + V_{\mathrm{SB}}|} - \sqrt{|2\emptyset_{\mathrm{F}}|}\right) \tag{4}$$

where V_{TH} is the threshold voltage, V_{TH0} the threshold voltage at no body bias, Υ is a body coefficient, $2\emptyset_{\mathrm{F}}$ is the Fermi potential of the bulk or body while V_{SB} is the source to body potential difference. From Eq. (4), it is clear that the only way for a circuit designer to vary a transistor's threshold voltage intentionally is by changing its V_{SB}.

3.3.1 Stability Analysis in Hold Operation

The hold stability of SRAM cell is defined by hold static noise margin (HSNM) that is obtained by the DC curve of two cross-coupled inverters used in SRAM cell. In hold operation, the cross-coupled inverters are disconnected from the bit-lines. Figure 4 shows the voltage transfer (VTC) or DC curve of cross-coupled inverters. The axis of the DC curve of right inverter has been inverted and merged with DC curve of left inverter to form the butterfly curve [8]. The V_{OHL} represents the higher output voltage of left side inverter while V_{IHR} represents the high input voltage of right inverter.

The difference between these two voltages gives the HSNM value which is evaluated in the following two cases.

$$\mathrm{HSNM} = V_{\mathrm{OHL}} - V_{\mathrm{IHR}} \tag{5}$$

Assume, V_1 is the voltage at node Q while V_2 is the voltage at node QBAR (as shown in Fig. 3).

Case 1 Estimation of V_{OHL} (From the DC curve of left side inverter as shown in Fig. 4).

From Fig. 3, for the left inverter $V_{\mathrm{in}} = V_2$ and $V_{\mathrm{out}} = V_1$, at the point A in the DC curve of left inverter (as shown in Fig. 4), the transistors M_6 and PM_2 operate in cut OFF and triode region, respectively, hence applying KCL at node Q.

$$I_{\mathrm{DSPM_2}} = I_{\mathrm{SubM_6}} \tag{6}$$

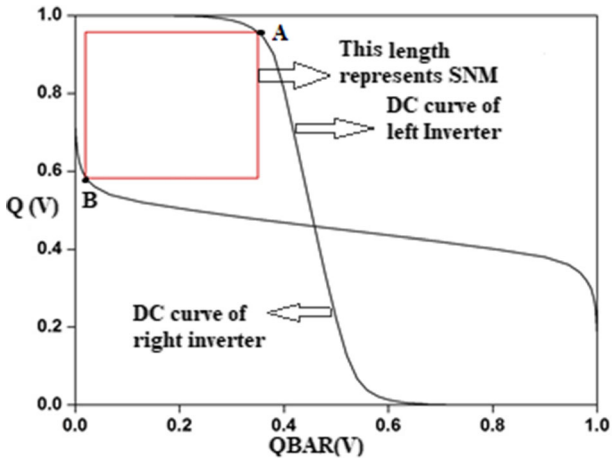

Fig. 4 Method of obtaining HSNM from butterfly curve

where I_{DSPM_2} is current through transistor PM_2 and I_{SubM_6} is the sub-threshold leakage current through M_6. On applying the expression for transistor operating in triode and sub-threshold mode, Eq. (6) becomes

$$\frac{K_{\mathrm{pPM}_2}}{2}\left\{2\left(V_{\mathrm{GSPM}_2}-V_{\mathrm{THPM}_2}\right)V_{\mathrm{DSPM}_2}-V_{\mathrm{DSPM}_2}^2\right\} = I_{\mathrm{S}}\exp\left\{\frac{V_{\mathrm{GSM}_6}-V_{\mathrm{THM}_6}}{\eta V_{\mathrm{T}}}\right\}\left\{1-\exp\left(\frac{-V_{\mathrm{DSM}_6}}{V_{\mathrm{T}}}\right)\right\} \tag{7}$$

During the hold operation, the threshold voltage of transistor M_6 is increased due to reverse body biased. Thus, it can be assumed that the sub-threshold leakage current is negligible through transistor M_6. Accordingly, Eq. (7) becomes

$$\frac{K_{\mathrm{pPM}_2}}{2}\left\{2\left(V_{\mathrm{GSPM}_2}-V_{\mathrm{THPM}_2}\right)V_{\mathrm{DSPM}_2}-V_{\mathrm{DSPM}_2}^2\right\}=0 \tag{8}$$

From Fig. 3, $V_{\mathrm{GSPM}_2}=-(V_{\mathrm{DD}}-V_2)$ and $V_{\mathrm{DSPM}_2}=-(V_{\mathrm{DD}}-V_1)$. On substituting these values, Eq. (8) becomes

$$\frac{K_{\mathrm{pPM}_2}}{2}\left\{2\left(-(V_{\mathrm{DD}}-V_2)-V_{\mathrm{THPM}_2}\right)(-(V_{\mathrm{DD}}-V_1))-(V_{\mathrm{DD}}-V_1)^2\right\}=0 \tag{9}$$

From Fig. 4 at point A, $V_1 \approx V_{\mathrm{OHL}}$ and $V_2 \approx 0$. On putting these values in Eq. (9), V_{OHL} is evaluated as:

$$V_{\mathrm{OHL}} \approx V_{\mathrm{DD}} - 2V_{\mathrm{THPM}_2} \tag{10}$$

Equation (10), presents the high output voltage of left side inverter for the proposed design.

Case II Estimation of V_{IHR} (From the inverted DC curve of right side inverter as shown in Fig. 4).

For right inverter $V_{\mathrm{in}} = V_1$ and $V_{\mathrm{out}} = V_2$, at the point B in the DC curve of right inverter (it is inverted curve of right inverter in Fig. 4), the transistor M_7 and PM_3 operate in triode and saturation region, respectively. Hence on applying the KCL at node QBAR

$$I_{\mathrm{DSPM}_3} = I_{\mathrm{DSM}_7} \tag{11}$$

On applying the expression for transistor operating in saturation and triode region, Eq. (11) becomes

$$\frac{K_{\mathrm{pPM}_3}}{2}\left(V_{\mathrm{GSPM}_3} - V_{\mathrm{THPM}_3}\right)^2 = \frac{K_{\mathrm{nM}_7}}{2}\left\{2\left(V_{\mathrm{GSM}_7} - V_{\mathrm{THM}_7}\right)V_{\mathrm{DSM}_7} - V_{\mathrm{DSM}_7}^2\right\} \tag{12}$$

where $V_{\mathrm{GSM}_7} = V_{\mathrm{in}} = V_1$, $V_{\mathrm{DSM}_7} = V_{\mathrm{out}} = V_2$ and $V_{\mathrm{GSPM}_3} = -(V_{\mathrm{DD}} - V_1)$.
Substituting these values in Eq. (12) becomes

$$\frac{K_{\mathrm{pPM}_3}}{2}\left(V_1 - V_{\mathrm{DD}} - V_{\mathrm{THPM}_3}\right)^2 = \frac{K_{\mathrm{nM}_7}}{2}\left\{2\left(V_1 - V_{\mathrm{THM}_7}\right)V_2 - V_2^2\right\} \tag{13}$$

And on differentiating Eq. (13) both sides with respect to V_1, the expression becomes

$$K_{\mathrm{pPM}_3}\left(V_1 - V_{\mathrm{DD}} - V_{\mathrm{THPM}_3}\right) = K_{\mathrm{nM}_7}\left\{\left(V_1 - V_{\mathrm{THM}_7}\right)\frac{\mathrm{d}V_2}{\mathrm{d}V_1} + V_2 - V_2\left(\frac{\mathrm{d}V_2}{\mathrm{d}V_1}\right)\right\} \tag{14}$$

From Fig. 4, for right inverter at point B where $\frac{\mathrm{d}V_2}{\mathrm{d}V_1} = -1$, voltage $V_{\mathrm{in}} = V_1 = V_{\mathrm{IHR}}$, and $V_{\mathrm{out}} = V_2 \approx 0$,
On putting these values in Eq. (14), V_{IHR} is evaluated as

$$K_{\mathrm{pPM}_3}\left(V_{\mathrm{IHR}} - V_{\mathrm{DD}} - V_{\mathrm{THPM}_3}\right) = K_{\mathrm{nM}_7}\left(-V_{\mathrm{IHR}} + V_{\mathrm{THM}_7}\right) \tag{15}$$

Assume, $K_{\mathrm{R}} = \frac{K_{\mathrm{nM}_7}}{K_{\mathrm{pPM}_3}}$, then

$$V_{\mathrm{IHR}} = \frac{V_{\mathrm{DD}} + V_{\mathrm{THPM}_3} + K_{\mathrm{R}}V_{\mathrm{THM}_7}}{1 + K_{\mathrm{R}}} \tag{16}$$

Equation (16) presents the high input voltage of right inverter. The DC curve of right inverter has been plotted in inverse form (as shown in Fig. 4) such that if the threshold voltage increases then the point B shifts downward. Hence, the gap between point A and B has been increased which subsequently had increased the stability of SRAM cell during hold mode.

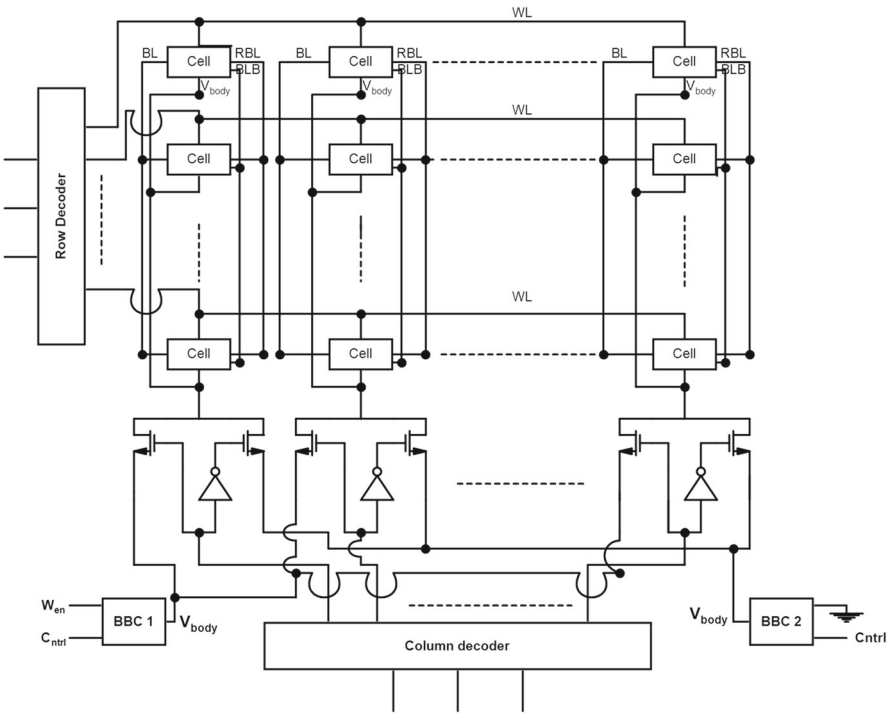

Fig. 5 SRAM array architecture with body bias controller

3.4 SRAM Array Architecture with Controller

Figure 5 depicts the implementation of the proposed body bias controller on an SRAM array using two body bias controllers BBC1 and BBC2. The output voltage of the controller is applied to the body terminal of the NMOS transistor in the bit-cells depending upon the output of the column decoder. The output of BBC1 depends on the W_{en} signal, while BBC2 always produces a negative voltage because one of its inputs is at the ground. The column decoder output points to the column to which data are to be written.

Hence when the W_{en} signal is high, the output of the column decoder turns on the NMOS pass gate of that column to which data are to be written. Thus, the output of BBC1 which is a positive voltage is passed to the V_{body} terminal of all the cells of that particular column. However, all the cells in other columns which are not undergoing any operation have their V_{body} terminal connected to the output of BBC2 by the NMOS pass gate operated by the complementary output of the column decoder. During read mode, both the controllers supply negative voltage to the V_{body} terminals of the cells but during hold operation BBC2 alone supplies negative voltage to the V_{body} terminal of the cells as during hold mode, all the output of column decoder is low. Hence, all the NMOS pass gates which are operated by complementary output of column decoder are turned ON and are connected to an output of BBC2. Moreover, for large

Table 1 Performance parameters of proposed BBC

Parameters	BBC [7]	BBC [2]	BBC [18]	Proposed BBC
Technology (nm)	28	28	28	28
Supply voltage (V)	1	1	1	1
Another power sources	Not required	Required	Not required	Not required
Output	FBB	RBB/FBB	RBB/FBB	RBB/FBB
Dynamic power	28 μW	10 μW	8 μW	12 μW
Response time	320 ps	30 ns	730 ps	100 ps
Area (μm^2)	1.3	12	28	4.48

memories the SRAM array uses two body bias controllers as shown in Fig. 5. For writing operation, the BBC1 provides FBB to the cell in a particular column while all other cells of SRAM array remains at RBB due to BBC2. Thus, the current due to FBB does not affect to all the cells of SRAM array.

However, the proposed design has a gray effect too which can be ignored. During write operation when a data is written into a cell, all other cells of the same column have their V_{body} terminal raised to some positive potential. This results in increased power consumption and reduced noise margin. However, that is momentary and is not of much concern as those cells which are not intended to be written have their access transistors in OFF state which prevents significant degradation in noise margin and increase in instantaneous power consumption.

4 Results and Discussion

The proposed design and array are simulated in UMC 28 nm CMOS technology using the cadence virtuoso circuit simulation tool at 1 V power supply. Several performance parameters of the proposed design are discussed in this section.

4.1 Performance Parameters of Proposed BBC

Table 1 presents various performance parameters of the proposed body bias controller. Moreover, the proposed BBC is compared with other existing body bias controller. It has been noticed that the proposed BBC provides both forward body biasing (FBB) and reverse body biasing (RBB), extra power supply is not required, response time is very less, and optimized area is also less as compared to other existing body bias controller. However, the dynamic or switching power is slightly large as compared to some other existing body bias controller.

4.2 Static Power Dissipation

Static power is consumed in an SRAM cell when no operation is performed on it, i.e., hold mode. It is simply achieved by keeping the access transistors OFF by applying a low signal to the WL of the respective SRAM cell. Even though there is no direct

Table 2 Static power dissipation at different body voltages

Body voltage (V)	Static power dissipation for a PD (single-cell) (nW)	Static power dissipation for 8 × 16 SRAM array (nW)
− 0.5	0.180	1.6
− 0.25	0.250	2.6
0	0.330	3.5
0.25	NA	NA
0.5	NA	NA

path between charged bit-lines and ground (V_{DD} and ground), still significant amount of sub-threshold leakage current flows through these paths resulting in static power dissipation which becomes even more significant when there is a large array of SRAM. However, during this mode, the controller reverse biases the body of access and pull-down transistor which in turn increases their threshold voltage. This subsequently decreases the static power dissipation. Table 2 presents the simulation results of static power consumption due to sub-threshold leakage current for a proposed design (single cell) and 8 × 16 SRAM array obtained at various body voltages. Table 2 conveys that static power consumption is reduced when the body terminal is more reverse biased. However, reverse biasing the body of access and pull-down transistors beyond certain critical voltage may result in increased static power consumption due to the rise of other leakage currents arising from latch-up and excessive tunneling. Thus, the limit of reverse body bias voltage was kept up to − 0.5 V in the proposed design. The power consumption in 8 × 16 SRAM array is less at reverse body bias using the controller circuit as compared to zero body bias or no bias. Figure 6a illustrates the variation in static power dissipation with temperature and is also compared with other existing SRAM cells. It indicates that the increase in static power dissipation with temperature is according to the expression of leakage current as described in Sect. 3.3. It can also be noticed that there is a reduction in static power dissipation of the proposed design (when body is reverse biased) by 40%, 28%, 41.9% and 30% when compared with 6T SRAM [22], 7T SRAM [17], WRE8T SRAM [20] and 9T SRAM [12], respectively, at 1 V supply voltage and 27 °C temperature.

Figure 6b represents the static power dissipation of the proposed design for different corners. The corner slow–slow (SS) results in the least power dissipation, while corner fast–fast (FF) results in the highest power dissipation. This happens owing to the fact that for corner SS, threshold voltages of the NMOS transistors are higher and hence sub-threshold leakage current is lower as compared to corner FF which has lower threshold voltage for the NMOS transistors. All other corners have threshold voltages in between corner SS and FF.

To determine and improve the yield, Monte Carlo analysis for process variation and mismatch has been performed. Monte Carlo simulation is a technique which uses a random value of transistor parameters (normally distributed uncorrelated) for the fixed Gaussian distribution. The simulation result demonstrates that the proposed design is less sensitive to process variations and mismatch as standard deviation (σ) is only 30.6

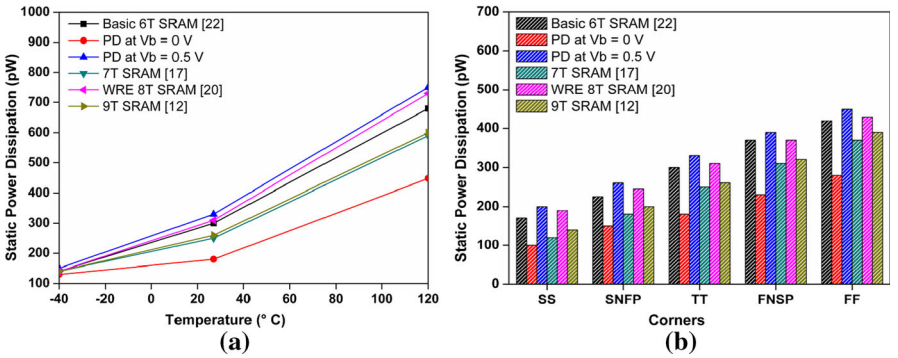

Fig. 6 **a** Static power dissipation verses temperature and **b** Static power dissipation at different corners

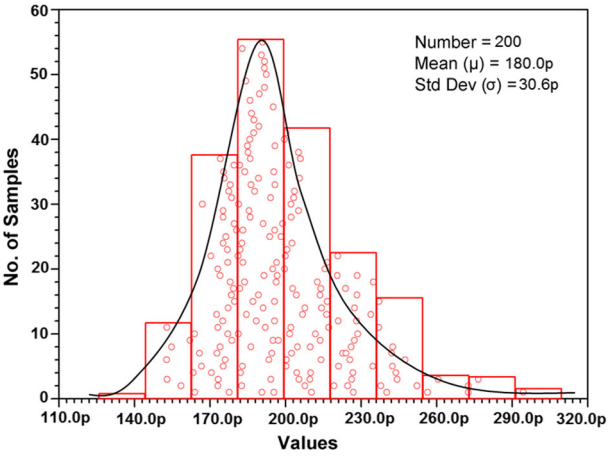

Fig. 7 Monte Carlo analysis for static power dissipation

pW (as shown in Fig. 7) when 200 numbers of samples have been considered for the analysis. The mean value (μ) of proposed design is 180 pW whereas the variability (σ/μ) is 0.17.

4.3 Static Noise Margin

The term static noise margin is a quantitative measure of DC noise voltage that is tolerable for an SRAM cell without flipping of data stored in it [13]. Various static noise margin parameters are described as:

4.3.1 Hold Static Noise Margin (HSNM)

HSNM denotes the capability of an SRAM cell to hold the data without flipping it when no operation is performed on it. The higher HSNM is desired for an SRAM cell to efficiently store the data even in the presence of noise. It can be determined from

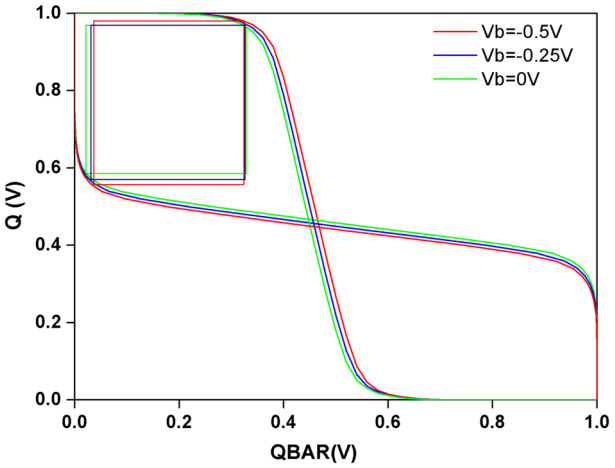

Fig. 8 HSNM at different body voltages

the butterfly curve for taking the side length of square formed in butterfly curve [13]. Figure 8 shows the butterfly curves for HSNM obtained at different body voltages. It has been observed that HSNM value is the 400 mV obtained at negative body voltage when operated at 1 V cell supply voltage. In hold operation, the body of pull-down and access transistors of proposed design are reversed biased which subsequently increases the threshold voltage of these transistors and it requires higher noise voltage to change their state, and hence, higher HSNM is obtained at high reverse body bias.

Figure 9a shows the variation in HSNM of the proposed design with temperature. The HSNM value decreases as temperature increases. The threshold voltage of the transistors falls with rise in temperature; hence, the HSNM of proposed design is decreased. It can also be observed that there is an enhancement of HSNM of proposed design by 19%, 14.3%, 6.6% and 5.2% as compared to basic 6T SRAM [22], 7T SRAM [17], WRE8T SRAM [20] and 9T SRAM [12], respectively, when design at 1 V cell supply voltage with 28 nm technology at 27 °C temperature. Figure 9b presents the HSNM of the proposed design for different process corners and also compared with other reported SRAM cell for different corners at 1 V supply voltage. It has been noticed that the fast NMOS and slow PMOS (FNSP) corner has least HSNM while slow NMOS and fast PMOS (SNFP) corner has maximum HSNM at different body voltages. This is due to the fact that a slow NMOS transistor has high threshold voltage and hence it can tolerate more noise than a faster NMOS transistor with a lower threshold voltage.

4.3.2 Read Static Noise Margin (RSNM)

RSNM denotes the capability of an SRAM cell to allow the read circuitry to read the data from an SRAM cell without affecting the data stored in it. Higher RSNM is desirable for an SRAM cell to have proper read operation without cell flipping. It is also obtained from the butterfly curve as discussed in Sect. 4.3.1. Figure 10

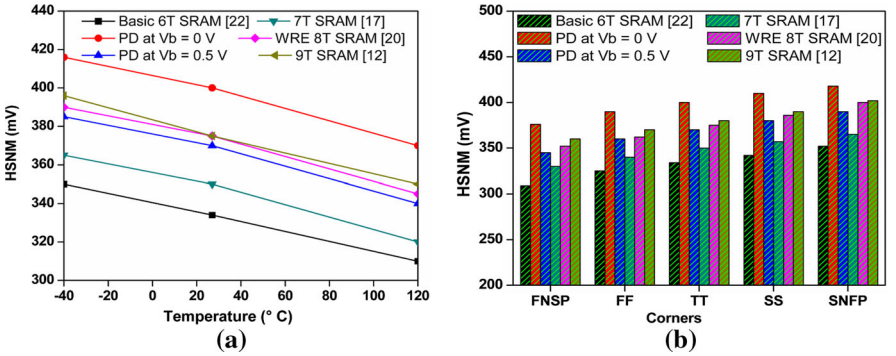

Fig. 9 **a** HSNM at different temperatures and **b** HSNM at different corners

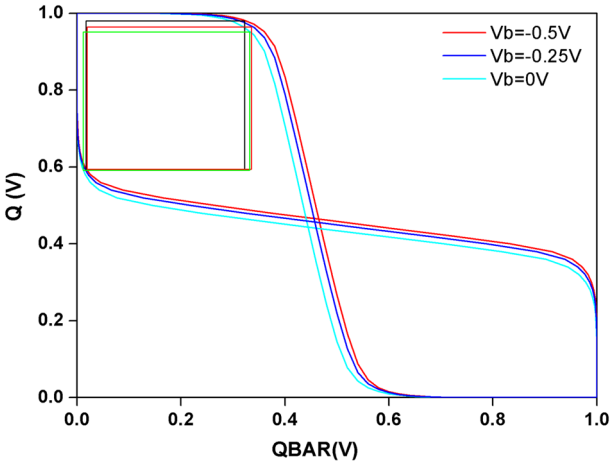

Fig. 10 RSNM at different body voltages

shows the butterfly curves for RSNM of proposed design at different body voltages which indicates the reduction in the RSNM with an increase in body voltage. In read operation, the body of transistor of proposed design is reverse biased. The maximum and minimum value of RSNM is 370 mV and 324 mV, respectively, at 1 V supply voltage. The reduction in RSNM with an increase in body voltage is again due to the fact that access and pull-down transistor's threshold voltage of proposed design is reduced and hence the leakage current through pre-charged RBL during read operation had also increased. This increased leakage current can change the storage node voltage more easily and can destroy the stored data.

Figure 11a shows the variation in RSNM of the proposed design with temperature. The RSNM value of proposed design also decreases as temperature increases. It can also be observed that there is an enhancement of RSNM of the proposed design by 38%, 5.7% and 8.8%, over 6T SRAM [22], 7T SRAM [17] and WRE8T SRAM [20], respectively, and decrement by 3.2% as compared to 9T SRAM [12] when designed at 1 V cell supply voltage with 28 nm technology at 27 °C temperature. Figure 11b

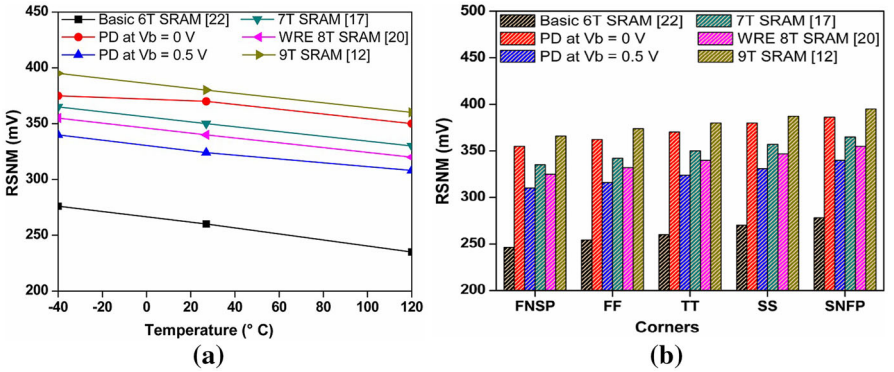

Fig. 11 **a** RSNM at different temperatures and **b** RSNM at different corners

presents the RSNM of the proposed design for different process corners and also compared with other reported design for different corners at 1 V supply voltage. It has been noticed that the RSNM value of the proposed design is 386 mV and 355 mV at SNFP and FNSP corner, respectively, at reverse body bias. This is due to the fact that a slow NMOS has a high threshold voltage and hence it can tolerate more noise than a faster NMOS with a lower threshold voltage.

4.3.3 Write Static Noise Margin (WSNM)

WSNM denotes the capability of an SRAM cell to be written correctly even in the presence of noise. An SRAM cell with high WSNM can perform well in a noisy environment also. The WSNM value is also obtained from the butterfly curve as discussed in Sect. 4.3.1. During write operation, the body of transistor of the proposed design is in forward bias. Figure 12 depicts the variation in WSNM of the proposed design with different body voltages. It has been observed that WSNM reduces with an increase in body voltage. This reduction in WSNM occurs due to a reduction in threshold voltage of access and pull-down transistors which subsequently increases their current driving capability. Thus, write ability of SRAM cell increases but noise-driven current also increases which consequently reduces WSNM. The value of WSNM is 338 mV and 322 mV at 0 V and 0.5 V body voltage, respectively, at 1 V supply voltage.

Figure 13a shows the variation in WSNM of the proposed design with temperature. The WSNM value of the proposed design also decreases as temperature increases. It can be observed that there is an enhancement of WSNM of the proposed design by 16%, 0.6%, over 7T SRAM [17], 9T SRAM [12] and decrement by 5.2%, 13% as compared to basic 6T SRAM [22], WRE8T SRAM [20], respectively, when design at 1 V cell supply voltage with 28 nm technology at 27 °C temperature. Figure 13b presents the WSNM of the proposed design for different process corners and also shows the comparison result with other reported design for different corners 1 V supply voltage. It has been noticed that the WSNM value of proposed design is 342 mV and 310 mV at SNFP and FNSP corner, respectively, at forward body bias. This is due to the fact

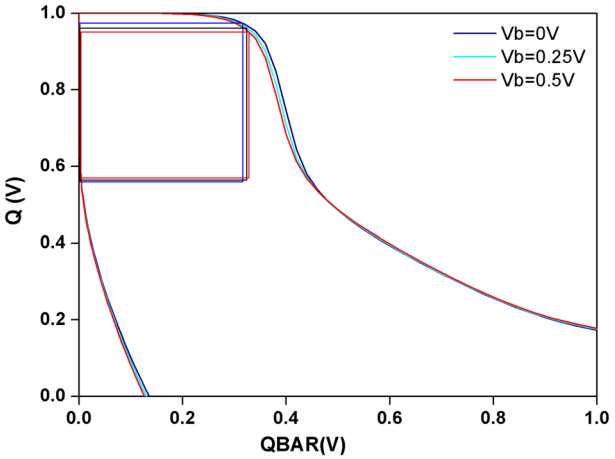

Fig. 12 WSNM at different body voltages

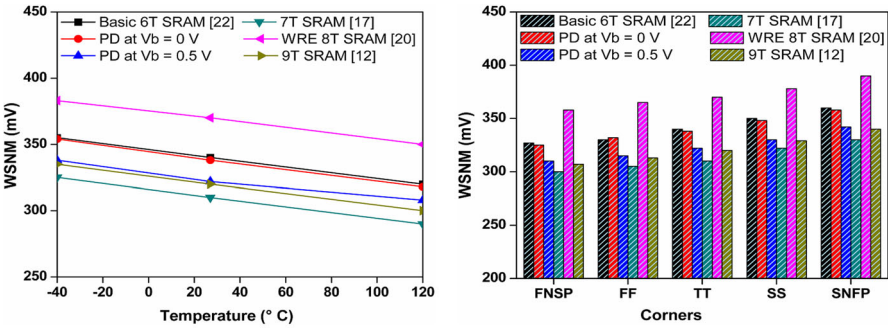

Fig. 13 **a** WSNM at different temperatures and **b** WSNM at different corners

that a slow NMOS has a high threshold voltage and hence it can tolerate more noise than a faster NMOS with a lower threshold voltage.

4.4 Write and Read Delay

Write and read delay in an SRAM cell depends on several factors like bit-line capacitance, size of access transistors, supply voltage, etc. One of the crucial factors which play an important role in deciding write and read delay for an SRAM cell is the current flowing through the access transistors which is responsible for charging or discharging of storage node capacitance. The larger the current flowing through access transistors, the faster is the charging or discharging of storage node capacitance and hence the read or write operation. In the proposed design, the controller generates a positive voltage which is applied to the body of pull-down and access transistors that reduces the threshold voltage and increases the current driving capability which significantly reduces the delay. Figure 14a illustrates the write delay of the proposed design (includ-

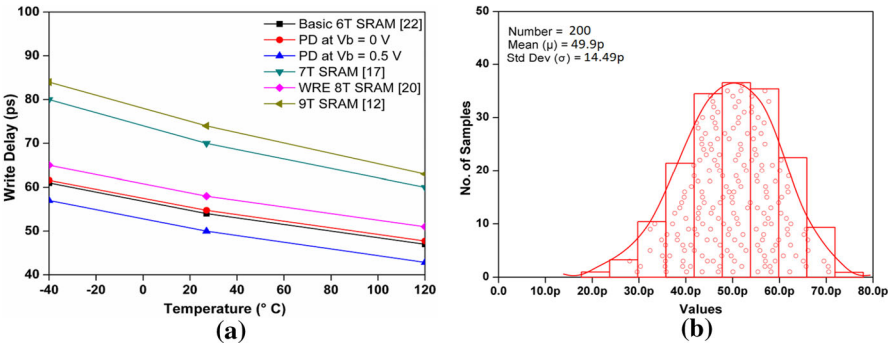

Fig. 14 **a** Write delay at different temperatures and **b** Monte Carlo analysis for write delay

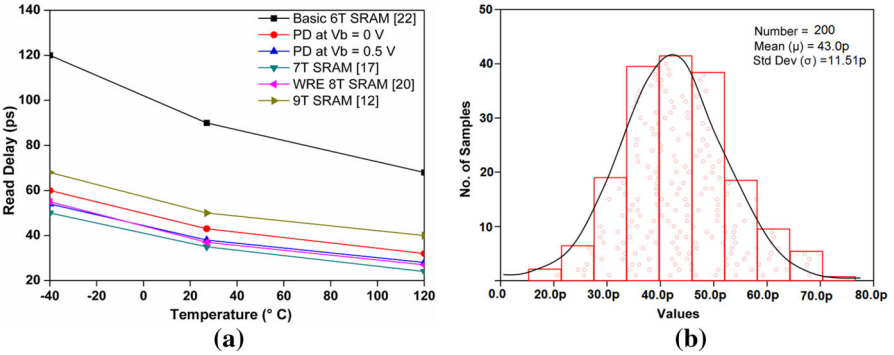

Fig. 15 **a** Read delay at different temperatures and **b** Monte Carlo analysis for read delay

ing parasitic components) at different temperatures. It has been observed that the write delay decreases with temperature because at the low voltage applications, the threshold voltage dominates to determine the drain current. This is also observed that the write delay of the proposed design has been decreased by 7%, 28%, 13% and 32% over 6T SRAM [22], 7T SRAM [17], WRE8T SRAM [20] and 9T SRAM [12], respectively. This is achieved due to reduction in threshold voltage during write operation. Moreover, Monte Carlo analysis has also been done for write delay of the proposed design as shown in Fig. 14b. It has been noticed that the standard deviation and mean value of write delay are 14.49 ps and 50 ps, respectively, for 200 samples, while the variability is 0.29. The minimum and maximum value of write delay is 17 ps and 78 ps.

Figure 15a illustrates the nominal value of the read delay of the proposed design at different temperatures. It has been observed that the read delay of the proposed design is reduced by 52%, 14% and increased by 18%, 13% as compared to 6T SRAM [22], 7T SRAM [17], WRE8T SRAM [20] and 9T SRAM [12], respectively. This is achieved due to increment in threshold voltage during read operation. Furthermore, the maximum value of the read delay of the proposed design at different temperatures are 105 ps, 75.07 ps and 52 ps at − 40 °C, 27 °C and 120 °C, respectively. Moreover, Monte Carlo analysis has also been done for the read delay of the proposed design as shown in Fig. 15b. It has been noticed that the standard deviation and mean value of

Table 3 Read and write power dissipation at different body voltages

Body voltage (V)	Read power (nW)	Write power (nW)
− 0.5	7	NA
− 0.25	11	NA
0	19	15
0.25	NA	26
0.5	NA	40

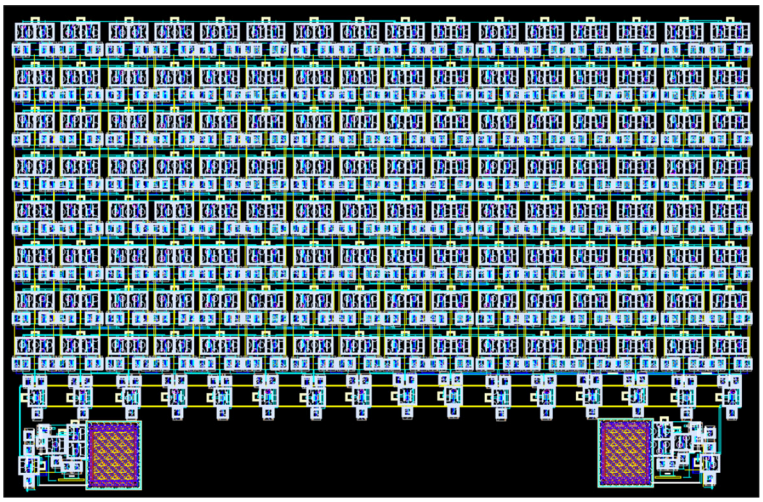

Fig. 16 Layout of SRAM array with body bias controller

read delay are 11.51 ps and 43 ps, respectively, for 200 samples, whereas the variability is 0.26. The minimum and maximum value of read delay is 15.56 ps and 75.07 ps.

4.5 Dynamic power dissipation

Dynamic power dissipation is obtained when an SRAM cell is operated in read or write mode. The decrease in threshold voltage with an increase in body bias results in higher driving capability of access and pull-down transistors leading to increased dynamic power dissipation. Table 3 shows the dynamic power dissipation during write and read operation of SRAM cell including parasitic components at different body voltages.

4.6 Layout

Figure 16 shows the layout of the 8×16 SRAM array. The area occupied by the proposed controller is 4.48 μm^2 while that of single 7T SRAM cell is 2.25 μm^2. Also, the total area occupied by 8×16 SRAM array is 302 μm^2. It has been observed that the total area occupied by 8×16 SRAM array with body bias controller is $46\times$ of

Table 4 Comparison of the proposed work with other existing SRAM cells

Parameters	Basic 6T SRAM cell [22]	PD at V_{body} = 0 V	PD at V_{body} = − 0.5 V	PD at V_{body} = 0.5 V	7T SRAM [17]	WRE8T SRAM [20]	9T SRAM [12]	8T SRAM [16]	9T SRAM [16]
Technology (nm)	28	28	28	28	28	28	28	28	28
Supply voltage (V)	1	1	1	1	1	1	1	1	1
Static power dissipation (pW)	300	330	180	NA	250	380	260	320	342
HSNM (mV)	334	370	400	NA	350	375	380	360	320
RSNM (mV)	260	324	370	NA	353	340	376	350	345
WSNM (mV)	340	338	NA	322	310	370	320	357	383
Read delay (ps)	90	38	43	NA	35	37	50	34	35
Write delay (ps)	54	54.74	NA	50	70	58	74	93	105

single SRAM cell with body bias controller. The total area occupied by the SRAM array is less because a two controller circuit shares a multiple column.

A comparison of proposed work with other existing SRAM cells is presented in Table 4. It can therefore be concluded that the proposed design showed better stability in standby and read mode while dissipating least power in comparison with other state-of-the-art work. This is due to variation in the threshold voltage which actually increases in hold and read operation while decreases during write operation. However, the proposed design will work properly if it would be designed beyond 28 nm or some advanced process. Some performance parameters would be affected, which can be improved by some optimization in design parameters of circuit.

5 Conclusion

SRAM design is governed by certain critical parameters such as static power dissipation, static noise margin and read and write delay. It is nearly impossible to design SRAM cell which shows improvement in all aforementioned parameters at the same time. Designers have always made compromises and have achieved improvement in some parameters at the cost of another. However, which parameter needs to be improved and which parameters can be compromised depends upon the requirement and application of the SRAM. In this paper, a novel body bias controller is implemented with 7T SRAM cell for reducing the static power dissipation and increasing the stability parameters. The changing of threshold voltage had increased the HSNM and reduction in write delay of SRAM besides achieving better result for power dissipation. It has been observed that there is a reduction of 40%, 28%, 41.9% and 30% in static power dissipation and enhancement of 19%, 14.2%, 6.6% and 5.2% in HSNM of the proposed design as compared to 6T SRAM cell, 7T SRAM cell, WRE8T SRAM cell and 9T SRAM cell, respectively. The proposed design is a suitable alternative for low power SRAMs. However, the WSNM of the proposed work can be further enhanced by implementing the proposed design with write assist technique. Furthermore, the proposed work can be designed at some advanced processes which results to enhance the capacity of memory that can be useful for high-performance networking applications.

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