Physical Design of 6T Cell of SRAM Devices and Comparative Analysis of Layout

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***Abstract*— The article discusses the possibilities of physical design of the most common 6T memory cell of modern SRAM devices and the physical design of 16-bit and 256-bit memory array based on it with 5 nm technology node. In the work, based on the schematic solution of the memory cell and information about the base of the used transistors and interconnections, five layout solutions of the 6T memory were proposed using two layers of metal. Based on them, the topology of array with 16, and 256 bits of memory were developed. Physical and schematic engineering simulations were performed for the proposed topological solutions. Based on the obtained results, a comparative analysis of the proposed layout solutions were performed in terms of the occupied area, current consumption and read/write delay times, temperature, supply voltages and process variation over a wide range.**

Keywords*— *6T SRAM cell, memory array, technological node, physical design, layout, power and current consumption, area, read/write delay

I. Introduction

The scaling of integrated circuit (IC) technologies has led to an increase of the leakage current flowing through transistors when operating in their static mode, resulting in power consumption increasing. As the technology scales, the influence of the physical structures and parameters of ICs on their electrical and functional characteristics increases. As the IC becomes more complex and the technological dimensions decrease, the influence of physical design on energy consumption, speed and placement of elements of the designed circuits increases, therefore the limitations presented to them become even more strict.

Static Random Access Memory (SRAM) devices have their unique place in modern ICs, the operating frequency of which reaches several GHz. At high frequencies the power consumption of SRAMs increases dramatically. In the production of modern ICs, the share of SRAMs accounts for about 60%, about 70% of the entire physical surface of the designed devices, about 50-70% of energy consumption is accounted for by the energy consumption of SRAM [1,2]. That is why intensive work is underway to develop new layout and circuit solutions that will help reduce the energy consumption of the designed SRAMs [3-7].

In the article, layout solutions of the most common 6T memory cell of modern SRAMs and 16 and 256 bit memory array based on them with technological node of 5 nm are proposed and their characteristics are investigated for various temperatures, power supply voltages and processes using Custom Compiler and HSPICE software tools.

II. 6T Memory Cell Structure And Layout Solutions

The electrical circuit of the 6T memory cell is shown in Fig. 1 [7].

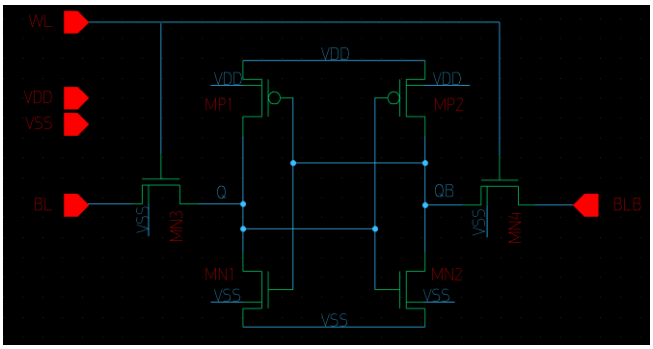

Fig. 1. The electrical circuit of the 6T memory cell

To read data from the 6T memory cell (Fig.1), the bit buses BL and BLB are precharged to logic 1 (VDD) level by the precharge circuit when the word bus WL is low. When WL=1, transistors MN3 and MN4 are open and the word bus is connected to the bit buses. In the case of a voltage difference ΔV on the bit buses, the M4 and M8 transistors are activated by the clock signal of the read amplifier and the output of the read amplifier switches to a logical "1" or "0" depending on the information stored in the memory cell, that is the difference in the voltage of the bit buses.

To ensure a stable reading from the 6T memory cell, it is necessary that the voltage at the Q node is lower than the threshold voltage, so that it does not turn on the MN2 transistor. This can be ensured by choosing the sizes of MN1 and MN2 transistors according to the following relation [8]:

$$\text{Cell Ratio}=\frac{W_{MN1}}{L_{MN1}}>\frac{W_{MN3}}{L_{MN3}} \quad (1)$$

Likewise, it is necessary that WMN3 = WMN4 and WMN1 = WMN2.

When registering 0, BL= 0 and BLB = 1 (VDD) and vice versa when registering 1, BL=1 (VDD) and BLB = 0 (VSS).

To ensure stable write in the 6T memory cell, it is necessary that the voltage at the Q node is less than the threshold voltage when the bit bus is at a low level, so that logical "0" is recorded. This can be ensured by selecting the sizes of MP2 and MN4 transistors according to the following relationship [8]:

$$\text{Pull up Ratio}=\frac{W_{MP2}}{L_{MP2}}/\frac{W_{MM4}}{L_{MN4}} \quad (2)$$

A. Cell Design and Sizing

2023 IEEE East-West Design & Test Symposium (EWDTS) | 979-8-3503-1484-7/23/$31.00 ©2023 IEEE | DOI: 10.1109/EWDTS59469.2023.10297065

Based on the physical design method proposed in [8-10], expressions (1) and (2), as well as taking into account the different placement of selection transistors and inverters, in case of having more than 1 word line (WL) to maintain the symmetry of BL and BLB signals and the principles of ensuring the smallest possible area, as well as the requirements of 5 nm technological nodes, five layout solutions of the 6T memory cell using two metal layers were proposed using the Custom Compiler tool, which are shown in Fig. 2 - Fig. 6. Figure 7 lists the designations used in the layout design.

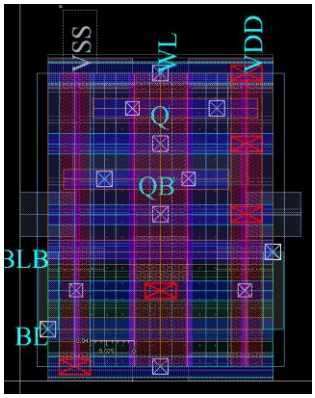

Fig. 2. The first layout solution of 6T memory cell - v1

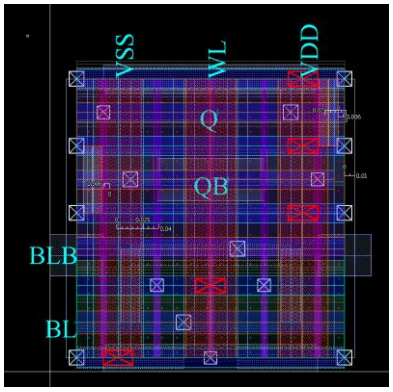

Fig. 3. The second layout solution of the 6T memory cell - v2

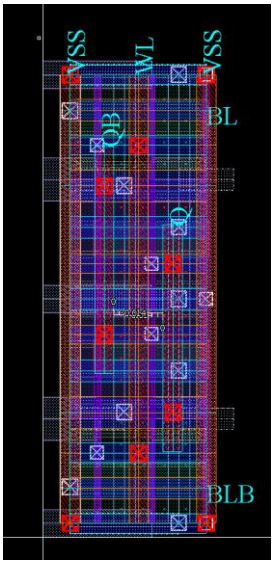

Fig. 4. The third layout solution of the 6T memory cell - v3

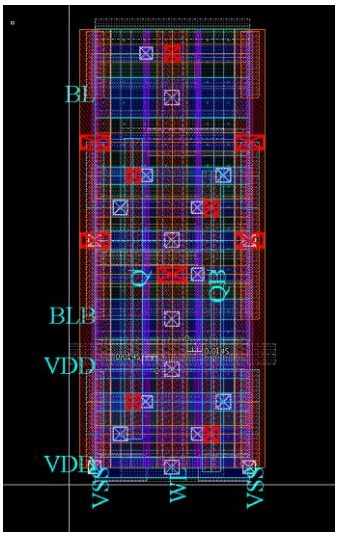

Fig. 5. The fourth layout solution of the 6T memory cell - v4

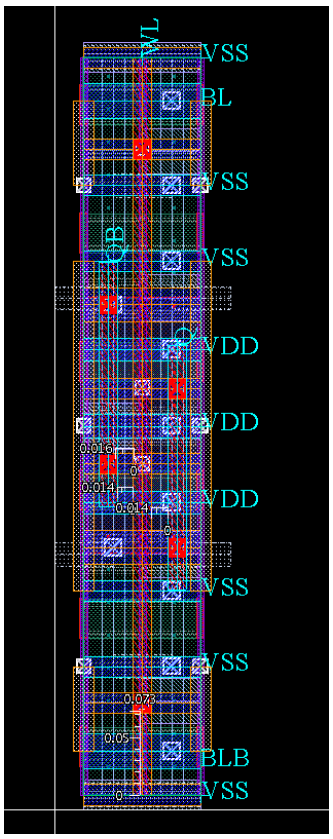

Fig. 6. The fifth layout solution of the 6T memory cell - v5

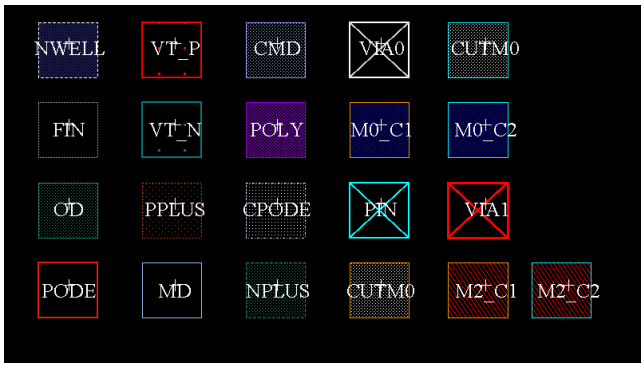

Fig. 7 Designations used in the layout design of the 6T memory cell

The results of the proposed layout solutions geometric sizes and area modeling based in 5nm technological nodes are given in Table 1.

TABLE I. AREA CELL

Type cell	Width (um)	Height (um)	Area (um^2)
v1	0.204	0.266	0.054264
v2	0.255	0.266	0.06783
v3	0.1275	0.42	0.05355
v4	0.153	0.434	0.066402
v5	0.102	0.644	0.065688

It can be seen from Table 1 that the smallest surface has the third version of the memory cell - v3.

B. Array Design and Area Comparison

Based on the layout solutions of the proposed memory cell, 16-bit and 256-bit memory arrays geometric sizes and area modeling were designed, the simulation results of which are presented in Table 2 (due to lack of space, the corresponding layout solutions are not presented).

TABLE II. AREA ARRAY SRAM

Type array	Width (um)	Height (um)	Area (um^2)
v1 - 4×4	0.816	1.064	0.868224
v2 - 4×4	1.02	1.064	1.08528
v3 - 4×4	0.51	1.68	0.8568
v4 - 4×4	0.612	1.736	1.062432
v5 - 4×4	0.408	2.576	1.051008
v1 - 16×16	3.264	4.256	13.89158
v2 - 16×16	4.08	4.256	17.36448
v3 - 16×16	2.04	6.72	13.7088
v4 - 16×16	2.448	6.944	16.99891
v5 - 16×16	1.632	10.304	16.81613

It can be seen from Table 2 that the smallest surface of the 16-bit and 256-bit memory array has the third version - v3.

III. CIRCUIT DESIGN AND MODELING OF 6T MEMORY CELL

Physical and circuit design simulations were performed for the proposed layout solutions. Based on the obtained results, comparative analyzes of the proposed layout solutions were performed according to the occupied area, current consumption and read/write delay times, temperatures, supply voltages and process variation within wide limits.

In the article, simulations of 6T memory cell, 16-bit and 256-bit memory arrays for temperature -40^{0}C - 125^{0}C, power supply voltage 0.6V - 0.9V, frequency 0.5GHz-2GHz intervals for slow, fast, and typical processes were performed using HSPICE software tools.

A. Read/Write Delay of Cells and Arrays

Based on the 6T memory cell and the proposed layout solutions of arrays with 16-bit and 256-bit information implemented on its basis, the results of schematic and technical simulations of write and read delays for 25^{0}C temperature, 1 GHz frequency and typical process are given in Fig. 8 - 10.

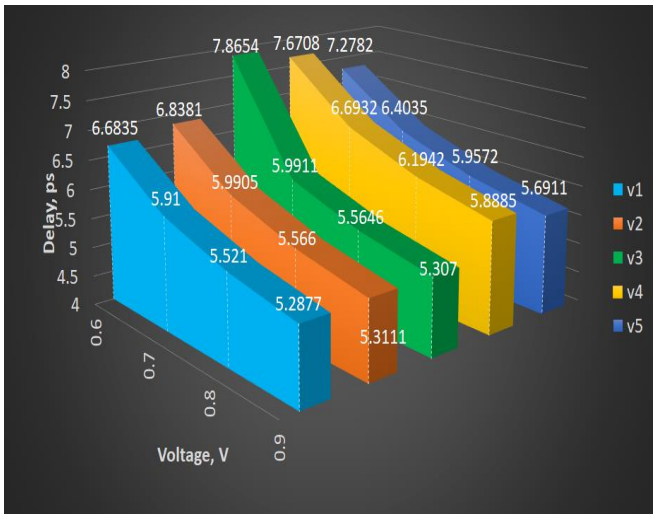

Fig. 8. The 6T memory cell read/write delays

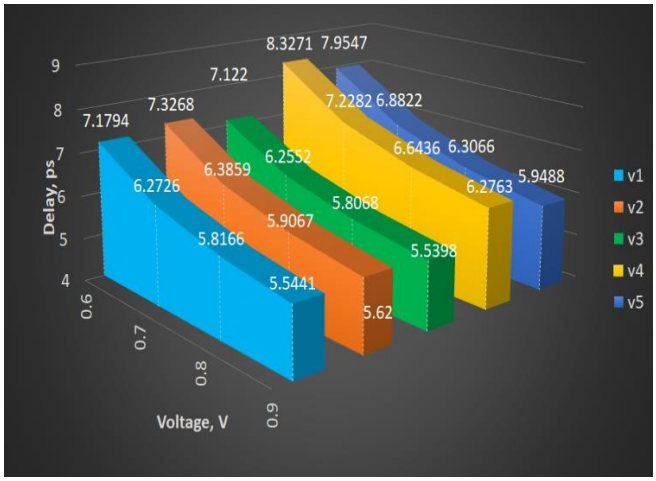

Fig. 9. The 6-bit (4×4) arrays read/write delays

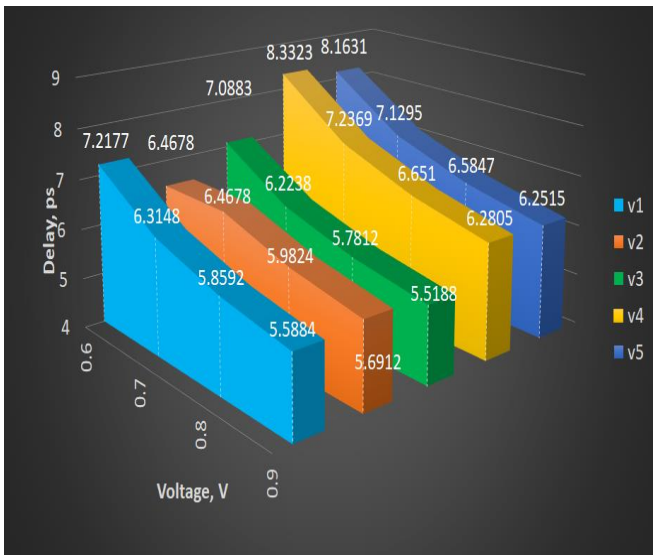

Fig. 10. The 256-bit (16×16) arrays read/write delays

It can be seen from Fig. 8 that the smallest delay has the v1 version of the layout solution of the memory cell, also, it can be seen from Fig. 9 and 10 that v3 version of the layout

solution of the 16-bit and 256-bit memory arrays has the smallest delay.

B. Current of Cells and Arrays

The results of circuit design and technical simulations of currents consumption based on the 6T memory cells and the proposed layout solutions of array with 16-bit and 256-bit for 25^0C temperature, 1GHz frequency and typical process are presented in Fig. 11 - 13.

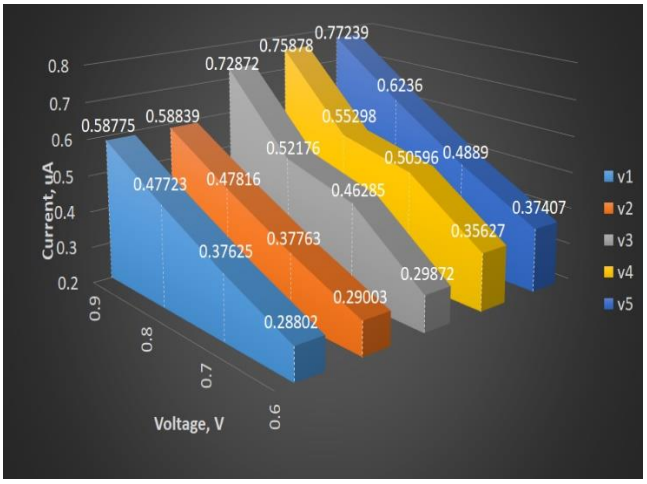

Fig. 11. The current consumption of the 6T memory cell

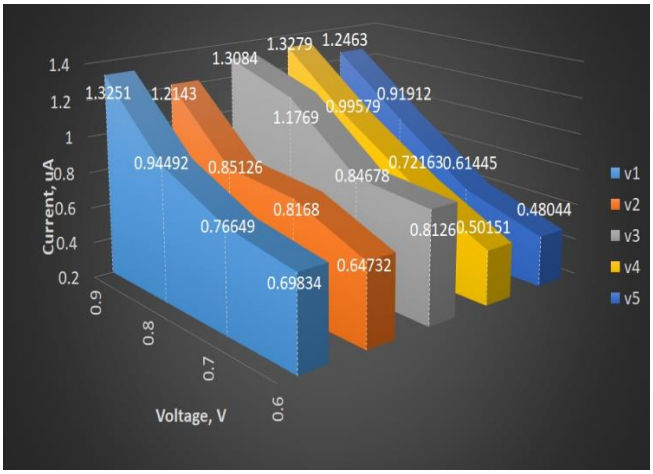

Fig. 12. The current consumption of a 16-bit (4×4) array

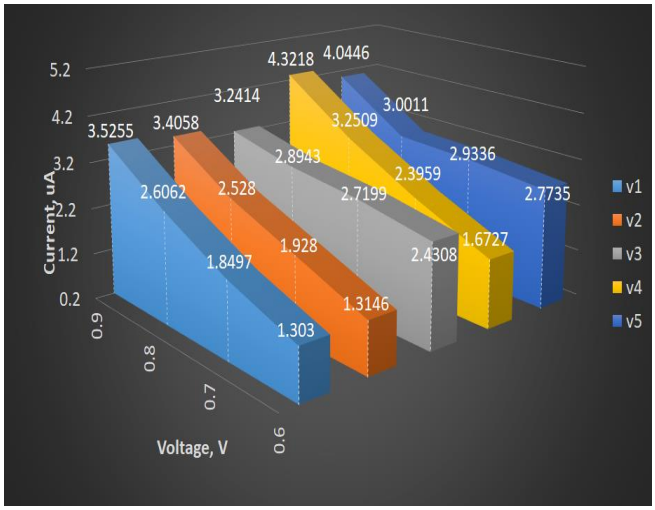

Fig. 13. The current consumption of a 256-bit (16×16) array

It can be seen from Fig. 11 that the smallest current consumption has the version v1 of the layout solution of the memory cell. It can be seen from Fig. 12 that the smallest current consumption has the v5 version of the layout solution of the 16-bit memory accumulator, and from Fig. 13 that the smallest current consumption has the version v1 of the layout solution of the 256-bit memory array.

The obtained results can be considered in the process of designing memory devices with high information memory for the selection of architectures and layout solutions of memory array with the required characteristics.

IV. Conclusion

The article discusses the possibilities of physical design of the most common 6T memory cell of modern SRAM devices and the physical design of 16-bit and 256-bit memory array based on it with 5 nm technology node. Their characteristics are investigated for temperature -40^{0}C - 125^{0}C, power supply voltage 0.6V - 0.9V, frequency 0.5GHz-2GHz intervals for slow, fast, and typical processes using Custom Compiler and HSPICE software tools. The obtained results can be used for the design of SRAMs.

Acknowledgment

The work was supported by the Science Committee of RA, in the frames of the research project № 21T -2B002.

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