2023 7th International Conference on Computation System and Information Technology for Sustainable Solutions (CSITSS) | 979-8-3503-4314-4/23/$31.00 ©2023 IEEE | DOI: 10.1109/CSITSS60515.2023.10333318

Low-Power 4 x 4 SRAM Memory Array Design Using Voltage Mode Technology

Kaartik R, Sujatha Hiremath, Eleena Mohapatra,
Department of ECE,RV College of Engineering, Bangalore, India, 560059
kaartikr.lvs21@rvce.edu.in, sujathah@rvce.edu.in, eleenamohapatra@rvce.edu.in

***Abstract*—The article describes an innovative design for a low power static random access memory (SRAM) cell, for high speed operations. The voltage mode method is adopted by the model to minimize voltage swings when performing write operation switching activity. In the design proposed, voltage sources are connected to the Bitline and Bitbarline which minimize voltage swing during the write state and is implemented using Cadence Virtuoso tool. The power consumption is calculated and tabulated with comparison to conventional 6-T SRAM cell. Overall, using this method, the power consumption of SRAM Cell is reduced by 6% and the overall delay is reduced by 26.2%. The layout area of proposed 6T SRAM cell is greater than conventional and this provides trade-off to achieve high speed and low power. Using proposed design, an array of 4*4 SRAM is designed using decoder circuits with precharge, sense amplifier and Write-driver unit. The proposed design can be used in various low-power applications of small or micro devices (Eg: Smartphone, Internet of Things devices), and other battery-operated systems.**

***Index Terms*—6T SRAM Cell, Decoders, Precharge Circuit, Sense Amplifier, Write-driver, CMOS, Cadence, 90nm technology, Power, Area, Delay**

I. Introduction

In low-power VLSI circuits created for high-quality applications, SRAM plays a key role. SRAM stands out among numerous integrated memory technologies. Low-power consumption has become an essential component in VLSI design, especially for high-speed systems. The dynamic dissipation of capacitance mainly depends on the frequency and voltage. Diminishing voltage stands as the simplest approach to decrease dynamic energy dissipation. Regrettably, this reduction in voltage significantly compromises performance.

Central to the evolution of CMOS technologies was the demand for devices that exhibit minimal power consumption. This focus has led to the establishment of CMOS devices as exemplars of low-power usage[1]. A vital challenge in VLSI design involves the implementation of low-power design, particularly in the context of high-speed systems[2]. In the majority of digital systems, dynamic power consumption usually takes the lead in power dissipation. Several variables, notably switching frequency, source voltage, and the voltage of the output swings, impact this dynamic power dissipation. The most effective way to cut down dynamic power dissipation is to opt for to lower supply voltage. Yet, the drawback lies in the marked performance degradation resulting from a lower supply voltage [3]. A reduction in the supply voltage causes a drop in the threshold voltage, leading to an increase in leakage current, consequently increasing rate of static power. Another avenue to reduce power and delay involves the limitation of the output voltage swing. Multiple methods are utilized to decrease voltage swings during behaviour changes within memory design[4].

II. Methodology

The design and performance analysis of SRAM is implemented with all cell designs created and tested using the Cadence tool. Initially, the different types of architectures of 6T-SRAM are studied and a proposed SRAM design is implemented in transistor level. The schematic is created by placing 6 transistors (4 n-type and 2 p-type) and connecting them according to the design of the memory cell. Similarly, the proposed memory cell is also created and placed. The Flow of implementation is represented in Fig. 1.

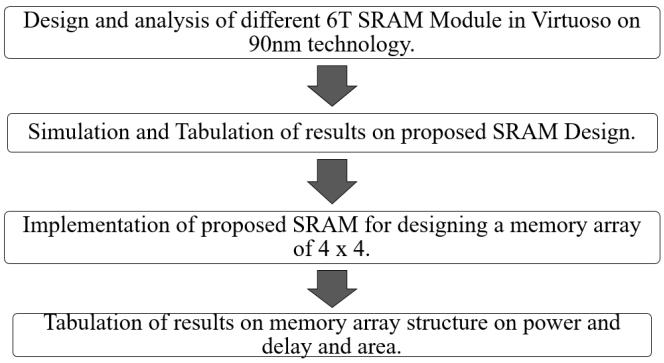


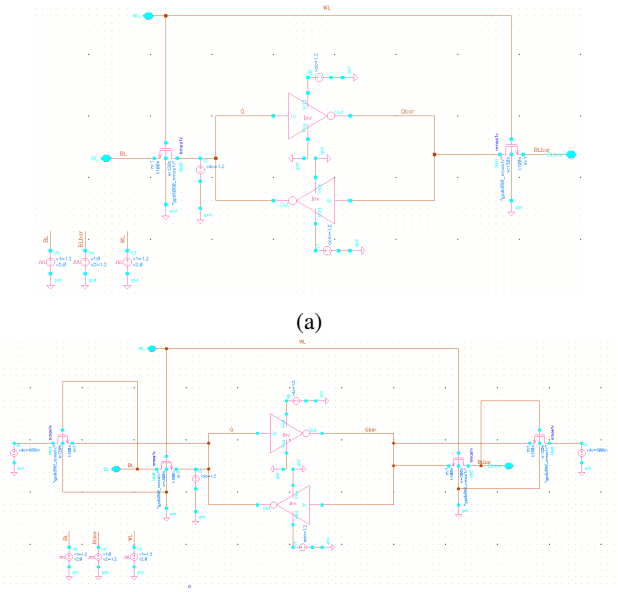
Fig. 1: Project Implementation Flow

Designing a 6T SRAM cell on transistor level using Cadence requires a thorough understanding of transistor-level design, layout guidelines, and simulation techniques. The SRAM selected is used for implementing the array of 4 x 4 logic using other circuits consisting of Decoders, Precharge Circuits, Write-driver Circuit and Sense Amplifiers and then analysed based on the performance with respect to delay and power of the array cell. Each design is first created on the schematic with all parameters fixed to a specific value for implementation and evaluation of the blocks. The custom array memory cell is designed to obtain an optimized layout on the Physical Design process.

A. *6T SRAM Cell*

The core element in the SRAM array is the 6-transistor SRAM cell[1]. Central to this circuit's functionality is a pair of

opposing inverters, which play a crucial role in preserving the stored data. Transistors M5 and M6 take charge of the reading and writing operations. In the Read operation, external sources refrain from driving the bit lines, allowing the stored data to expeditiously transfer to the bit lines upon the activation of the word line, facilitated by M5 and M6. During the Write operation, M5 and M6 steer a high and low signal, effectively altering the states of Q and Q-bar. The block diagram is similar to conventional memory Cell, but with an extra two nMOS transistors provided to the access transistors with voltage control as input to the same. The sizing of the cell is as shown in Table I. The conventional 6T SRAM Cell sizing is similar to the proposed but without the extra voltage control transistors. The schematic of both designs is shown in Fig. 2.



(a)

(b)

Fig. 2: (a) Schematic of 6T SRAM Cell (b) Schematic of proposed 6T SRAM Cell

TABLE I: Sizing of Proposed 6T SRAM Cell

Description	*Transistor*	*Width*
Memory Element of SRAM	P1	480n
	P2	480n
	N1	240n
	N2	240n
Access Transistors	AT1	120n
	AT2	120n
Voltage Control Transistors	VT1	300n
	VT2	300n

B. *Memory Array Structure*

Based on the proposed 6T SRAM Cell, this project aims to design an SRAM memory array structure of 4*4 using decoders and Precharge, Sense Amplifier and Write-driver circuit. The same design structure is shown in Fig. 3. The array structure consists of the memory cell, row and column decoders and Precharge units.

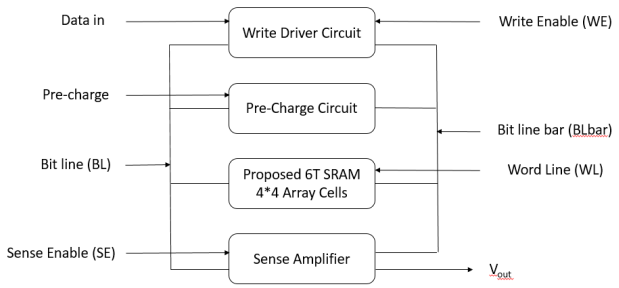


Fig. 3: Basic Memory Architecture

*1) **Row Decoders & Column Decoders**:* The row address & column address input signals are decoded with the help of Row & Column decoder and they help in selecting the appropriate row of memory cells in the array. The decoder circuit typically consists of a set of CMOS inverters connected in a specific pattern. The pattern is designed such that each row of memory cells corresponds to a unique combination of row & column address input signals. When the appropriate combination of input signals is received, the decoder circuit activates the corresponding row or column-select transistor.

*2) **Write-drivers**:* Write-drivers are used to write data to the memory cells by driving the bit lines with the appropriate voltage level. Write-drivers are implemented as CMOS transistors that are connected to the bitlines of the memory array cell. During write operation, the appropriate voltage level is applied to the bitlines to write the data to the memory cell.

*3) **Precharge Circuit**:* The Precharge circuit is an essential component of memory cell. It's in charge of getting the memory cell ready for a fresh read- or write-operation by resetting the internal nodes of the cell. The Precharge circuit operates by applying a pre-charge voltage to the bitline and word line, which resets the memory cell to a known state. During a read operation, the Precharge circuit is first activated, which sets the bit line and word line to a pre-determined voltage level. The Precharge circuit is also used during a write operation to ensure that the memory cell is properly prepared for the new data input. When a write operation is initiated, the Precharge circuit is first activated to restart the memory cell. The new data is then written to the memory cell by activating the appropriate word line and bit line, which changes the voltage level of the memory cell.

*4) **Sense Amplifier**:* It is used to amplify and detect the voltage difference in the bitlines of the memory array, for reading data stored in memory cells. Sense amplifiers are typically implemented as differential amplifiers. The output is sent to the output buffer for further processing.

The differential amplifier is responsible for amplifying the voltage difference between the bitlines of the selected memory cell. The amplifier typically consists of two CMOS inverters connected in a differential configuration. The output of the

differential amplifier is connected to the input of the precharge circuit.

The precharge circuit is responsible for restoring the voltage levels on the bitlines to their initial state before the next read operation. The circuit typically consists of a set of PMOS transistors that connect the bitlines to the power supply during the precharge phase.

The speed and precision of a sense amplifier are two important design considerations. The circuit should be able to accurately detect small voltage differences between the bit lines and provide a fast response time to enable high-speed data access. Additionally, the power usage of the sense amplifier is crucial since it has an impact on the memory array's overall power usage.

With the theoretical aspects as discussed in this section, the same is incorporated using the tool in the next section where all the results and their observations and noted and represented for the inputs considered.

III. Results and Observations

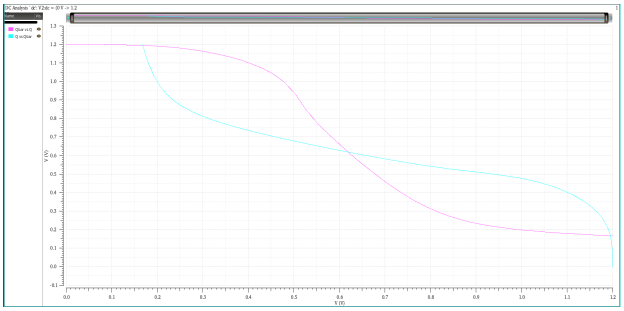
This paper presents the implementation of low-power memory array constructed using 6T SRAM cells, accompanied by essential circuitry including Precharge circuits, decoder circuits, Write-driver circuits, and sense amplifier circuits using Cadence tool. The design and analysis are carried out using Cadence Virtuoso tool and Spectre tool on 90nm technology and the results are tabulated. Also, each circuit layout is implemented using Cadence Virtuoso Editor tool. This work provides an analysis of critical performance metrics such as delay, power consumption, and layout area for each circuit. Before moving forward with the implementation of the array, Stability analysis is performed on SRAM designs.

A. *Stability*

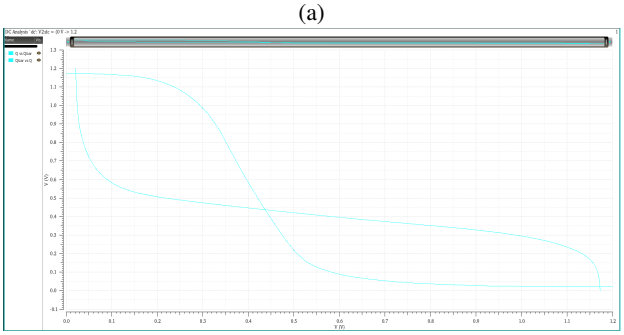
The stability of a SRAM cell can be determined by its Static Noise Margin(SNM) levels. There are three different types of Static Noise Margin levels one can obtain while performing DC analysis on the behaviours of the SRAM cells. One can determine the SNM through the measurement of the butterfly curve method. They are categorized as:

- *Read SNM* - Read Stability (or) Read Margin can be defined as the ability to prevent the SRAM from changing a stored value during the read operation.
- *Write SNM* - Write Stability (or) Write Margin can be defined as the ability of the SRAM cell to allow a change in the stored value.
- *Hold SNM* - Hold Stability is defined as the capability of SRAM to withhold or not allow the change in output when the 'WL' is not active.

The SNM analysis is conducted for both the SRAM modules designed. The DC analysis is performed for the schematic & the Read Noise Margin Values for each SRAM cell design are obtained as shown in Fig. 4. and tabulated.



(a)

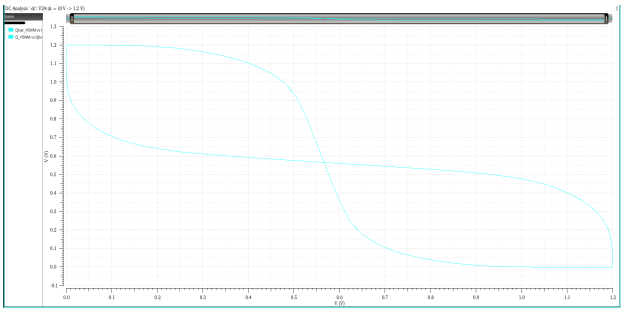


(b)

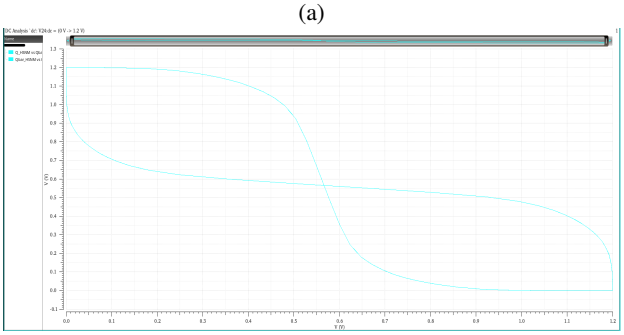
Fig. 4: (a) Read SNM of 6T SRAM Cell (b) Read SNM of proposed 6T SRAM Cell

Similarly, The DC analysis is performed for the schematic & the Hold Noise Margin Values for each SRAM cell design are obtained as shown in Fig. 5. and tabulated.

Also, the DC analysis is performed for the schematic & the Write Noise Margin Values for each SRAM cell design are obtained as shown in Fig. 6. and tabulated.

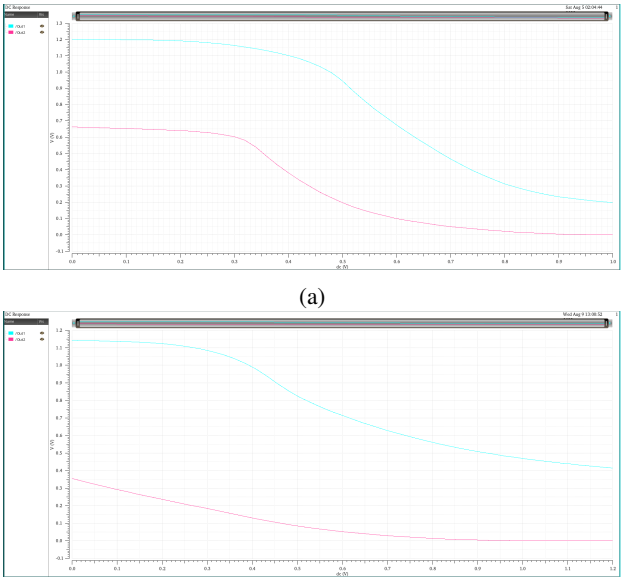


(a)



(b)

Fig. 5: (a) Hold SNM of 6T SRAM Cell (b) Hold SNM of proposed 6T SRAM Cell



(a) (b)

Fig. 6: (a) Write SNM of 6T SRAM Cell (b) Write SNM of proposed 6T SRAM Cell

Table II provides the tabulated results of Stability margins for SRAM's designed above.

TABLE II: Stability Margin of SRAM Modules

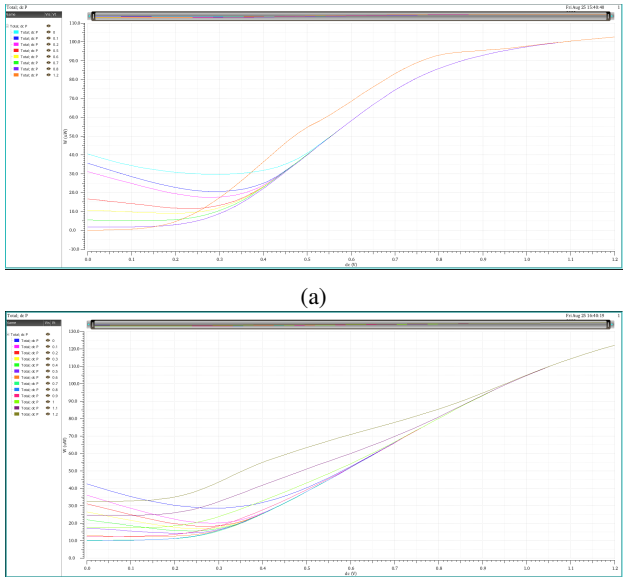
Stability (SNM)	*6T SRAM Cell*	*Prop. 6T SRAM Cell*
Read	68mV	50mV
Hold	240mV	235mV
Write	510mV	490mV

Based on the above Transient & DC Analyis performed for both the SRAM design Cells, the delay and power are also estimated and the same result is tabulated in Table III. The input supply voltage provided for the analysis is 1.2V, with a period of 100ns. The sizing of the transistors was considered as required.

TABLE III: Delay and Power Consumption of 6T SRAM Cell & Prop. 6T SRAM Cell Design

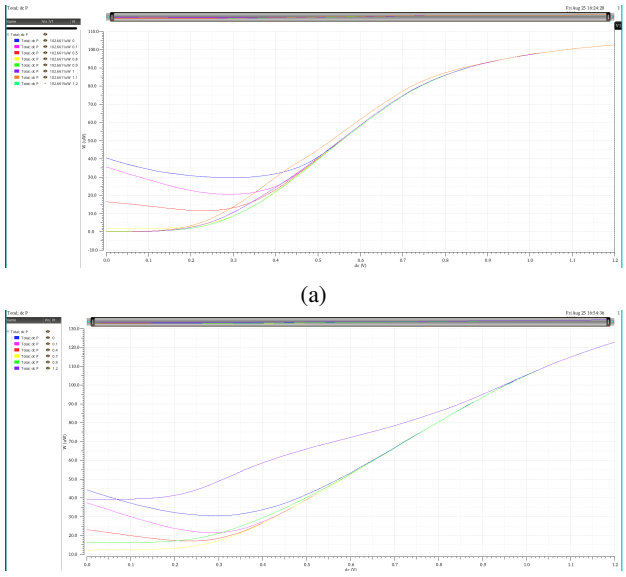
SRAM Design	*Read Power (μ W)*	*Write Power (μ W)*	*Read Access Time (ps)*	*Write Access Time (ps)*
6T SRAM Cell	102.6615	102.6615	79.75	68.62
Prop. 6T SRAM Cell	70.4688	122.307	68.23	42.58

Also, for both the SRAM's a parametric analysis is conducted for both Read and Write operations with variable supply voltage from 0V to 1.2V in linear steps of 0.1V and the DC analysis of the same is shown in Fig. 7 for Read Operation and Fig. 8. for Write Operation. From both graphs, it can be seen that, the total power consumption increases as the supply voltage increases and attains the peak value at a maximum supply voltage of 1.2V.



(a) (b)

Fig. 7: (a) Parametric analysis of Read SNM of 6T SRAM Cell (b) Parametric analysis of Read SNM of proposed 6T SRAM Cell

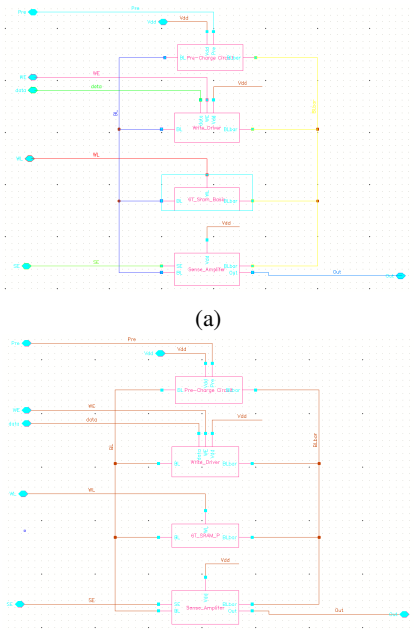


(a) (b)

Fig. 8: (a) Parametric analysis of Write SNM of 6T SRAM Cell (b) Parametric analysis of Write SNM of proposed 6T SRAM Cell

B. Single Bit SRAM Cell

With all the necessary circuits required to implement an array of SRAM cells, one has to first design a single-bit SRAM Cell which includes the other circuits such as Precharge Circuit, Write-driver Circuit and Sense Amplifier Circuit and check its functionality for correct behaviour of the design as per requirement. The same is designed using both the conventional memory cell and the proposed memory cell and their schematic is as shown in Fig. 9.



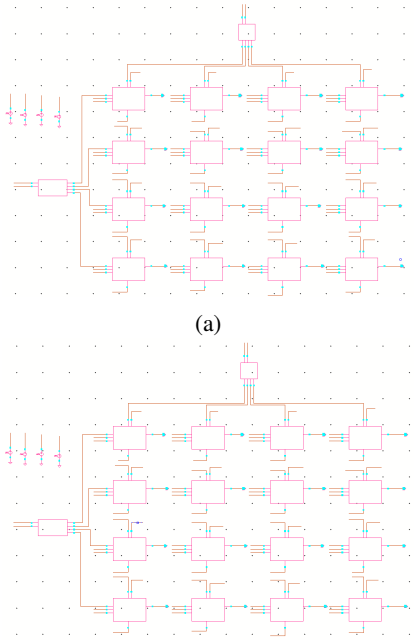
(a)

(b)

Fig. 9: (a) Schematic of Single Bit 6T SRAM circuit (b) Schematic of Single Bit Prop. 6T SRAM circuit

C. *Array*

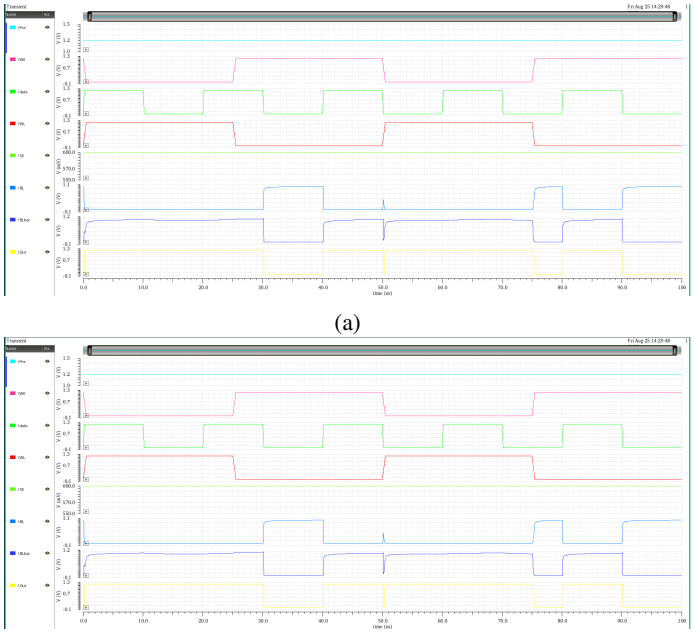
With the single bit 6T SRAM & Prop. 6T SRAM Cell working, the design and implementation of 4*4 SRAM Cell Array is implemented for both the designs and the schematic is as shown in Fig. 10. Both the array designs are tested for correctness through transient analysis for a period of 100ns by providing the required input bit signals and the same is shown in Fig. 11.



(a)

(b)

Fig. 10: (a) 4*4 Array of Conventional 6T SRAM circuit (b) 4*4 Array of Proposed 6T SRAM circuit



(a)

(b)

Fig. 11: (a) Transient Analysis of 4*4 Array of Conventional 6T SRAM circuit (b) Transient Analysis of 4*4 Array of Proposed 6T SRAM circuit

For the Array of Conventional 6T SRAM Cell, with the bit inputs for Row Decoder a & b as 1 & 0 and Column Decoder c & d as 0 & 1, the SRAM Cell of Third Row, Second Column is selected to perform operations on the particular SRAM Cell. The same can be seen in Fig. 11a. It can be seen that, the output bit line is changing as the Write-Enable(WE) and Word-Line(WL) change with the data provided. The change observed in the output bit line shows that, the SRAM cell of the particular array is performing the write, read (or) hold operation.

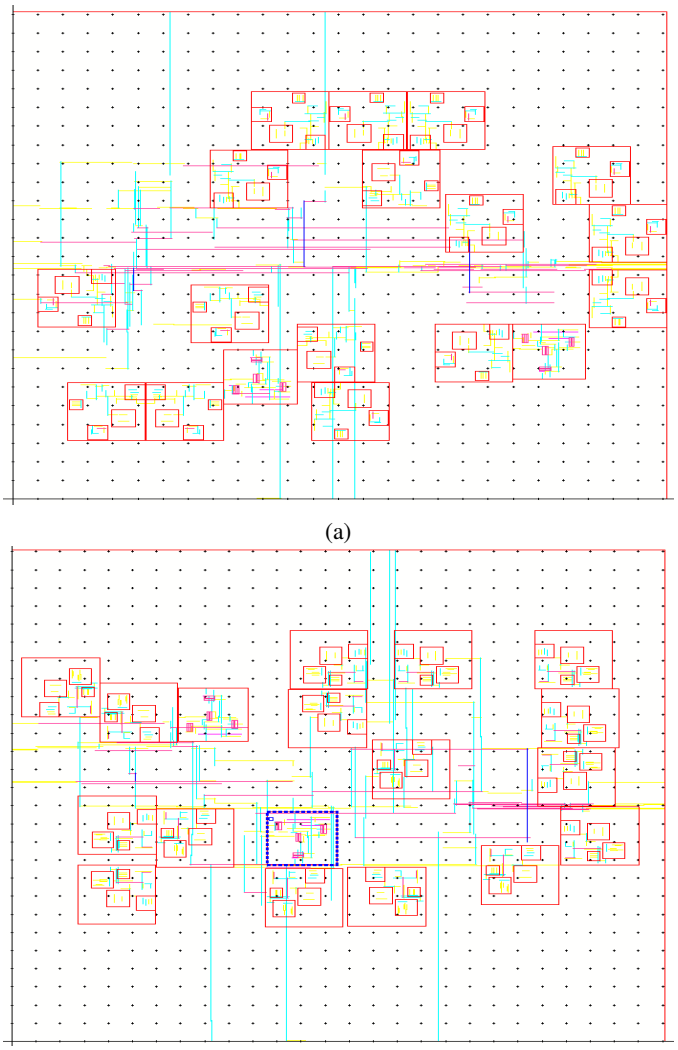
Similarly, For the array of proposed 6T SRAM Cells, when row decoder inputs a & b are selected as 0 & 1 and Column Decoder c & d as 1 & 1, the SRAM Cell of the Second Row, Fourth Column is selected to perform operations of either read, write or hold data based on other input variable parameters provided & the same is shown in Fig. 11b.

The functionality check over the array working is found to be correct and then we have continued to implement the layout of each cell design using Cadence Virtuoso Layout Editor tool. The next section provides more information on the same.

D. *Layout*

From the above results and observations, each circuit is then implemented on the layout using Cadence Virtuoso Layout Editor tool on 90nm technology file as a base and following the design-based and the λ based rules, the circuit schematics are represented and ending with tabulation of the total layout area calculation of each circuit. The layout of both proposed 4*4 SRAM array v/s layout of conventional 4*4 SRAM array is as shown in Fig. 12a. & Fig. 12b. From the schematic of Single Bit SRAM Cells of both conventional and proposed, the

layout is constructed accordingly. The layout area is found to be 17082.5 μmm^2 & 18357.54 μmm^2.



(a)

(b)

Fig. 12: (a) 4*4 Array Layout of conventional 6T SRAM (b) 4*4 Array Layout of proposed 6T SRAM

After the optimization of the layout of each cell, the overall layout area is calculated and tabulated in Table IV.

TABLE IV: Layout Area of Cell Designs

Cell Name	***Area (μmm^2)***
6T SRAM	15.449
Proposed 6T SRAM	20.4304
Precharge Circuit	6.94
Write-driver Circuit	15.6816
Row Decoder & Column Decoder	213.306
Sense Amplifier	22.441
Single bit 6T SRAM Cell Module	240.25
Single bit proposed 6T SRAM Cell Module	260.176
4*4 Array of 6T SRAM Cell	17082.5
4*4 Array of proposed 6T SRAM Cell	18357.54

E. Conclusion

From the above results and observations sections, it can be concluded that, by using the Proposed 6T SRAM Array, we can achieve higher speeds and less power consumption but with trade-off for total area v/s as power and delay. As the idea was to have better read efficiency of 6T SRAM Cells, a voltage-controlled better readability Proposed 6T SRAM cell was introduced which provided us with better read access time as to the original. This also provided low power consumption as compared to conventional 6T SRAM cell and therefore, depending on the trade-off between total area consumption & delay, power a designer can consider the following 6T Cell for applications of low power such as IoT Devices, Mobiles etc.

REFERENCES

[1] Xue, Xingsi, Aruru Sai Kumar, Osamah Ibrahim Khalaf, Rajendra Prasad Somineni, Ghaida Muttashar Abdulsahib, Anumala Sujith, Thanniru Dhanuja, and Muddasani Venkata Sai Vinay. 2023. "Design and Performance Analysis of 32 × 32 Memory Array SRAM for Low-Power Applications" Electronics 12, no. 4: 834.

[2] Y. Wang, S. Zhang, Y. Li, J. Chen, W. Zhao and Y. Ha, "A Reliable and High-Speed 6T Compute-SRAM Design With Dual-Split-VDD Assist and Bitline Leakage Compensation," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 5, pp. 684-695, May 2023, doi: 10.1109/TVLSI.2023.3243027.

[3] J. Chen, W. Zhao, Y. Wang, Y. Shu, W. Jiang and Y. Ha, "A reliable 8T SRAM for high- speed searching and logic-in-memory operations", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 30, no. 6, pp. 769-780, Jun. 2022.

[4] Anil Kumar Rajput, Manisha Pattanaik, Gaurav Kaushal, "Local bit-line shared pass-gate 8T SRAM based energy efficient and reliable In-Memory Computing architecture", Microelectronics Journal, Volume 129, 2022, 105569, ISSN 0026-2692.

[5] Xinpeng Jiang, Junlin Bao, Li Zhang, Lei Bai, "A novel dual-reference sensing scheme for computing in memory within STT-MRAM", Microelectronics Journal, Volume 121, 2022, 105355, ISSN 0026-2692

[6] J. Chen, W. Zhao, Y. Wang and Y. Ha, "Analysis and design of reconfigurable sense amplifier for compute SRAM with high-speed compute and normal read access", IEEE Trans. Circuits Syst. II Exp. Briefs, vol. 68, no. 12, pp. 3503-3507, Dec. 2021.

[7] Z. Lin et al., "Two-direction in-memory computing based on 10T SRAM with horizontal and vertical decoupled read ports", IEEE J. Solid-State Circuits, vol. 56, no. 9, pp. 2832-2844, Sep. 2021.

[8] X. Si et al., "A local computing cell and 6T SRAM-based computing-in-memory macro with 8-b MAC operation for edge AI chips", IEEE J. Solid-State Circuits, vol. 56, no. 9, pp. 2817-2831, Sep. 2021.

[9] T. Alan, A. Gerstlauer and J. Henkel, "Cross-layer approximate hardware synthesis for runtime configurable accuracy", IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 29, no. 6, pp. 1231-1243, Jun. 2021.

[10] J. Chen, W. Zhao, Y. Wang and Y. Ha, "Analysis and optimization strategies toward reliable and high-speed 6T compute SRAM", IEEE Trans. Circuits Syst. I Reg. Papers, vol. 68, no. 4, pp. 1520-1531, Apr. 2021.

[11] Chinmay, C., M. S. Kenchannavar, A. Tejaswini, and B. S. Kariyappa. "VTEAM model based in-memory computation using memristors." International Journal of Innovative Technology and Exploring Engineering 9 (2019): 3426-3432.

[12] H. V. Ravish Aradhya, J. Fadnavis and S. G. Gojanur, "Memory Design and Verification of SRAM-based Energy Efficient Ternary Content Addressable Memory," 2021 5th International Conference on Information Systems and Computer Networks (ISCON), Mathura, India, 2021, pp. 1-7, doi: 10.1109/ISCON52037.2021.9702386.

[13] N. H. Yatagiri and S. K.B., "Low Power Self-Controlled Pre-Charge Free Content Addressable Memory," 2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2019, pp. 1225-1229, doi: 10.1109/ICECA.2019.8821852.

[14] Manoj Y, Dr. B S. Kariyappa, "A review on Buffer Chips and growing Memory Bandwidths", 2022 International Journal for Research in Applied Science & Engineering Technology (IJRASET), ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.538; Volume 10; Issue VII, pp. 3935-3942, doi: https://doi.org/10.22214/ijraset.2022.45912.