Implementation of High Performance 6T-SRAM Cell

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Abstract- Now a days each and every device equipped with large capacity memories in order to full fill all the needs of customers. And there are some other parameters which plays an important role in the determination of performance of the device they are power consumption and delay. In many widgets, memory is an integral part and its size also scales down as the device size is reduced. For this reason, every computerized device has low power and high speed is a prime concern**.** Current day scenario suggests that 6T SRAM is commonly used for the SRAM based memorydesignsas they are advantageouscompared to other cells. Low power is the major concern of today's electronics industries where, Static as well as Dynamic power dissipation are the two key parameters that should be taken into consideration. To meet consumer needs high bandwidth and low power and high speed consuming storages are also required.This paper mainly focuses on reducing powerdissipation of Static Random Access Memory (SRAM). Power reduction and Delay reductions are the major challenge of digital Industry. A simple and advantageous configuration of a SRAM cell is by connecting two CMOS inverters back to back. This configuration has good noise immunity.

1. Introduction

The technological innovation of low power circuits has been on rise as the demand as there is a considerable growth in the battery driven portable consumer electronics in a daily usage. The importunity forlighter, smaller andextremely durable electronic products implies to low power requirements. When dealing with the portable systems, the battery life becomes a big product differentiator. And also, an exponential growth in the consumer electronics like laptops, cellular networks and portable systems, has glorified the research efforts in low power microelectronics. For any of these consumer systems, low power consumption is the prime objective, as it directly affects their performance. Considering the advancements in the way a consumer wants the electronics handled, low power VLSI design has acquired great importance as an active and rapidly developing field.

Considering the technological advancements, it has become possible and inevitable to scale down the electronics involved in numerous applications. The advantage being that the technology becomes more portable and its applications increases, MTCMOS and gated V_{DD} are the two different techniques which are used to reduce the power dissipation compared to that of the standard 6 transistor SRAM.

SRAMswith ultra-low power are the paramount parts of many VLSI chips. The on-chip cache capacity is exponentially growing in current day microprocessors as the demand to close in on the gap between the main memory and the speeds of the processors justifies. For this to work, low power operation has become inevitable. As there is a raise in the integration and speeds at which the microprocessors are working, the dissipation of power remains the point of interest as the appliances that are driven by battery power keep on increasing.

Two key purposes in the SRAM (Static Random Access Memory) design can be noticed. The first is to accommodate a direct connectivity with the CPU,with speeds that DRAMs do not support and second is to replace DRAMs in system that requires low power consumption. SRAM serves two different roles

in each of the functions. In the first function, the SRAM works as cache memory, which interfaces DRAMs and the CPU. And as second function, SRAMs arebeing in the applications that require ultra-low power.

2. CMOS based 6T-SRAM Cell

Static random-access memoriesare special setof memory which can hold on to its stored information as long as the power rails are ON. Whereas the traditional DRAMs need periodic refreshes. The term "random access" impliesto the mechanism that any cellin the array of SRAM cellscan be written or read irrespective of the last accessed cell.

A single 6T-SRAM memory cell comprises of two access transistors along with two cross-coupled inverters. Access transistors connect SRAM cell to the external side. The conterminously connected inverters actlike a memory cell that stores one single data bit ('0' or '1')in the cell as long as the supply voltage (V_{DD}) is intact. The access transistors connect the cell to the bit-lines(BL and BLB).In the figure below (Figure 1.), the configuration of CMOS based SRAM cell is illustrated.

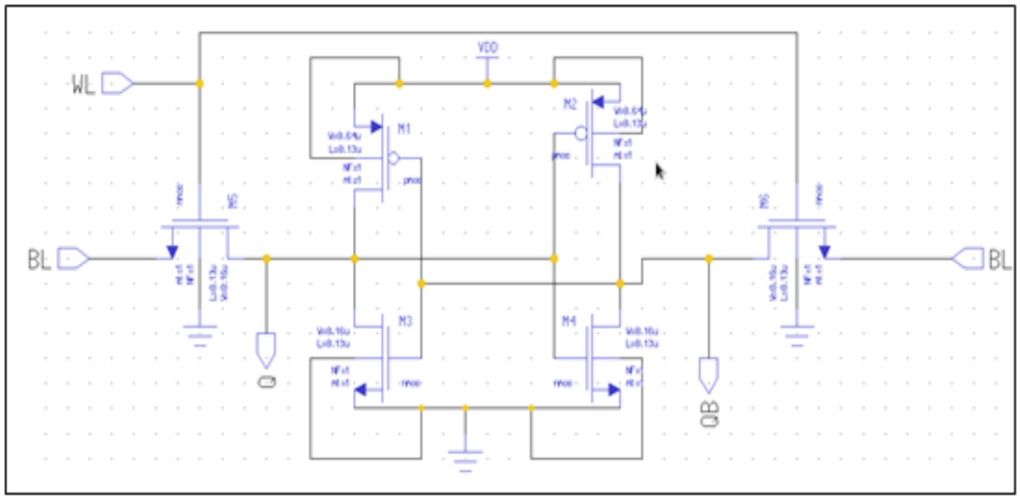

Figure 1. Schematic of one bit6T-SRAM cell

Variegated operating modes in which the SRAM cell are described as below.

2.1 Operating Modes of SRAM

An SRAM cell essentially has three distinguishedoperating states.

i) Hold/Standby mode:If the word line (WL) is set tologic'0', the SRAM cell enters into 'Hold mode'. As the name indicates, when the cell is in hold mode it holds the previous state.

ii) Write mode:If the word line (WL) is at logic '1' and the bit lines (BL and BLB) are used as inputs to memory cells, then the cell in the write mode. In this write mode the data to bewritten into the memory cell will be fed as input to the bit lines.

iii) Read mode:In this mode the data bit present in the memory cellcan be read. For this operation, the bit lines (BL and BLB) should be pre-charged to V_{DD} i.e. logic '1'. The word line should then be enabled by configuring it to logic '1'. Based on the data bit present in the memory cell, a bit line BL and BLB gets discharged slightly (and slowly) through an access transistor and pull-down transistor. This operation results in impulsing a differential voltage drops in between the bit lines (BL and BLB). This principally is the output i.e., the bit stored.

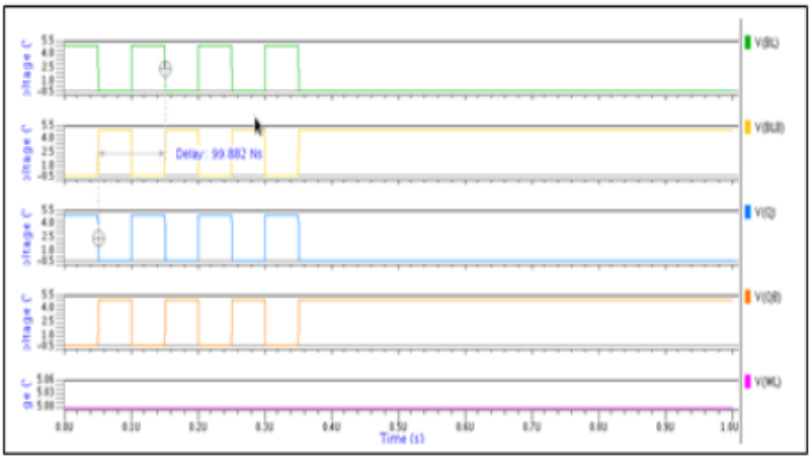

Figure 2. Input and output waveforms of CMOS based SRAM

3. Implementation of 6T SRAM cell Using Low Power VLSI Techniques

In this paper SRAM cell can be designed by using two techniques they are Gated V_{DD} and Multi Threshold CMOS technique. By using these techniques, the dynamic power dissipation will be reduced.

3.1 Design of 6T SRAM Cell Using Gated V_{DD} Technique

This technique uses one more n-channel MOS transistor connected to the pull-down network in the SRAM memory cell as pictured below in figure 3.

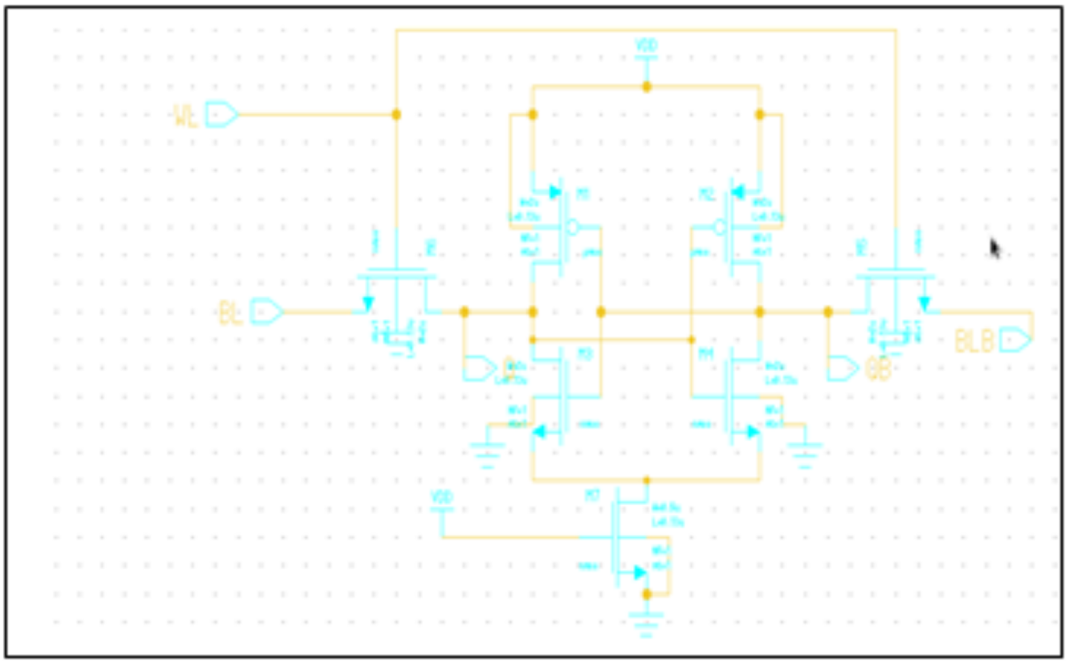

Figure 3. Schematic of Gated V_{DD}-SRAM cell

This approach initiates a switching mechanism which disables the power supply rails, when the SRAM is not under working condition. Introducing such a transistor helps in reducing the reverse leakage power dissipated by a large amount. To attain such a mechanism, a transistor with higher threshold voltage "High Vt" should be used for the ground path enabling all the left-over transistors in low threshold voltage "Low Vt". The "Low Vt" transistors are utilized as the switching speed is faster than that of

High Vt transistors. This can also imply the switching rate of High Vt MOSFETs is lower than that of Low Vt MOSFETs. A 'Gated V_{DD} control' signal can be used in order to toggle the SRAM cell. And so the word" Gated" is mentioned to explain such a mechanism.

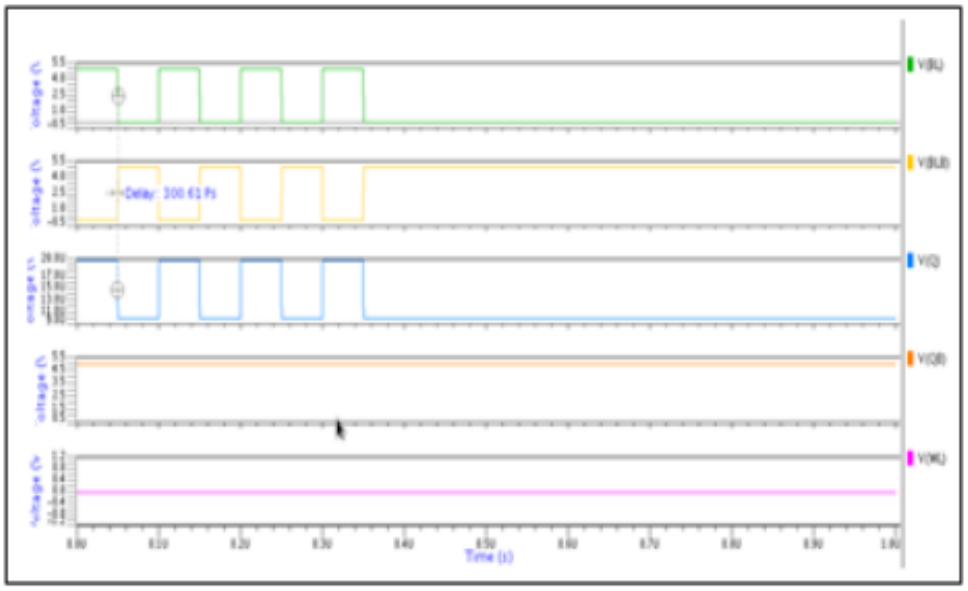

Figure 4. Input and output waveforms of SRAM cell using Gated V_{DD}

3.2 Design of 6T SRAM Cell Using MTCMOS Technique

MTCMOS (Multi Threshold CMOS) is a potent method for reducing leakage currents in the hold mode. This approach uses transistors that possess multiple threshold voltages for power and better latency. This involves usage of high Vttransistors for gating the supply rails of the low-Vtconfigurable logic block as shown in figure 5. When the high- Vttransistors are turned on, the low- Vtlogic is connected to virtual ground. Power and switching is performed through fast devices. As there are irregularities in the sizes of the transistors, a MTCMOS circuitry will go through"performance penalty" compared to basic CMOS based circuitry.

The transistors (high-Vt gating) are triggered, when the cell enters the standby mode. This makes the flow of a very low sub threshold leakage current from V_{DD} to ground. The PMOS and NMOS gating transistors are shown in Fig. 5. Only single type of sleep device is necessary, either NMOS transistor or PMOS transistor is good enough to minimize the leakage currents if in case the configurable logic cell is solely combinational. The preference is more for NMOS sleep transistors due to their lower resistance.

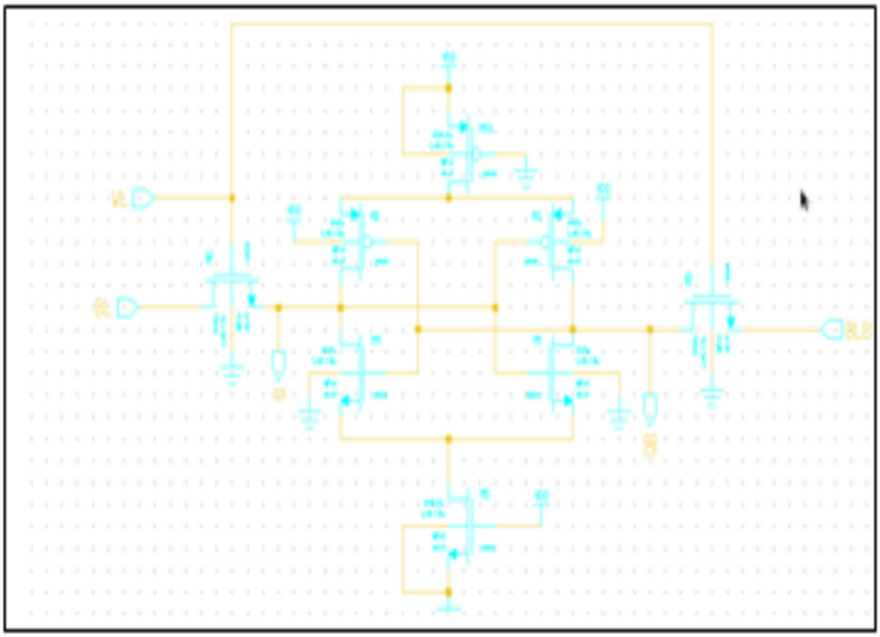

Figure 5. Schematic of MTCMOS SRAM cell

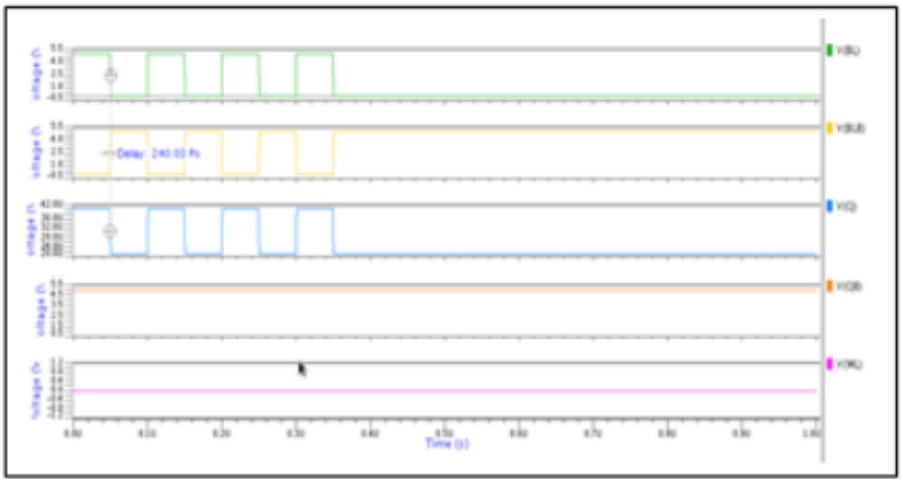

Figure 6. Input and output waveforms of SRAM cell using MTCMOS

MTCMOS technique reduces the leakage current exponentially due to increase in threshold voltage. In the case of the sleep transistors being turned off strongly, further reduction can be obtained. MTCMOS is one of the potent techniques for the reduction of leakage currents during hold modes as it is not complicated to convert existing CMOS circuit to convert into MTCMOS blocks. This can be done by adding high-Vt switches at the power supply rails.

4. Results

The write power dissipation and write latencyare calculated for numerous SRAM cells. Schematics of aMTCMOS based SRAM cell, gated SRAM cell and abasic SRAM cell are designed and simulated with the use ofa ‘mentor graphics backend tool’. All the transistors are sized to obtain the optimum delay. The below shown are simulation results of 6T SRAM cell using CMOS and Gated V_{DD} and MTCMOS

techniques respectively in the figures 2, 4and 6 respectively. The table.1 is the power dissipation results comparison and then followed bar graph representation shown in figure 7, table 2 is the delay comparison of various circuits and then represented by using bar graph as shown in figure 8.

Table 1. Power Dissipation of SRAM cells

Supply Voltage (V)	CMOS (nW)	Gated V_{DD} (nW)	MTCMOS (nW)
0.75	77.3955	77.3300	77.2627
1.25	78.9590	78.9244	78.8818
1.8	81.9316	81.9041	81.8691
2.5	89.1835	89.1582	89.1253
3.3	107.1267	107.099	107.0635

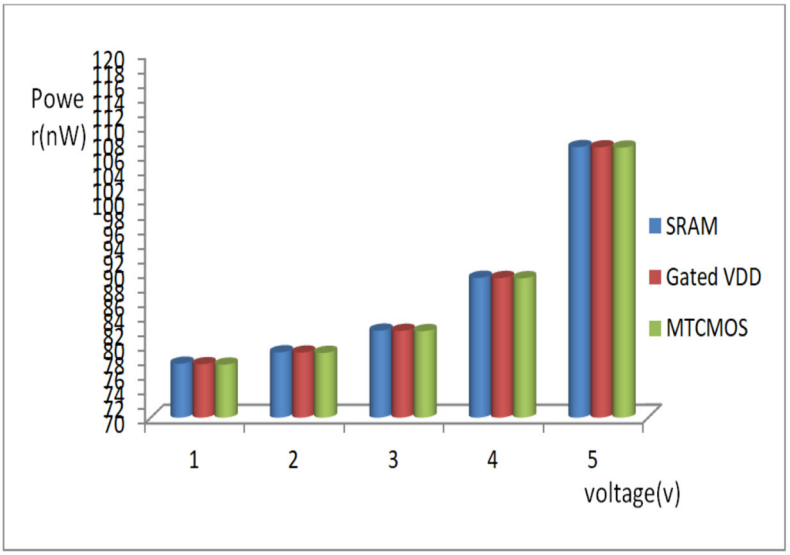

Figure 7: Comparison of Power Dissipation for Various Logics

Table 2. Delay performance of SRAM cells

Supply Voltage (V)	CMOS (ps)	Gated V_{DD} (ps)	MTCMOS (ps)
0.5	291.17	192.52	152.76
1	259.5	309.38	249.39
1.25	309.25	290.43	262.74
2.5	494	289.16	274.36
3.3	490	299.79	157.5
5	394.78	300.61	240.03

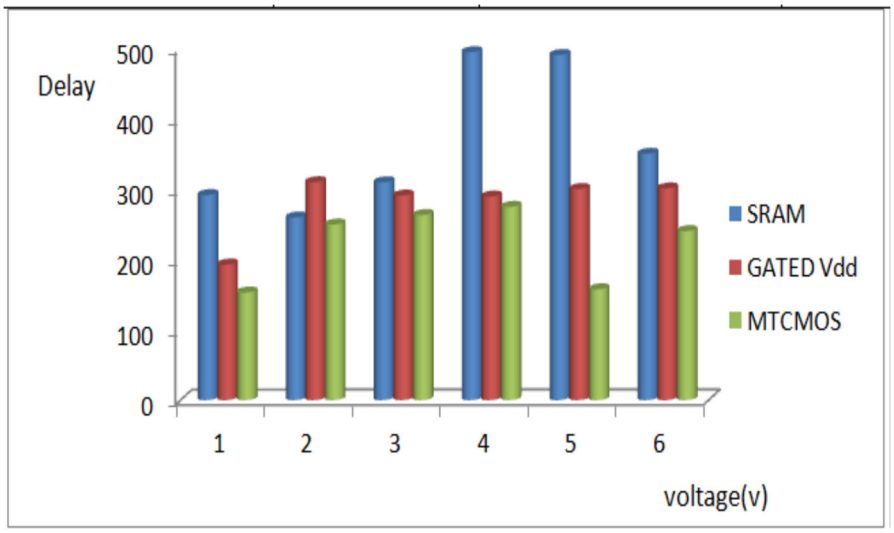

Figure 8: Comparison of Delay Report for Various Logics

5. Conclusions

Couple of power reduction techniques are analyzed for Gated V_{DD} and MTCMOS basedSRAM cell designed with 130nm technology. The SRAM cell made with the MTCMOS technique consumes less power along with the high speed in comparison to Gated V_{DD} SRAM cell and even the basic SRAM cells. Gated V_{DD} technique also reduces the power in considerable amount. Hence, we can use these techniques for the optimum performance of the SRAM cell.

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