## → Logic Gates:-

### i> Basic gates:-

- AND
- OR
- NOT

### ii> Universal gates:- It is called universal, it can used to implement basic gate.

- NAND
- NOR

### iii> Special gate:-

Ex-OR, Ex-NOR

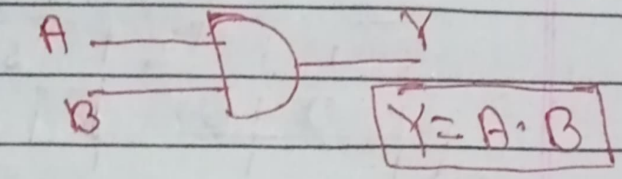
Gates have two types of input:-

| 1 | and | 0 |
|---|---|---|
| high | | low |
| True | | false |
| ON | | OFF |

Truth Table -> It shows output of gates according to different input value.

## → AND Gate:-

Symbol:-




- Truth Table:-

for 2 input:-

| $I_1$ | $I_2$ | O |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 0 | 0 | 0 |

For n input no. of combination will be $2^n$.

for 3 input:-

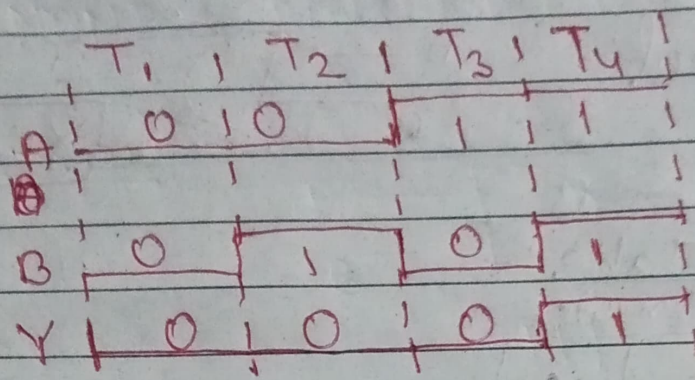
| $I_1$ | $I_2$ | $I_3$ | O |
|---|---|---|---|
| 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

T.T.

0 → low
1 → high

- Timing diagram :-

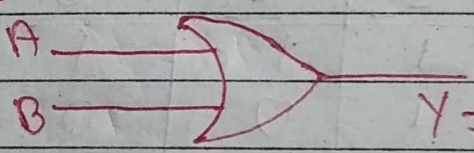



Timing diagram is based on Truth table.

FOR 2-Input AND IC-no.- 7408
3 " AND " " - 7411
4 " " " " - 7421

→ OR gate :-

Symbol :-

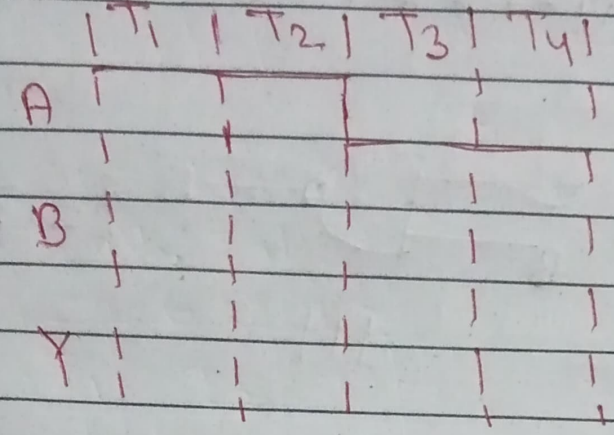



no of input can be 'n' but output must be '1'.

- Truth table :-

| A | B | Y |
|---|---|---|
| 1 | 1 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

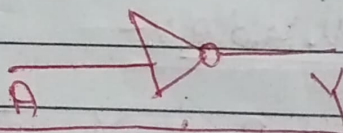
- Timing diagram:-




IC No. of 2 ~~input~~ OR - 7432

→ NOT gate :-

Symbol:-




For this gate only 1 input is possible.

- Truth Table:-

| A | Y |
|---|---|
| 1 | 0 |
| 0 | 1 |

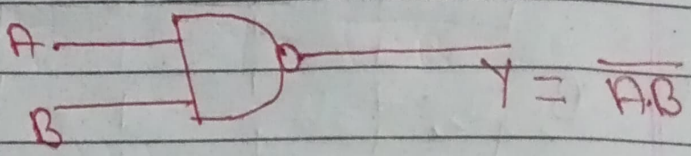
IC No of NAND Gate → 2 → 7400, 3 → 7410, 4 → 7420

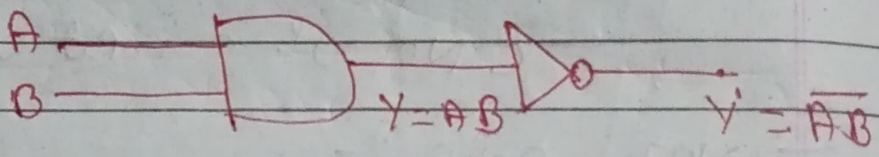


## → NAND Gate :-

NAND = ~~NOT A~~ AND + NOT

Symbol :-

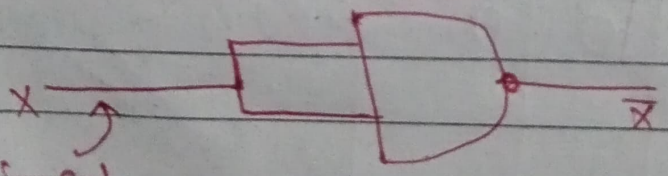



• Truth table :-

| A | B | $Y = \overline{AB}$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

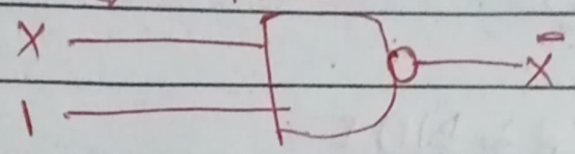
• ~~NAND~~ as inverter :-




all input combined

inverter

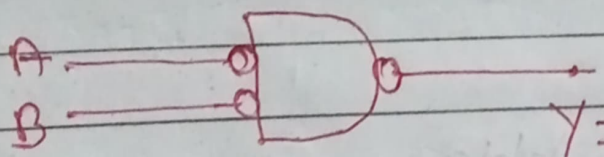
~~all input combined~~
↓ except one




controled inverter

ie. can see from ~~truth table~~ of NAND gate, if either input value in '1' result will

- bubble NAND as OR gate:-



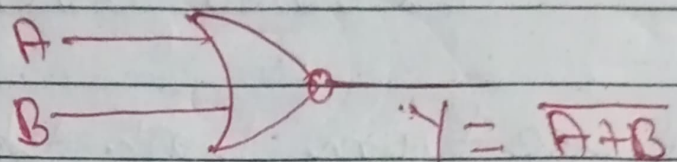

$Y = \overline{\bar{A} \cdot \bar{B}} = A + B$

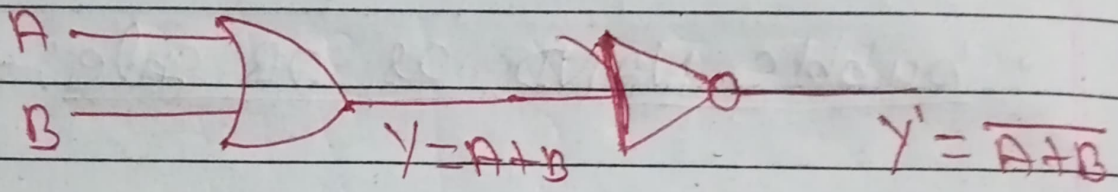
2 -> 7402
3 -> 7427
4 -> 7425



## -> NOR gate :-

NOR = OR + NOT

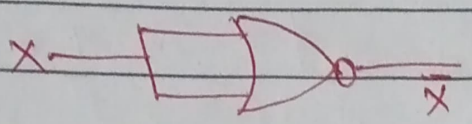


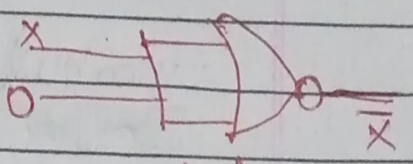

- Truth table :-

| A | B | Y |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

NOR as inverter:-



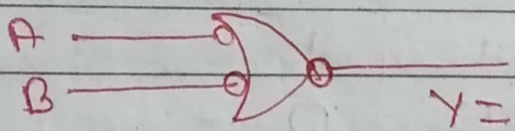

inverter




controlled inverter

~~XXXXXXXX~~

• bubble NOR gate as AND gate:-



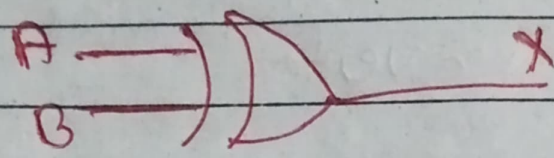

$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$

| A | B | $\overline{A}$ | $\overline{B}$ | $\overline{A} + \overline{B}$ | $\overline{\overline{A} + \overline{B}}$ | $A \cdot B$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 |

So, as we see $\overline{\overline{A} + \overline{B}} = A \cdot B$

## → X-OR :-

Symbol :-




$X = A \oplus B$

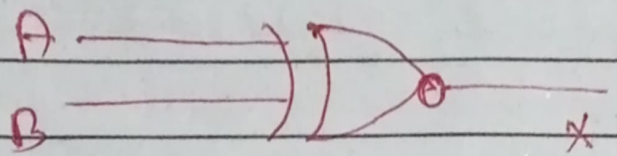
$= A\bar{B} + \bar{A}B$

• Truth table :-

| A | B | $X = A\bar{B} + \bar{A}B$ |
|---|---|---|
| 1 | 1 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 0 | 0 | 0 |

→ X-NOR

Symbol :-




$X = A \odot B$

$= \overline{A \oplus B}$

$= AB + A'B'$

• Truth table :-

| A | B | X |
|---|---|---|
| 0 | 1 | 0 |
| 0 | 0 | 1 |
| 1 | 1 | 1 |
| 1 | 0 | 0 |