Integrated ZCS Quasi-Resonant Power Factor Correction Converter Based on Flyback Topology

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***Abstract*—An integrated zero current switching (ZCS) quasiresonant converter (QRC) for the power factor correction with a single switch is presented in this paper. The power factor correction can be achieved by the discontinuous conduction mode (DCM) operation of an input current. The proposed converter offers the good power factor, low level line current harmonics, and tight output regulation. The design equations are suggested and a prototype converter has been designed based on these equations and experimentally investigated. The input current waveform of the prototype shows less than 15% of total harmonic distortion. Also, the efficiency and power factor can be obtained about 84% and 0.977, respectively, under the rated condition.**

***Index Terms*—Power factor correction, quasi-resonant converter, soft switching.**

I. Introduction

CONVENTIONAL off-line power supplies usually include the full-bridge rectifier and large input filter capacitor at their input stages. They generate highly distorted input current waveforms with large amount of harmonics. Recently, standards such as IEEE 519 and IEC 61 000 impose a limit on the harmonic current drawn by equipments connected to an ac line in order to prevent the distortion of an ac line voltage [1], [2]. Consequently, a power factor preregulator is an unavoidable choice. To meet the requirement, a number of power factor preregulators have been developed and these can be divided into two categories: the two stage approach and the single stage approach. In the two stage approach, it is customary to add a power factor corrector ahead of a dc/dc converter to provide a regulated and isolated dc output. This approach is widely used because of good characteristics of the continuous line current, small choke filter, high power factor, and fast output regulation, but the power factor preregulator increases the cost and size [3], [4]. Therefore, the two stage approach is not desirable in low power level applications. To solve this problem, many single stage topologies have been suggested to achieve both power factor correction (PFC) and power conversion from an ac line to a desired dc output. Most of them adopt the pulse-width-modulation (PWM) control method for an output regulation but they are useful when the switching frequency is lower than 100 kHz due to the heavy switching losses which affect the overall efficiency and size [5]. To overcome this disadvantage, a resonant power factor correction technique has been introduced. However, most of them have dealt with power factor preregulators with multiplier type input current controllers and only a small number of papers have suggested and analyzed DCM resonant topologies [6], [7]. Unfortunately, they suffer from the input current distortion at line zero-crossings and large output voltage ripple. In these topologies, the output voltage controller should have a low bandwidth, since an attempt to remove the 120 Hz ripple from the output voltage would degrade the input current waveform. Thus, a large output voltage ripple is not good for the tight and fast output voltage regulation and high quality input current waveform. In this paper, an integrated zero current switching (ZCS) QRC for the power factor correction based on a flyback converter is proposed. This converter offers tight and fast output regulation and does not have the input current distortion at line zero-crossings. Design equations which are obtained from a large signal model are derived for a systematic design procedure. Based on this procedure, a prototype is designed and experimented to show the advantages of the proposed converter through some comparisons with SEPIC QRC.

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II. Mode Analysis

Fig. 1 shows the circuit diagram of the proposed converter with an conventional single output voltage loop. The basic structure can be understood as a cascade connection of a boost converter followed by a flyback QRC. As shown in Fig. 2, each switching period is subdivided into six modes and their topological states are shown in Fig. 3. To illustrate the steady-state operation, the following assumptions are made.

a) The switch Q is ideal except for its internal diode.
b) The link capacitor voltage is assumed to be a constant dc voltage, V_C.
c) The output voltage is assumed to be a constant dc voltage, V_o.
d) The magnetizing inductance of the transformer is so large that it is assumed to be a constant current source.

Mode 1 ($t_o < t \leq t_1$): Mode 1 begins at t_o when the switch Q is turned on. Since the resonant inductor current, $I_{Lr}(t)$, is smaller than the magnetizing current reflected to the transformer primary, I_2/n, the rectifying diode, D_3, is still turned on and the resonant capacitor voltage, $V_{Cr}(t)$, is clamped by the output voltage, V_o. Thus, $I_{Lr}(t)$ is linearly increased and can be expressed as

$$I_{Lr}(t) = \frac{V_C + nV_o}{L_r}(t - t_o). \tag{1}$$

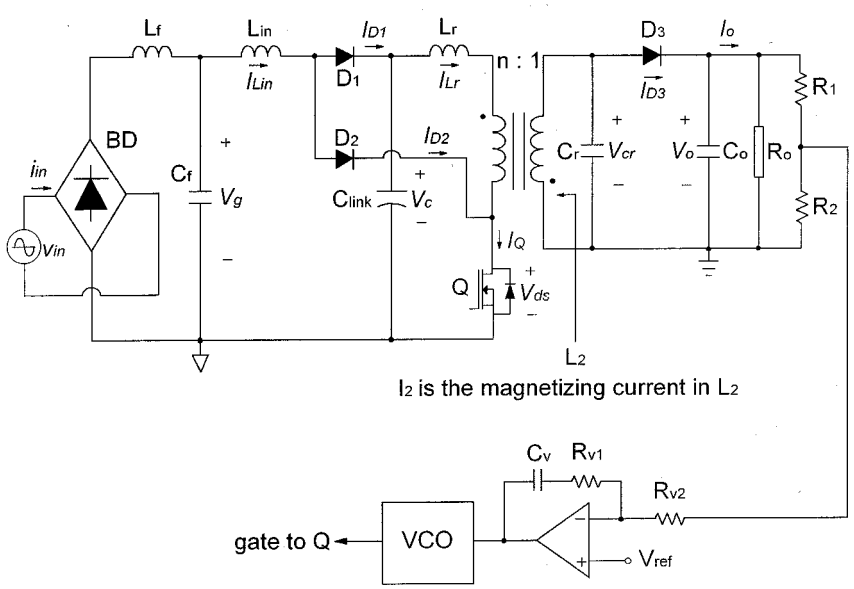


Fig. 1. Schematic of the proposed converter.

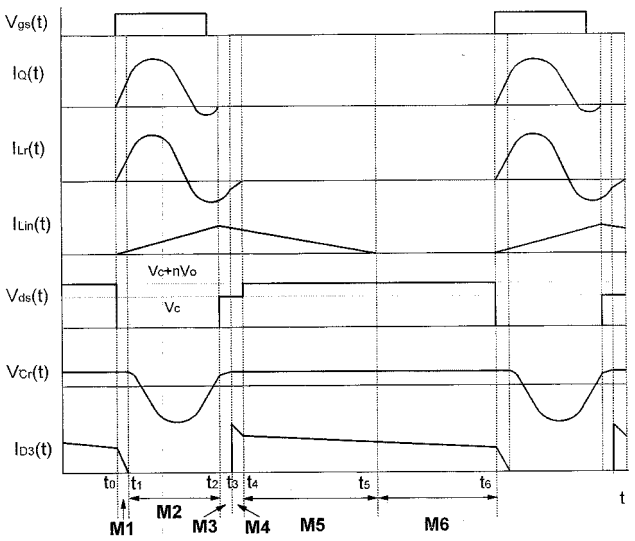


Fig. 2. Key waveforms for mode analysis.

Also the input inductor current is linearly increased with the slope of V_g/L_{in} as follows:

$$I_{L\,\text{in}}(t) = \frac{V_g}{L_{\text{in}}}(t - t_o). \tag{2}$$

This mode stops when $I_{Lr}(t)$ reaches I_2/n. The duration of this mode can be expressed as

$$T_{d1} = \frac{L_r I_2}{nV_C + n^2 V_o}. \tag{3}$$

Mode 2 $(t_1 < t \leq t_2)$: The rectifying diode, D_3, is reverse biased as the resonant capacitor discharges its energy to the resonant inductor. From the equivalent circuit (b) in Fig. 3, the voltage across the resonant capacitor, $V_{Cr}(t)$, decreases sinusoidally as

$$\frac{dV_{Cr}(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_{Lr}(t)}{C_r} \tag{4}$$

and the rate of increase of the resonant current becomes

$$\frac{dI_{Lr}(t)}{dt} = \frac{V_C}{L_r} + \frac{nV_{Cr}(t)}{L_r}. \tag{5}$$

The solutions of (4) and (5) with the initial conditions of $I_{Lr}(t_1) = I_2/n$ and $V_{Cr}(t_1) = V_o$ are as follows:

$$I_{Lr}(t) = \frac{I_2}{n} + \frac{1}{Z_r}(V_C + nV_o)\sin\omega_r(t - t_1) \tag{6}$$

$$V_{Cr}(t) = \frac{1}{n}[(V_C + nV_o)\cos\omega_r(t - t_1) - V_C] \tag{7}$$

where $Z_r = n\sqrt{L_r/C_r}$ and $\omega_r = n/\sqrt{L_r C_r}$. In this mode, $I_{L\,\text{in}}(t)$ is still increased linearly and expressed as

$$I_{L\,\text{in}}(t) = \frac{V_g}{L_{\text{in}}}(t - t_1 + T_{d1}). \tag{8}$$

The switch current will continue to oscillate and feed energy back to the link capacitor. The duration of mode 2 can be found by setting $I_Q(t_2) = I_{Lr}(t_2) + I_{L\,\text{in}}(t_2) = 0$. The approximated expression of T_{d2} is

$$T_{d2} \approx \frac{4(V_C + nV_o)/Z_r - I_2/n - T_{d1}V_g/L_{\text{in}}}{V_g/L_{\text{in}} + 2\omega_r(V_C + nV_o)/\pi Z_r}. \tag{9}$$

Mode 3 $(t_2 < t \leq t_3)$: Mode 3 begins after Q is turned off at t_2. Since the current flowing in the resonant inductor cannot change abruptly, the diode D_2 is still turned on to make the path for $I_{Lr}(t)$ and the diode D_1 also starts to conduct to transfer the energy charging in L_{in} to the link capacitor. Thus, the resonant

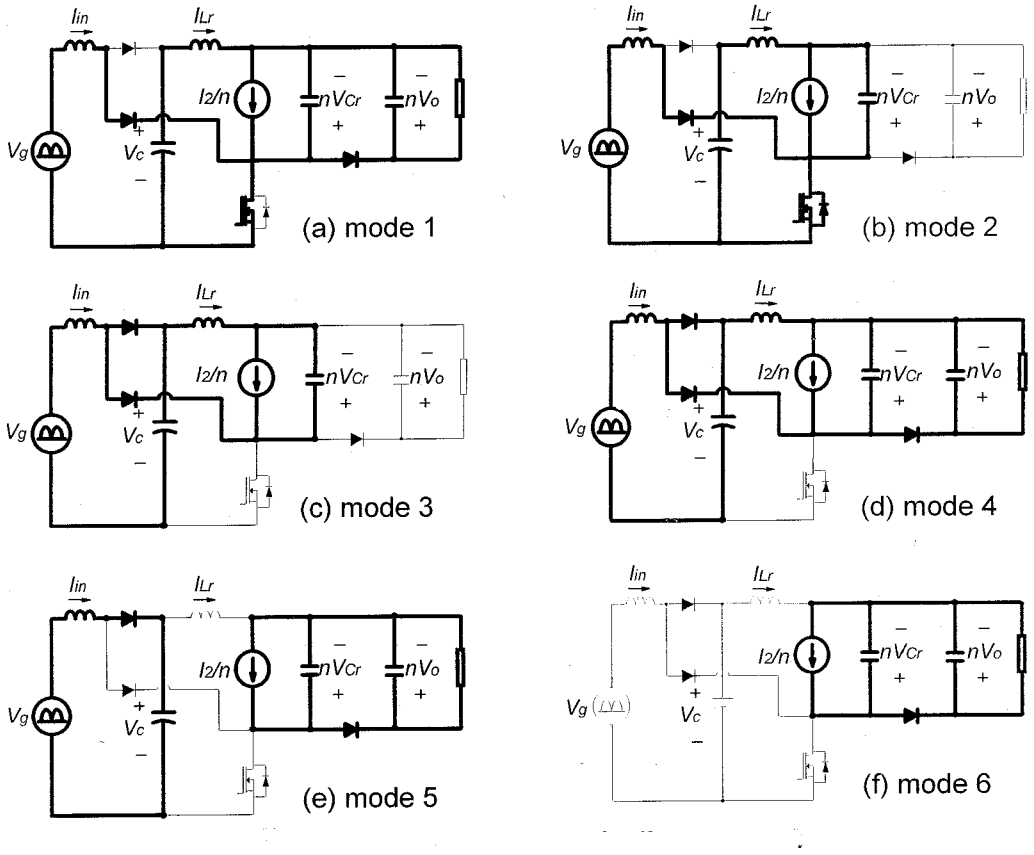


Fig. 3. Operational mode diagrams.

capacitor, C_r, is able to be charged by $I_{Lr}(t)$ and I_2/n through D_1 and D_2. Fig. 3(c) is the diagram of this mode and the differential equations can be written from this mode diagram as follows:

$$\frac{dI_{Lr}(t)}{dt} = \frac{nV_{Cr}(t)}{L_r} \tag{10}$$

$$\frac{dV_{Cr}(t)}{dt} = \frac{I_2}{C_r} - \frac{nI_{Lr}(t)}{C_r}. \tag{11}$$

Therefore, the solutions are

$$I_{Lr}(t) = \frac{V_{Cr}(t_2)}{Z_r}\sin\omega_r(t-t_2) + \left[I_{Lr}(t_2) - \frac{I_2}{n}\right]\cos\omega_r(t-t_2) + \frac{I_2}{n} \tag{12}$$

$$V_{Cr}(t) = V_{Cr}(t_2)\cos\omega_r(t-t_2) - Z_r\left[\frac{I_{Lr}(t_2)}{n} - \frac{I_2}{n^2}\right]\sin\omega_r(t-t_2) \tag{13}$$

where $V_{Cr}(t_2)$ and $I_{Lr}(t_2)$ are initial conditions of this mode, which are found from (6), (7), and (9). Since the switch Q is turned off after mode 2, $I_{L\,\mathrm{in}}(t)$ begins to be linearly decreased as follows:

$$I_{L\,\mathrm{in}}(t) = \frac{V_g - V_C}{L_{\mathrm{in}}}(t-t_2) + \frac{V_g}{L_{\mathrm{in}}}(T_{d1}+T_{d2}). \tag{14}$$

This mode stops when $V_{Cr}(t)$ is equal to V_o and the duration of this mode can be found from (13) as follows:

$$T_{d3} = \frac{1}{\omega_r}\left[\theta - \sin^{-1}\left(\frac{V_o}{\sqrt{V_{Cr}(t_2)^2 + [Z_r(I_2/n^2 - I_{Lr}(t_2)/n)]^2}}\right)\right] \tag{15}$$

where $\theta = \tan^{-1}(V_{Cr}(t_2)/(Z_r[I_2/n^2 - I_{Lr}(t_2)/n]))$.

Mode 4 ($t_3 < t \le t_4$): Since the output bulk capacitor is connected to the resonant capacitor, C_r, in parallel, $V_{Cr}(t)$ is clamped by V_o and $I_{Lr}(t)$ is linearly increased as shown in (16) and (17):

$$I_{Lr}(t) = \frac{V_o}{L_r n}(t-t_3) + I_{Lr}(t_3) \tag{16}$$

$$V_{Cr}(t) = V_o \tag{17}$$

where $I_{Lr}(t_3)$ is the initial condition of mode 3 and it can be found from (12) and (15). Since $I_{Lr}(t)$ reflected to the transformer secondary flows to the load, the powering mode is initiated. This mode stops when $I_{Lr}(t)$ reaches zero and the duration of mode 4 is

$$T_{d4} = -\frac{I_{Lr}(t_3)L_r n}{V_o}. \tag{18}$$

It is noted that until the energy hold in L_r is fully transferred to the resonant capacitor and the output bulk capacitor, both D_1 and D_2 keep conducting. Therefore, as can be seen in the mode

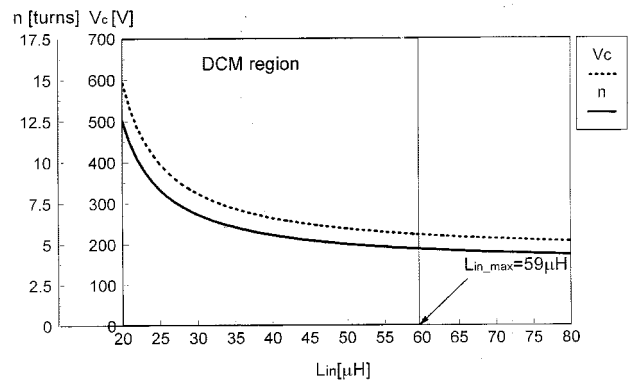


Fig. 4. Link voltage V_c and transformer turns ratio n versus $L_{\rm in}$ at $V_g = 120\ V_{\rm rms}$ and $P_o = 70$ W.

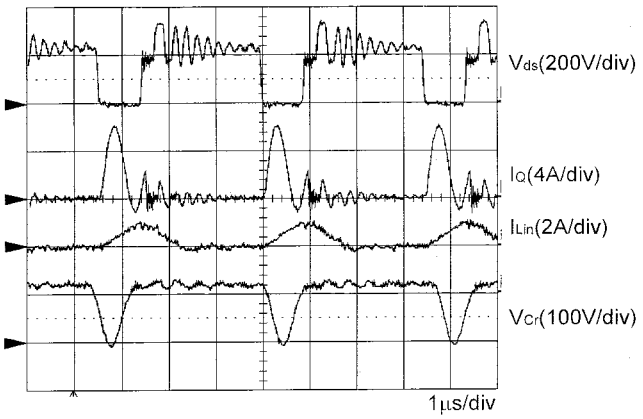


Fig. 5. Experimental waveforms of $V_{\rm ds}, I_Q, I_{L\,\rm in}$, and V_{Cr}.

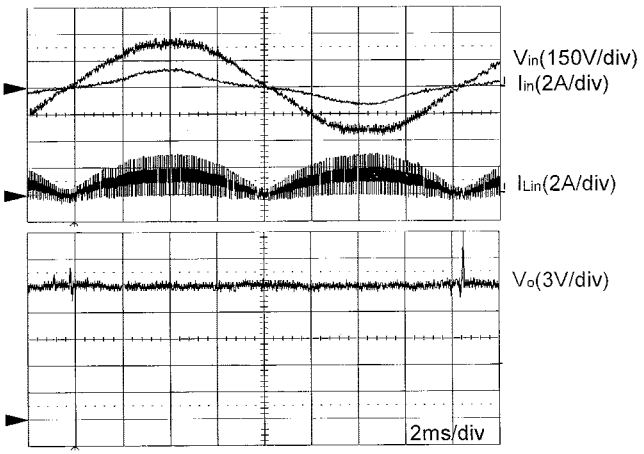


Fig. 6. Experimental waveforms of $V_{\rm in}, I_{\rm in}, I_{L\,\rm in}$, and V_o.

diagram, the drain-source voltage of the switch Q is equal to the link voltage during modes 3 and 4.

Mode 5, 6 ($t_4 < t \le t_6$): During modes 5 and 6, the input inductor current is reduced to zero and the energy charged in the transformer is transferred to the load which is the same as the conventional flyback operation. By setting (14) to zero, the duration of mode 5 is founded as

$$T_{d5} = \frac{V_g}{V_C - V_g}(T_{d1} + T_{d2}) - T_{d3} - T_{d4} \tag{19}$$

and that of mode 6 is

$$T_{d6} = T_s - \sum_{i=1}^{5} T_{di} \tag{20}$$

where T_s means a switching period.

It is noted that since almost all of the 120 Hz ripple energy of the input inductor current is absorbed by the link capacitor, a large low frequency output voltage ripple is not shown in the output voltage inherently. Furthermore, while achieving the ZCS of the switch, the proposed converter has the good characteristic of low distortion of the input current at line zero-crossings, since the input inductor current of the proposed converter does not disturbed by the resonance for ZCS of the switch and its slopes are determined only by the line and link voltages.

III. Model Equations

The design of the proposed converter begins with deriving large signal model equations. By assuming that the duration of mode 4 is negligible, the model equations can be obtained by averaging the currents and voltages over one switching cycle as follows [1]:

$$i_{L\,\rm in} = \frac{1}{R_e}\left(v_g + \frac{v_g^2}{v_c - v_g}\right) \tag{21}$$

$$\frac{dv_c}{dt} = -\frac{i_2}{nC_{\rm link}}d_f + \frac{1}{C_{\rm link}R_e}\left(\frac{v_g^2}{v_c - v_g}\right) \tag{22}$$

$$\frac{di_2}{dt} = \frac{v_c}{L_2 n}d_f - \frac{v_o}{L_2}(1 - d_f) \tag{23}$$

$$\frac{dv_o}{dt} = \frac{i_2}{C_o}(1 - d_f) - \frac{v_o}{C_o R_o} \tag{24}$$

where $R_e \equiv 2L_{\rm in}/(T_{d1} + T_{d2})^2 f_s, d_f \equiv f_s/f_r$, and f_s is the switching frequency which is the control input, and f_r is the resonant frequency.

IV. Design

A. Selection of $L_{\rm in}$ and n

To determine $L_{\rm in}$, a steady state analysis must be performed in advance. By averaging the large signal model equations given in (21)–(24) over half a line cycle, the solutions of V_C and V_o can be obtained. If the converter efficiency, η, is considered as a design parameter, these solutions become

$$V_C = \frac{V_{g\,\rm rms}}{\sqrt{2}}\left(1 + \sqrt{1 + \frac{0.852n^2\eta R_o(1 - d_{fs})^2}{L_{\rm in}d_{fs}f_r}}\right) \tag{25}$$

$$V_o = \frac{d_{fs}}{1 - d_{fs}}\frac{V_c}{n} \tag{26}$$

where d_{fs} is a steady state value of d_f. To maintain a sinusoidal input current, the input inductor current must flow in DCM. This requirement is guaranteed by the following condition as

$$\frac{\sqrt{2}V_{g\,\rm rms}}{V_C - \sqrt{2}V_{g\,\rm rms}}(T_{d1} + T_{d2})f_{\rm ss} \le 1 - (T_{d1} + T_{d2})f_{\rm ss} \tag{27}$$

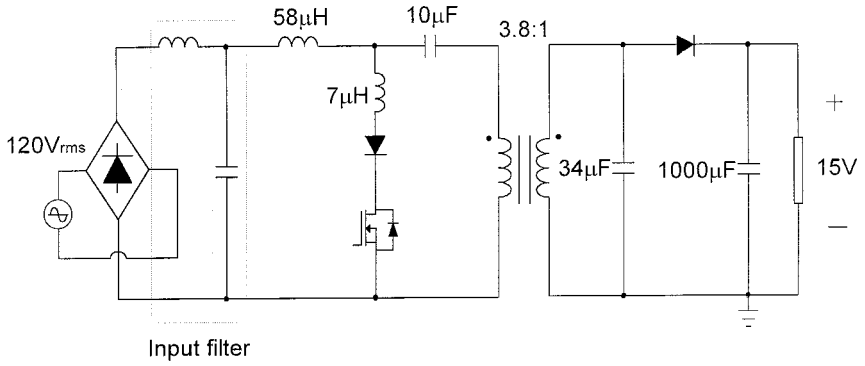


Fig. 7. Schematic of SEPIC QRC.

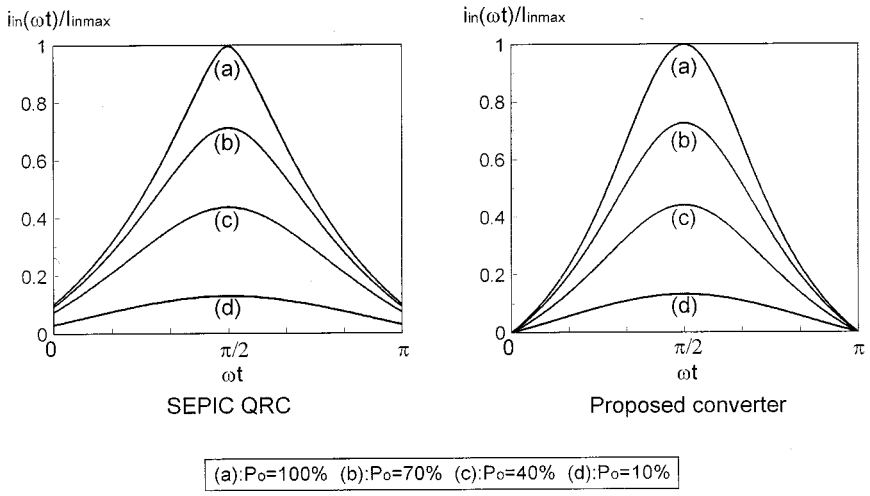


Fig. 8. Normalized input current waveforms under load variations.

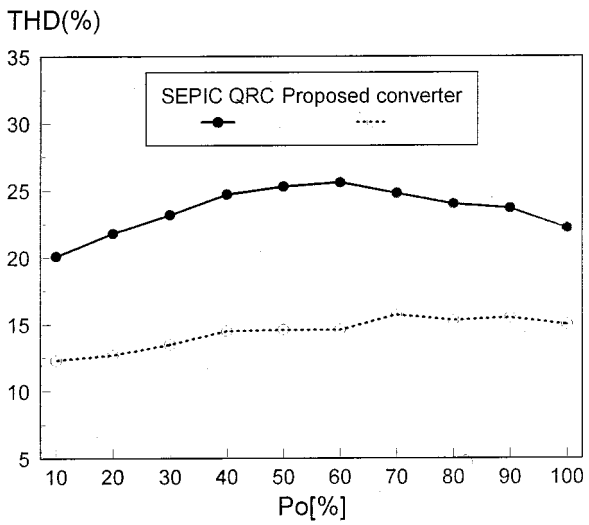


Fig. 9. Measured THD's of SEPIC QRC and the proposed converter.

where $f_{\rm ss}$ is a steady state value of f_s. Since T_{d1} and T_{d2} are also the function of the link voltage, V_C, the derivation of a design equation for $L_{\rm in}$ is difficult. However, since the relationship between $T_{d1}+T_{d2}$ and the resonant period T_r over the entire cycle is

$$T_{d1}+T_{d2}\le T_r \tag{28}$$

Equation (27) can be written as follows:

$$\frac{\sqrt{2}V_{g\,\rm rms}}{V_c-\sqrt{2}V_{g\,\rm rms}}d_{fs}\le 1-d_{fs}. \tag{29}$$

With (25), (26), and (29), the maximum *Lin* to meet DCM can be calculated as follows:

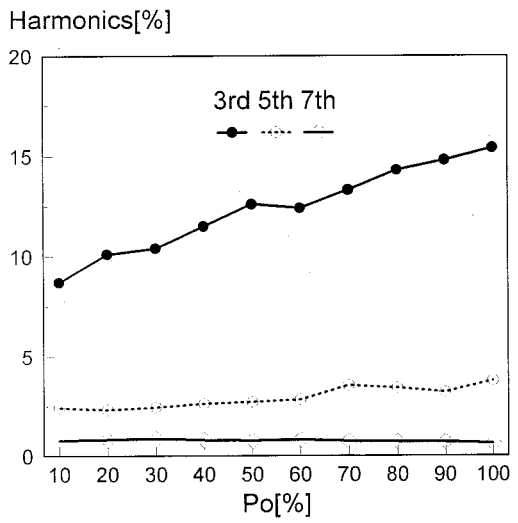
$$L_{\rm in}\le\frac{0.426d_{fs}\eta R_oV_{g\,\rm rms}^2}{f_{\rm ss}V_o^2}. \tag{30}$$

Once $L_{\rm in}$ is found using (30) and design specifications at the worst case, the transformer turns ratio, n, can be obtained using (25) and (26).

B. Selection of L_r and C_r

During mode 2, the switch current is written as

$$I_Q(t)=\frac{I_2}{n}+\frac{1}{Z_r}(V_C+nV_o)\sin\omega_r(t-t_1)+\frac{V_g}{L_{\rm in}}(t-t_1+T_{d1}). \tag{31}$$



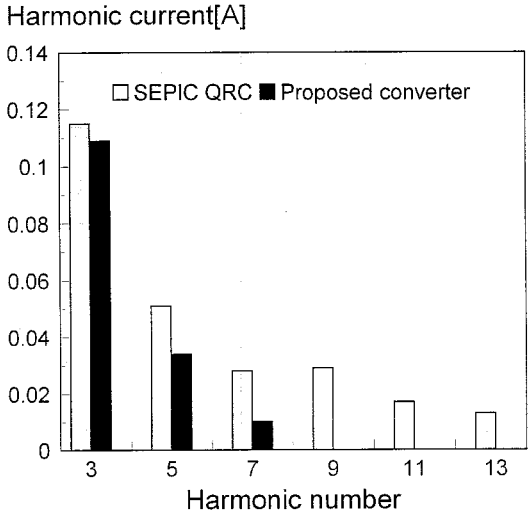


Fig. 10. Peak value of the main harmonics of the proposed converter under load variation and harmonic currents of SEPIC QRC and the proposed converter at $P_o = 70$ W.

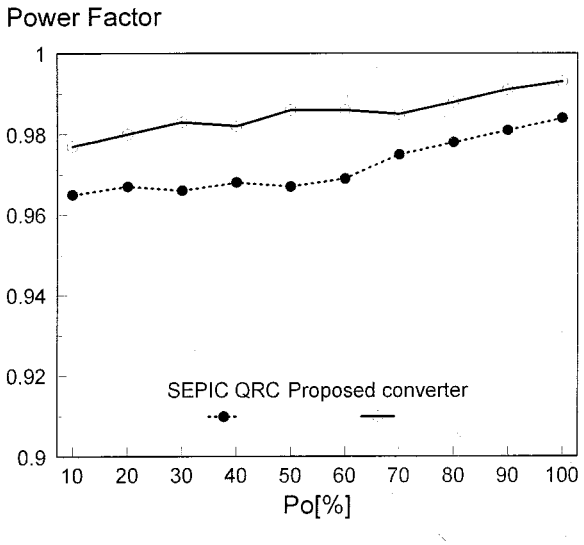


Fig. 11. Power factor of SEPIC QRC and the proposed converter.

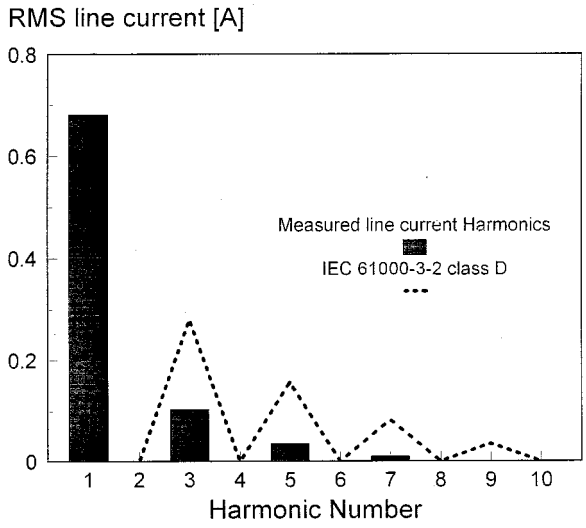


Fig. 12. Measured line current harmonics superimposed on IEC 61 000-3-2 class D limits.

In order to achieve a ZCS condition over the entire line cycle, the switch current must be zero at the end of mode 2 when the line voltage has a peak value. This can be written as follows:

$$\frac{I_2}{n} + \frac{1}{Z_r}(V_C + nV_o)\sin\zeta + \frac{\sqrt{2}V_{g\,\mathrm{rms}}}{L_{\mathrm{in}}}\left(\frac{\zeta}{\omega_r} + T_{d1}\right) = 0 \tag{32}$$

where ζ is defined as $\omega_r T_{d2}$. This condition may be satisfied when ζ has a value between π and 2π. Furthermore, due to the heavy current stress on the switch which is the general characteristic of a ZCS QRC, it is necessary to select a suitable value such that the current stress can be minimized. As can be seen in (31), a minimum current stress can be accomplished when the characteristic impedance, Z_r, satisfying a given resonant frequency is selected as large as possible. If (32) is rearranged to find ζ minimizing the current stress, it becomes as follows:

$$Z_r = -\frac{(V_C + nV_o)\sin\zeta}{\frac{I_2}{n} + \frac{\sqrt{2}V_{g\,\mathrm{rms}}}{L_{\mathrm{in}}}\left(\frac{\zeta}{\omega_r} + T_{d1}\right)}. \tag{33}$$

To find out ζ maximizing Z_r, (33) is differentiated with respect to ζ and it becomes

$$\frac{dZ_r}{d\zeta} = \frac{-M(\zeta)(V_C + nV_o)\cos\zeta + \frac{\sqrt{2}V_{g\,\mathrm{rms}}}{\omega_r L_{\mathrm{in}}}(V_C + nV_o)\sin\zeta}{M(\zeta)^2} = 0 \tag{34}$$

where $M(\zeta) = (I_2/n) + (\sqrt{2}V_{g\,\mathrm{rms}}/L_{\mathrm{in}})((\zeta/\omega_r) + T_{d2})$. Since ζ should have a value larger than, $M(\zeta)$ is much larger than

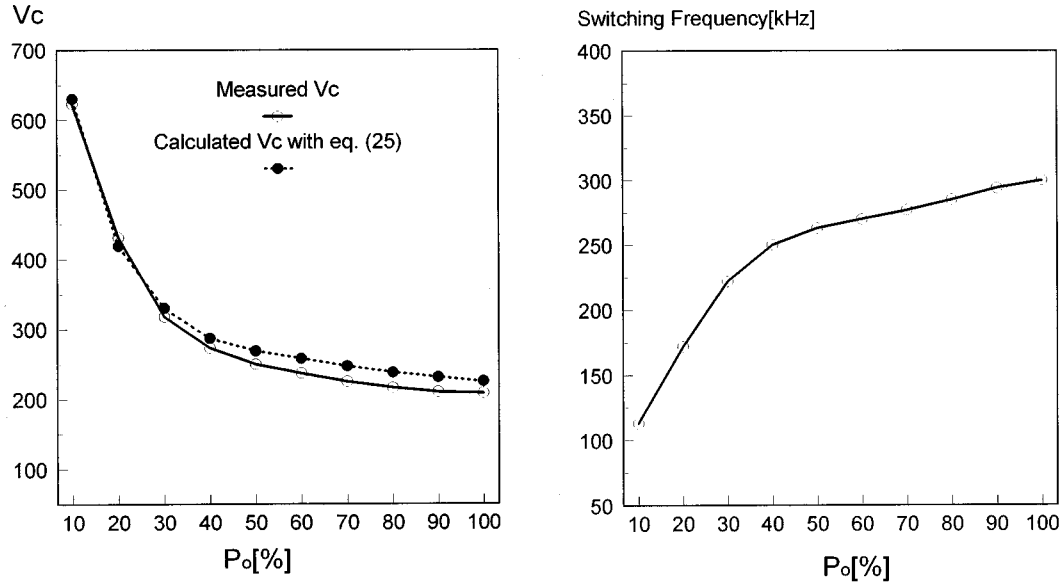


Fig. 13. Link voltage V_C and switching frequency variations under load variation at $V_g = 120\ \mathrm{V_{rms}}$.

$\sqrt{2}V_{g\,\mathrm{rms}}/(\omega_r L_{\mathrm{in}})$. Thus (34) can be approximately rewritten as

$$M(\zeta)(V_C + nV_o)\cos\zeta \approx 0. \tag{35}$$

From (35), ζ minimizing the current stress can be chosen as $3\pi/2$, which is the similar condition as the conventional QRC circuit. Thus (32) becomes

$$\frac{I_2}{n} - \frac{1}{Z_r}(V_C + nV_o) + \frac{\sqrt{2}V_{g\,\mathrm{rms}}}{L_{\mathrm{in}}}\left(\frac{\zeta}{\omega_r} + T_{d1}\right) = 0. \tag{36}$$

Therefore, L_r and C_r are determined using (3), (25), (36), and a desired resonant frequency ω_r.

C. Selection of Switch

The voltage stress on the switch can be expressed as follows:

$$V_{\mathrm{ds}} = V_C + nV_o. \tag{37}$$

The worst case of voltage stress happens at a light load. Thus, the maximum voltage stress can be found using (25) and (37) with $R_o = R_{o,\max}$ and $f_{\mathrm{ss}} = f_{s,\min}$. Also, the worst case of current stress happens at a full load and peak line voltage. The peak current stress can be expressed as

$$I_{Q,pk} = \frac{\sqrt{2}V_{g\,\mathrm{rms}}}{L_{\mathrm{in}}}\left(\frac{\pi}{2\omega_r} + T_{d1}\right) + \frac{I_2}{n} + \frac{1}{Z_r}(V_C + nV_o). \tag{38}$$

V. Power Stage Design Example

The prototype converter has been implemented to show the operation of the proposed converter based on the design equations with the following specifications.

1) Line voltage, $V_g = 120\ \mathrm{V_{rms}}$.
2) Output voltage, $V_o = 15$ V.
3) Output power, $P_o = 7$ W–70 W.
4) Resonant frequency, $f_r = 1.25$ MHz.
5) Maximum switching frequency, $f_{s,\max} = 300$ kHz
6) Desired efficiency, $\eta = 85\%$.

Fig. 4 shows the link capacitor voltage, V_C, and transformer turns ratio, n, as a function of the input inductor using (25) and (26). From (30), the maximum input inductor, L_{in}, to meet DCM is calculated as 59 μH. In this prototype, 58 μH is used for L_{in} and $n = 4.7$ is obtained based on this value. With the designed values of L_{in} and n, C_r and L_r are selected as 40 nF and 9 μH, respectively, using (3), (25), (36), and the resonant frequency given in the design specifications. From (37) and (38), APT8056BVR has be chosen as main switch, which has $\mathrm{BV}_{DSS} = 800$ V and $I_{D(\mathrm{on})} = 16$ A.

VI. Experimental Results

Fig. 5 shows key waveforms of the proposed converter. It can be seen that the switching waveforms are well agreed with the theoretical analysis except the ringing of V_{ds} which comes from the resonance of the output capacitance of the switch and the inductances connected in series during the off-state of the switch. In addition, Fig. 6 shows that the filtered input current follows the line voltage without any distortion at line zero-crossings and the output voltage is tightly regulated. To show the advantages of the proposed converter, some comparisons are made with SEPIC QRC. Fig. 8 shows the normalized input current waveforms of SEPIC QRC in Fig. 7 and the proposed converter as a function of load for one half-cycle. This figure shows that the line current of the proposed converter does not have an offset at the line zero-crossing and it is closer to the sinusoidal waveform than the line current of SEPIC QRC. Figs. 9 and 10 show that the line current of the proposed converter contains smaller harmonic currens the SEPIC QRC. Due to the lower THD of the proposed converter compared with that of SEPIC QRC, the power factor of the proposed converter stays more higher as shown in Fig. 11. Fig. 12 is the plot of the measured line current harmonics superimposed on IEC 61 000-3-2 class D. As can be seen in this figure, the proposed converter meets the limits with sufficient margin. The link voltage and switching

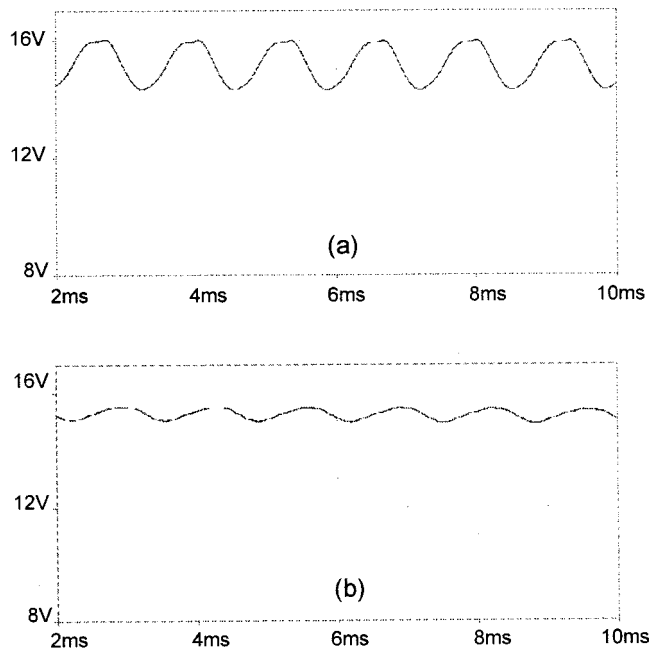


Fig. 14. Open loop oputput voltage waveforms of (a) SEPIC QRC and (b) proposed converter.

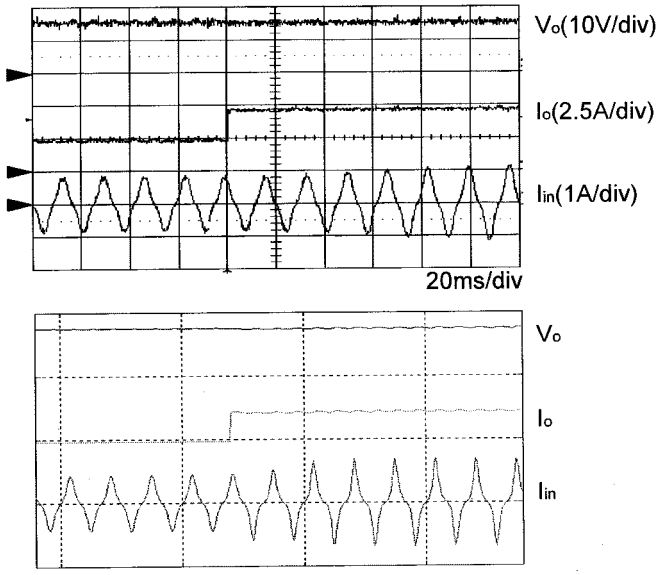


Fig. 15. Experimental waveforms of dynamic response and their simulations from full load to half load using (21)–(24).

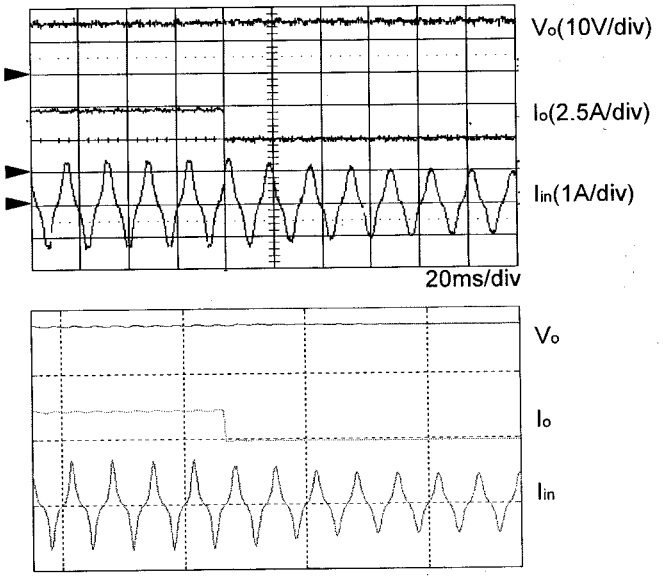


Fig. 16. Experimental waveforms of dynamic response and their simulations from half load to full load using (21)–(24).

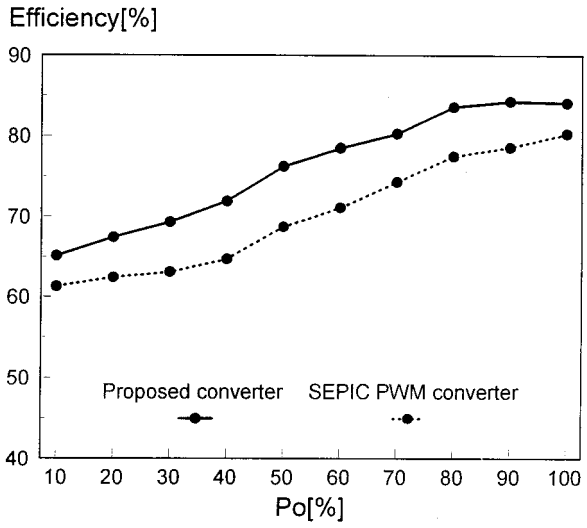


Fig. 17. Efficiency comparisons between the proposed converter and hard-switching SEPIC PFC PWM converter operating in DCM with 100 kHz switching frequency.

frequency changes under load variations are depicted in Fig. 13. It shows that the link voltage stress becomes higher as load becomes lighter, which is the general characteristic of DCM PFC converters. The open loop simulations of the output voltage using the PSPICE are shown in Fig. 14. The output voltage of SEPIC QRC is affected by 120 Hz ripple energy of the input inductor since the DCM current flowing in the input inductor is directly transferred to the output when the switch is turned off. Thus the output voltage ripple of SEPIC QRC is much larger than that of the proposed converter. This may result in a distortion of an input current waveform in the case that the controller has a high bandwidth for tight and fast output regulation. Therefore, a large output voltage ripple is not desirable characteristic in single-stage DCM PFC converters, especially at low output voltage applications. Figs. 15 and 16 show the experimental waveforms of dynamic response and their simulations using (21)–(24) to verify the large signal model equations. A simple PI controller with $P_{\rm gain}$ of 1.5 and $I_{\rm gain}$ of 50 has been designed using UC3860 from Unitrode Corporation. The simulation waveforms are similar to the experimental results and it can be said that the proposed converters can be well described by the model equations. The efficiency comparison between the

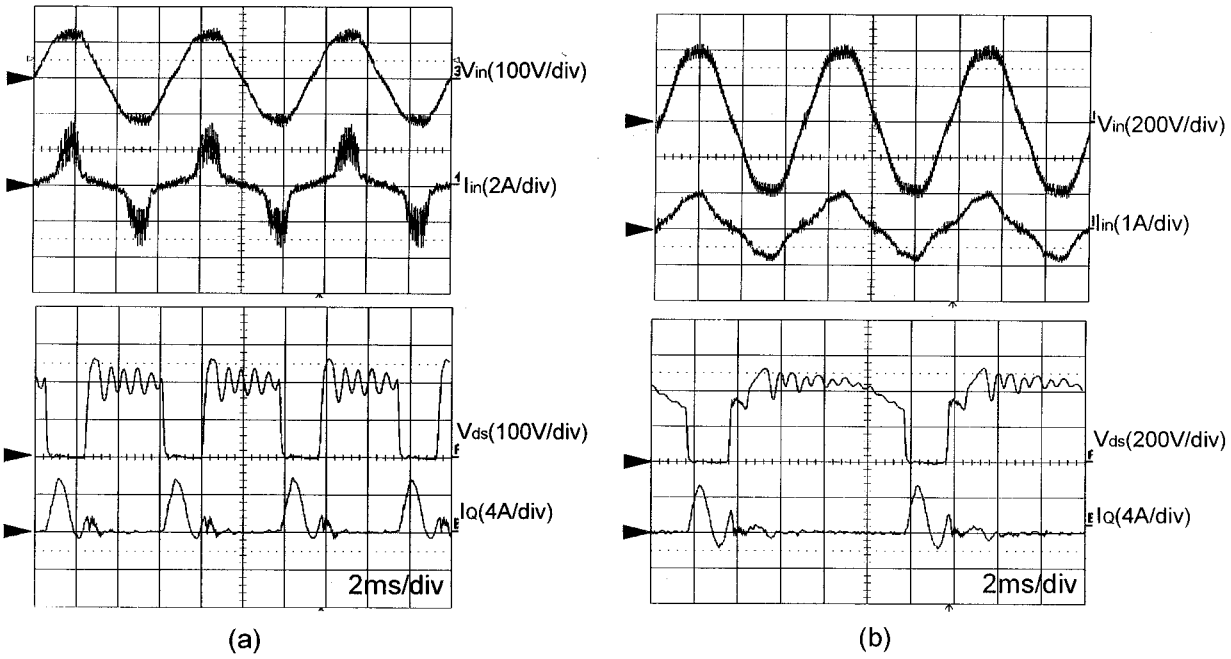


Fig. 18. Experimental waveforms $V_{\rm in}, I_{\rm in}, V_{\rm ds}$, and I_Q at (a) $V_g = 90\ \mathrm{V_{rms}}$ and (b) $V_g = 264\ \mathrm{V_{rms}}$ with $L_{\rm in} = 132\ \mu$H.

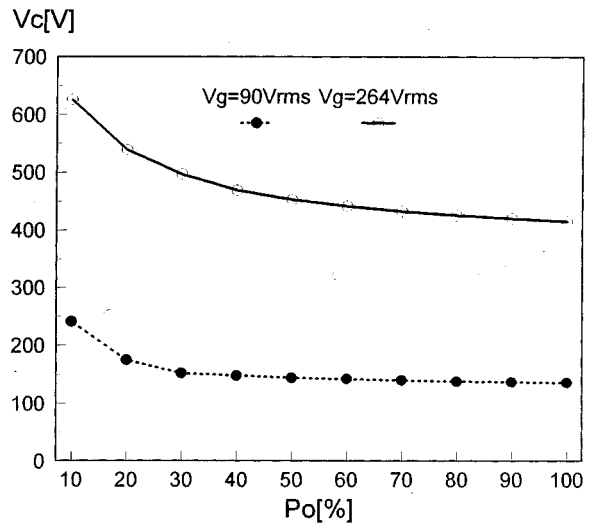


Fig. 19. Measured link voltage stress under load variations.

proposed converter and hard-switching SEPIC PFC PWM converter operating in DCM with 100 kHz switching frequency is shown in Fig. 17. This figure shows that the measured efficiency is about 84% at the rated condition and it has higher efficiency than that of hard-switching SEPIC converter. Recently, single-stage converters are required to operated in the universal input voltage from 90 $\mathrm{V_{rms}}$ to 264 $\mathrm{V_{rms}}$. To meet this requirement, it is necessary to reduce the link voltage stress, which is a function of $L_{\rm in}$ as shown in (25). It is noted that the link voltage stress can be reduced to an acceptable range by increasing $L_{\rm in}$, while the input current still meets the harmonic regulation. By using $L_{\rm in} = 132\ \mu$H, the prototype converter can be operated in the universal input voltage. The experimental waveforms are shown in Figs. 18 and 19 is the plot of the measured link voltage under load variations.

VII. Conclusion

This paper has presented the analysis and experimental results of an integrated boost-flyback QRC for PFC operating in DCM. By eliminating the distortion of the input current waveform at line zero-crossings, THD and power factor can be improved. Furthermore, the proposed converter is capable of producing the desired output voltage without a significant output voltage ripple. This is the desirable characteristic since a high bandwidth output voltage controller can be used for the tight and fast output regulation without degrading the input current waveform. To design a prototype converter in a more systematic way, the modeling is performed and design equations are derived using model equations which are verified through experiments. The measured power factor is above 0.977 and a high efficiency of 84% can be obtained under the rated condition. In addition, the feasible study on the operation in universal input voltage has been suggested. Therefore, the proposed converter is expected to be suitable for a compact power supply with tight output regulation and a switching frequency of more than several hundreds kHz.

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