CSE-3103: Microprocessor and Microcontroller

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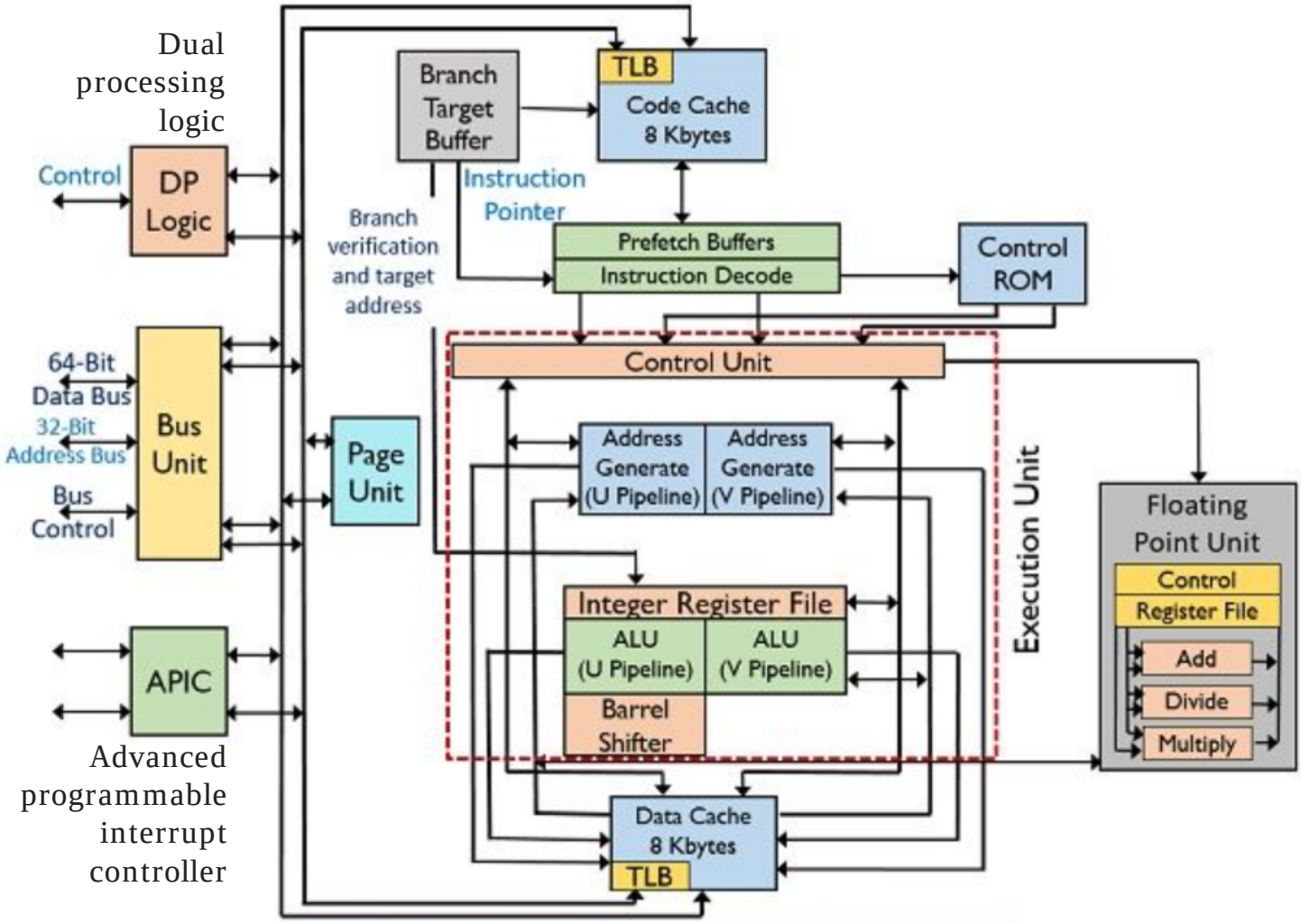
Intel Pentium Microprocessors

Improvement to architecture in 80486 →

- improved cache structure →
  - 2 caches, each 8K bytes in size,
  - one for caching data,
  - other for instructions.
- wider data bus width →
  - increased from 32 bits to 64 bits.
- faster numeric coprocessor →
  - operates at 5 times faster than 80486 numeric coprocessor.
- dual integer processor →
  - allows 2 instructions per clock cycle.
  - = instruction-level parallelism (superscalar processors).
- branch prediction logic.
- addition of MMX instructions.

pipelining =
single execution unit,
multiple phases to execute multiple instructions.

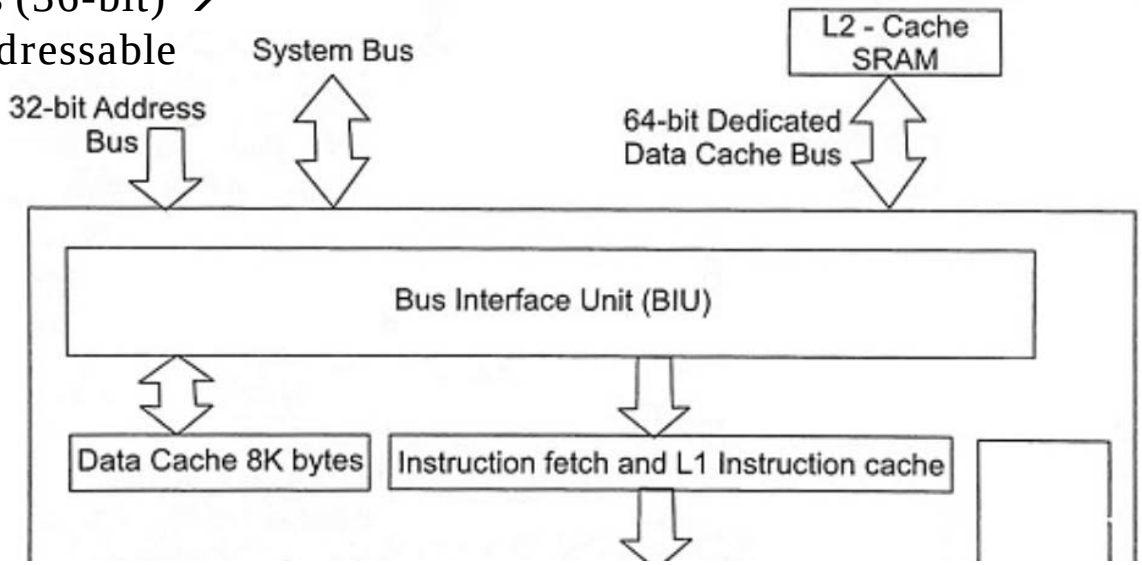
Intel Pentium Microprocessors



Intel Pentium Microprocessors

Pentium Pro →

faster version of Pentium (14-stage superpipelined architecture).
can schedule up to 5 instructions for execution,
faster floating point unit.
contains 256K byte or 512K byte level 2 cache.
includes error correction circuitry (ECC) →
corrects one-bit error,
indicates two-bit error.
added 4 additional address lines (36-bit) →
64G bytes of directly addressable memory space.



Intel Pentium Microprocessors

Memory system →

4G bytes in size.

numbered from byte 00000000H to byte FFFFFFFFH.

separate memory banks →

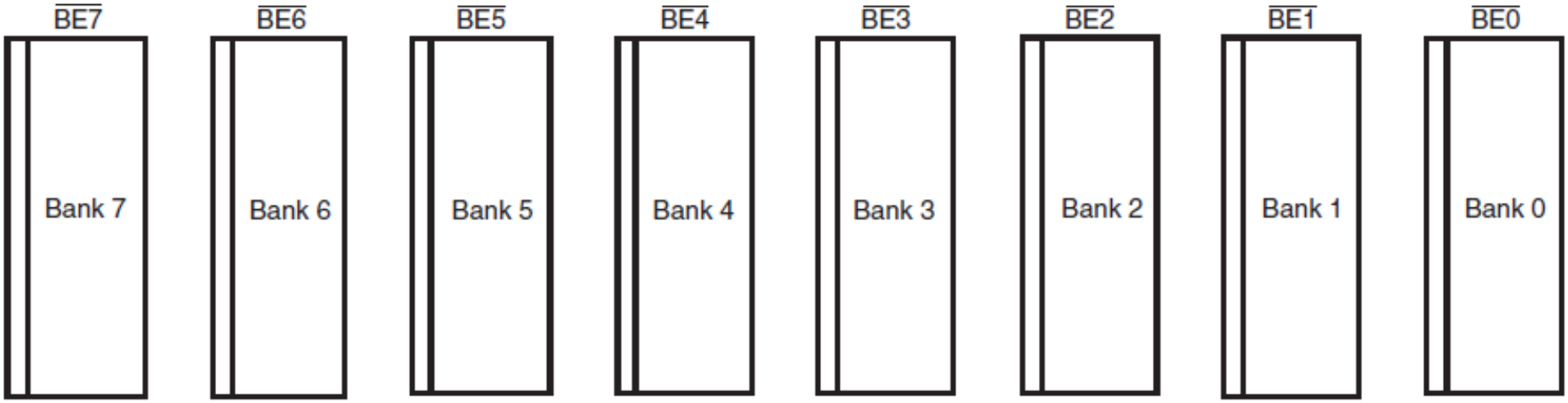
organized in 8 banks,

each bank contains 512M bytes of data. ($2^{29} \times 2^{3}$)

each bank stores byte-wide data with a parity bit.

can access single byte, word, doubleword, or quadword,

with one memory transfer cycle.



Intel Pentium Microprocessors

Memory system →

64-bit data bus,
can retrieve double-precision floating-point data with one read cycle.

address parity error →

employs internal parity generation and checking logic.
capable to check and generate parity for (A_{31}–A_5).
indicates bad parity check for address bus.
takes no action when address parity error is detected.
error is assessed by system and initiate interrupt.

Input/output system →

compatible with earlier Intel microprocessors.
I/O port number appears on A15–A3 (2^{13} = 8 KB).
I/O privilege information is added to TSS (task state segment) →

allows I/O ports to be selectively inhibited.

blocked I/O location is accessed →

generates type 13 interrupt,
signal I/O privilege violation.

Intel Pentium Microprocessors

Branch Prediction Logic →

reduces time required for branch caused by internal delays.

branch instruction is encountered →

microprocessor begins prefetch instruction at branch address.

instructions are loaded into instruction cache,

branch occurs →

instructions are present,

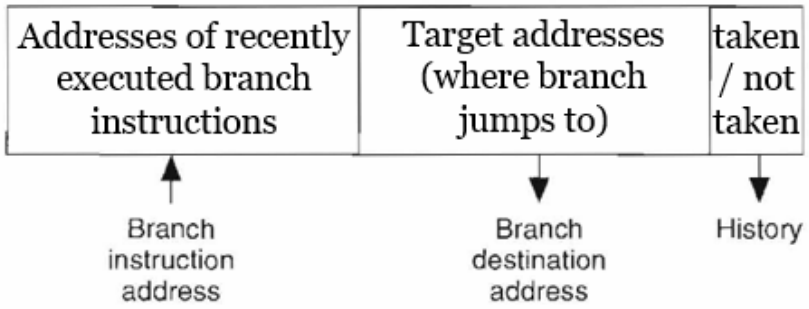
branch executes in one clocking period.

branch prediction logic errors →

requires extra 3 clocking periods to execute.

branch target buffer →

augments instruction cache for dynamic branch prediction.



Intel Pentium Microprocessors

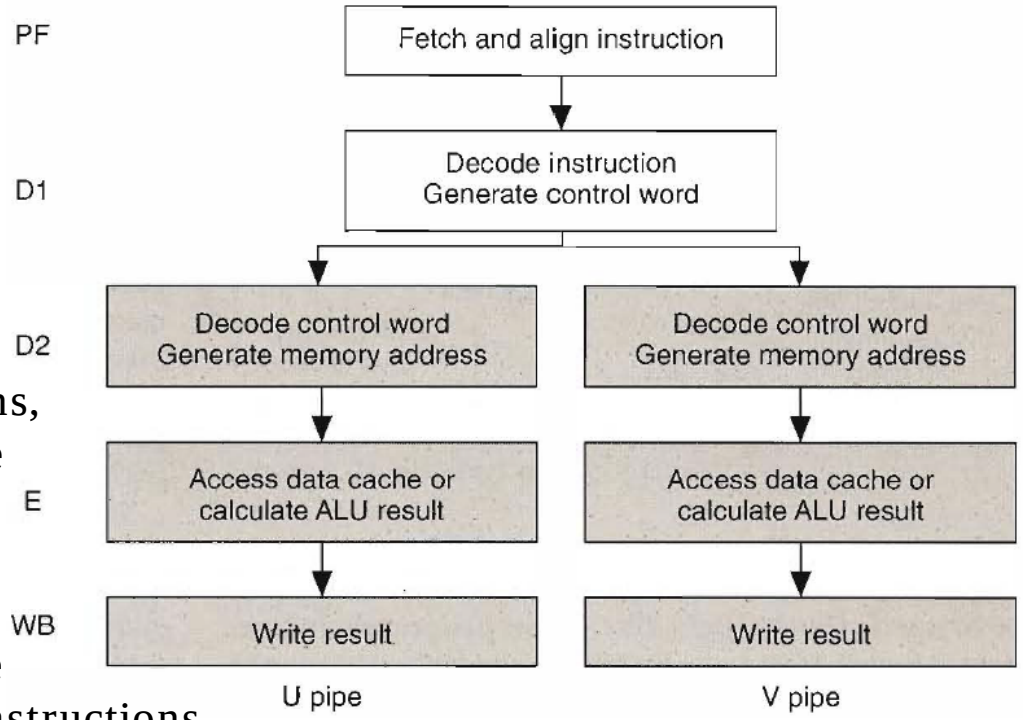
Cache Structure →

contains two 8K byte cache memories.
one 8K byte data cache,
another 8K byte instruction cache.

Superscalar Architecture →

organized with 3 execution units.
one executes floating-point instructions,
other two (U-pipe and V-pipe) execute integer instructions.
= superscalar feature.
software should be written →

dependent instructions can be separated by nondependent instructions.
result in up to 40% execution speed improvement.



Paging Unit

Paging Unit →

paging mechanism functions with →

1) 4K byte memory pages →

translation = page directory (10 bit) + page table (10) + offset (12).

2) 4M byte memory pages →

new extension available to Pentium.

translation = page directory (10) + offset (22).

new 4M byte paging feature →

single page directory,

no page table entry in linear address.

page sizes are selected by PSE (page size extension) bit in CR0 or CR4.

leftmost 10 bits (22–31) of linear address select entry in page directory.

example →

linear address 00200001H

repaged to memory location 01000001H.

Paging Unit

Paging Unit →

new 4M byte paging feature →