CSE-3103: Microprocessor and Microcontroller

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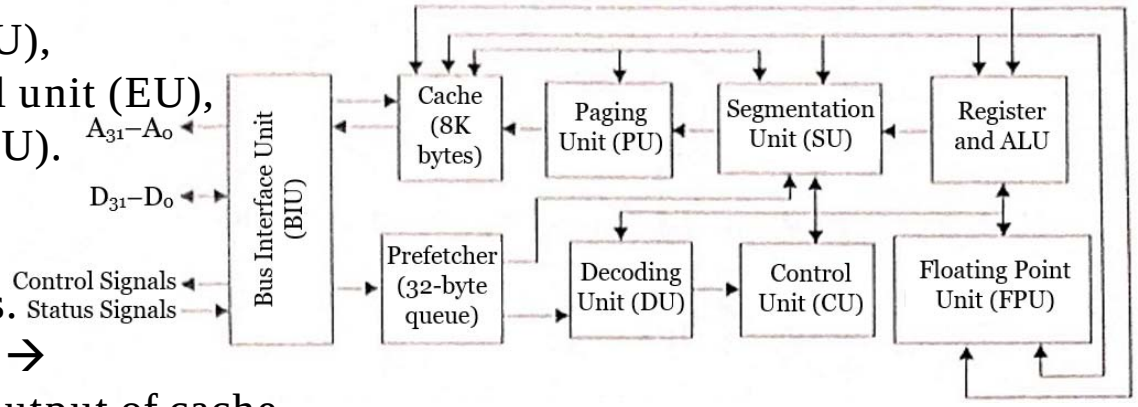
Intel 80486 Microprocessors

Architecture →

32-bit processor.

3 different sections →

1) Bus interface unit (BIU),
2) Execution and control unit (EU),
3) Floating-point unit (FU).



Bus Interface Unit (BIU) →

used to organize all bus activities.

address driver is connected with →

internal 32-bit address output of cache,
32-bit system bus.

data bus transreceivers are interconnected between →

internal 32-bit data bus and system bus.

write data buffer = queue of four 80-bit registers.

data = 32 bits
address = 32 bits
control = 16 bits

Parity generation and control unit →

generates parity,
carries out checking during processor operation.

Intel 80486 Microprocessors

Architecture →

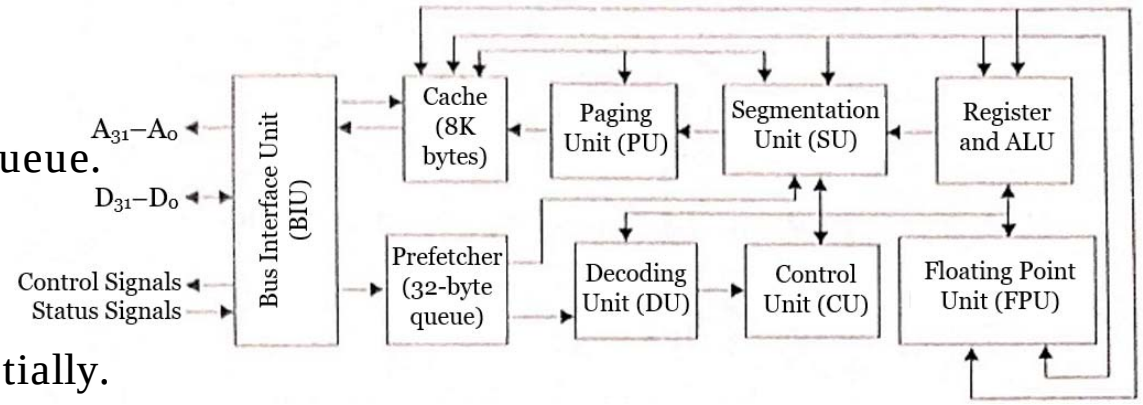
Boundary scan control unit →

checks motherboard connections,
detects hardware faults.

boundary scan tests operation,
ensures correct operation of all components of circuit on motherboard.

Prefetcher unit →

fetches codes from memory,
arranges them in 32-byte code queue.



Instruction decoder →

receive code from code queue,
decodes instruction code sequentially.
decoder output is fed to control unit.
CU derives control signals.

Protection unit →

check all protection norms before execution.
any violation = appropriate exception is generated.

Page Fault
General Protection Fault
Segment Not Present
Stack Fault
Invalid Opcode

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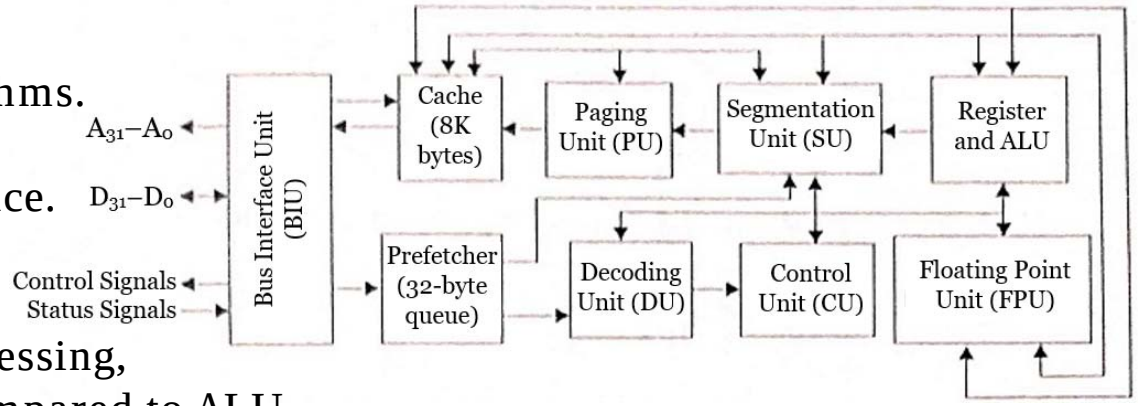
Architecture →

Control ROM →

stores microprogram.

Barrel shifter →

performs shift and rotate algorithms.
uses multiple parallel paths,
allowing shifts up to 31 bits at once.



Floating-point unit (FPU) →

used for mathematical data processing,
processing speed is very high compared to ALU.
FPU communicates with BIU under control of
memory management unit (MMU),
64-bit internal data bus.

microcode = set of low-level control signals:
internal CPU operations
data movement between registers
activate ALU, shifter, FPU, memory interface
implement complex instructions

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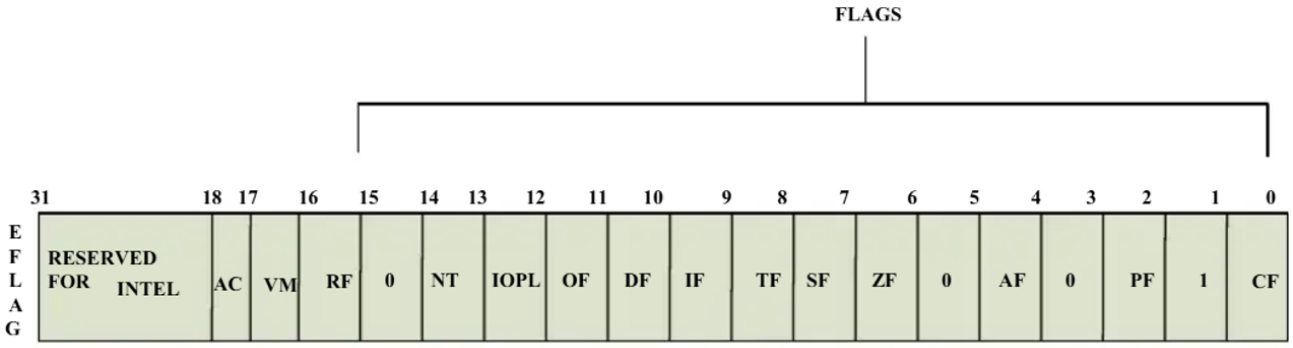
Architecture →

Register bank →

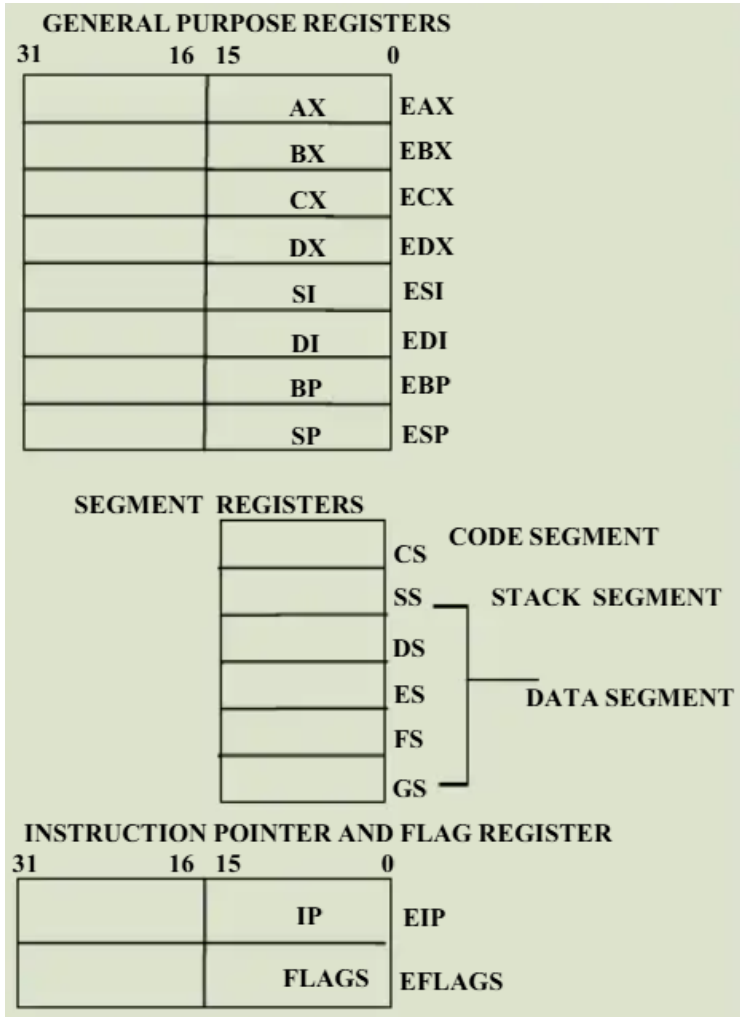
used for their usual operation.



CF: Carry Flag
AF: Auxiliary carry
ZF: Zero Flag
SF : Sign Flag
TF : Trap Flag
IE : Interrupt Enable
AC : Alignment Check
DF : Direct Flag

OF : Over Flow
IOPL : I/O Privilege Level
NT : Nested Task Flag
RF : Resume Flag
VM : Virtual Mode

FS/GS points to:
process control block
exception handlers
system tables
kernel memory.



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Register bank (EFLAGS) →

AC = Alignment Check Flag →

enables alignment checking for memory accesses.
detecting memory access bugs in protected-mode programs.

IOPL = I/O Privilege Level →

controls access level for I/O instructions.
restricting user programs from accessing hardware ports.

NT = Nested Task Flag →

set by hardware when one task invokes another task.

RF = Resume Flag →

prevents debugger from re-triggering breakpoint.
RF = 1, CPU ignores next instruction breakpoint.

VM = Virtual 8086 Mode →

enables virtual 8086 mode inside protected mode.
running DOS programs inside Windows/Linux protected-mode systems.

Intel 80486 Microprocessors

Features →

1st processor with in-built 80387 floating-point unit.
complete 32-bit architecture,
support 8-bit, 16-bit, 32-bit data types.
have 8 KB unified level 1 cache for code and data.
packaged in 168-pin grid array package.
versions = 25 MHz, 33 MHz, 50 MHz, 100 MHz.
data exists in cache →
load, store, arithmetic instructions are executed in one cycle.
operates at much faster bus transfers.

retains all complex instruction sets of 80386,
5-stage pipelining has been introduced →
IF → ID1 → ID2 → EX → WB
2 out of 5 stages are used for decoding complex instructions,
other 3 stages are used for execution.

Intel 80486 Microprocessors

Features →

advanced i486 processors →

clock-doubling and clock-tripling technology has been incorporated.
operate in existing motherboards with 20-33 MHz bus frequency.

Memory System →

addresses 4 GB of memory through →

32-bit address bus.

virtual addressing →

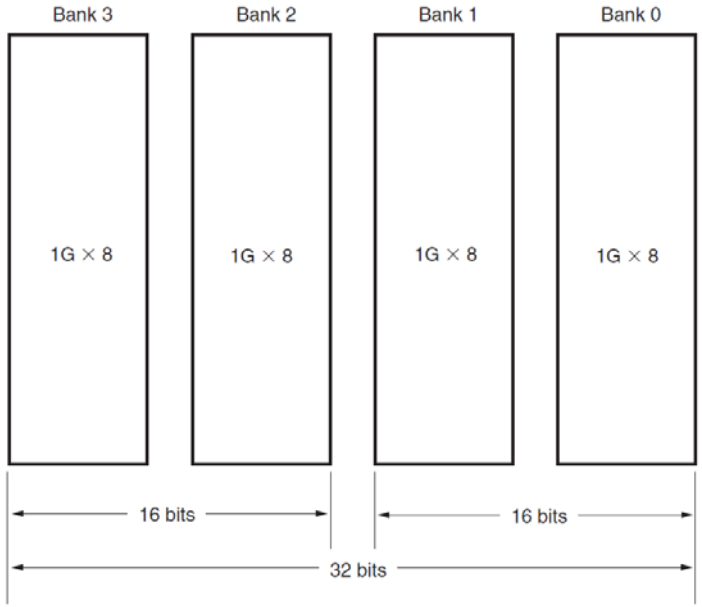
64 TB are mapped into 4 GB of physical space,
by MMU and descriptors.

memory = four 8-bit wide memory banks,

each containing up to 1 GB of memory.
each banks are accessed via
4 byte enable signals (BE0, BE1, BE2, BE3).

32-bit-wide memory organization →

bytes, words, doublewords of memory data
to be accessed directly.



46-bit virtual/linear addresses → 64 TB virtual space,
uses segmentation + paging.

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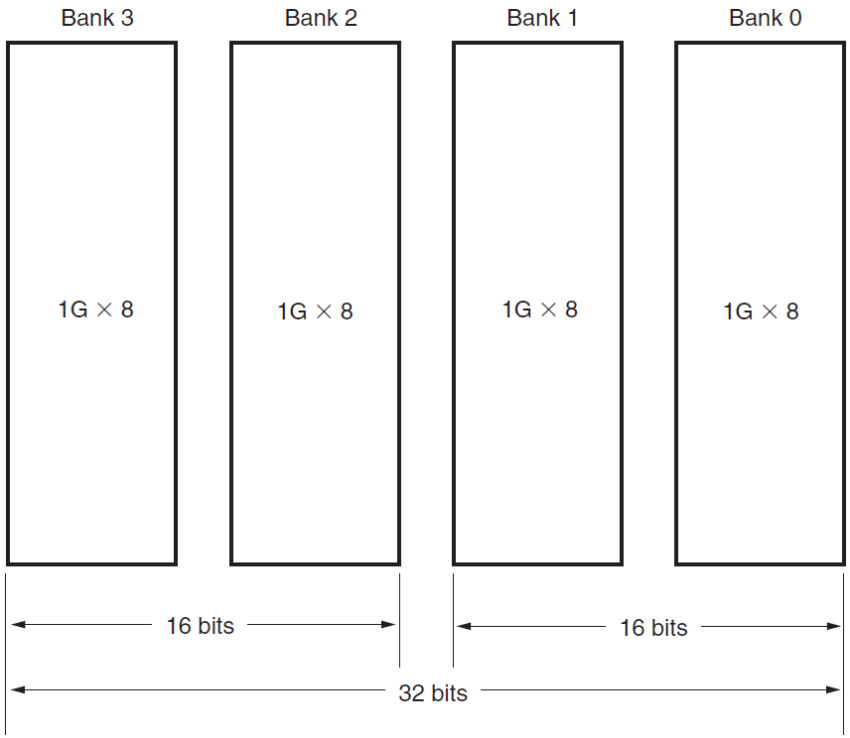
Memory System →

memory location →

00000000H to FFFFFFFFH,
00000000H is in bank 0,
00000001H is in bank 1,
00000002H is in bank 2,
00000003H is in bank 3.

data width is important →

single-precision floating-point
numbers = 32 bits wide.
faster execution of high-level software.



Input/Output System →

almost all 80486 systems use isolated I/O,
64K different bytes of I/O space are available.
full 32-bit-wide I/O system is divided into 4 banks.
most I/O transfers are 8 bits wide.

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Input/Output System →

ASCII code = 8-bit, Unicode = 16-bit,

disk memory and video display interfaces = 16 and 32 bits wide.

I/O locations →

0000H to FFFFH.

coprocessor = 800000F8H–800000FFH.

specific memory-mapped I/O range.