CSE-3103: Microprocessor and Microcontroller

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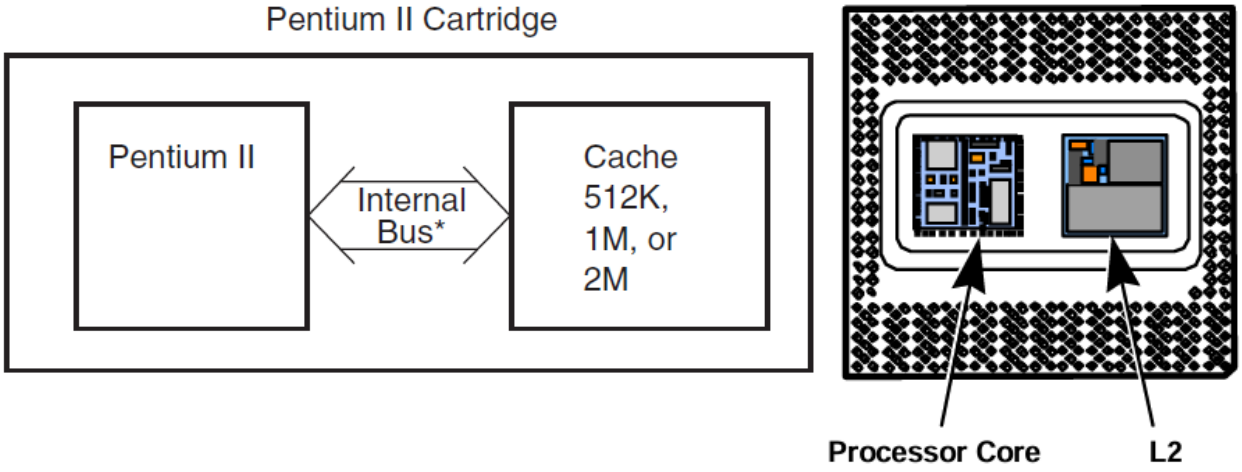
Pentium II Processor

Cache architecture →

Level 1 (L1) cache →
32 KB (16 KB for instruction + 16 KB for data),
embedded directly on processor die for high speed.

Level 2 (L2) cache →
moved off main processor die,
placed separate, SRAM chips on same PCB as processor,
achieve very close proximity at much lower cost.
cache was connected to CPU via dedicated back-side bus (BSB).



Pentium II Processor

Memory system →

64G bytes in size.
memory system = 64 bits wide,
address bus = 36 bits wide (2^{36} = 64G bytes).
most systems use SDRAM →

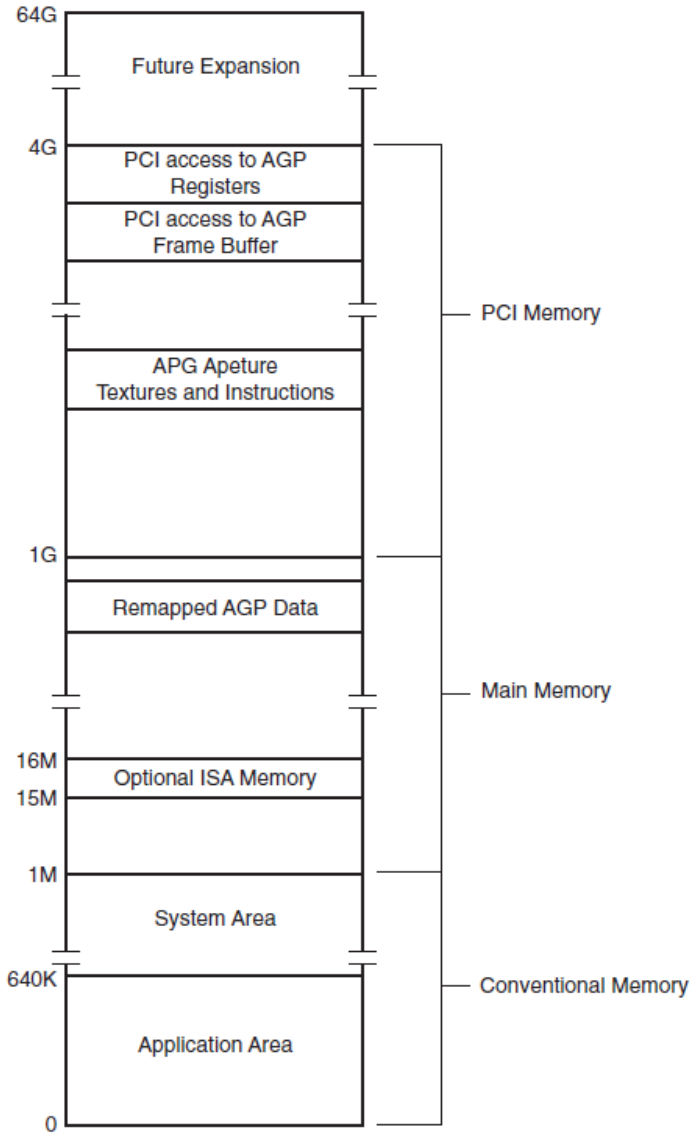
66 MHz system: access time = 10 ns,
100 MHz system: access time = 8 ns.

memory system is divided into 8 or 9 banks,
each stores one byte of data.
9th byte is present →

stores error-checking code (ECC).

employs internal parity generation and checking logic.

memory system is numbered in bytes,
byte 000000000H to byte FFFFFFFFH.



Pentium II Processor

Memory system →

basic memory map using AGP →

area of memory is used for AGP area →

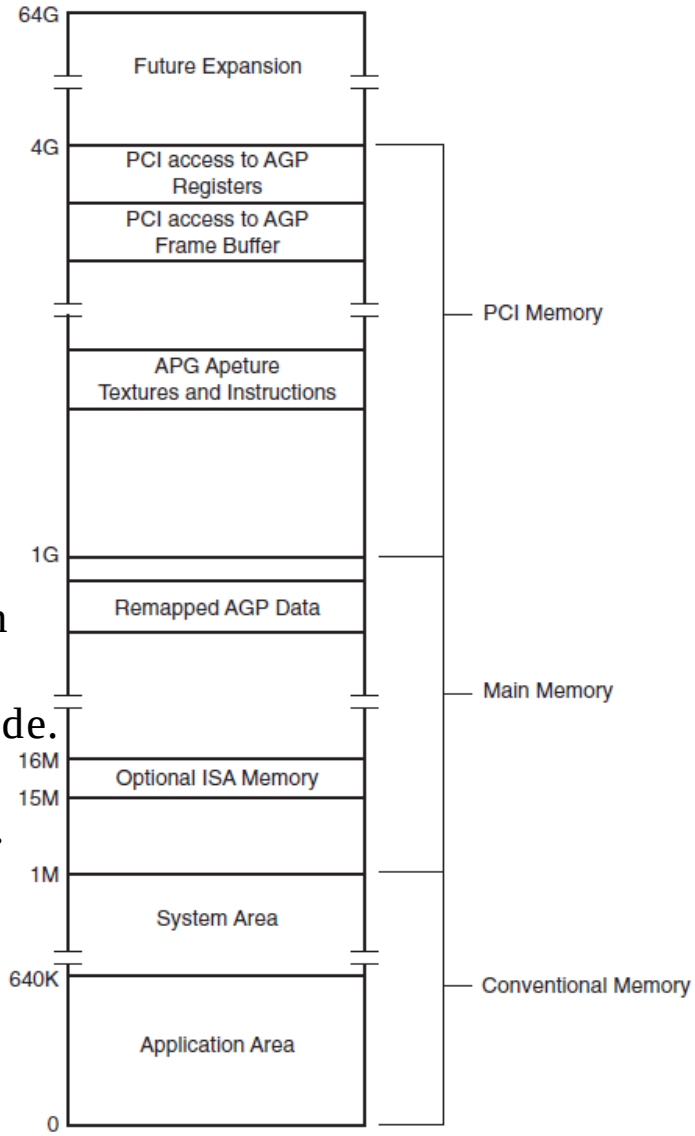
mapped into linear address space.
allows video card and Windows to access large video information.
much faster video updates.

data transfers between Pentium II and memory system = controlled by 440 LX or 440 BX chip set.
transfers between Pentium II and chip set = 8 bytes wide.
traditional method =

microprocessor directly connected to memory.

Pentium II connects only directly to cache,
cache = on Pentium II cartridge.

CPU → L2 Cache → Chipset → Main Memory
CPU → Chipset → AGP Bus → Video Card → AGP Aperture in main memory



Pentium II Processor

Input/Output System →

completely compatible with earlier Intel microprocessors.

A_{15}–A_3 →

I/O port number (2^{13} = 8192 ports).

A_2–A_0 →

select byte, word, or double-word inside port.

bank-enable signals →

select memory banks used for I/O transfer.

chipset activates required bank enable signals.

= transfers are controlled by chip set.

Pentium III Processor

Improved version of Pentium II microprocessor.

2 versions of Pentium III →

1) with non-blocking 512K byte L2 cache,
runs at half of processor speed.

2) with 256K byte advanced transfer L2 cache,
packaged in integrated circuit.
runs at processor clock frequency.

non-blocking =
CPU continues executing instructions
even if cache miss occurs.

Chip sets →

Pentium III uses Intel 810, 815, or 820 chip set.

Bus →

bus speed = 100 MHz or 133 MHz.
last released version = 1 GHz microprocessor with 133 MHz bus.

Pin-Out →

packaged in 370-pin, pin grid array (PGA) socket.

Pentium 4 and Core2 Processor

Recent version of Pentium Pro architecture →
Pentium 4 microprocessor,
Core2 from Intel.

Pentium 4 →
released initially with speed of 1.3 GHz.
currently available in speeds up to 3.8 GHz.

earlier versions use 100 MHz memory bus speed,
quad pumped = bus speed can approach 400 MHz.
recent versions = 133 MHz bus listed as 533 MHz.

Memory Interface →
uses Intel 945, 965, or 975 chip set.
chip sets provide dual-pipe memory bus to microprocessor,
each pipe interfaced to 32-bit-wide section of memory.
memory is populated with pairs of DDR2 memory devices,
memory devices operate at 600 MHz, 800 MHz, or 1033 MHz.

CPU → L2 Cache → Chipset → Main Memory
Main Memory = DDR2 (64-bit) + DDR2 (64-bit)

Pentium 4 and Core2 Processor

Memory Interface →

memory support for serial ATA disk interface has been added.
AGP interface is replaced by PCI Express (PCIe) for video support.
IDE support remains for interface to legacy devices.
Legacy devices = HDD, CD-ROM, DVD drives.

ATA = Advanced Technology Attachment.
PCI = Peripheral Component Interconnect.
IDE = Integrated Drive Electronics.

Register Set →

register set is nearly identical to all other versions of Pentium.
MMX registers are separate entities from legacy floating-point registers.
eight 128-bit wide XMM registers are added →
registers are numbered from MM0 to MM7.
used with SIMD (single-instruction, multiple data) instructions.
XMM registers = double-width MMX registers,
hold → pair of 64-bit double-precision floating-point numbers or
4 single-precision floating-point numbers.
= 16-byte wide numbers.

PCI: used to connect peripheral devices to motherboard,
sound cards, network cards, graphics cards etc.
standardized way for hardware to communicate with processor.

Pentium 4 and Core2 Processor

Hyper-threading technology →

combines 2 microprocessors into single package.

processor contains 2 execution units,

each EU →

contains complete set of registers,

capable of running software independently or concurrently.

share common bus interface unit.

processor is capable of running thread (process) independently,

application is written using multiple threads.

bus interface unit →

contains L2 and L3 caches,

interface to memory and I/O structure of machine.

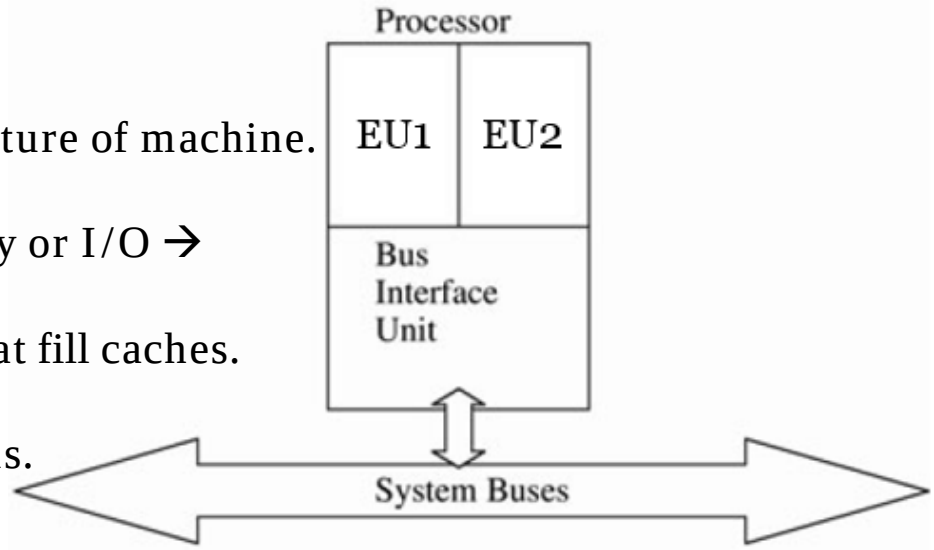
1st microprocessor needs to access memory or I/O →

it shares bus interface unit.

BIU accesses memory in bursts that fill caches.

2nd processor =

busy executing instructions.



Pentium 4 and Core2 Processor

Multiple core technology →

new versions of Pentium 4 and Core2 →

contain either dual or quad cores.

each core =

separate version of microprocessor,

independently executes separate task.

3 versions →

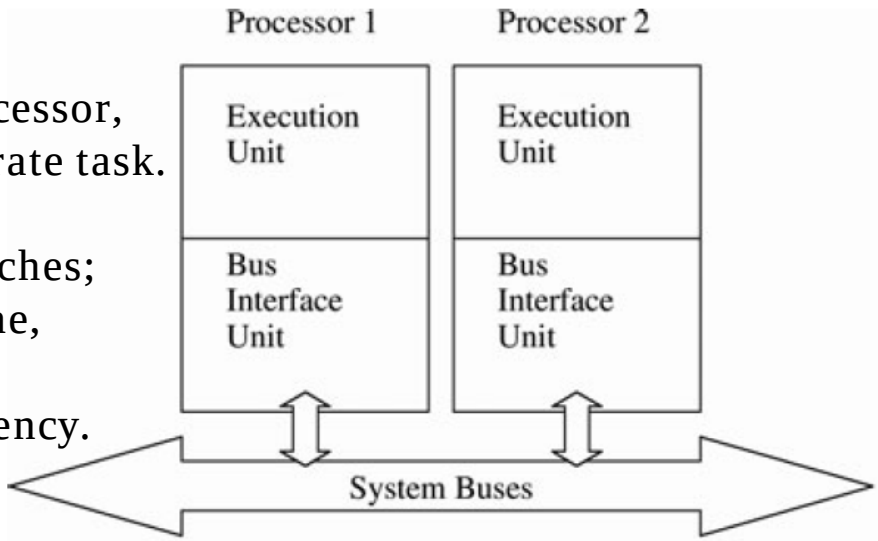
Pentium D = 2 cores with separate caches;

Core2 Duo = 2 cores with shared cache,

2M or 4M byte cache,

operates at 3 GHz frequency.

Quad core = contains 4 cores.



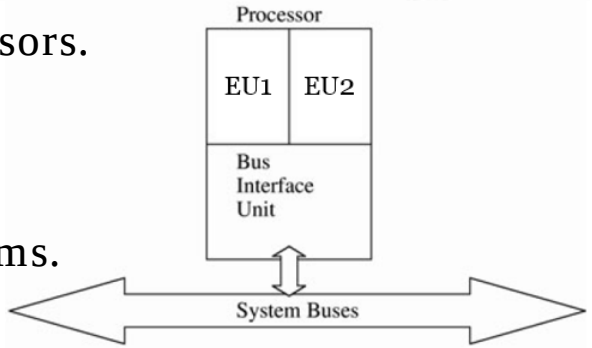
Intel migrates to shared cache for multiple core microprocessors.

future Pentium may contain up to 80 cores.

clock frequency has stabilized at between 3 and 4 GHz.

future prospect = multiple cores using threaded application.

efficient programming = increasing speed of computer systems.



Pentium 4 and Core2 Processor

Model-specific registers (MSRs) →

Pentium 4 and Core2 each have 1743 MSRs,
MSRs are numbered from 000H to 6CFH.
Intel does not provide information on all of them.
ECX is loaded with register number to be accessed,
data are transferred through EDX:EAX as 64-bit number.

Performance-monitoring registers (PMRs) →

Pentium 4 has set of performance-monitoring registers.
time-stamp counter = only register accessed via user software.
ECX specifies register number,
result appears in EDX:EAX.
there is no write instruction for PMRs.

MSRs = control hardware features,
monitor performance,
manage system-level operations.

Pentium 4 and Core2 Processor

64-bit extension technology →

Intel has released 64-bit extension technology for most 32-bit architecture family.
instruction set and architecture are backwards compatible to 8086.

register set →

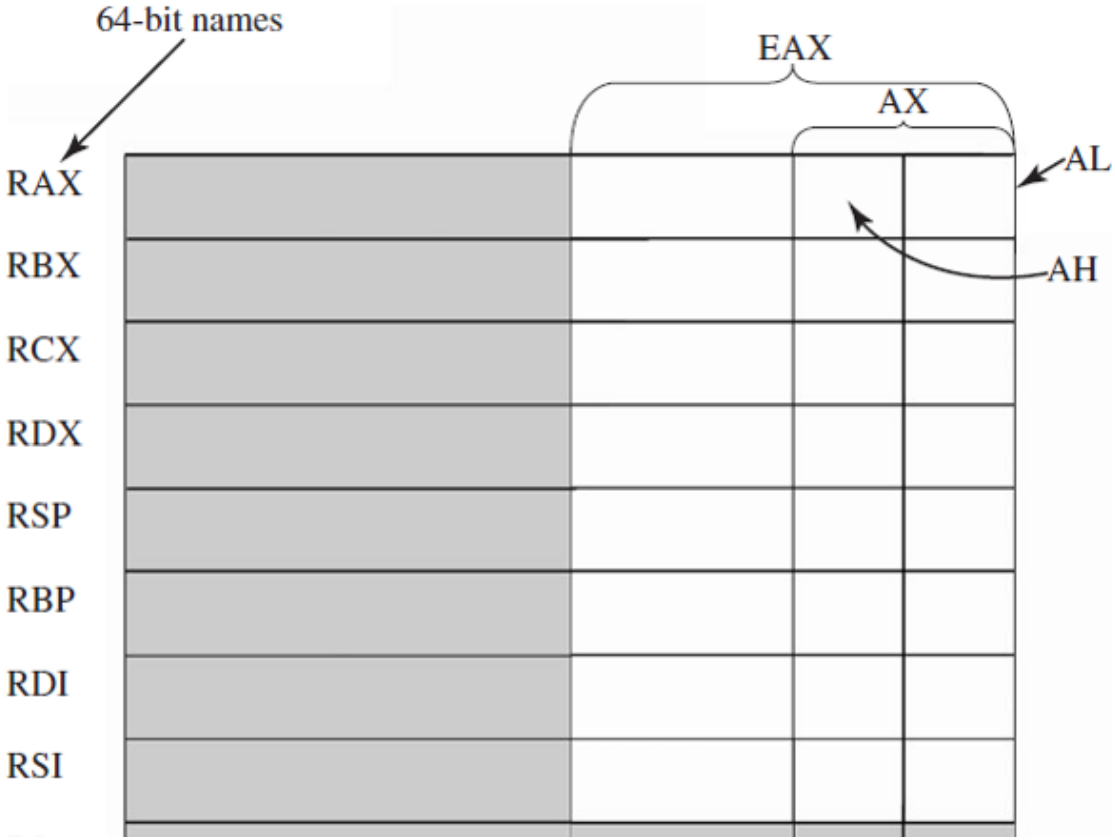
sixteen 64-bit-wide general-purpose registers,
8 legacy registers = RAX, RBX, RCX, RDX, RSP, RBP, RDI, RSI,
8 numbered registers = R8–R15.
IP = 64 bits.
registers are addressed as 64-bit, 32-bit, 16-bit, 8-bit registers.

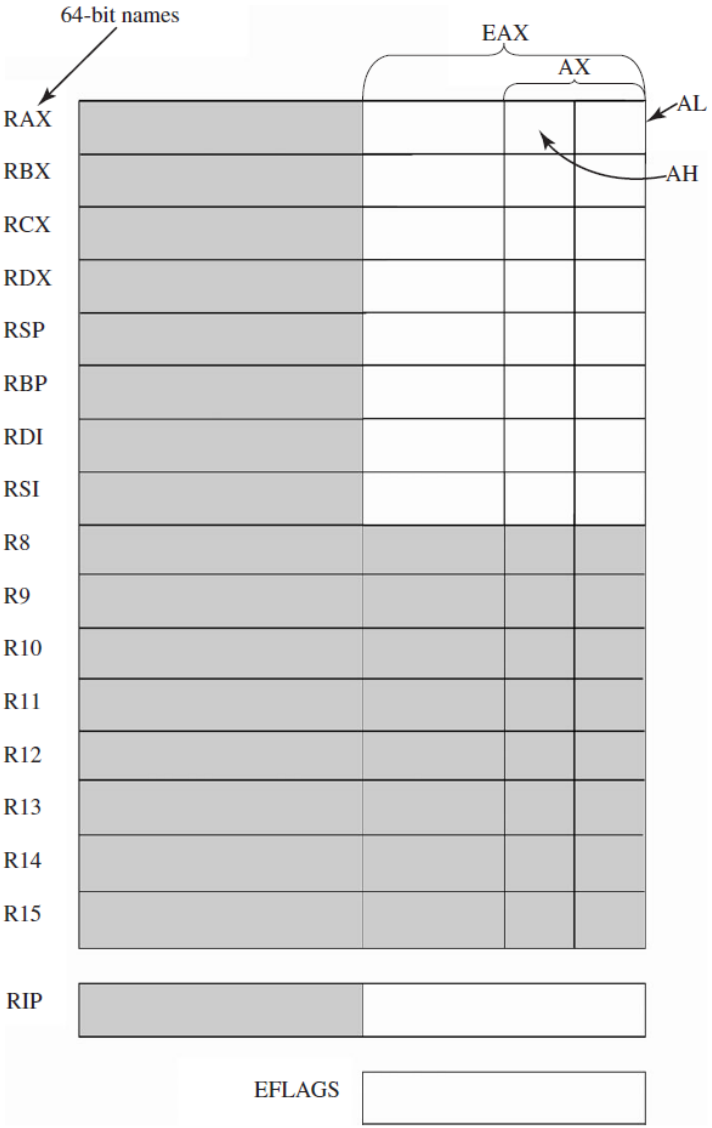
numbered registers (R8–R15) →

R8 (64 bits), R8D (32 bits), R8W (16 bits), R8L (8 bits).
no way to address high byte as in AH or BH,
only low byte can be addressed.

Pentium 4 and Core2 Processor

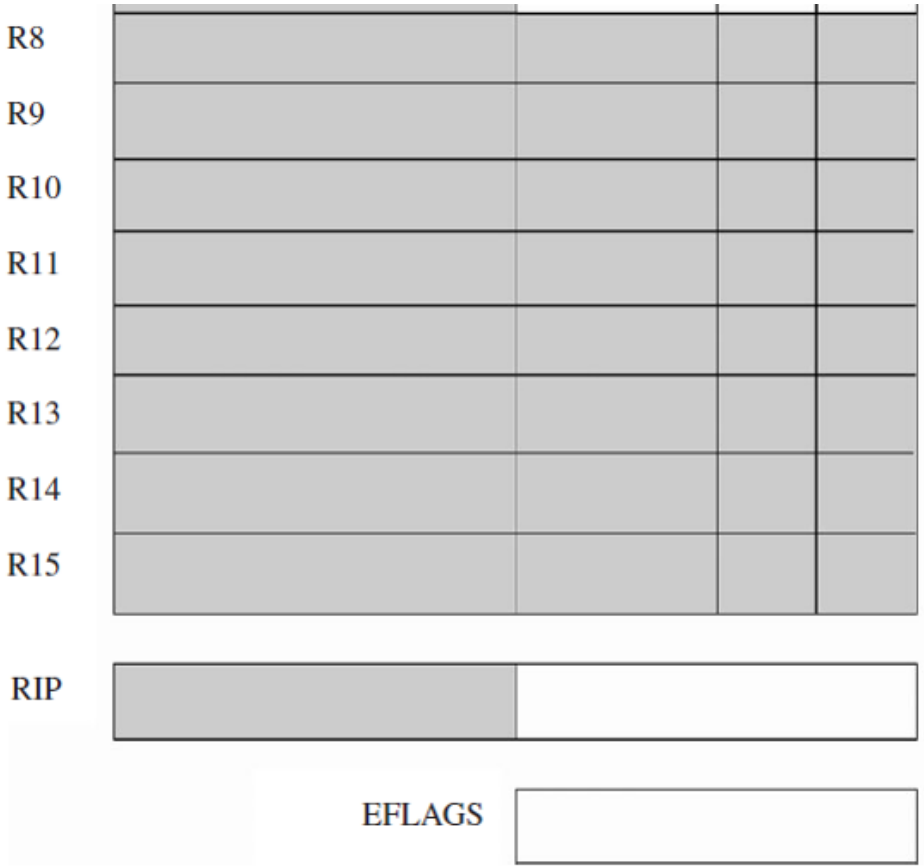
Integer register set of Pentium 4 and Core2 in 64-bit mode →

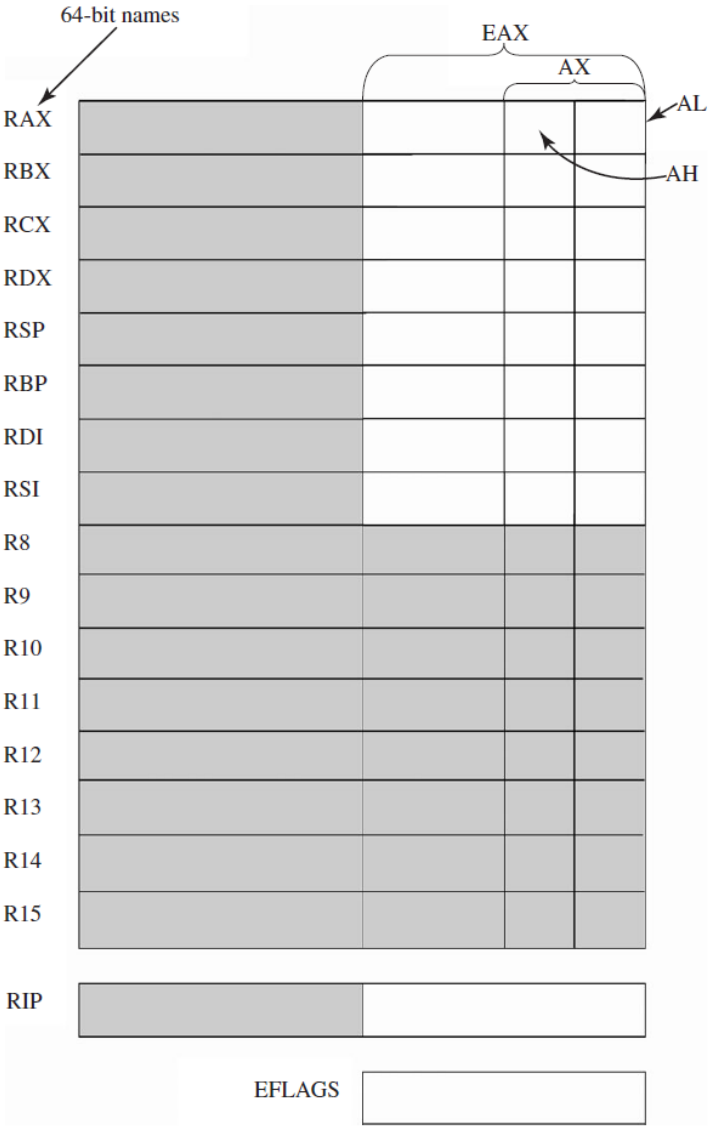




Pentium 4 and Core2 Processor

Integer register set of Pentium 4 and Core2 in 64-bit mode →





Pentium 4 and Core2 Processor

64-bit extension technology →
- register set →
  - MOV AL, R9L is allowed.
  - MOV AH, R9L →
    - not allowed,
    - no error will occur,
    - will be changed to MOV BPL, R9L.
  - AH, BH, CH, DH = low-order 8 bits of BPL, SPL, DIL, SIL.

Paging: to manage huge address space efficiently,
address is split into multiple parts,
each selecting entry from different level of page table.

Protected mode descriptor table registers →
- expanded in extended 64-bit mode.
- base address for CS = 0000000000000000H,
- base address for DS, ES, SS are ignored.

Segmentation is mostly disabled.
To reduce segmentation complexity
and use pure flat addressing,
CS = 0 → All instruction fetches
use flat, zero-based address system.

Paging unit →
- supports translation of 64-bit linear address into 52-bit physical address.
- 52-bit address accesses 4P (peta) bytes of memory,
- 64-bit linear address accesses 16E (exa) bytes of memory.
- translation uses 4 levels of page tables.