CSE-3103: Microprocessor and Microcontroller

Dept. of Computer Science and Engineering
University of Dhaka

Prof. Sazzad M.S. Imran, PhD
Dept. of Electrical and Electronic Engineering
sazzadmsi.webnode.com

Bit-Level Logic Instructions

Ladder diagram language →
symbolic set of instructions,
used to create controller program.

Symbolic instructions →
= command to perform specific operation.
arranged to obtain desired control logic.
entered into memory of PLC.

3 fundamental symbols →
translate relay control logic to contact symbolic logic.
1) Examine If Closed (XIC),
2) Examine If Open (XIO),
3) Output Energize (OTE).
each instruction relates to single bit of PLC memory,
memory address is specified by instruction's address.

Bit-Level Logic Instructions

Examine If Closed (XIC) instruction →

also called Examine-on instruction.

memory bit is linked to →

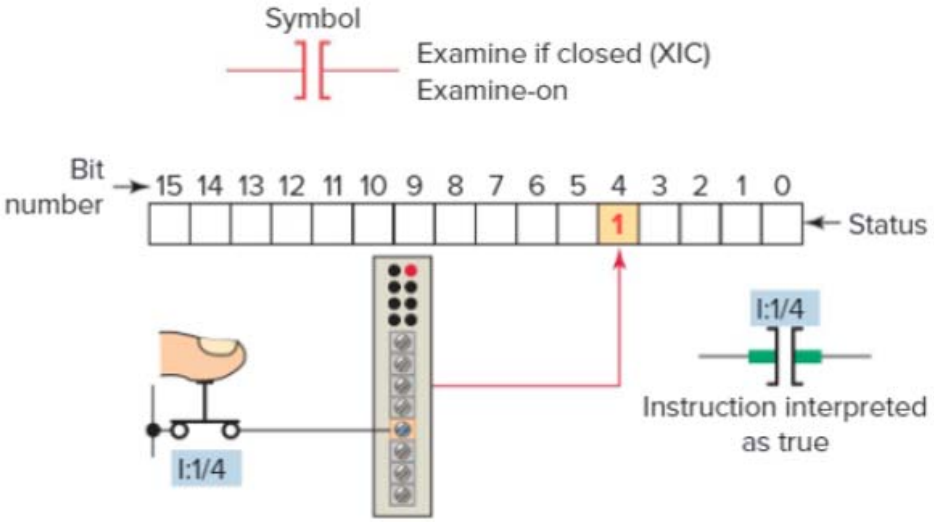
status of input device or

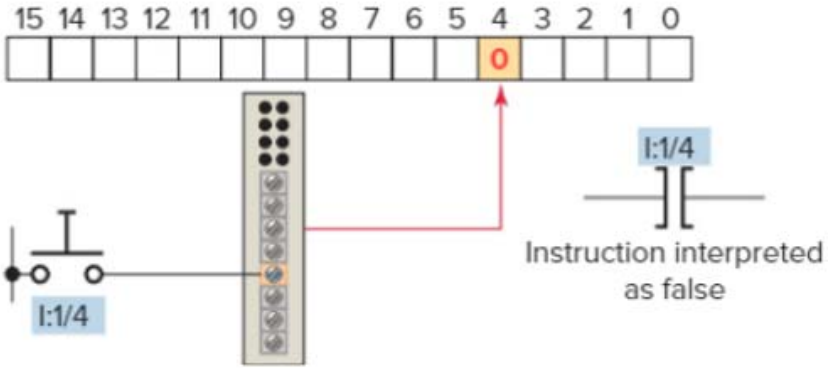
internal logical condition in rung.

asks PLC's processor to examine if contact is closed.

How it is done →

Symbol	Name	Bit status	Instruction status
	XIC	0	FALSE
		1	TRUE
	XIO	0	TRUE
		1	FALSE

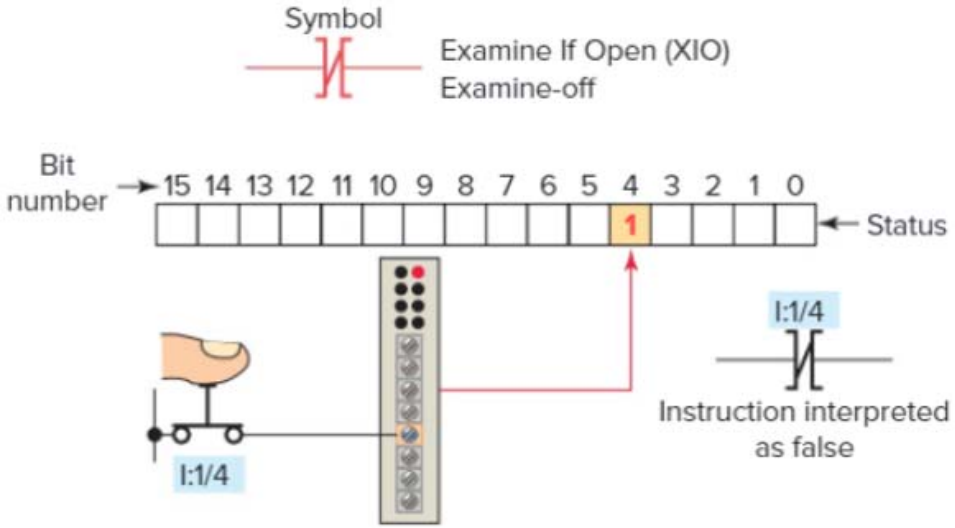


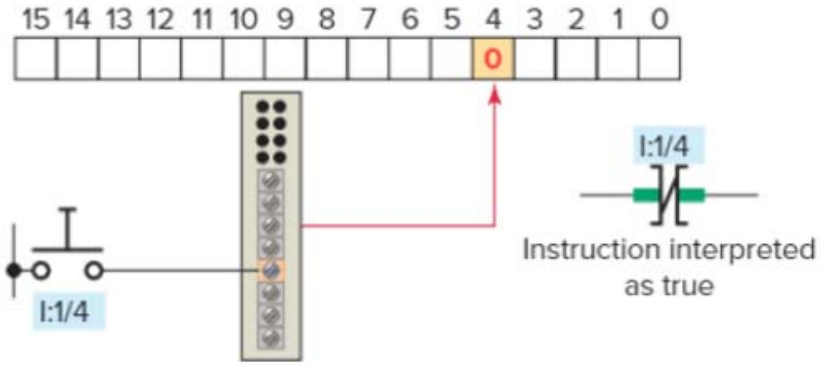


Bit-Level Logic Instructions

Examine If Open (XIO) instruction →
also called Examine-off instruction,
= normally closed relay contact.
memory bit is linked to →
status of input device or
internal logical condition in rung.
asks PLC's processor to examine if contact is open.
How it is done →

Symbol	Name	Bit status	Instruction status
	XIC	0	FALSE
		1	TRUE
	XIO	0	TRUE
		1	FALSE





Bit-Level Logic Instructions

Output Energize (OTE) instruction →

looks and operates like relay coil,

associated with memory bit.

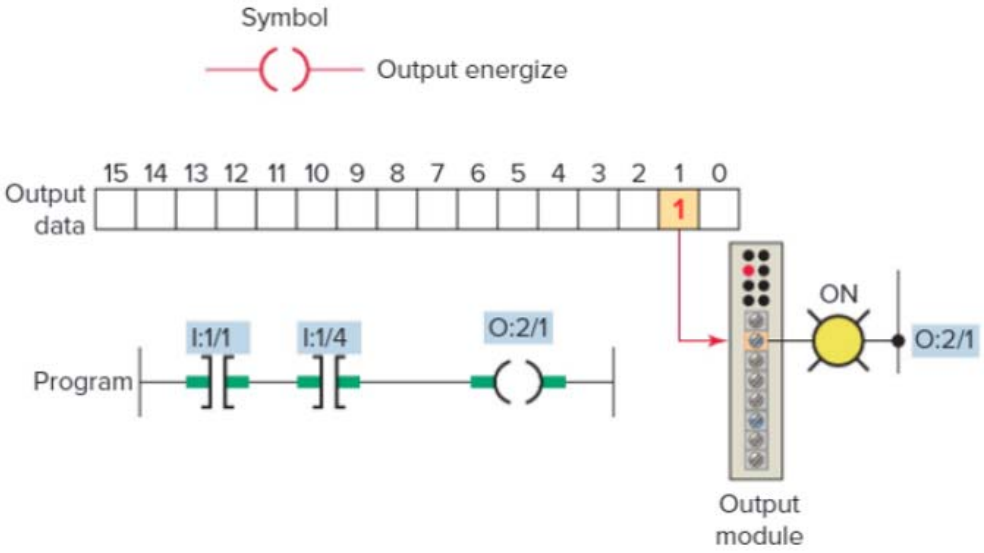
signals PLC to energize or de-energize output.

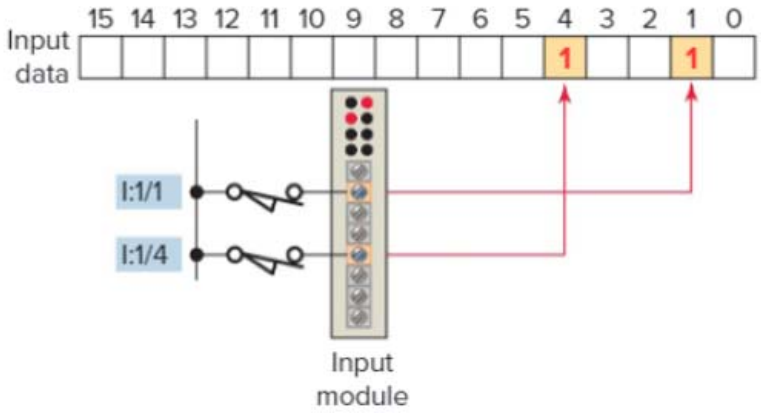
logical path of true XIC and XIO instructions in rung →

processor makes this instruction true,

analogous to energizing coil.

operation of OTE instruction →





Programming XIC and XIO Instructions

Program using both XIC and XIO instructions →

If the data table bit is	The status of the instruction is		
	XIC EXAMINE IF CLOSED	XIO EXAMINE IF OPEN	OTE OUTPUT ENERGIZE
Logic 0	False	True	False
Logic 1	True	False	False

Time	Instruction outcome		
	XIC	XIO	OTE
t_1 (initial)	False	True	False
t_2	**True**	**True**	**Goes true**
t_3	True	False	Goes false
t_4	False	False	Remains false

Input bit status		
XIC	XIO	OTE
0	0	0
1	**0**	**1**
1	1	0
0	1	0

Instruction Addressing

Assign address to each instruction →

indicates →

what PLC input is connected to what input device,

what PLC output will drive what output device.

links it to particular bit in data table portion of memory.

PLC model →

addressing of real inputs and outputs,

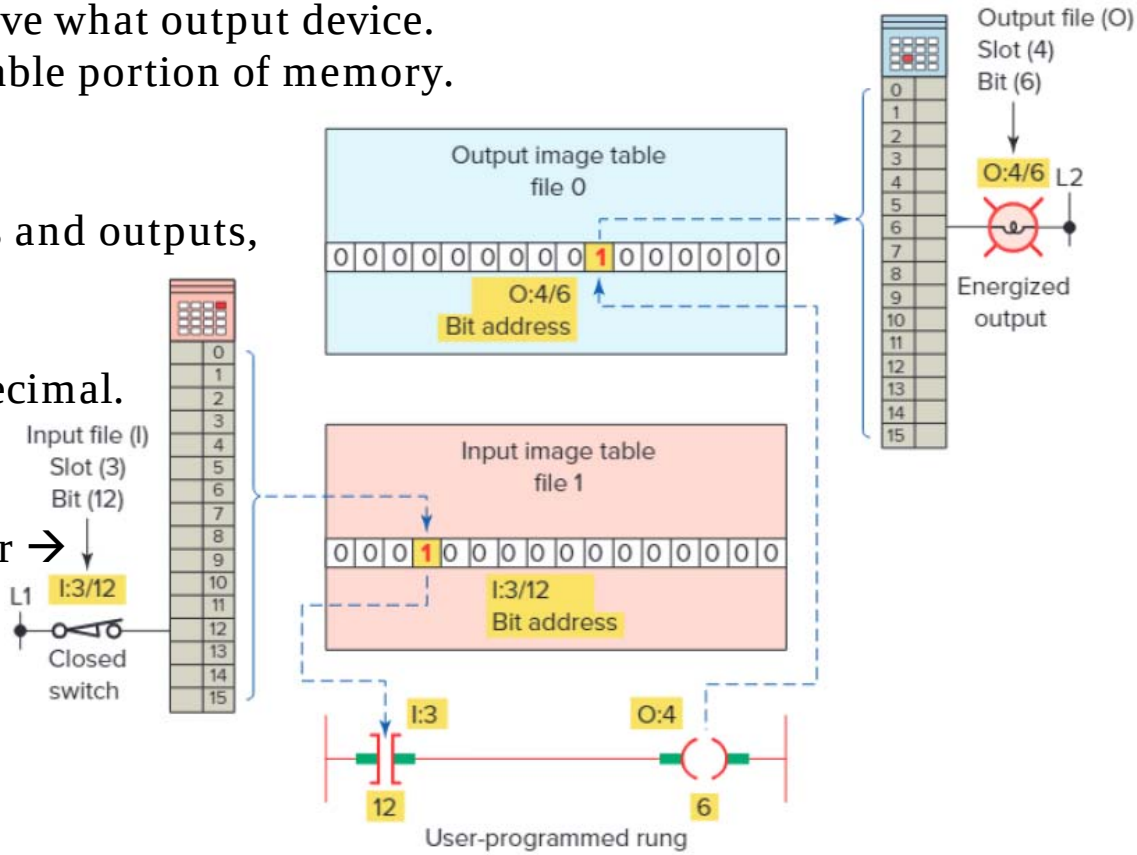
addressing formats.

number system used by PLC →

decimal, octal, or hexadecimal.

Addressing format for

Allen-Bradley SLC 500 controller →



Branch Instructions

OR logic (input) →

at least one of parallel branches forms true logic path →

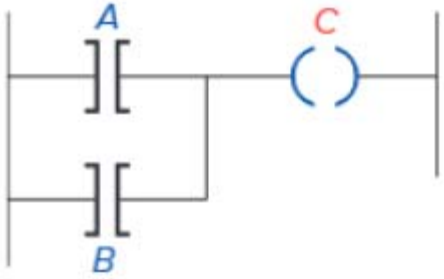
rung logic is true,

output will be energized.

none of parallel branches complete logical path →

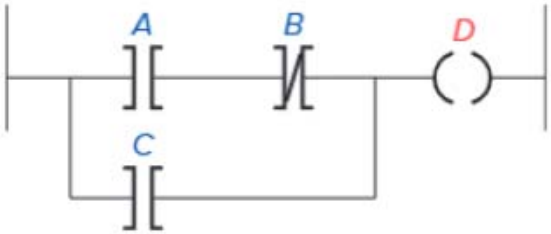
logic rung continuity is not established,

output will be de-energized.



Parallel input branching →

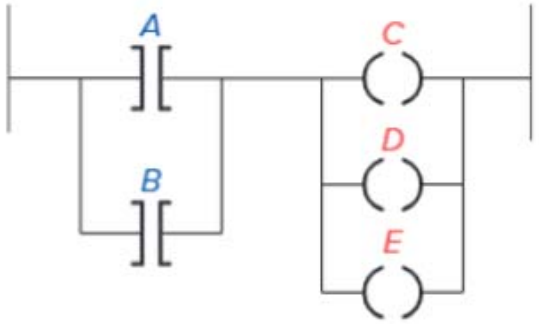
allows more than one combination of input conditions.



Parallel output branching →

program parallel outputs on rung,

allows true logic path to control multiple outputs.

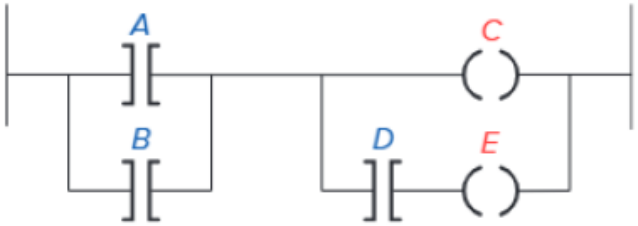


Branch Instructions

Parallel output branching with conditions →

additional input logic instructions is programmed in output branches.

enhances conditional control of outputs.

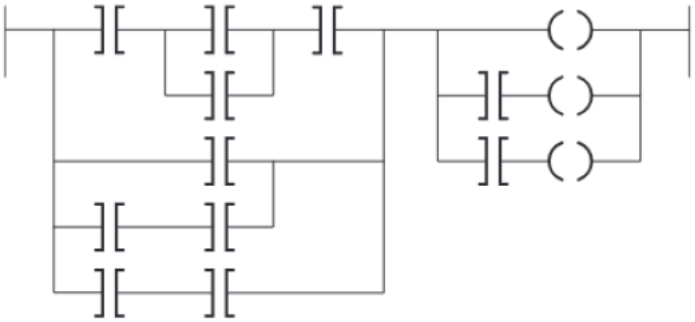


Nested input and output branches →

nested branch starts or ends within another branch.

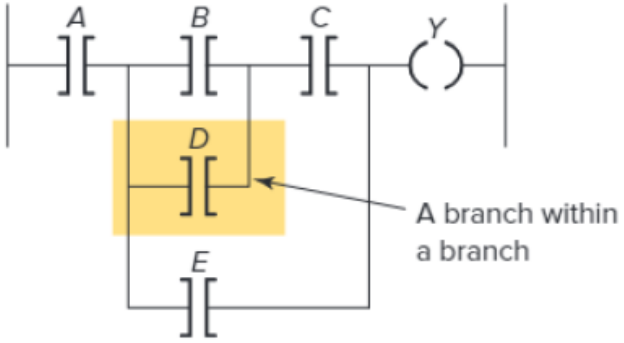
to avoid redundant instructions,

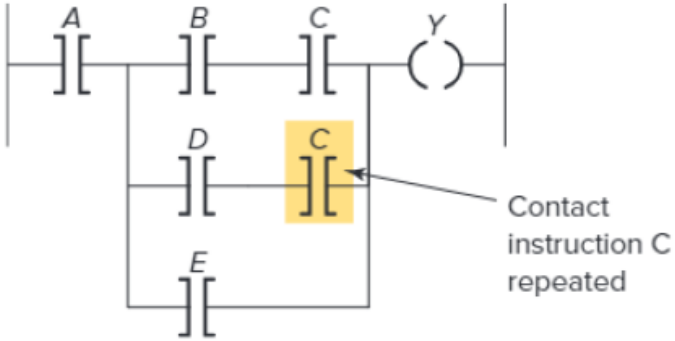
to speed up processor scan time.



Program required to eliminate nested contact →

by repeating instructions to make parallel equivalents.



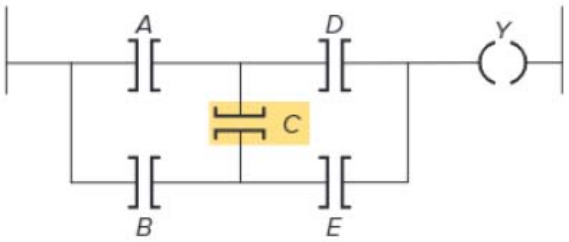


Branch Instructions

PLC matrix limitations →

= limitations on →

allowable series elements,
parallel branches, or
outputs.

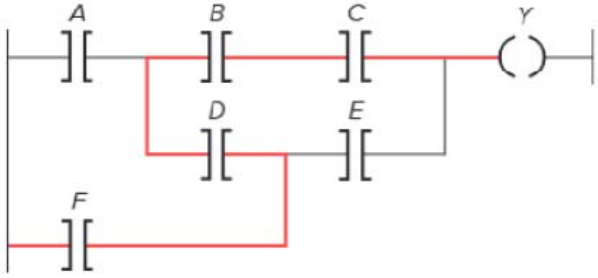


Boolean equation: $Y = (AD) + (BCD) + (BE) + (ACE)$

Program with vertical contact.

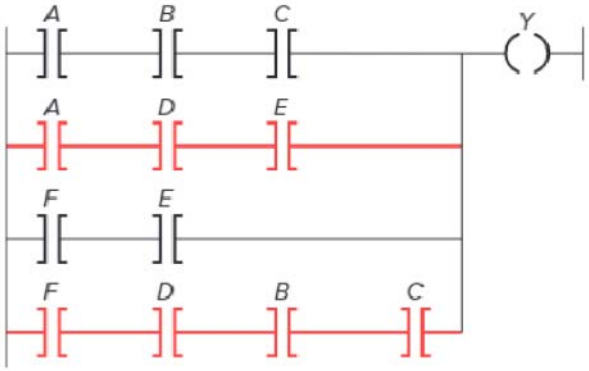
Another limitation to branch circuit programming →

programming of vertical contacts is not allowed.
processor never allows for flow from right to left.

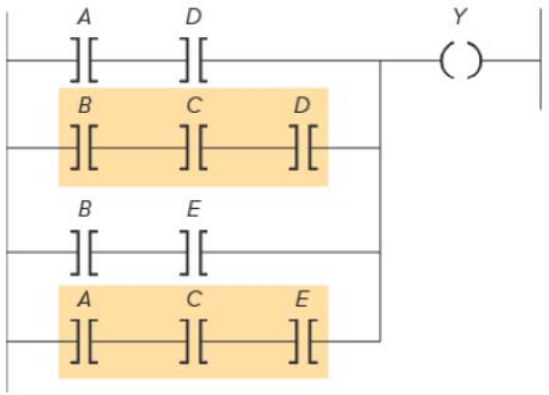


Boolean equation: $Y = (ABC) + (ADE) + (FE) + (FDBC)$

Original circuit.



Reprogrammed circuit.



Reprogrammed to eliminate vertical contact.

Internal Relay Instructions

Internal storage bits →

area of memory in PLCs.

also called →

internal outputs, internal coils,
internal control relays, or internal bits.

Internal outputs →

on/off signals generated by programmed logic.
does not directly control output field device.
used strictly for internal purposes.

output instruction is required in program but
no physical connection to field device is needed.

no physical outputs are wired to bit address,
address is used as internal storage bit or point.
storage bits are programmed by user,
perform relay functions without occupying physical output.

Internal Relay Instructions

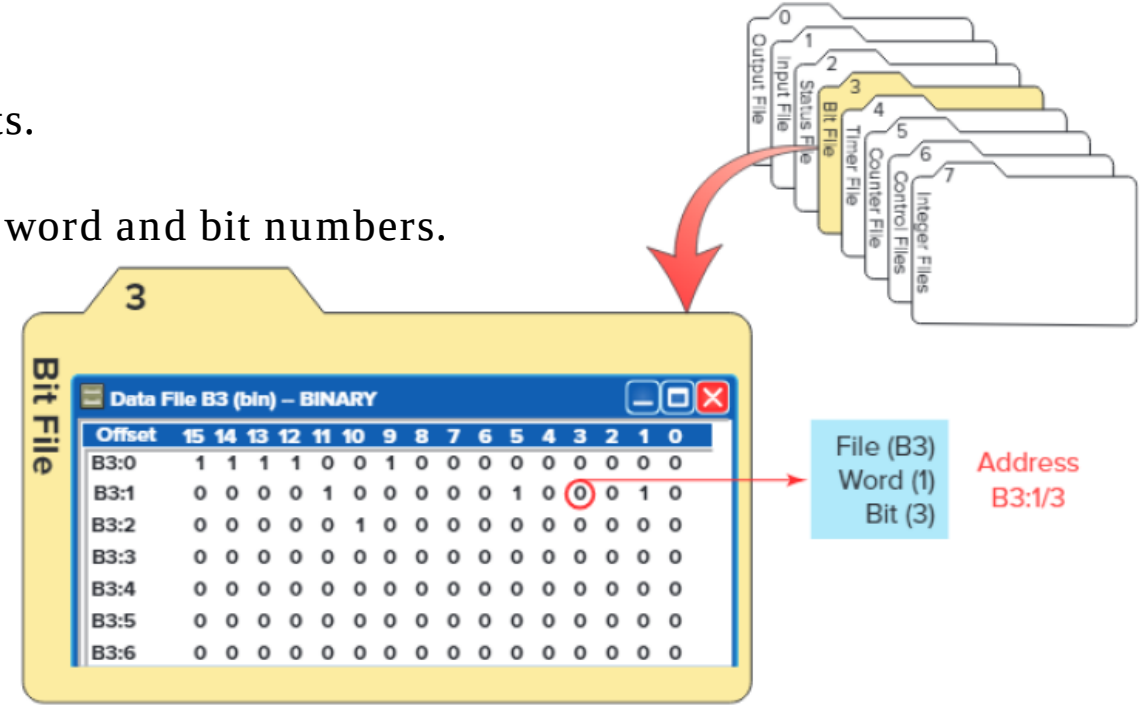
Internal outputs →

= single-bit storage locations in memory.

SLC 500 controllers →

use bit file B3 for storage and
addressing of internal output bits.
addressing for bit B3:1/3 =

file number followed by word and bit numbers.



Internal Relay Instructions

Internal control relay →

used when program requires
more series contacts than rung allows.
circuit allows for 7 series contacts,
12 are actually required for programmed logic.

Solution →

contacts are split into 2 rungs.