CSE-3103: Microprocessor and Microcontroller

Dept. of Computer Science and Engineering
University of Dhaka

Prof. Sazzad M.S. Imran, PhD
Dept. of Electrical and Electronic Engineering
sazzadmsi.webnode.com

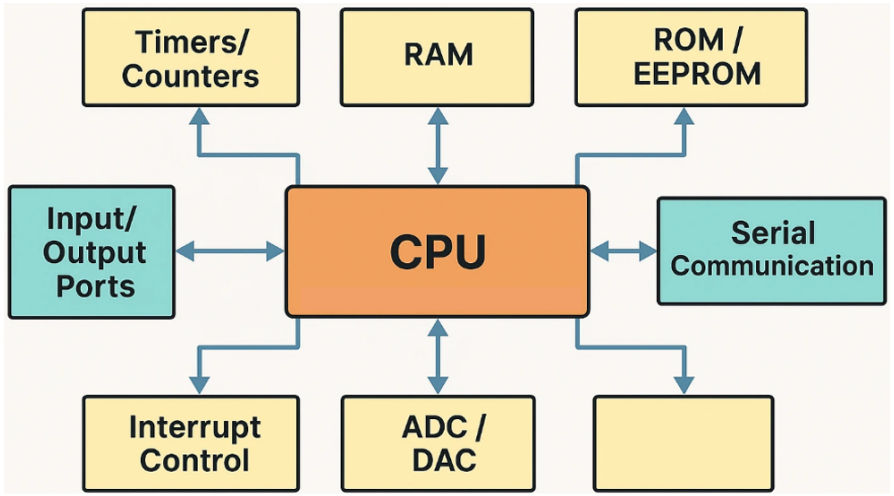
Microcontroller

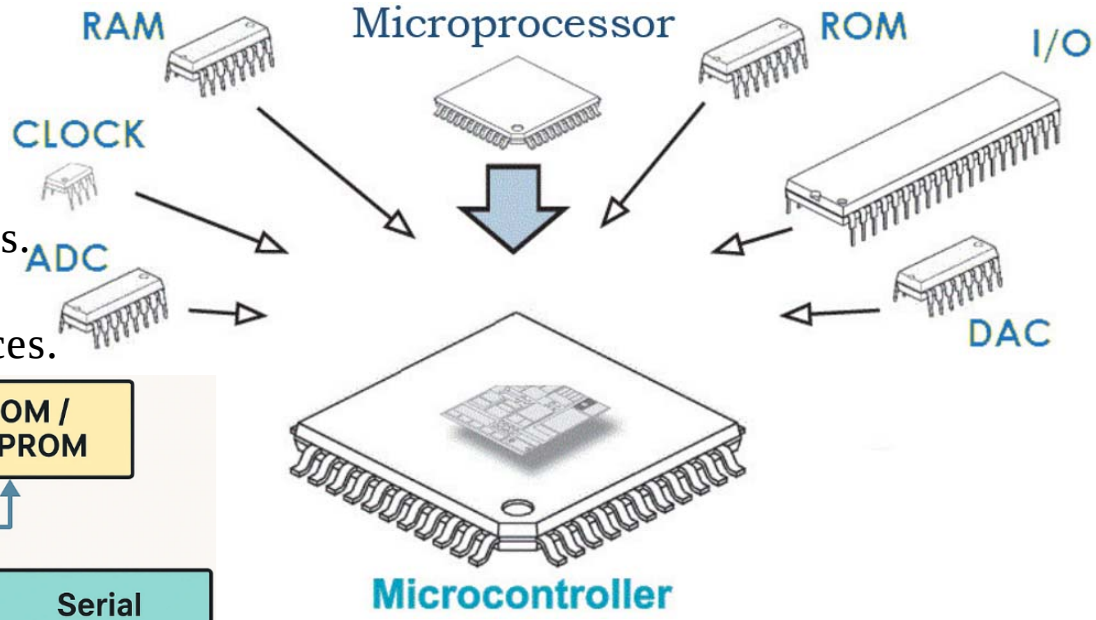
Microcontroller →

small, self-contained computer system,
housed within single integrated circuit (IC).
combines on single chip →

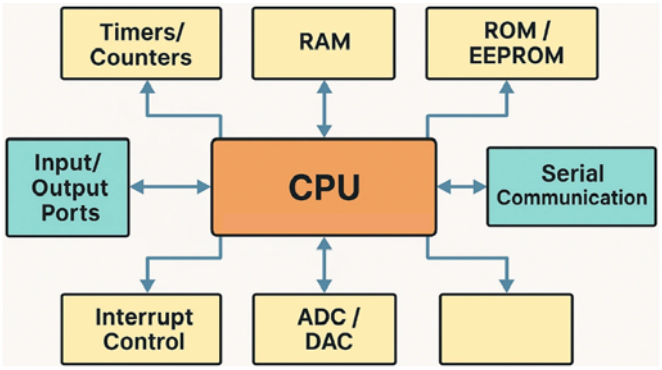
- microprocessor core,
- memory,
- Input/output peripherals,
- other essential components.

designed for specific tasks,
applications = industries and devices.





Microcontroller



Microcontroller components →

Microprocessor core =

central processing unit (CPU),
executes instructions and performs calculations.

Memory =

program memory (ROM or flash) for storing firmware,
data memory (RAM) for temporary storage during program execution.

I/O ports =

microcontroller interacts with external devices,
devices = sensors, actuators, displays, communication modules.

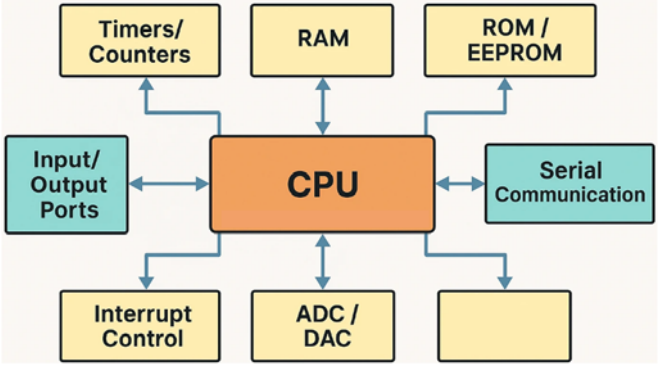
Timers and Counters =

measure time intervals or count events accurately.

Analog-to-Digital Converters (ADC) =

convert analog signals from sensors or other sources into
digital data for processing.

8051 Microcontroller



Microcontroller components →
- Communication interfaces =
  - for data exchange with other devices or systems.
  - serial ports, USB ports, Ethernet interfaces,
  - wireless communication modules.

Architecture of 8051 →

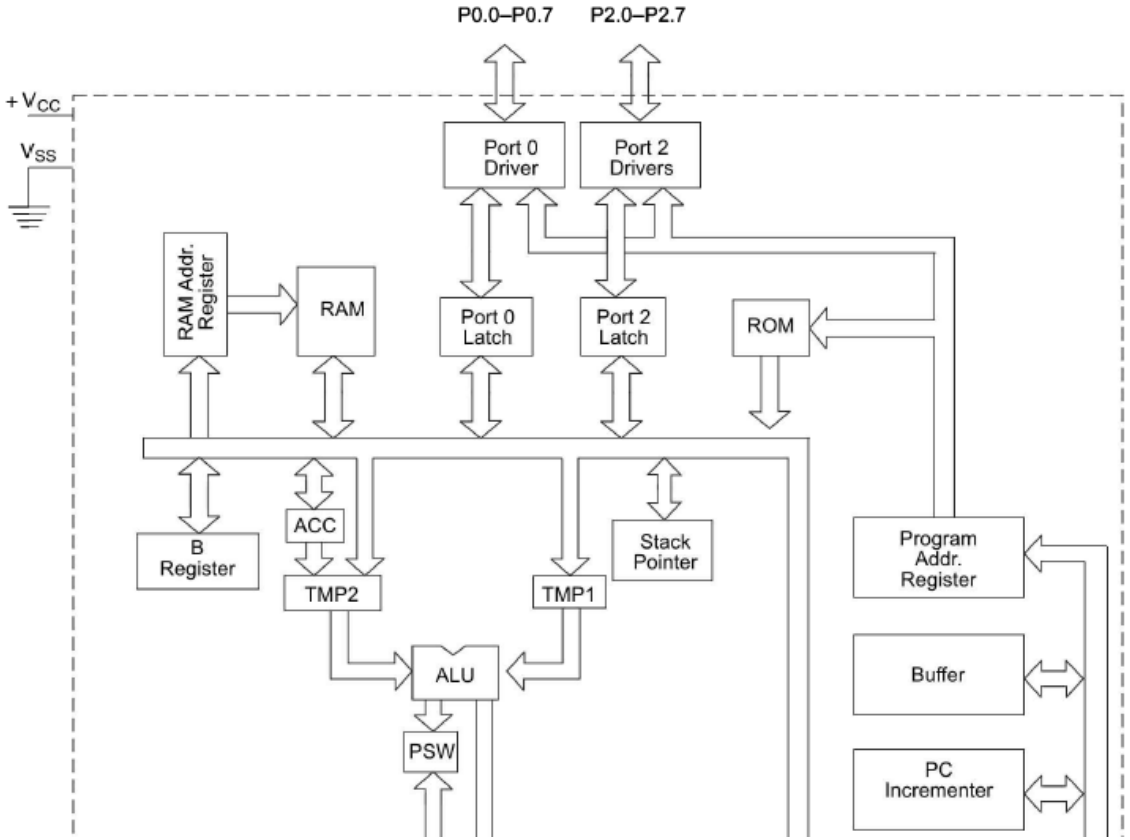
Accumulator (ACC or A) register →
- acts as operand register,
- implicit or specified in instruction.
- address is allotted in on-chip special function register bank.

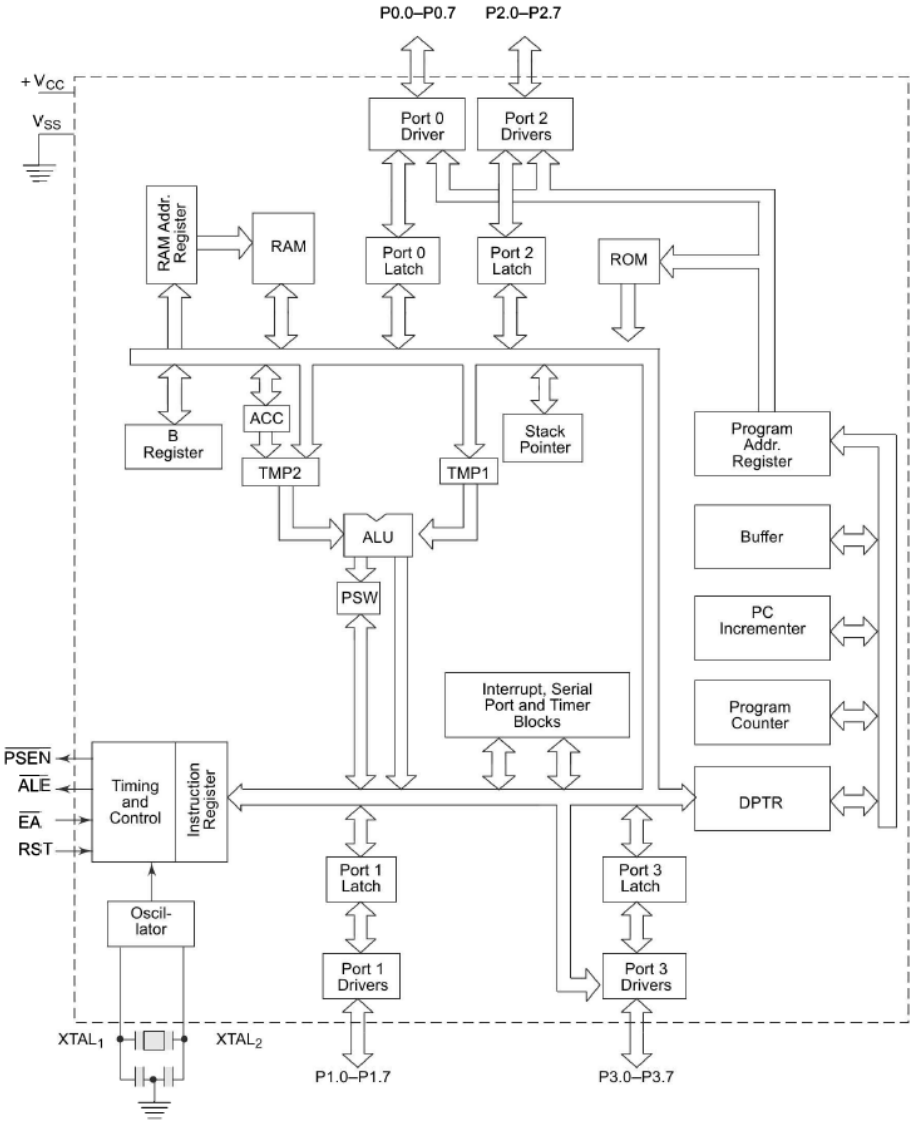
B register →
- store one of operands for multiply and divide instructions.
- used as scratch pad in other instructions.

scratch pad =
general-purpose temporary register

Program status word (PSW) →
- set of flags,
- contains status information.

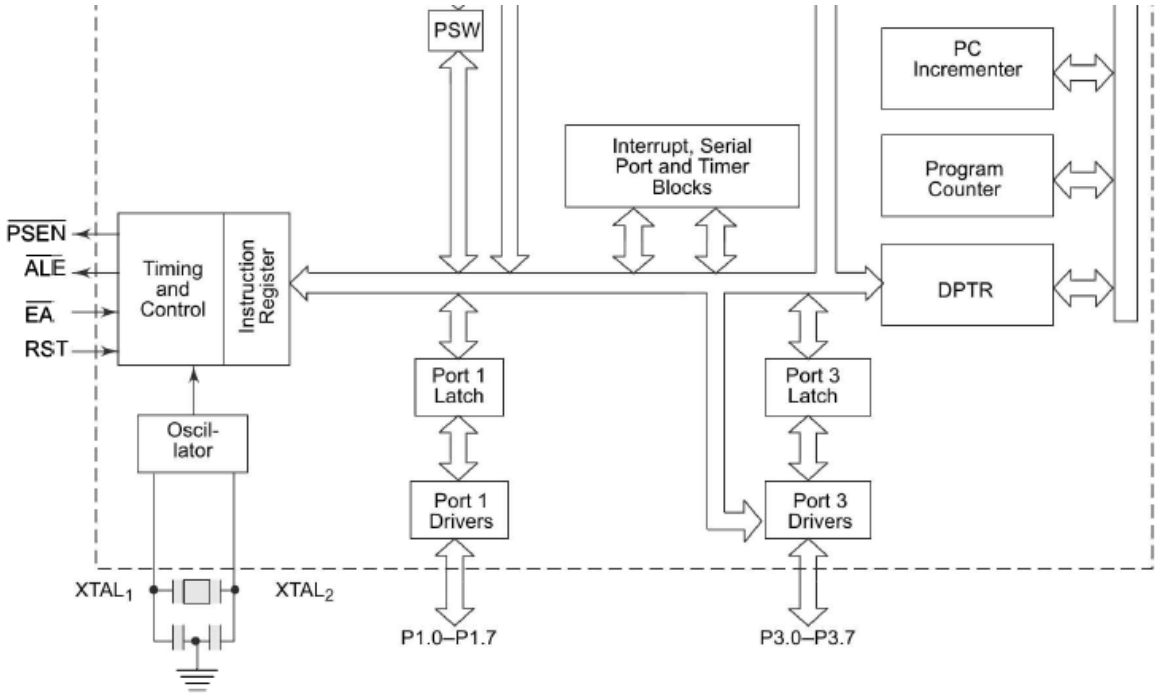
8051 Microcontroller

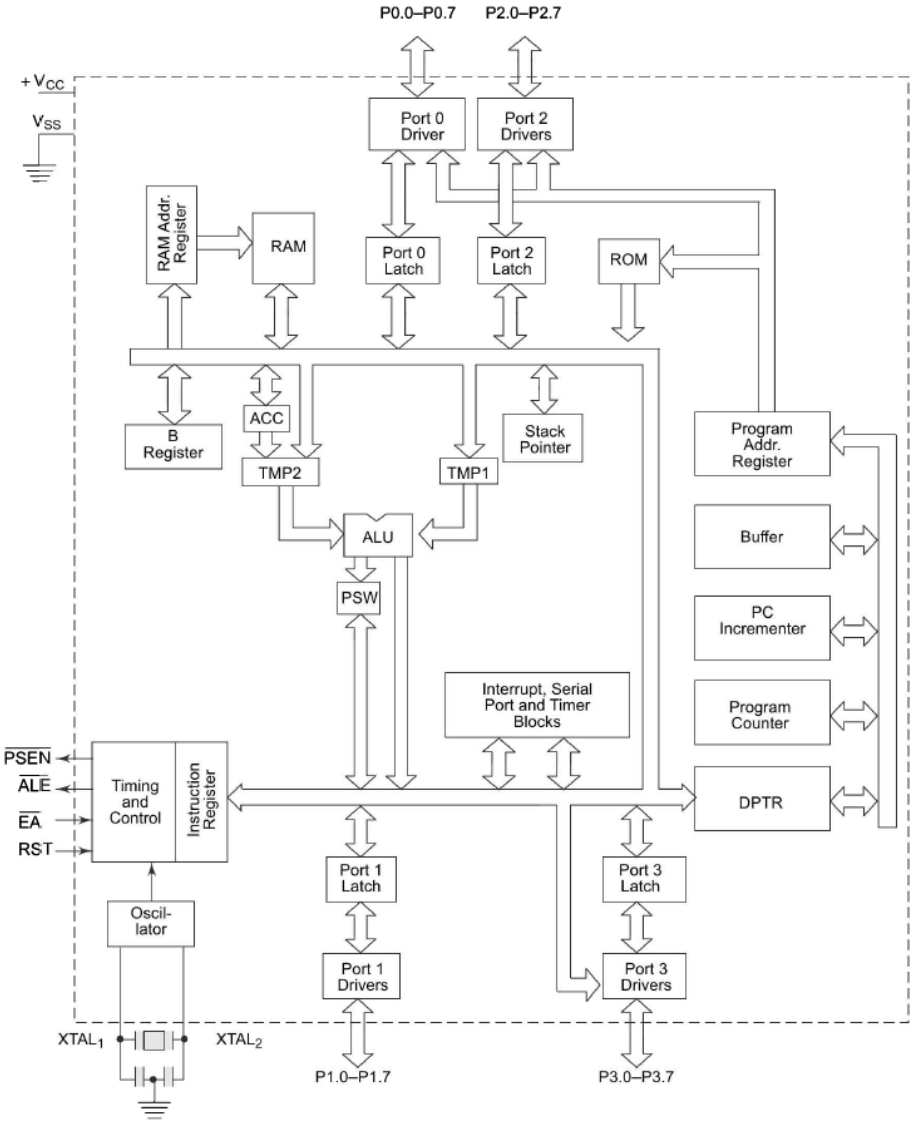




8051 Microcontroller

.





8051 Microcontroller

Architecture of 8051 →
Stack pointer (SP) →
- 8-bit wide register,
- contains 8-bit stack top address.
- initialized to 07H after reset.
- stack is defined anywhere in on-chip 128-byte RAM.
- push or call instructions →
  - SP is incremented by one,
  - data is stored onto stack.
- address is allotted in on-chip special function register bank.

Data pointer (DTPR) →
- 16-bit register →
  - higher byte (DPH) and lower byte (DPL).
  - accessed as 16-bit or two 8-bit registers.
- contains 16-bit external data RAM addresses.
- 2 addresses are allotted in special function register bank →
  - 2 bytes DPH and DPL.

8051 Microcontroller

Architecture of 8051 →
Port 0 to 3 latches and drivers →
- allotted to 4 on-chip I/O ports.
- addresses are allotted in special function register bank.
- port communication →
  - through allotted addresses.
  - identified as P0, P1, P2 and P3.

Serial data buffer (SBUF) →
- internally contains 2 independent registers →
  - transmit buffer = parallel-in-serial-out register.
  - receive buffer = serial-in-parallel-out register.
- byte is written to SBUF =
  - initiates serial transmission.
- SBUF is read →
  - reads received serial data.

8051 Microcontroller

Architecture of 8051 →
Timer registers →
- two 16-bit registers.
- accessed as lower and upper bytes (TL0, TH0, TL1, TH1),
- 4 addresses are allotted in special function registers,

Control registers →
- control how certain hardware components work.
- contain control and status information for →
  - interrupts,
  - timers/counters,
  - serial port.
- IP, IE, TMOD, TCON,
- SCON = serial port mode control register,
- PCON = power control register,

8051 Microcontroller

Architecture of 8051 →

Timing and control unit →

derives all necessary timing and control signals for
internal operation of circuit,
controlling external system bus,
execution of instruction.

Oscillator →

generates basic timing clock signal,
uses crystal oscillator.

Instruction register →

decodes opcode of instruction,
gives information to timing and control unit.

EPROM and program address register →

provide on-chip EPROM and mechanism to address it.

8051 Microcontroller

Architecture of 8051 →
RAM and RAM address register →
provide internal 128 bytes of RAM and mechanism to address it.

ALU →
performs 8-bit arithmetic and logical operations.
operands are held by temporary registers TMP1 and TMP2.

SFR register bank →
set of special function registers,
addresses lie in range 80H to FFH.

Interrupt, serial port and timer units →
control and perform specific functions,
under control of timing and control unit.

8051 Microcontroller

Memory Addressing of 8051 →

Total memory is logically divided into →

1) program memory →

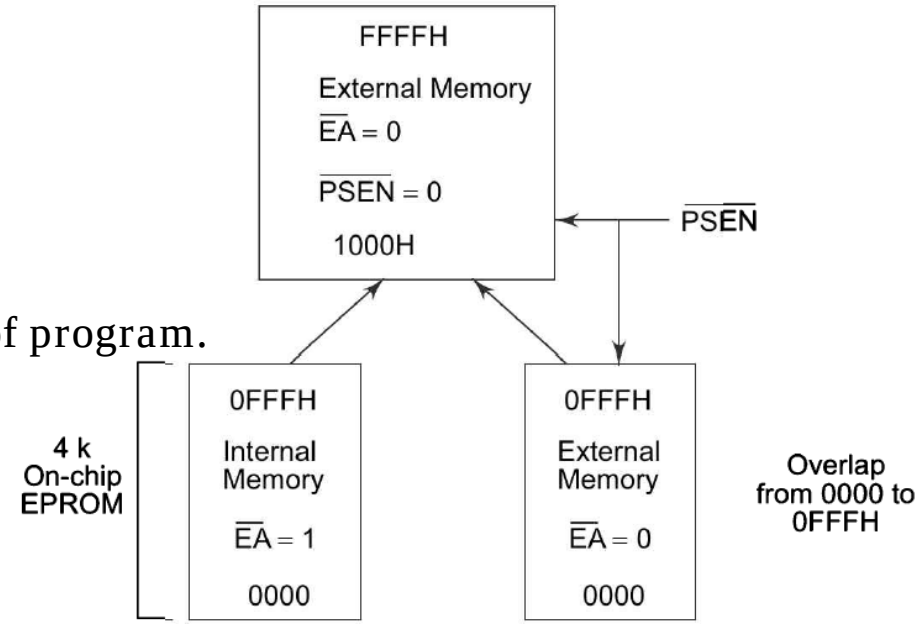
stores programs to be executed.

implemented using EPROM.

2) data memory →

stores data required for execution of program.

implemented using RAM.



Program memory categories →

1) on-chip (internal) memory →

physically exists on chip.

4K bytes can be addressed, from 0000H to 0FFFH.

2) external memory →

externally interfaced.

64K bytes can be addressed, from 0000H to FFFFH.

map of internal memory overlaps with that of external memory →

distinguished using $\overline{PSEN}$ signal.

EA: External Access

PSEN: Program Store Enable

16-bit program counter,
can address up to 2^{16} = 64 KB

8051 Microcontroller

Memory Addressing of 8051 →

Data memory categories →

1) on-chip (internal) memory →

consists of 2 parts →

a) RAM block of 128 bytes or 256 bytes.

b) set of addresses from 80H to FFH →

addresses allotted to special function registers.

2) external memory →

64K bytes can be addressed, from 0000H to FFFFH.

register DPTR stores addresses for memory access.

8051 generates $\overline{RD}$ and $\overline{WR}$ signals during memory access.

chip select line is derived from address lines.

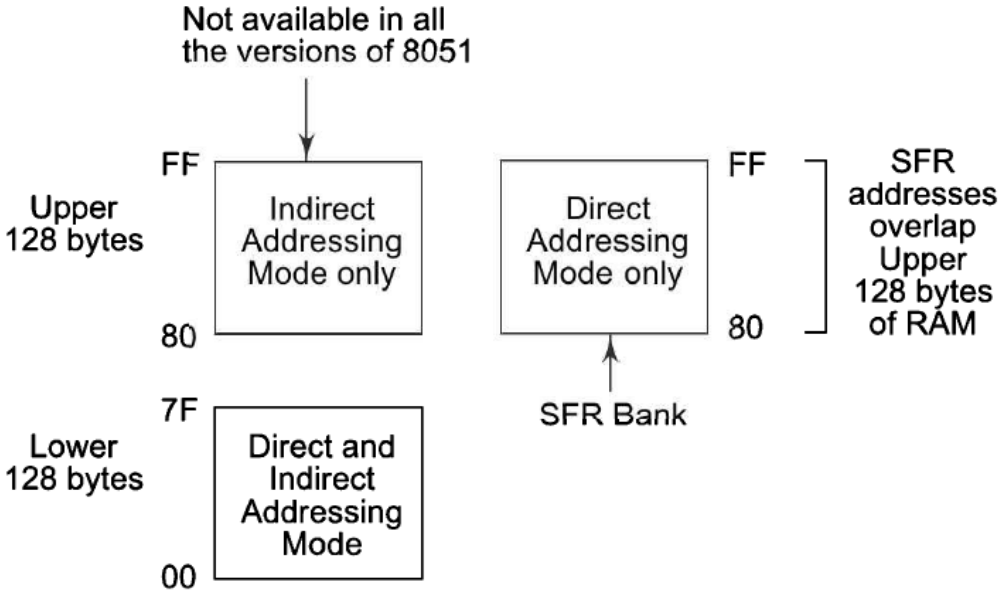
8051 Microcontroller

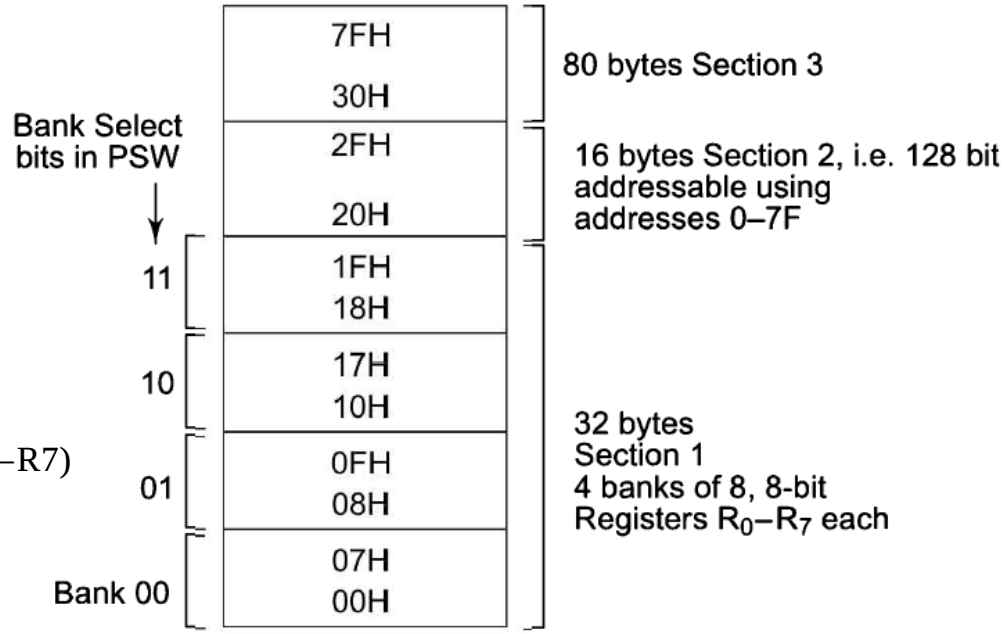
Memory Addressing of 8051 →
RAM block of 128 bytes →
- address map starts from 00H and ends at 7FH.
- addressed by using direct or indirect mode of addressing.
- special function register address map = 80H to FFH →
  - accessible only with direct addressing mode.

256 bytes version →
- map starts from 00H and ends at FFH.
  - upper 128 bytes access = indirect addressing.
  - lower 128 bytes access = direct or indirect addressing.
  - address map of special function registers = 80H to FFH.
  - SFR 128 bytes overlaps with upper 128 bytes RAM →
    - upper 128 bytes access = indirect addressing.
    - SFR 128 bytes access = direct addressing.

8051 Microcontroller

Memory Addressing of 8051 →

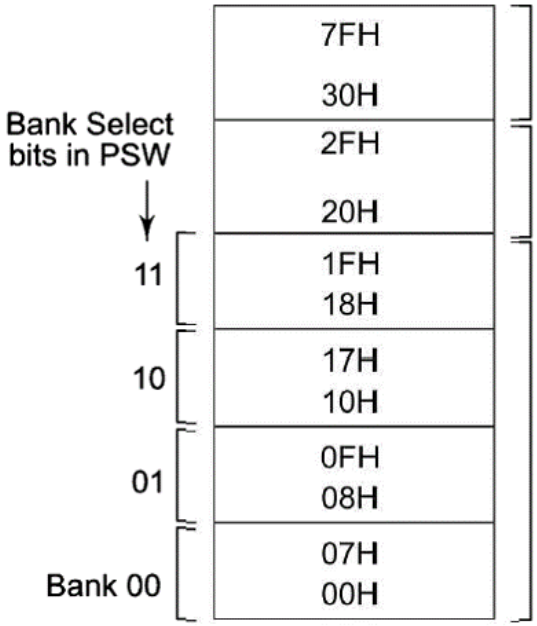




00H – 1FH: Working registers (R0–R7) and register banks
20H – 2FH: Bit-addressable RAM
30H – 7FH: General-purpose RAM

8051 Microcontroller

Memory Addressing of 8051 →
RAM block of lower 128 bytes →
address map starts from 00H and ends at 7FH.
functionally organized in 3 sections →
1) lowest 32 bytes form first section.
address block = from 00H to 1FH.
divided into 4 banks →
bank 00, 01, 10, 11.
each bank contains eight 8-bit registers.
bank 00 = reset bank, 00H to 07H.
bank 01, 10, 11 = stack pointer →
gets initialized at address 07H.
stack data is stored from 08H onwards.
bank addressing bits of register bank →
present in PSW,
select one of banks at a time.



8051 Microcontroller

Memory Addressing of 8051 →
RAM block of lower 128 bytes →
functionally organized in 3 sections →
2) second section extends from 20H to 2FH,
bit-addressable block of memory, 16×8 = 128 bits.
address of each bit = 00H to 7FH.
2 ways to access any bit →
a) number is directly mentioned in instruction.
b) bit is mentioned with its position in respective register byte.
bits 0 to 7 = 0 to 7 or 20.0 to 20.7

3) third block occupies addresses from 30H to 7FH.
byte addressable memory space.
used as stack memory.

all internal data memory locations →
accessed using 8-bit addresses,
under appropriate modes of addressing.