CSE-3103: Microprocessor and Microcontroller

Dept. of Computer Science and Engineering
University of Dhaka

Prof. Sazzad M.S. Imran, PhD
Dept. of Electrical and Electronic Engineering
sazzadmsi.webnode.com

8259A Programmable Interrupt Controller

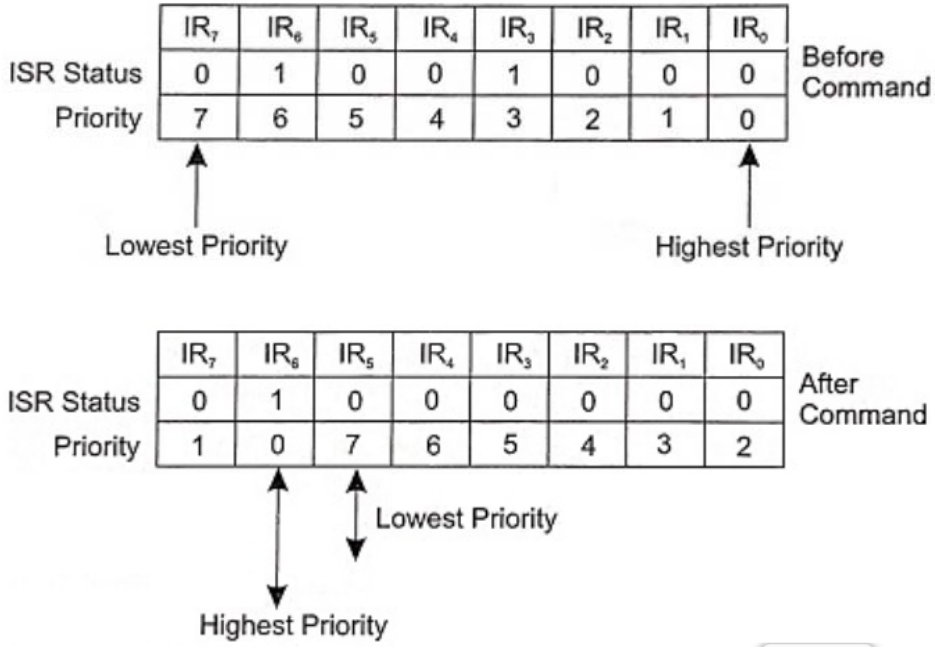
Status Register →
three 8-bit status registers are readable in 8259A.
(1) Interrupt request register →
indicates which interrupt request inputs are active.

(2) In-service register →
contains level of interrupt being serviced.

(3) Interrupt mask register →
indicates which interrupts are masked off.

IRR and ISR are read by programming OCW_3;
$A_0 = 0$; D_0 and D_1 select which register is read.

IMR is read through OCW_1;
$A_0 = 1$.



Intel 80186 Microprocessors

Intel 80186 and 80286 →

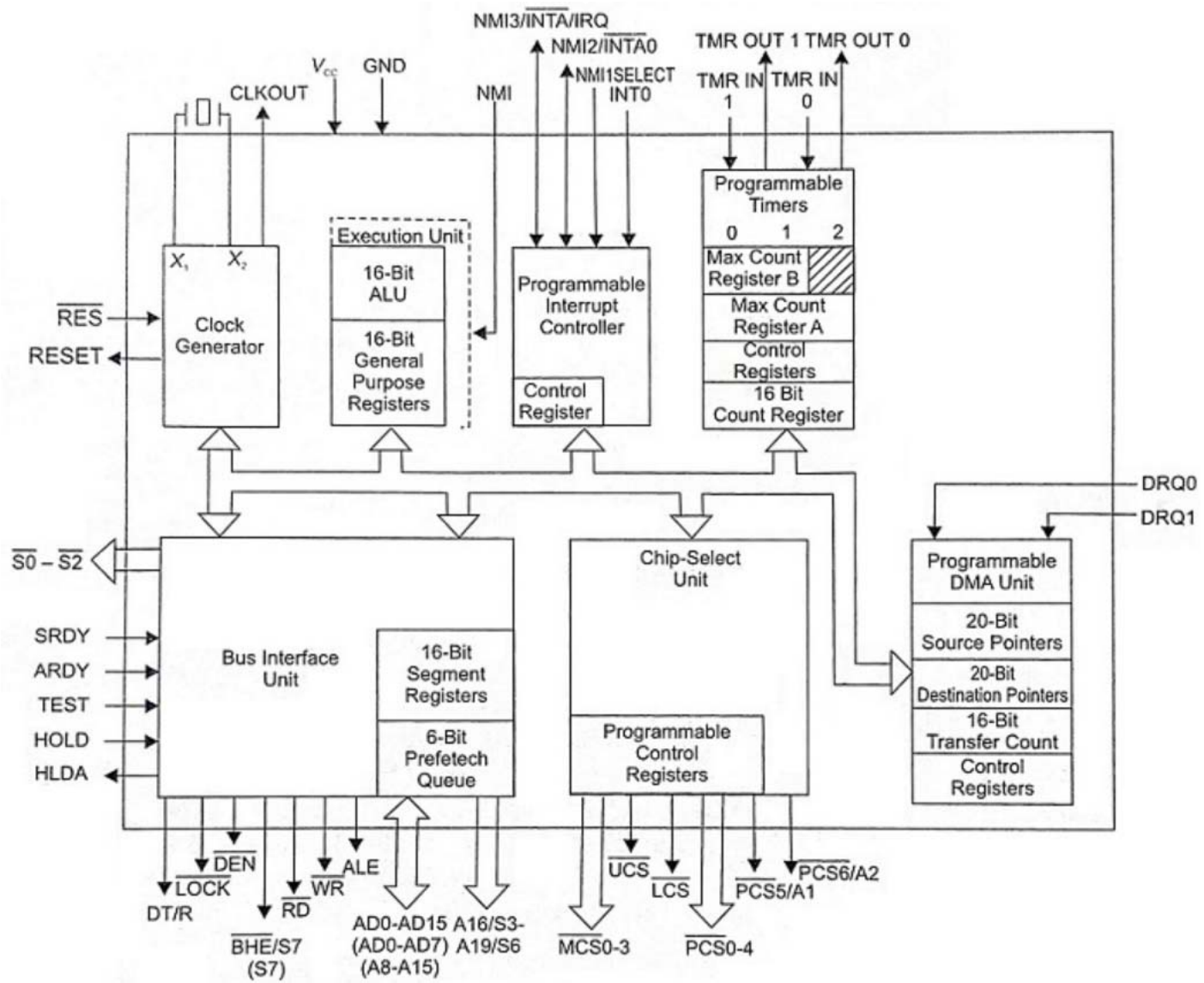
enhanced versions of 80x86 family of microprocessors.
16-bit microprocessors,
upward-compatible with 8086.
hardware is similar to earlier versions.

Intel 80186 →

16-bit data bus, 20-bit address bus.
internal register structure = 8086.
contain → additional reserved interrupt vectors,
very powerful built-in I/O features.
= embedded controllers.
versions →

80C186XL: extended temp range and enhanced speed,
80C186EA: enhanced architecture,
80C186EB: further refined,
80C186EC: enhanced, complete.

Basic block diagram of 80186 →



Intel 80186 Microprocessors

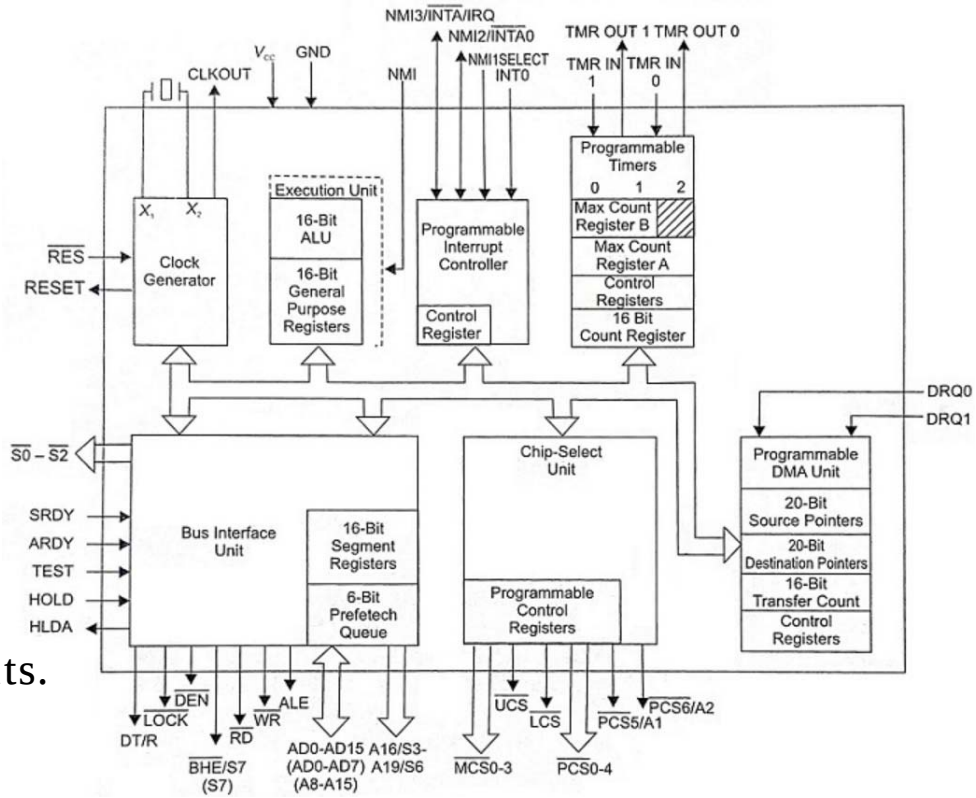
Prefetch queue = 6 bytes.

Contains →

BIU and EU,
clock generator,
programmable interrupt controller,
programmable timers,
programmable DMA controller,
programmable chip selection unit.

Enhancements benefits →

greatly increases system utility,
reduces number of peripheral components.
caching disk controllers,
LAN controllers.
cellular telephone network as switches.
software for 80186 = that of 80286.

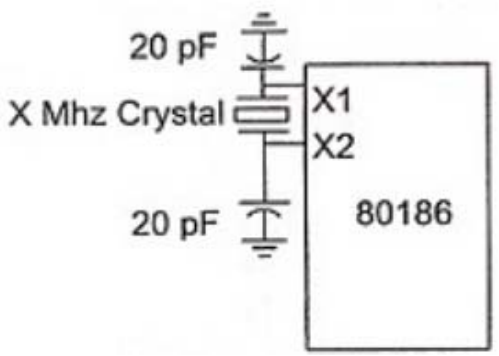


Intel 80186 Microprocessors

Basic features →

Clock Generator →

- internal clock generator replaces external 8284A clock generator.
- clock pins are connected to crystal →
  - twice operating frequency of microprocessor.
- CLKOUT pin →
  - system clock signal = ½ of crystal frequency,
  - duty cycle = 50%.



Programmable Interrupt Controller (PIC) →

- arbitrates internal and external interrupts,
- controls up up to 2 external 8259A PICs →
  - external 8259 = slave.
  - internal PIC = master.
- without external 8259 →
  - 5 interrupt inputs: INT0 to INT3, NMI.

Intel 80186 Microprocessors

Basic features →

Timers →

contains 3 fully programmable l6-bit timers.

timers 0 and 1 →

generate waveforms for external use,

driven by either master clock of 80186 or by external clock.

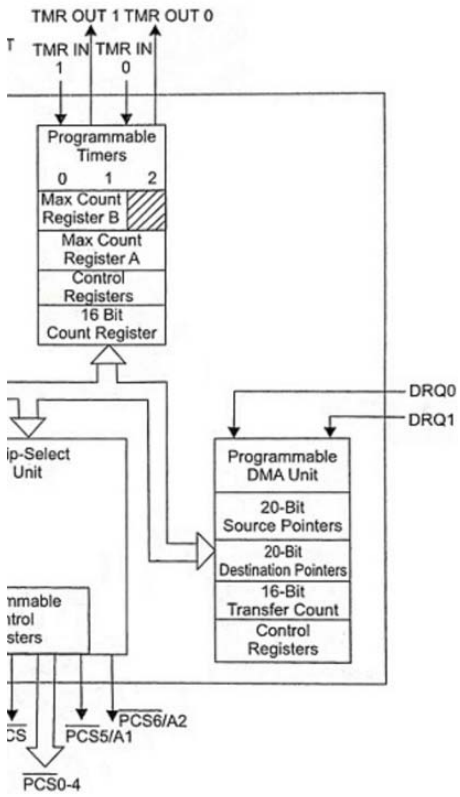
used to count external events.

timer 2 →

internal and clocked by master clock.

generates interrupt after specified number of clocks,

can provide clock to other timers.



Programmable DMA Unit →

contains 2 DMA channels.

each channel can transfer data between →

memory locations,

memory and I/O,

I/O devices.

Intel 80186 Microprocessors

Basic features →

Programmable Chip Selection Unit →

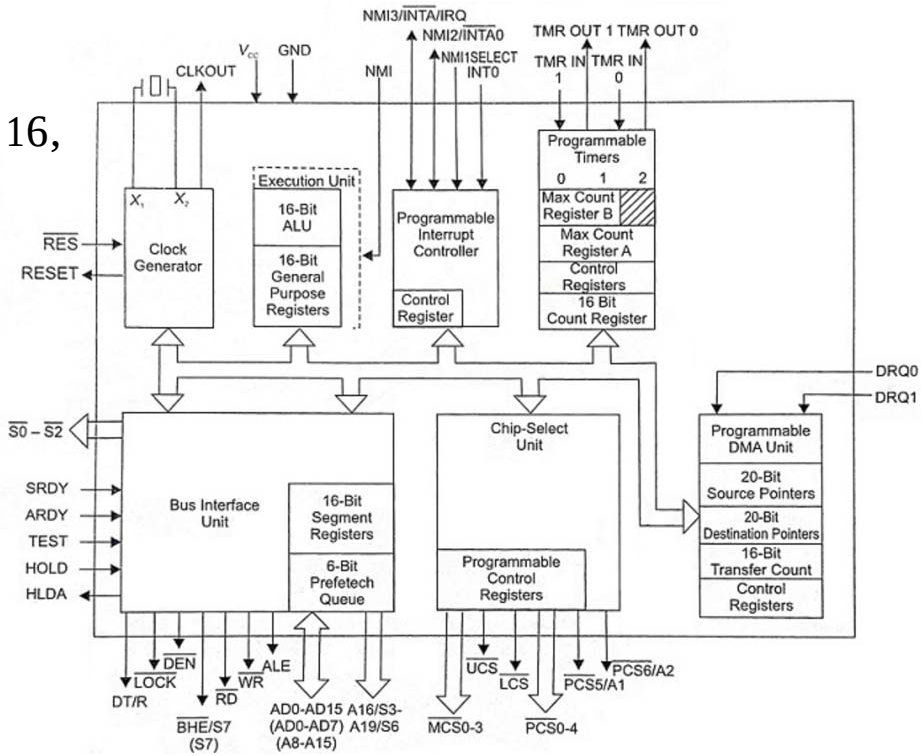
= built-in programmable memory and I/O address decoder.
6 output lines to select memory,
7 lines to select I/O.

Power Save Feature →

allows system clock to be divided by 4, 8, or 16,
reduce power consumption.
started by software,
exited by interrupt.

Power Down Feature →

stops clock completely,
entered by execution of HLT instruction,
exited by any interrupt.



Intel 80186 Microprocessors

Basic features →

Refresh Control Unit →

- automatically refreshes dynamic RAM (DRAM).
- generates refresh row address at interval programmed.
- refresh address + control signal is provided to memory system.
- memory system runs refresh cycle during active time of control signal.

Peripheral Control Block (PCB) →

- set of 256 registers located in I/O or memory space.
- 16-bit-wide registers control all internal peripherals.
- 80186 is reset →
  - PCB is automatically located at top of I/O map,
  - I/O addresses = FF00H–FFFFH.
- PCB may be relocated at any time to any other area of memory or I/O.
- relocation →
  - changing contents of relocation register,
  - offset addresses = FEH and FFH.

Intel 80186 Microprocessors

Basic features →

Interrupts in 80186 →

interrupts in 80186 = interrupts in 8086,

additional interrupt vectors →

some of internal devices.

array BOUND, unused opcode, ESC opcode, ... etc.

Intel 80286 Microprocessors

Features →

= iAPX 286 (Intel Advanced Performance Architecture),
x86 16-bit microprocessor with 134,000 transistors.
clock frequency = 6 MHz (0.9 MIPS), 8 MHz (1.5 MIPS), 12.5 MHz (1.8 MIPS).
16-bit data bus, 16-bit internal register.
24-bit address bus →
able to address up to 16 MB of memory.

can run →
multitasking applications,
digital communications,
real-time process control systems,
multi-user systems.

no on-chip clock generator circuit.
external 82284 chip →
generates external clock.
clock is divided by 2 internally to generate internal clock.
provides 80286 RESET and READY signals.

Intel 80286 Microprocessors

Features →

1st x86 processor to operate in protected mode.
operates in two different modes →
real mode and protected mode.

real mode →
compatibility with existing 8086 software base,
80286 is booted in real mode,
not possible to switch it from protected mode to real mode.

protected mode →
enhanced system level features.
memory management: 24-bit address, access up to 16 MB memory,
multitasking: run multiple programs safely,
protection: protect each program from interfering with others.

Intel 80386 Microprocessors

Features →

- manufactured by Intel using 0.8-micron CHMOS technology.
- 32-bit microprocessor =
  - 32-bit internal and external data bus,
  - 32-bit registers.
- support 8-bit, 16-bit, 32-bit operands.
- 32-bit address bus →
  - can address up to 4 GB of physical memory.
- physical memory →
  - organized in segments,
  - segment size = 4 GB maximum.
  - support 16k number of segments,
  - total virtual memory space = 4 GB × 16k = 64 TB.
- 16-byte prefetch queue.
- clock speeds = 16 MHz to 33 MHz.
- operates in →
  - real, protected and virtual real mode.

Intel 80386 Microprocessors

Features →

memory management unit (MMU) =

responsible for handling memory addresses.

1) segmentation unit →

gives protection to data or code present in memory.

provides 4 privilege levels (or protection rings) →

highest: operating system kernel,

high: device drivers,

medium: system utilities,

lowest: user applications

2) paging unit →

operates only in protected mode,

changes linear address into physical address.

provides virtual memory and memory isolation.

instruction set is upward compatible.

supports Intel 80387 numeric data processor.