CSE-3103: Microprocessor and Microcontroller

Dept. of Computer Science and Engineering
University of Dhaka

Prof. Sazzad M.S. Imran, PhD
Dept. of Electrical and Electronic Engineering
sazzadmsi.webnode.com

8259A Programmable Interrupt Controller

Problem without 8259A PIC →

only 1 hardware interrupt input (INTR),

multiple external devices have to share same INTR line.

CPU cannot tell →

which device is requesting interrupt?

what priority to serve first?

no automatic vector number generation.

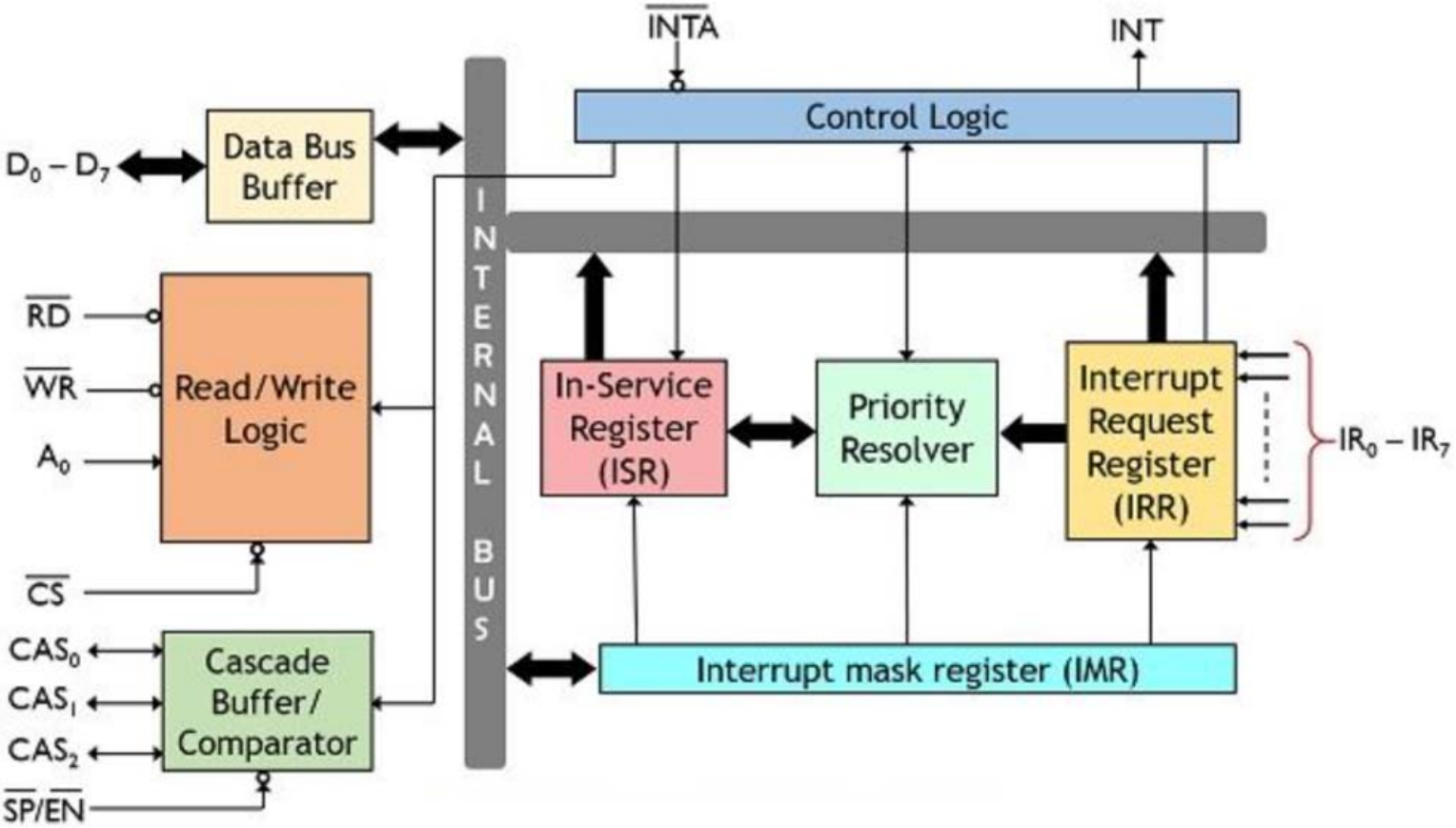
Solution →

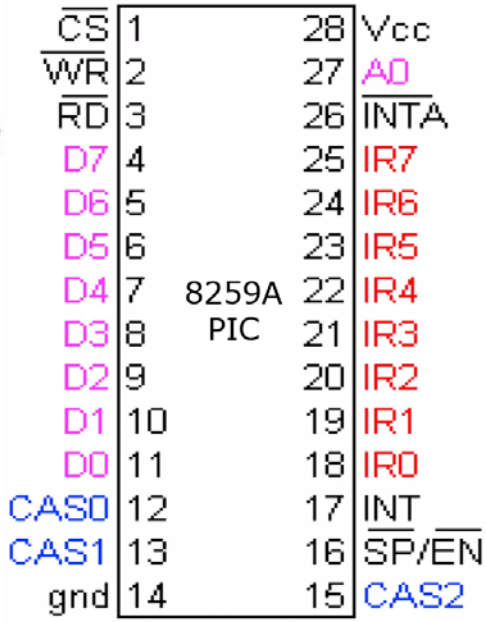
1) using extra hardware or complex software to mask specific devices.

2) poll all devices to find out who requested service.

3) using 8259A PIC as interrupt manager between CPU and peripheral devices.

8259A Programmable Interrupt Controller





8259A Programmable Interrupt Controller

8259A PIC →

adds 8 vectored priority encoded interrupts to microprocessor.
can be expanded to accept up to 64 interrupt requests.
expansion requires →

1) one master 8259A and
2) eight 8259A slaves.

IR_0-IR_7 →

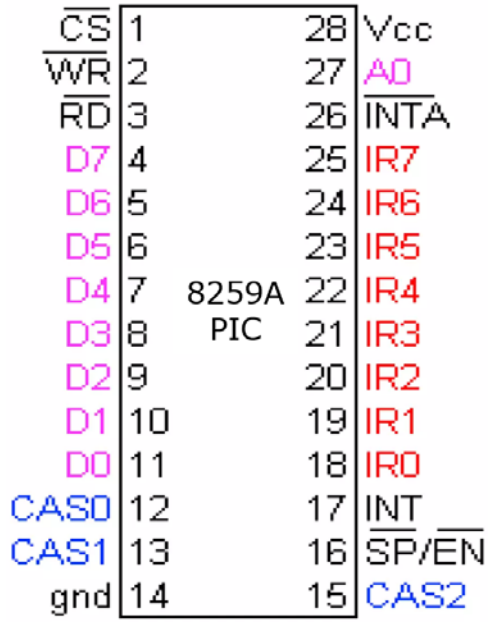
receive interrupt request from peripherals or slaves.
can be individually masked by software.
default = IR_0 has highest priority, IR_7 has lowest.
can be rotated.

IRR (interrupt request register) →

stores interrupt requests generated by peripheral devices.

INT →

master = connects to CPU's INTR pin,
slave = connects to master IR pin.



8259A Programmable Interrupt Controller

$\overline{\text{INTA}}$ →

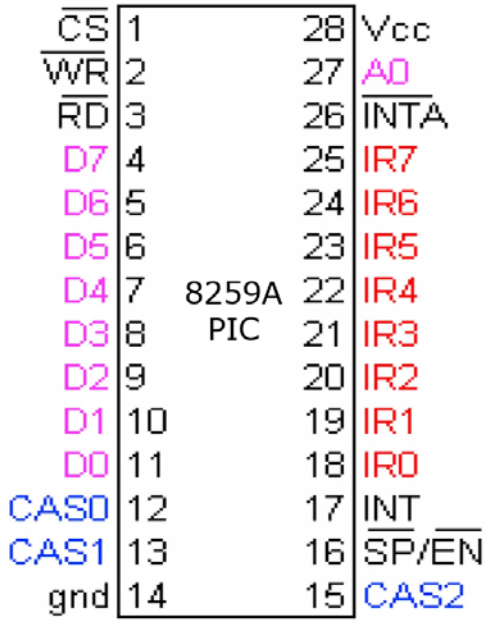
connects to $\overline{\text{INTA}}$ signal on system.
only master $\overline{\text{INTA}}$ signal is connected.
CPU sends 2 acknowledge pulses →
1st pulse = 8259A identifies which device caused interrupt.
2nd pulse = 8259A places interrupt vector number on data bus.

SP/$\overline{\text{EN}}$ →

= slave program/enable buffer,
dual-function pin →
1) buffered mode →
controls data bus transceivers.
2) not in buffered mode →
programs device as master (1) or slave (0).

In-Service Register →

stores interrupts which are currently being executed by processor.



8259A Programmable Interrupt Controller

A_0 →

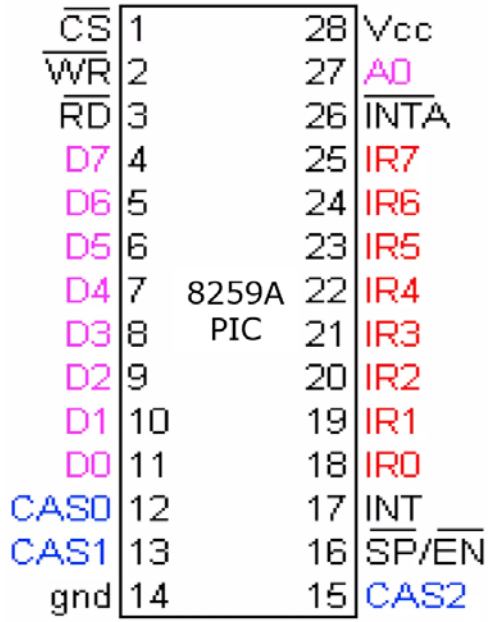
= address line,
selects which internal register is being accessed →
0 for command register.
1 for data register.

D_0-D_7 →

bidirectional data bus lines,
exchange with CPU →
command words, status, mask bits,
interrupt type numbers.

CAS_0-CAS_2 →

used for cascading multiple 8259A PICs,
allows comparison of IDs of different 8259As cascaded.
identify which slave issued interrupt.
master's CAS pins (output) are connected in parallel to CAS pins (input) of all slaves.



8259A Programmable Interrupt Controller

8259A is programmed by →

1) initialization command words →

programmed before 8259A is able to function,
define basic configuration of 8259A.

2) operation command words →

programmed during normal operation,
control and modify operation of 8259A.

Initialization Command Words (ICW) →

$A_0 = 0$ →

4 ICWs are selected.

8259A is first powered up →

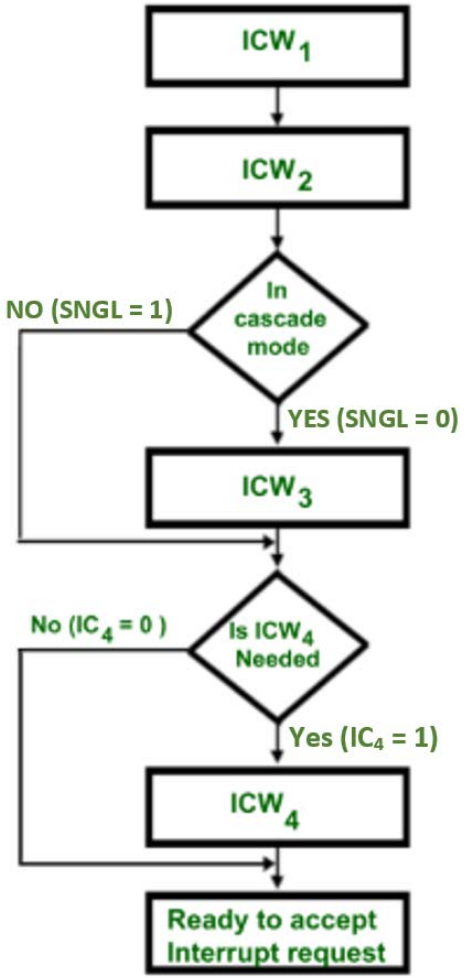
it must be sent ICW_1 and ICW_2.

8259A is programmed in cascade mode by ICW_1 →

we must program ICW_3.

ICW_4 is needed →

must be specified in ICW_1.



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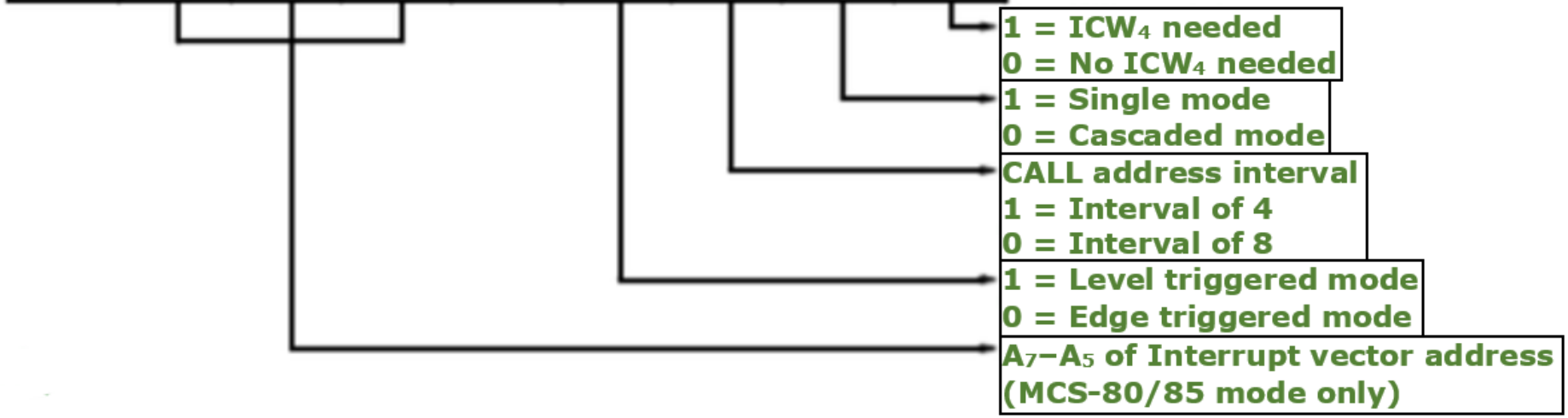
Initialization Command Words (ICW) →

ICW_1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LTIM	ADI	SNGL	IC_4



8259A Programmable Interrupt Controller

Initialization Command Words (ICW) →

ICW_1 →

programs basic operation of 8259A.

to program ICW_4, place logic 1 in bit IC_4.

bits ADI, A_7, A_6 and A_5 →

don't cares for 8086 – Pentium 4 microprocessors.

used with 8085 microprocessor.

SNGL bit →

selects single or cascade operation.

cascade is selected = we must program ICW_3.

LTIM bit →

determines whether interrupt request inputs are positive edge-triggered or level-triggered.

ICW_2 →

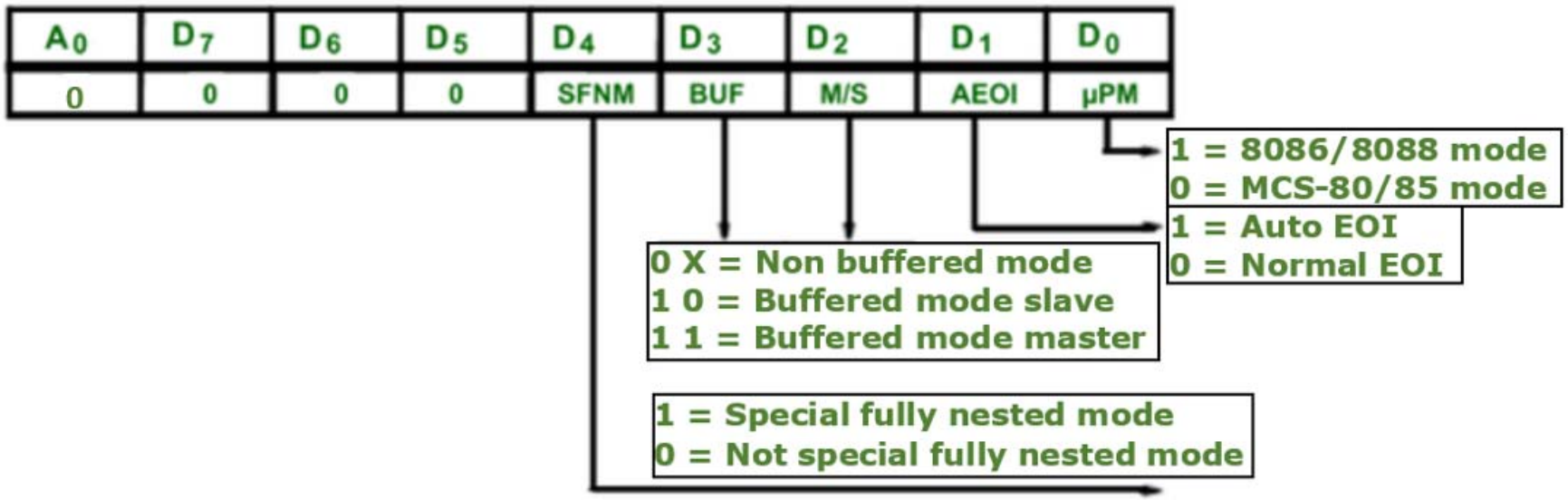
selects vector number used with interrupt request inputs.

8259A Programmable Interrupt Controller

Initialization Command Words (ICW) →

ICW4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	SFNM	BUF	M/S	AEOI	µPM



8259A Programmable Interrupt Controller

Initialization Command Words (ICW) →

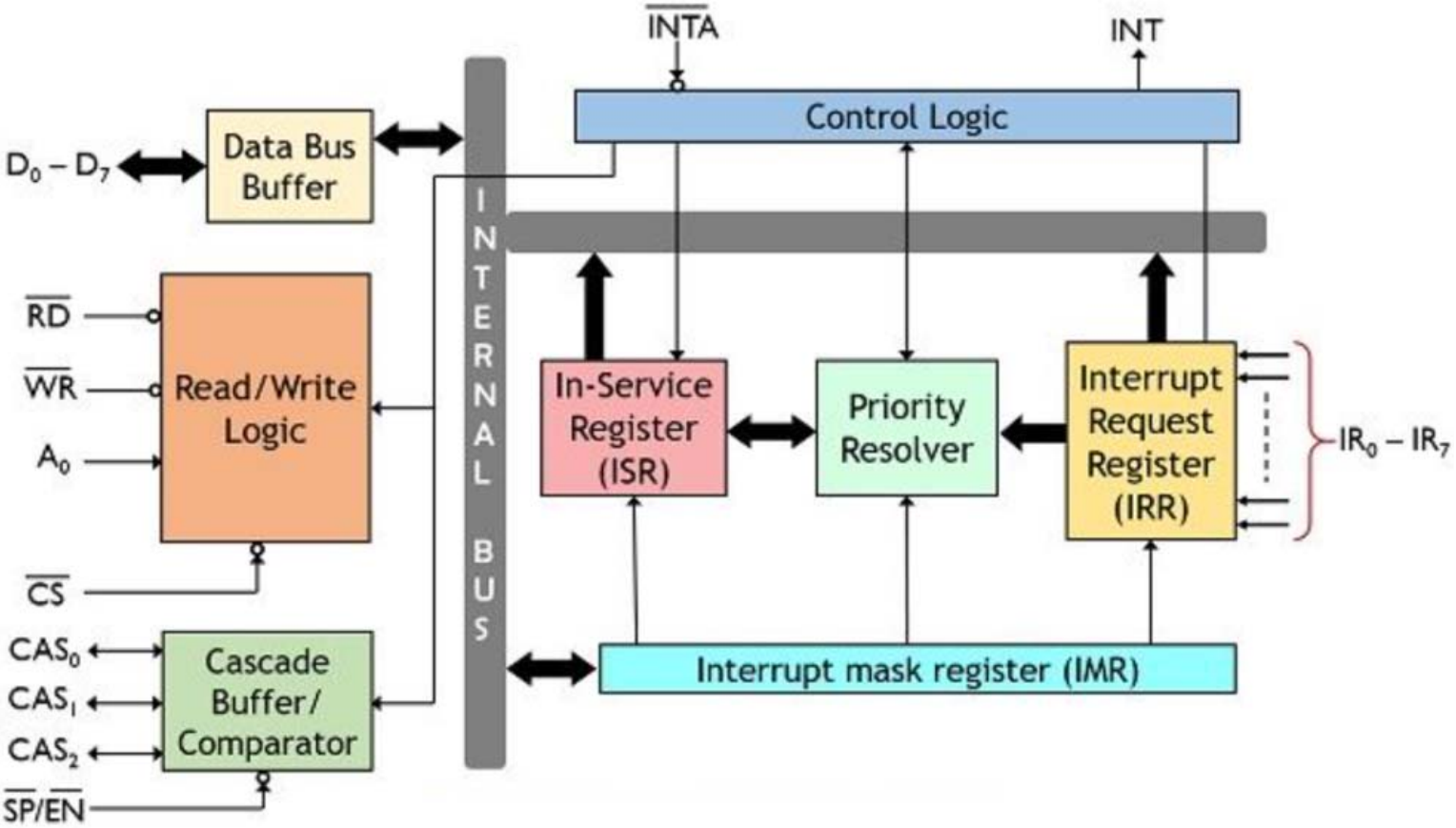
ICW_3 →

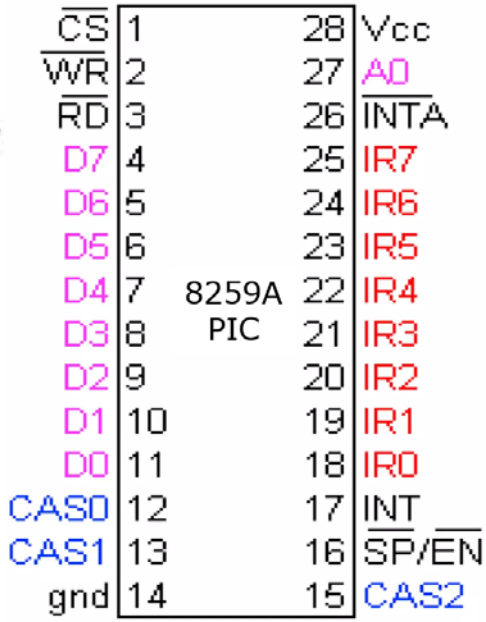
used when ICW_1 indicates = system is operated in cascade mode.
indicates where slave is connected to master.

ICW_4 →

programmed for use with 8086 – Pentium 4 microprocessors.
rightmost bit must be logic 1 to select operation.
SFNM →
allows highest priority interrupt request from slave,
request is recognized by master,
while master is processing another interrupt from slave.
BUF and M/S →
select buffered or nonbuffered operation as master or slave.
AEOI →
selects automatic or normal end of interrupt.
AEOI is selected →
interrupt automatically resets interrupt request bit,
does not modify priority.

8259A Programmable Interrupt Controller





8259A Programmable Interrupt Controller

Operation Command Words (OCW) →

direct operation of 8259A.

OCW_1 is selected when $A_0 = 1$.

OCW_2 and OCW_3 is selected when $A_0 = 0$.

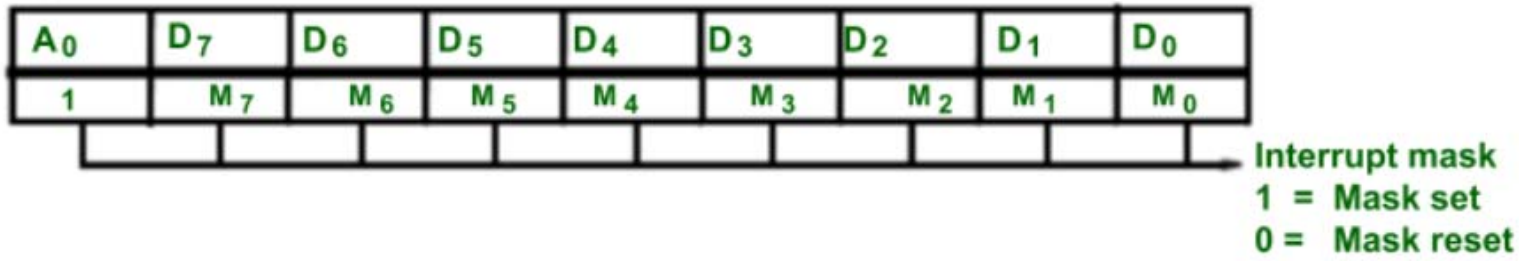
OCW_1 →

set and read interrupt mask register (IMR).

mask bit is set = turn off corresponding interrupt input.

mask register is read when OCW_1 is read.

OCW_1



8259A Programmable Interrupt Controller

Operation Command Words (OCW) →

OCW_2 →

OCW_2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	R	SL	EOI	0	0	L_2	L_1	L_0

programmed when AEOI mode (in ICW_4) is not selected.
selects way 8259A responds to interrupt.
Nonspecific End-of-Interrupt →
command sent by ISP to signal EOI.
automatically determines which interrupt level was active,
resets interrupt status register →
interrupt to take action again or
lower priority interrupt to take effect.
Specific End-of-Interrupt →
programmer specifies which interrupt line is to be cleared.
position is determined with bits L_2-L_0.

8259A Programmable Interrupt Controller

Operation Command Words (OCW) →

OCW_2 →

OCW_2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	R	SL	EOI	0	0	L_2	L_1	L_0

Rotate-on-Nonspecific EOI →

functions exactly like Nonspecific EOI.

rotates interrupt priorities after resetting interrupt status register.

level reset by this command = lowest priority interrupt.

Rotate-on-Specific EOI →

functions as specific EOI,

selects rotating priority.

Rotate-on-Automatic EOI →

selects automatic EOI with rotating priority.

CLEAR command is used to turn off this mode.

Set priority →

programmer sets lowest priority interrupt input using L_2-L_0 bits.

8259A Programmable Interrupt Controller

Operation Command Words (OCW) →

OCW_3 →

selects which internal register is accessed when read from PIC.

controls whether PIC will enter poll mode.

P = 1 →

CPU performs read operation from 8259A.

PIC responds with 8-bit poll word.

Poll word →

Bit 7	1 = valid interrupt request pending. 0 = no pending interrupt
Bits 6-3	Unused in poll word.
Bits 2-0	Indicates which IR input (IR_0-IR_7) has highest priority active request.

Poll mode →

CPU asks PIC directly (via software), whether any device is requesting interrupt, without using INT line.