Simple Digital I/O in C

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Digital Input/Output (I/O) Ports

- The digital I/O features include:
  - Independently programmable individual I/Os
  - Any combination of input or output
  - Individually configurable P1 and P2 interrupts.
    - Some devices may include additional port interrupts.
  - Independent input and output data registers
  - Individually configurable pullup or pulldown resistors

Digital Input/Output (I/O) Ports

- Devices within the family may have up to twelve digital I/O ports implemented (P1 to P11 and PJ). Most ports contain eight I/O lines; however, some ports may contain less. Each I/O line is individually configurable for input or output direction, and each can be individually read or written. Each I/O line is individually configurable for pullup or pulldown resistors.

- Ports P1 and P2 always have interrupt capability. Each interrupt for the P1 and P2 I/O lines can be individually enabled and configured to provide an interrupt on a rising or falling edge of an input signal. All P1 I/O lines source a single interrupt vector (P1IV), and all P2 I/O lines source a different single interrupt vector (P2IV). Additional ports with interrupt capability may be available and contain their own respective interrupt vectors.

- On the MSP430FR5739 Ports P1, P2, P3 and P4 can operate as an interrupt.

Digital Input/Output (I/O) Ports

- Individual ports can be accessed as byte-wide ports or can be combined into word-wide ports and accessed by word formats. Port pairs P1 and P2, P3 and P4, P5 and P6, P7 and P8, and so on, are associated with the names PA, PB, PC, PD, and so on, respectively.
  - All port registers are handled in this manner with this naming convention except for the interrupt vector registers, P1IV and P2IV; that is, PAIV does not exist.
- When writing to port PA with word operations, all 16 bits are written to the port. When writing to the lower byte of port PA using byte operations, the upper byte remains unchanged. Similarly, writing to the upper byte of port PA using byte instructions leaves the lower byte unchanged.
  - When writing to a port that contains less than the maximum number of bits possible, the unused bits are don't care.
  - Ports PB, PC, PD, PE, and PF behave similarly.
- Reading port PA using word operations causes all 16 bits to be transferred to the destination. Reading the lower or upper byte of port PA (P1 or P2) and storing to memory using byte operations causes only the lower or upper byte to be transferred to the destination, respectively. Reading of port PA and storing to a general-purpose register using byte operations writes the byte that is transferred to the least significant byte of the register. The upper significant byte of the destination register is cleared automatically.
- When reading from ports that contain fewer than the maximum bits possible, unused bits are read as zeros (similarly for port PJ).

Digital I/O Operation

- **Input Registers (PxIN)**
  - Each bit in each PxIN register reflects the value of the input signal at the corresponding I/O pin when the pin is configured as I/O function. These registers are read only.
    - Bit = 0: Input is low
    - Bit = 1: Input is high
  - ***NOTE: Writing to read-only registers PxIN***
    - Writing to these read-only registers results in increased current consumption while the write attempt is active.

Digital I/O Operation

- **Output Registers (PxOUT)**
  - Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction.
    - Bit = 0: Output is low
    - Bit = 1: Output is high
  - If the pin is configured as I/O function, input direction and the pullup or pulldown resistor are enabled; the corresponding bit in the PxOUT register selects pullup or pulldown.
    - Bit = 0: Pin is pulled down
    - Bit = 1: Pin is pulled up

Digital I/O Operation

- **Direction Registers (PxDIR)**
  - Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function.
    - Bit = 0: Port pin is switched to input direction
    - Bit = 1: Port pin is switched to output direction

Digital I/O Operation

- **Pullup or Pulldown Resistor Enable Registers (PxREN)**
  - Each bit in each PxREN register enables or disables the pullup or pulldown resistor of the corresponding I/O pin. The corresponding bit in the PxOUT register selects if the pin contains a pullup or pulldown.
    - Bit = 0: Pullup or pulldown resistor disabled
    - Bit = 1: Pullup or pulldown resistor enabled

Summary of the use of PxDIR, PxREN, and PxOUT for proper I/O configuration.

I/O Configuration

PxDIR	PxREN	PxOUT	I/O Configuration
0	0	x	Input
0	1	0	Input with pulldown resistor
0	1	1	Input with pullup resistor
1	x	x	Output

Digital I/O Operation

- **Function Select Registers (PxSEL0, PxSEL1)**
  - Port pins are often multiplexed with other peripheral module functions.
  - Each port pin uses two bits to select the pin function – I/O port or one of the three possible peripheral module function. The Table below shows how to select the various module functions.
  - See the device-specific data sheet to determine pin functions.
  - Each PxSEL bit is used to select the pin function – I/O port or peripheral module function.

I/O Function Selection

PxSEL1	PxSEL0	I/O Function
0	0	General purpose I/O is selected
0	1	Primary module function is selected
1	0	Secondary module function is selected
1	1	Tertiary module function is selected

Digital I/O Operation

- **Function Select Registers (PxSEL0, PxSEL1)**
  - Setting the PxSEL1 or PxSEL0 bits to a module function does not automatically set the pin direction.
  - Other peripheral module functions may require the PxDIR bits to be configured according to the direction needed for the module function.
  - When a port pin is selected as an input to peripheral modules, the input signal to those peripheral modules is a latched representation of the signal at the device pin.
  - While PxSEL1 and PxSEL0 is other than 00 [Alternate function selected], the internal input signal follows the signal at the pin for all connected modules.
  - However, if PxSEL1 and PxSEL0 = 00 [GP I/O], the input to the peripherals maintain the value of the input signal at the device pin before the PxSEL1 and PxSEL0 bits were reset.

Digital I/O Operation

- **Function Select Registers (PxSEL0, PxSEL1)**
  - Because the PxSEL1 and PxSEL0 bits do not reside in contiguous addresses, changing both bits at the same time is not possible.
  - For example, an application might need to change P1.0 from general purpose I/O to the tertiary module function residing on P1.0. Initially, P1SEL1 = 00h and P1SEL0 = 00h. To change the function, it would be necessary to write both P1SEL1 = 01h and P1SEL0 = 01h. This is not possible without first passing through an intermediate configuration, and this configuration may not be desirable from an application standpoint.
  - The PxSELC complement register can be used to handle such situations. The PxSELC register always reads 0. Each set bit of the PxSELC register complements the corresponding respective bit of the PxSEL1 and PxSEL0 registers. In the example, with P1SEL1 = 00h and P1SEL0 = 00h initially, writing P1SELC = 01h causes P1SEL1 = 01h and P1SEL0 = 01h to be written simultaneously.

Digital I/O Operation

- **Function Select Registers (PxSEL0, PxSEL1)**
  - **Interrupts are disabled when PxSEL1 = 1 or PxSEL0 = 1**
  - When any PxSEL bit is set, the corresponding pin interrupt function is disabled. Therefore, signals on these pins do not generate interrupts, regardless of the state of the corresponding PxIE bit.

Digital I/O Operation

- **Port Interrupts**
  - At least each pin in ports P1 and P2 have interrupt capability, configured with the PxIFG, PxIE, and PxIES registers. Some devices may contain additional port interrupts besides P1 and P2.
  - All Px interrupt flags are prioritized, with PxIFG.0 being the highest, and combined to source a single interrupt vector. The highest priority enabled interrupt generates a number in the PxIV register. This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled Px interrupts do not affect the PxIV value. The PxIV registers are word access only.
  - Each PxIFG bit is the interrupt flag for its corresponding I/O pin, and the flag is set when the selected input signal edge occurs at the pin. All PxIFG interrupt flags request an interrupt when their corresponding PxIE bit and the GIE bit are set. Software can also set each PxIFG flag, providing a way to generate a software-initiated interrupt.
    - Bit = 0: No interrupt is pending
    - Bit = 1: An interrupt is pending

Digital I/O Operation

- **Port Interrupts**
  - Only transitions, not static levels, cause interrupts. If any PxIFG flag becomes set during a Px interrupt service routine or is set after the RETI instruction of a Px interrupt service routine is executed, the set PxIFG flag generates another interrupt. This ensures that each transition is acknowledged.
  - **NOTE: PxIFG flags when changing PxOUT, PxDIR, or PxREN**
    - Writing to PxOUT, PxDIR, or PxREN can result in setting the corresponding PxIFG flags.
  - Any access (read or write) of the PxIV register automatically resets the highest pending interrupt flag. If another interrupt flag is set, another interrupt is immediately generated after servicing the initial interrupt.
  - For example, assume that P1IFG.0 has the highest priority. If the P1IFG.0 and P1IFG.2 flags are set when the interrupt service routine accesses the P1IV register, P1IFG.0 is reset automatically. After the RETI instruction of the interrupt service routine is executed, the P1IFG.2 generates another interrupt.

Digital I/O Operation

- **Interrupt Edge Select Registers (PxIES)**
  - Each PxIES bit selects the interrupt edge for the corresponding I/O pin.
    - Bit = 0: Respective PxIFG flag is set on a low-to-high transition
    - Bit = 1: Respective PxIFG flag is set on a high-to-low transit
  - **NOTE: Writing to PxIES**
  - Writing to P1IES or P2IES for each corresponding I/O can result in setting the corresponding interrupt flags.

PxIES	PxIN	PxIFG
0 → 1	0	May be set
0 → 1	1	Unchanged
1 → 0	0	Unchanged
1 → 0	1	May be set

Digital I/O Operation

- **Interrupt Enable Registers (PxIE)**
  - Each PxIE bit enables the associated PxIFG interrupt flag.
    - Bit = 0: The interrupt is disabled
    - Bit = 1: The interrupt is enabled

Digital I/O Operation

- **Configuration After Reset**
  - After a reset, all port pins are configured as inputs with their module functions disabled. To prevent floating inputs, all port pins, including unused ones, should be configured according to the application needs as early as possible during the initialization procedure.
- **Configuration of Unused Port Pins**
  - To prevent a floating input and to reduce power consumption, unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PC board. The value of the PxOUT bit is don't care, because the pin is unconnected. Alternatively, the integrated pullup or pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent a floating input. See the *System Resets, Interrupts, and Operating Modes, System Control Module (SYS) chapter for termination of unused pins*.

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Digital I/O Operation

- **NOTE: Configuring port PJ and shared JTAG pins:**
  - The application should make sure that port PJ is configured properly to prevent a floating input. Because port PJ is shared with the JTAG function, floating inputs may not be noticed when in an emulation environment. Port J is initialized to high-impedance inputs by default.

- **Configuration for LPMx.5 Low-Power Modes**
  - Refer to MSP430FR57xx Family User Guide Section 8.3.3

Port Pin Electrical Characteristics

Schmitt-Trigger Inputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{\text{RST}}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		2 V	0.45		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		2 V	0.25		0.8	V
			3 V	0.30		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Inputs – Ports P1 and P2 (1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing (2)	External trigger pulse duration to set interrupt flag	2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5, $\overline{\text{RST}}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1) (2)	2 V, 3 V	-50	50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Port Pin Electrical Characteristics

Outputs – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA (1)	2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA (2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA (1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA (2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA (1)	2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA (2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA (1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA (2)		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Output Frequency – General Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.1, PJ.0 to PJ.5)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y (1) (2)	2 V		16	MHz
			3 V		24	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, or MCLK at configured output port, C_L = 20 pF, no DC loading (2)	2 V		16	MHz
			3 V		24	

(1) A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. C_L = 20 pF is connected from the output to V_{SS}.

(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Digital I/O Example

```
void Init_Port4(void){
//-------------------------------------------------------------------------
// Configure PORT 4
// Port 4 has only two pins
// Port 4 Pins
// SW1                  (0x01) // Switch 1
// SW2                  (0x02) // Switch 2
//-------------------------------------------------------------------------
  P4SEL0 = 0x00;               // P4 set as I/0
  P4SEL1 = 0x00;               // P4 set as I/0
  P4DIR = 0x00;                // Set P4 direction to input
  P4OUT = 0x00;
// SW1
  P4SEL0 &= ~SW1;              // SW1 set as I/0
  P4SEL1 &= ~SW1;              // SW1 set as I/0
  P4OUT |= SW1;                // Configure pullup resistor
  P4DIR &= ~SW1;               // Direction = input
  P4REN |= SW1;                // Enable pullup resistor
  P4IES |= SW1;                // SW1 Hi/Lo edge interrupt
// SW2
  P4SEL0 &= ~SW2;              // SW2 set as I/0
  P4SEL1 &= ~SW2;              // SW2 set as I/0
  P4OUT |= SW2;                // Configure pullup resistor
  P4DIR &= ~SW2;               // Direction = input
  P4REN |= SW2;                // Enable pullup resistor
  P4IES |= SW2;                // SW2 Hi/Lo edge interrupt
//-------------------------------------------------------------------------
}
```