Question	Answer
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Test 3

Name_____

You are permitted 75 minutes to take this test. This is a closed book, closed notes test. You are allowed the following items for the test: calculators, pencils, pens, and erasers. You are not permitted to have a computer or other electronic assistance.

There are 25 questions. Each question is valued at 4 points each. You receive 1 bonus point if your name is on all pages of the test. All answers must be on this answer sheet.

Please read and sign this statement: I have not received assistance from anyone nor assisted others while taking this test. I have also notified the test proctor of any violations of the above conditions.

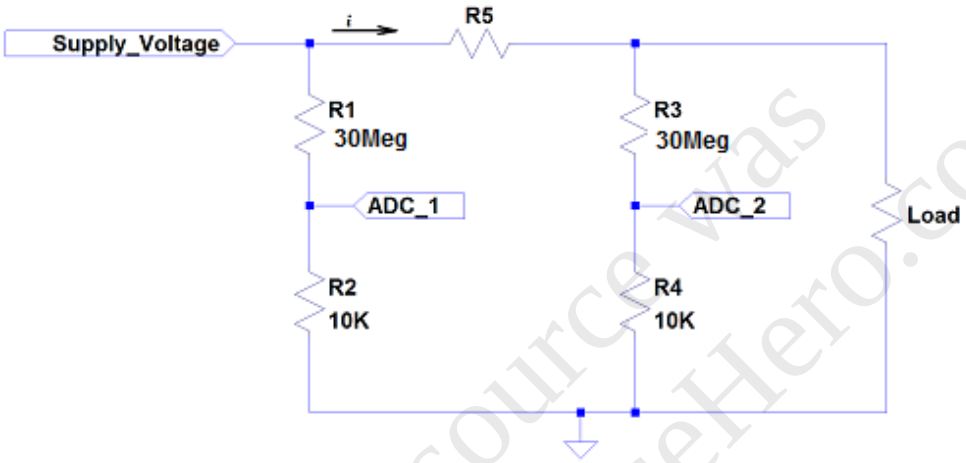
Signature _____

Name _____

In the figure the High Voltage Industrial Monitor is used to trigger abnormal load conditions. The ADC_1 and ADC_2 are inputs into a microcontroller's 16 bit analog to digital converter. The microcontroller measures the voltage on either side of R5 to determine the current into the Load. With Vref+ of 5.0 volts and Vref- of 0.1v answer the questions below.

n = converted code
Vin = sampled input voltage
V+ref = upper end of input voltage range
V-ref = lower end of input voltage range
N = number of bits of resolution in ADC

$$n = \left\lfloor \frac{(V_{in} - V_{-ref})2^N}{V_{+ref} - V_{-ref}} + 1/2 \right\rfloor$$



1. What is the highest voltage measureable by ADC_1, no load?
   a. 500.0
   b. 505.0
   c. 12002
   d. 15005
2. What is the lowest voltage measureable by ADC_1, no load?
   a. 301
   b. 300.1
   c. 120
   d. 50.5

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3. What is the measurable supply voltage step, no load?

a.	0.006935	c.	0.2244
b.	0.02244	d.	0.000980

4. If the supply voltage is 450v what is the Hexadecimal value of your ADC converter at ADC_1?

a.	0x029C	c.	0xDDDD
b.	0x0026	d.	0x67EC

5. If the processor power is limited to 5.5V, at what high voltage supply value can damage occur to the processor?

a.	16000.0	c.	555.5
b.	8000	d.	16,505.5

Name _____

Consider the following set of tasks for the next few questions. Assume preemptive scheduling.

$$U = \sum_{i=1}^{n} \frac{T_i}{\tau_i}$$

$$a_0 = \sum_{j=0}^{i} T_j \qquad a_{n+1} = T_i + \sum_{j=0}^{i-1} \left\lceil \frac{a_n}{\tau_j} \right\rceil T_j$$

Task Name	Duration T_i		Period τ_i	
a	2	ms	14	ms
b	4	ms	50	ms
c	3	ms	75	ms
d	1	ms	11	ms
e	3	ms	31	ms
f	5	ms	30	ms
g	8	ms	100	ms

6. What is the processor utilization for task g?
   a. 0.0080
   b. 0.0800
   c. 0.2500
   d. 0.1429
7. What is the total processor utilization?
   a. 0.1429
   b. 0.2500
   c. 0.6972
   d. 0.6927
8. List the tasks in order of decreasing priority (highest to lowest) when using **rate-monotonic scheduling**.
   a. d, a,e, c, b, f, g
   b. e, d, a, c, f, b, g
   c. e, g, d, a, c, b, f
   d. d, a, f, e, b, c, g

9. When using rate-monotonic scheduling, what is the completion time of the **highest priority** task in the worst case?
   a. 3 ms
   b. 1 ms
   c. 5 ms
   d. 100 ms

Name _____

10. When using rate-monotonic scheduling, what is the completion time of the **second-highest priority** task in the worst case?

a. 23 ms
b. 4 ms
c. 14 ms
d. 13 ms

11. What is the utilization bound [$U_{Max} = m(2^{1/m} - 1)$] for a rate-monotonic-scheduled system with the seven tasks?

a. 0.7241
b. 0.7348
c. 0.7286
d. 0.7435

Using the Exact Schedulability Test, how does the lowest priority task stack up?

12. Is the task schedulable?

a. always schedulable
b. Inconclusive
c. Not schedulable
d. Does not matter

13. Is the task set guaranteed to be schedulable with rate monotonic scheduling?

a. always schedulable
b. Inconclusive
c. Not schedulable
d. Does not matter

Consider the Run-to-Completion Scheduler for the following three questions.

14. Can a high priority task preempt a lower priority task?

a. Yes
b. Unknown
c. No
d. Depends on time

15. Can an interrupt service routine preempt a task?

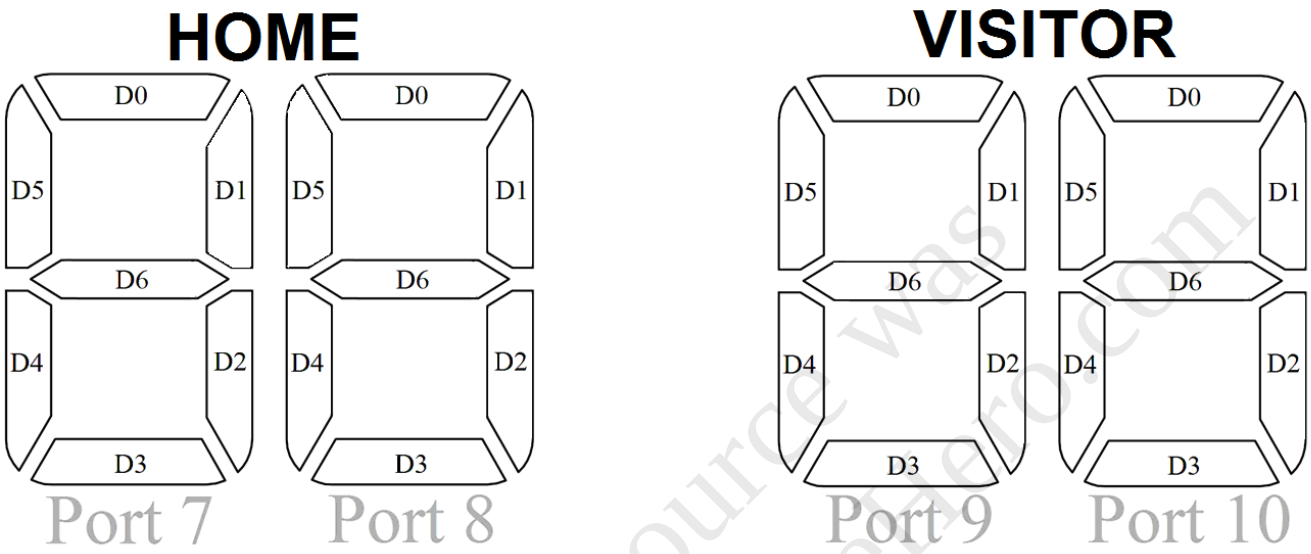
a. Depends on time
b. Unknown
c. No
d. Yes

16. Consider the situation in which a low priority task (T2) is running but is interrupted. As the ISR runs, two more tasks (T1: higher priority, T3: lower priority) become ready to run. After the ISR executes its REIT (return from interrupt) instruction, which code runs?

a. T1
b. T2
c. T3
d. T4

Name _____

You have been given a task to develop a score board for Carolina to keep patrons reminded of the score when they leave their seats for consessions. In the most recent game in this once rivalry game [to have a rival each must occasionnaly win] NC State was AGAIN victorious. The final score was NC State 29, UNC 25; as a suggestion color in the appropriate segments below. You have defined an unsigned integer, home and an unsigned integer visitors to store the 16 bit value; 8 bits for tens digit and 8 bits for ones digit. You have mapped the upper byte of each to the tens digit and the lower byte to the ones digit. The data is stored in Seven Segment code with the segments identified below.



17. What is the unsigned integer value for home? 01011011 01101101

a. 0x2529
b. 0x2925
c. 0x6D07
d. 0x5B6D

18. What is the unsigned integer value for visitors? 01011011 01100111

a. 0x2529
b. 0x5B67
c. 0x5B6D
d. 0x5B69

19. Could this be developed and implemented with a QSK board?

a. Yes
b. no

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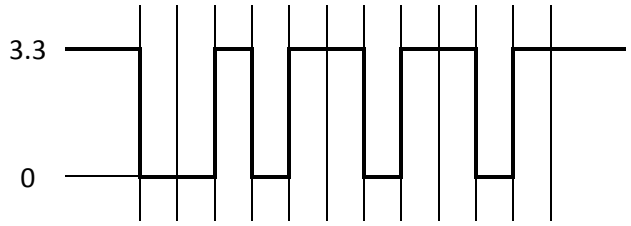
The serial stream sends the shots on goal in a binary coded decimal. It transmits the home score first followed by the visitor team score. In the final home game of the season, the score was Home 25, Visitors 29. The the value transmitted would be 0x25 0x29.

20. From the UNC – NC State game, select the pattern for the UNC team transmission. 8 bits, 1 stop bit even parity

0x25 ➔ 0010 0101 ➔ 1010 0100

a



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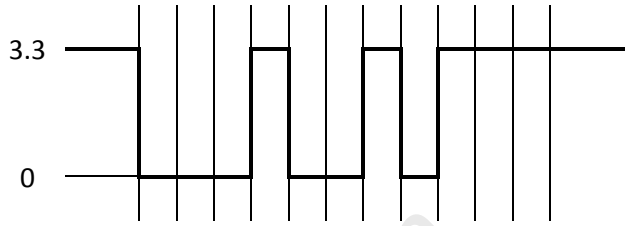

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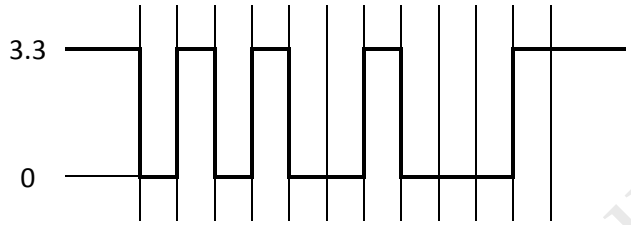

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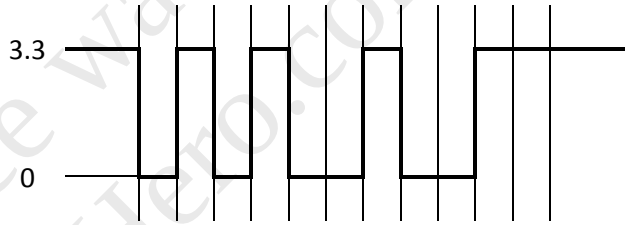
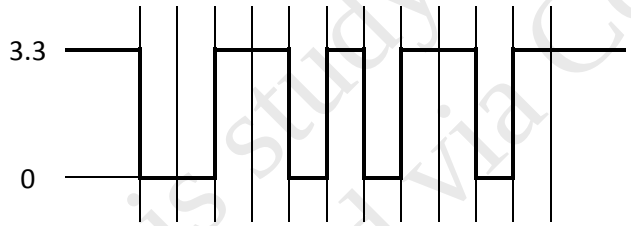


21. From the UNC – NC State game, select the pattern for the NC State team transmission. 8 bits, 1 stop bit even parity

0x29 ➔ 0010 1001 ➔ 1001 0100

a



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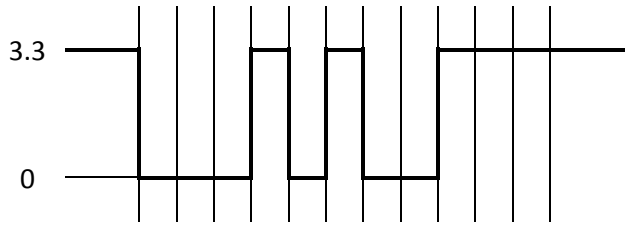

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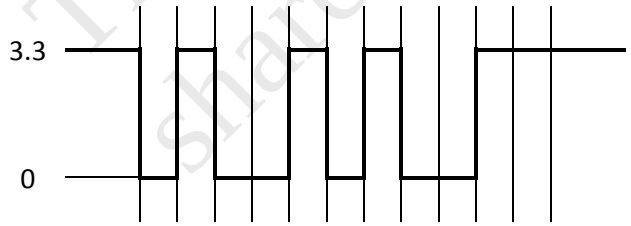

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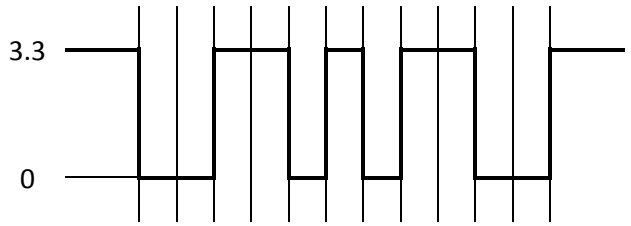

22. In order to safely switch contexts between threads, must all the M16C registers R0 through R3 saved and restored?

a. Yes
b. It is a don't care
c. No
d. Unknown

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23. If the structure of your code is to run one task sequentially after the next then returning to the first repeating the sequence after all tasks have run, what type operating system have you employed?

    a. Round Robin
    b. Square Chicken
    c. Foreground / Background
    d. Run –to-Completion

24. What happens if the watchdog timer on the MCU on your QSK26A expires?

    a. It changes a status bit to let the program know that it expired.
    b. The processor executes the watchdog timer ISR, assuming interrupts are enabled.
    c. The processor executes the watchdog timer ISR, regardless of whether interrupts are enabled or not.
    d. Nothing happens.

For the next question, consider a microcontroller which requires a supply voltage of least 2.2 V for proper RAM and register retention and at least 3.0 V for proper CPU operation. Below 3.0 V the CPU pauses and does not execute instructions.

25. Assume the supply voltage briefly (e.g. 100 us) drops to **2.5 V**. We know the address of the last instruction which finished executing before the supply voltage fell below 3.0 V. What MUST be done when the voltage returns to at least 3.0 V?

    a. Execute the reset ISR code (pointed to by the reset vector) without resetting the processor
    b. Reset the processor and execute the reset ISR code (pointed to by the reset vector).
    c. Reset the processor and then resume the program at the next instruction without executing the reset ISR code.
    d. Nothing special needs to be done. Just resume the program at the next instruction.