Power Plant - Schematics - Templates

Today

- Power Plant?
- Schematics?
- Project Write-up?

• What do we need (voltage and current)? Look at manual for voltage and current for microcontroller and other circuits

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage during program execution and FRAM prog	2.0		3.6	٧		
V _{SS}	Supply voltage (AVSS = DVSS)	upply voltage (AVSS = DVSS)					
T _A	Operating free-air temperature	-40		85	°C		
T_{J}	Operating junction temperature	-40		85	°C		
C _{VCORE}	Required capacitor at VCORE		470		nF		
C _{VCC} / C _{VCORE}	Capacitor ratio of VCC to VCORE	10					
f _{SYSTEM}		No FRAM wait states $^{(3)}$, $2 \text{ V} \leq \text{V}_{CC} \leq 3.6 \text{ V}$	0		8.0		
	Processor frequency (maximum MCLK frequency) (2)	With FRAM wait states $^{(3)}$, NACCESS = $\{2\}$, NPRECHG = $\{1\}$, $2 \lor 5 \lor $	0		24.0	MHz	

⁽¹⁾ It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.

⁽²⁾ Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

⁽³⁾ When using manual wait state control, see the MSP430FR57xx Family User's Guide (SLAU272) for recommended settings for common system frequencies.

• What do we need (voltage and current)? Look at manual for voltage and current for microcontroller and other circuits

Active Mode Supply Current Into V_{cc} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted) (1) (2) (3)

	EXECUTION MEMORY	V _{cc}	Frequency (f _{MCLK} = f _{SMCLK}) ⁽⁴⁾												
PARAMETER			1 MHz		4 MHz		8 MHz		16 MHz ⁽⁵⁾		20 MHz ⁽⁵⁾		24 MHz ⁽⁵⁾		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
I _{AM, FRAM_UNI} (6)	FRAM	3 V	0.27		0.58		1.0		1.53		1.9		2.2		mA
I _{AM,0%} ⁽⁷⁾	FRAM 0% cache hit ratio	3 V	0.42	0.73	1.2	1.6	2.2	2.8	2.3	2.9	2.8	3.6	3.45	4.3	
I _{AM,50%} ⁽⁷⁾ ⁽⁸⁾	FRAM 50% cache hit ratio	3 V	0.31		0.73		1.3		1.75		2.1		2.5		
I _{AM,68%} ⁽⁷⁾ ⁽⁸⁾	FRAM 66% cache hit ratio	3 V	0.27		0.58		1.0		1.55		1.9		2.2		mA
I _{AM,75%} ⁽⁷⁾ ⁽⁸⁾	FRAM 75% cache hit ratio	3 V	0.25		0.5		0.82		1.3		1.6		1.8		
I _{AM,100%} ⁽⁷⁾ ⁽⁸⁾	FRAM 100% cache hit ratio	3 V	0.2	0.43	0.3	0.55	0.42	0.8	0.73	1.15	0.88	1.3	1.0	1.5	
I _{AM, RAM} (8) (9)	RAM	3 V	0.2	0.4	0.35	0.55	0.55	0.75	1.0	1.25	1.20	1.45	1.45	1.75	mA

• What do we need (voltage and current)? Look at manual for voltage and current for microcontroller and other circuits

- All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
- Characterized with program executing typical data processing.
- (4) At MCLK frequencies above 8 MHz, the FRAM requires wait states. When wait states are required, the effective MCLK frequency, f_{MCLK,eff}, decreases. The effective MCLK frequency is also dependent on the cache hit ratio. SMCLK is not affected by the number of wait states or the cache hit ratio. The following equation can be used to compute f_{MCLK,eff}. f_{MCLK,eff,MHz} x 1 / [# of wait states x ((1 cache hit ratio percent/100)) + 1]
- (5) MSP430FR573x series only
- (6) Program and data reside entirely in FRAM. No wait states enabled. DCORSEL = 0, DCOFSELx = 3 (fDCO = 8 MHz). MCLK = SMCLK.
- (7) Program resides in FRAM. Data resides in SRAM. Average current dissipation varies with cache hit-to-miss ratio as specified. Cache hit ratio represents number cache accesses divided by the total number of FRAM accesses. For example, a 25% ratio implies one of every four accesses is from cache, the remaining are FRAM accesses.
 - For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK. No wait states enabled.
 - For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz).MCLK = SMCLK. One wait state enabled.
 - For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz).MCLK = SMCLK. Three wait states enabled.
 - For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz).MCLK = SMCLK. Three wait states enabled.
- (8) See Figure 1 for typical curves. Each characteristic equation shown in the graph is computed using the least squares method for best linear fit using the typical data shown in Active Mode Supply Current Into V_{CC} Excluding External Current. f_{ACLK} = 32786 Hz, f_{MCLK} = f_{SMCLK} at specified frequency. No peripherals active.
 - XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.
- (9) All execution is from RAM.
 - For 1, 4, and 8 MHz, DCORSEL = 0, DCOFSELx = 3 (f_{DCO} = 8 MHz). MCLK = SMCLK.
 - For 16 MHz, DCORSEL = 1, DCOFSELx = 0 (f_{DCO} = 16 MHz). MCLK = SMCLK.
 - For 20 MHz, DCORSEL = 1, DCOFSELx = 2 (f_{DCO} = 20 MHz). MCLK = SMCLK.
 - For 24 MHz, DCORSEL = 1, DCOFSELx = 3 (f_{DCO} = 24 MHz). MCLK = SMCLK.

- Where do we get the power?
- Plug into wall
 - Wall Need to drop 120 VAC to Low Voltage VDC
 - Transformer-based
 - Switching
- Use batteries
 - Battery Voltage changes with discharge
 - Conversion from variable voltage to constant voltage
 - Regulator
 - Switcher

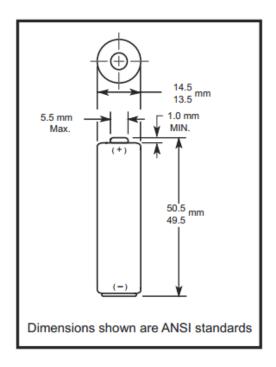
Batteries

- Battery $\equiv >1$ cell
- Cell can be modeled as ideal voltage source with a series resistance
 - Series resistance induces a voltage drop as current rises
- How long will it last?
 - Cells can be modeled as having a constant capacity (1 amp-hour
 - = 3600 coulombs = 3600 amp-seconds) (less accurate)
 - Battery life (hours) = capacity (amp-hours)/current (amps)
 - Can also predict life based on discharge plot (more accurate)
- What if voltage or current isn't right?
 - Can put cells in series (add voltages) or parallel (add currents)
 - Can use a voltage regulator (linear or switch-mode)

 A 800 mAhr battery will power a device that draws 200mA for how long?
 800 mAhr / 200mA = 4 hr

• What is the voltage of a "AA" battery?

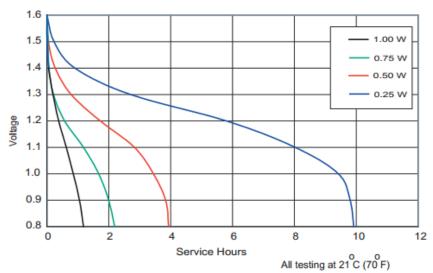
• What is the current capabilities?



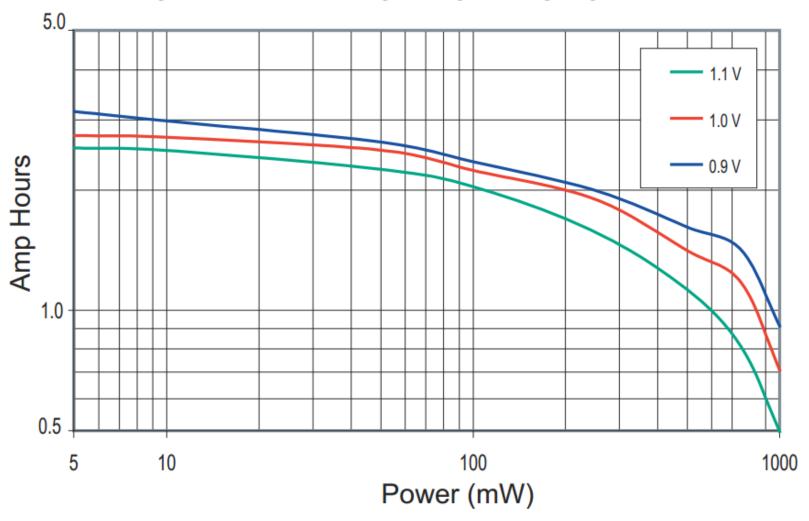
Nominal Voltage:	1.5 V						
Operating Voltage	1.6 - 0.75V						
Impedance:	81 m-ohm @ 1kHz						
Typical Weight:	24 gm (0.8 oz.)						
Typical Volume:	8.4 cm ³ (0.5 in. ³)						
Terminals:	Flat						
Storage Temperature Range:	-20 °C to 35 °C						
Operating Temperature Range:	-20 °C to 54 °C (-4 °F to 130 °F)						
ANSI: IEC:	15A LR6						

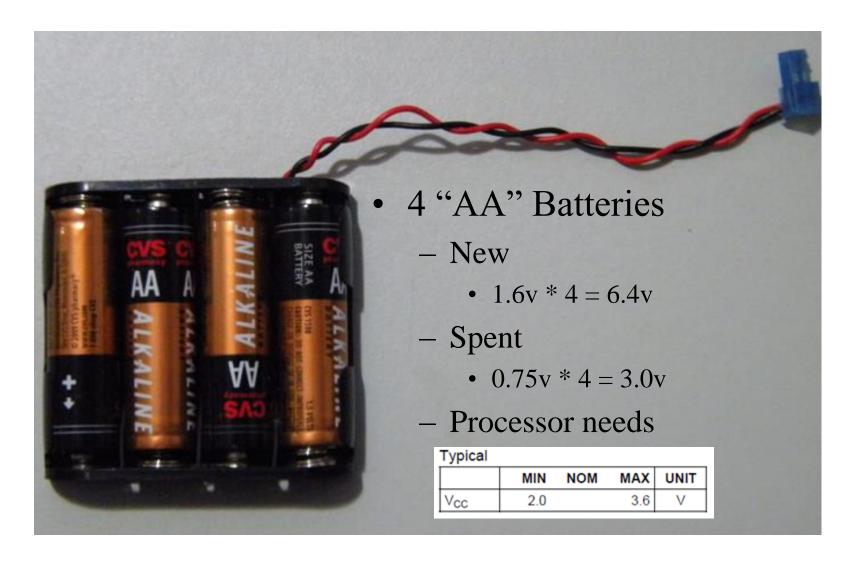


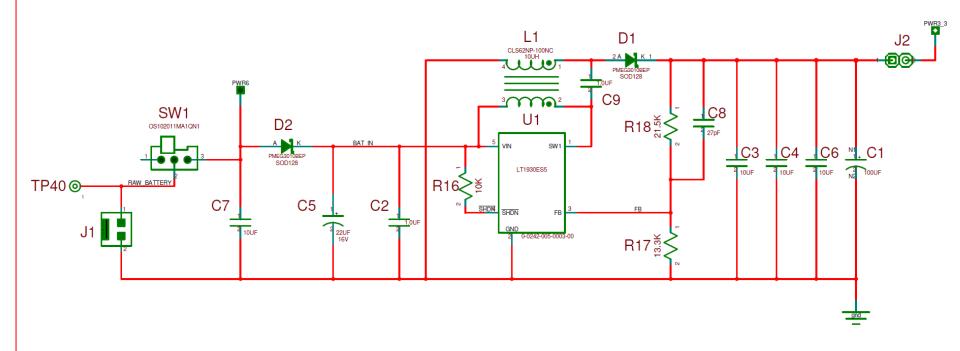
TYPICAL DISCHARGE CHARACTERISTICS AT VARIOUS POWER DRAINS



TYPICAL DELIVERED CAPACITY VS POWER DRAIN







Boost Converter as Sepic Converter

Single Inductor

Regulated Output with Input Voltages

Above, Below or Equal to the Output

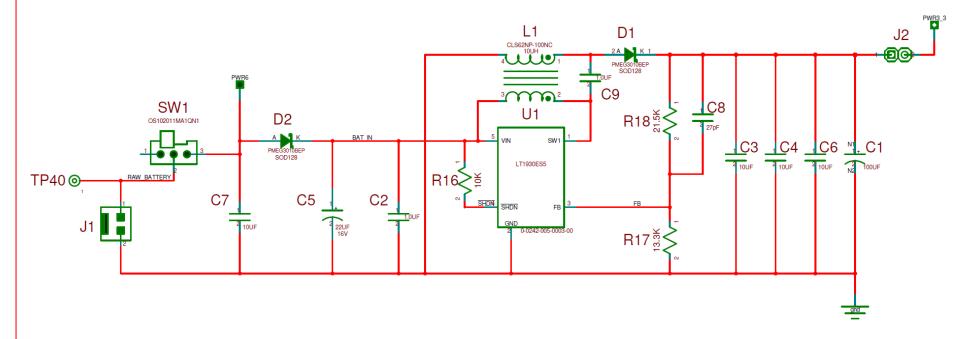
Wide VIN Range: 2.6V to 16V

VOUT Range: 2.4V to 5.25V

Low Shutdown Current: <1uA

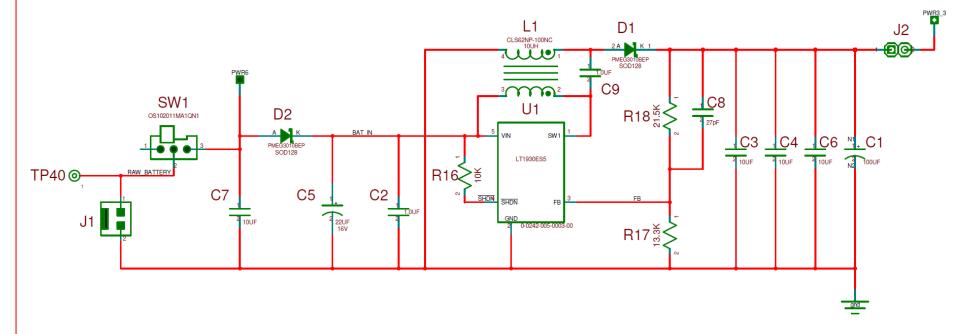
Low Profile (1mm) ThinSOT Package

■ Wide VIN Range: 2.6V to 16V



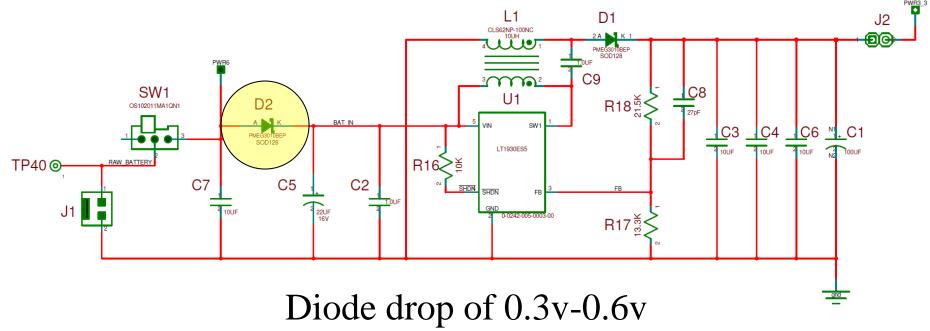
■ Wide VIN Range: 2.6V to 16V

4 "AA" Batteries ~ 6v



■ Wide VIN Range: 2.6V to 16V

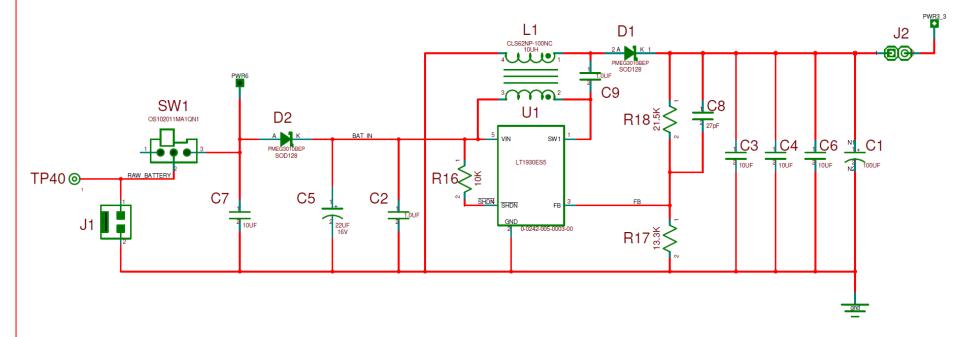
4 "AA" Batteries ~ 6v

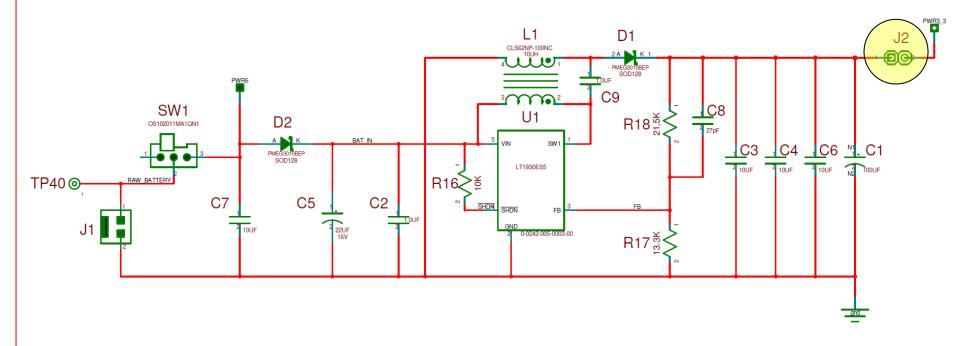


10ae arop of 0.3v-0.6v P-FET drop 0.1-0.3v

Protection against Batteries installed backward

■ Synchronous Rectification: Up to 87% Efficiency

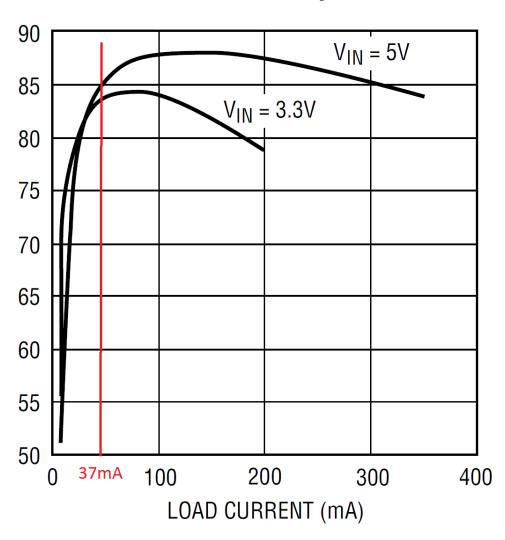


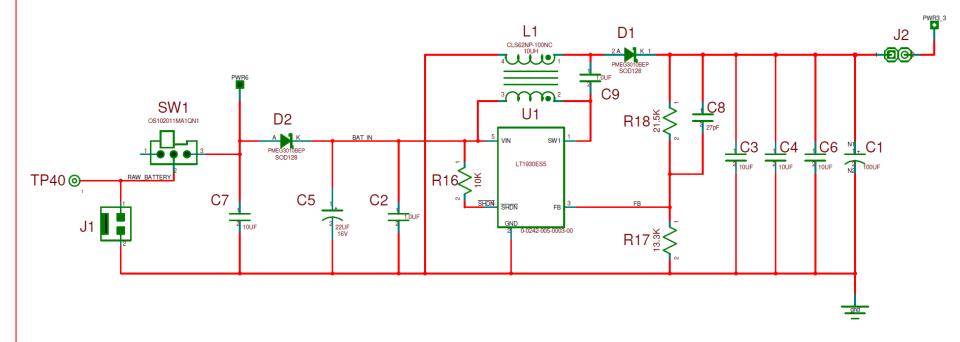


If you measure the current into the load as 31ma, measured at J2.

How long will the batteries last with continuous use?

Efficiency



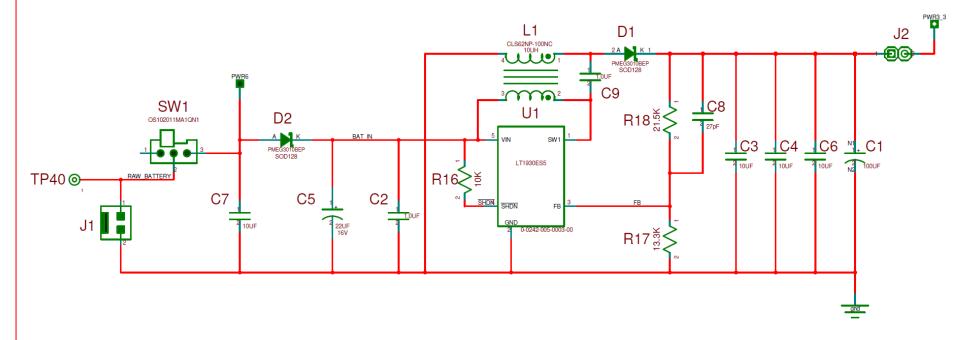


Voltage = Current * Resistance

Power = Voltage * Current

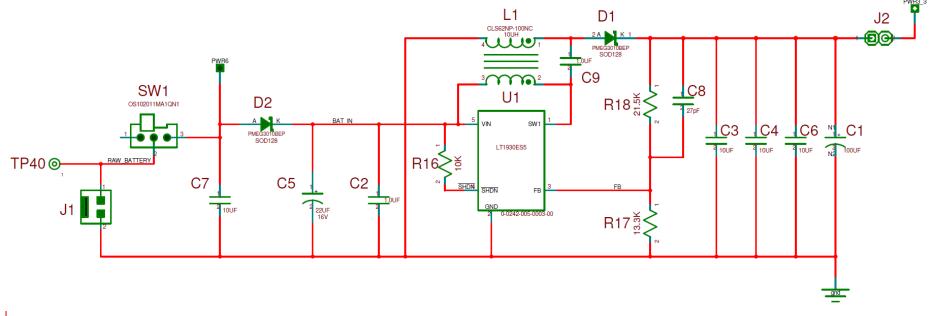
Battery Voltage changes – What about current?

How can you solve this problem?



Voltage = 3.3v Current = 31mAPower = 3.3v * 31mA 102.3mW

■ Synchronous Rectification: From Graph ~85% Efficient



Voltage = 3.3v Current = 31mA

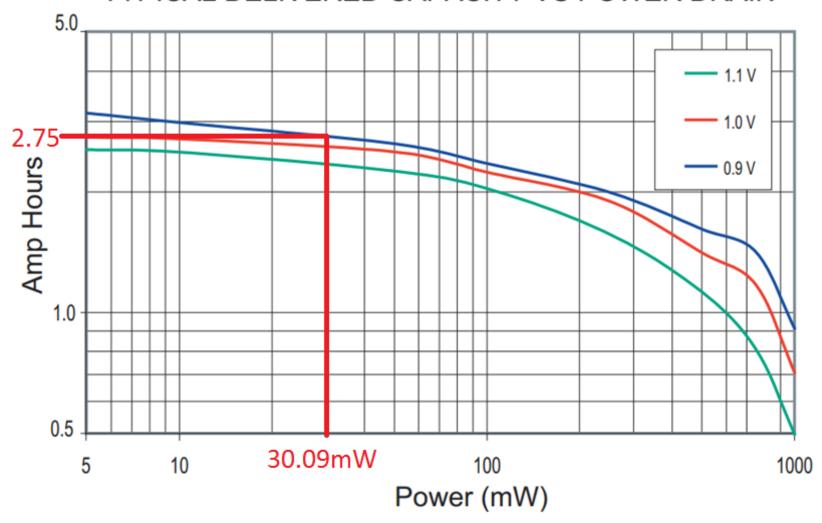
Power = $3.3v * 31mA \rightarrow 102.3mW$

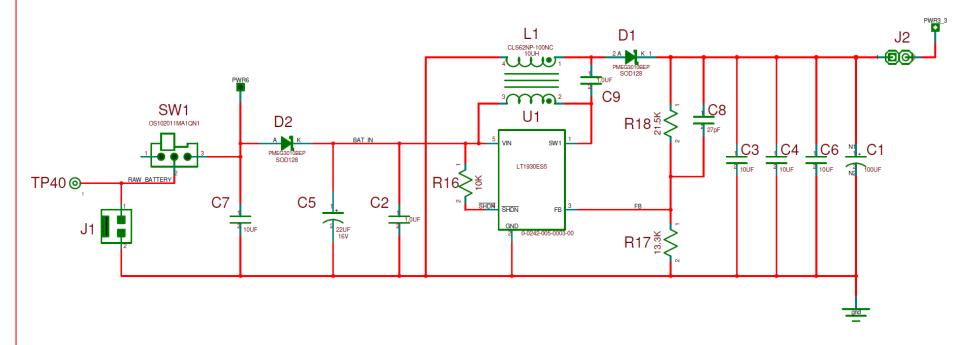
102.3 mW / 85% efficiency = 120.35mW from Batteries

With 4 Batteries –

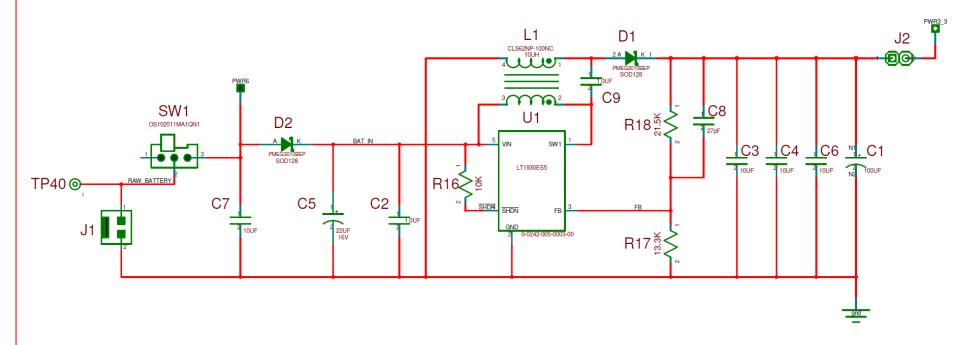
120.35mW / 4 batteries = 30.09mW per battery

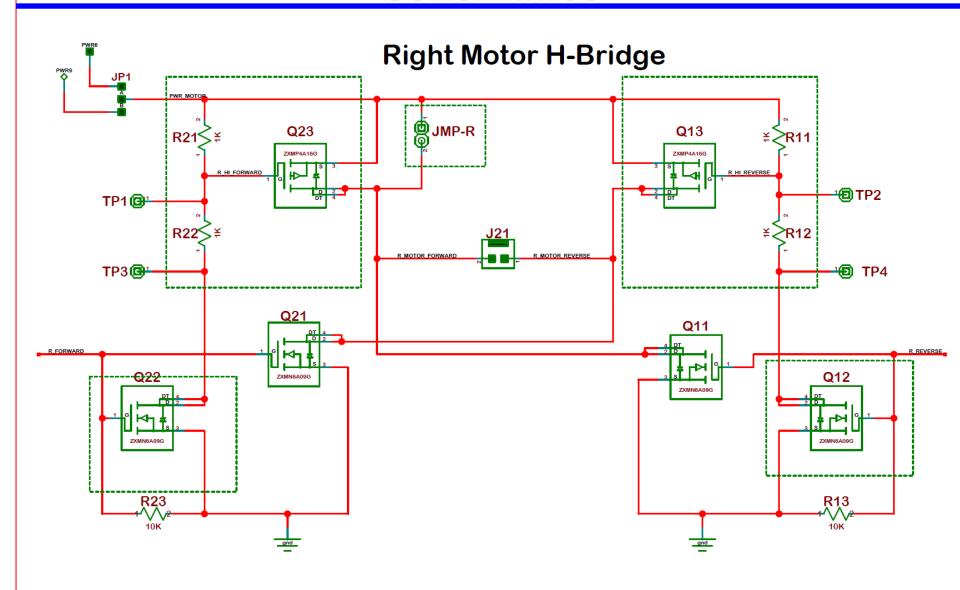
TYPICAL DELIVERED CAPACITY VS POWER DRAIN



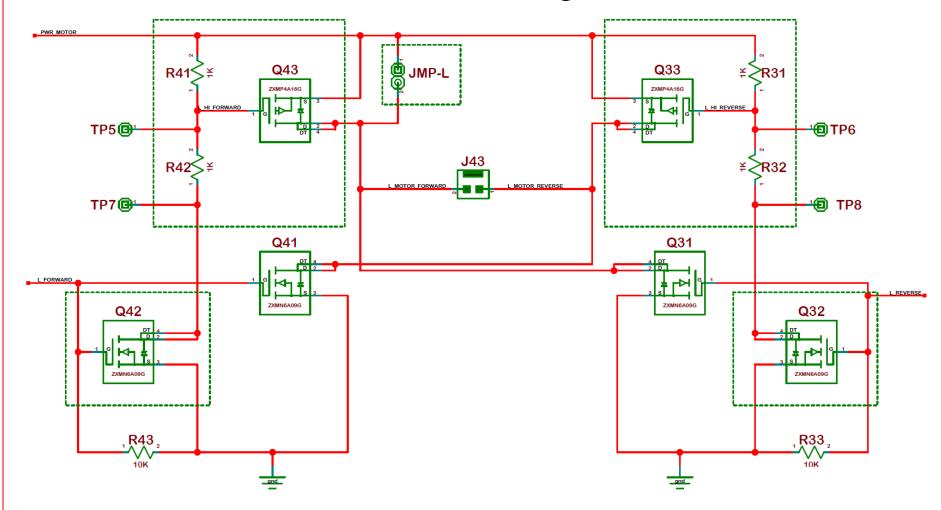


Time = 2.75 Amp-Hour / 0.031 Amp = 88.7 Hours





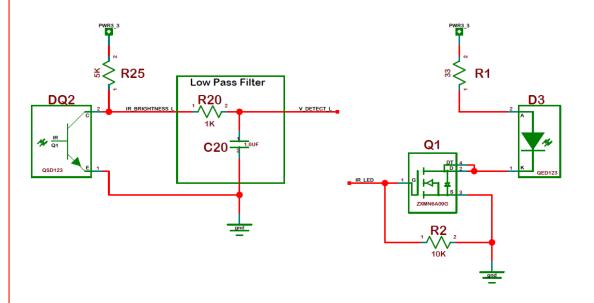
Left Motor H-Bridge

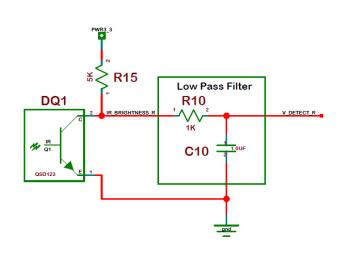


Left Side Line Detect

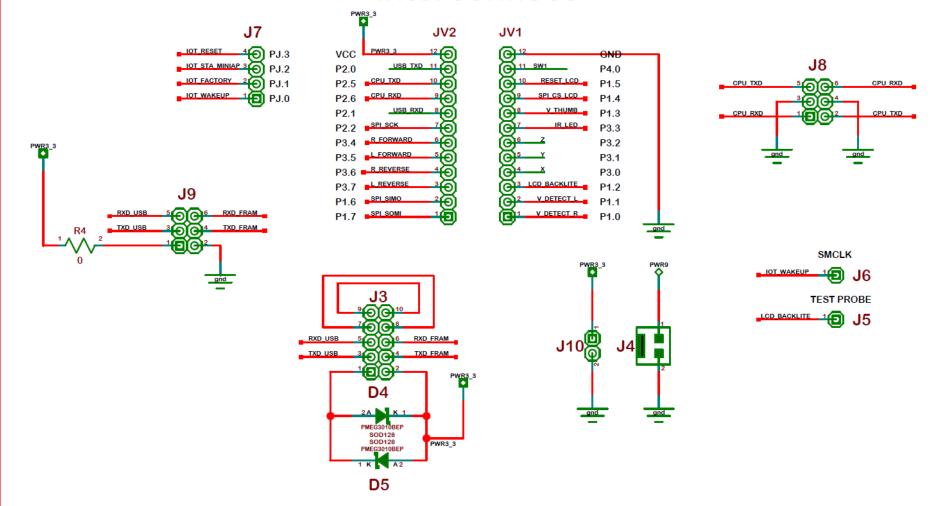
Center Emitter

Right Side Line Detect

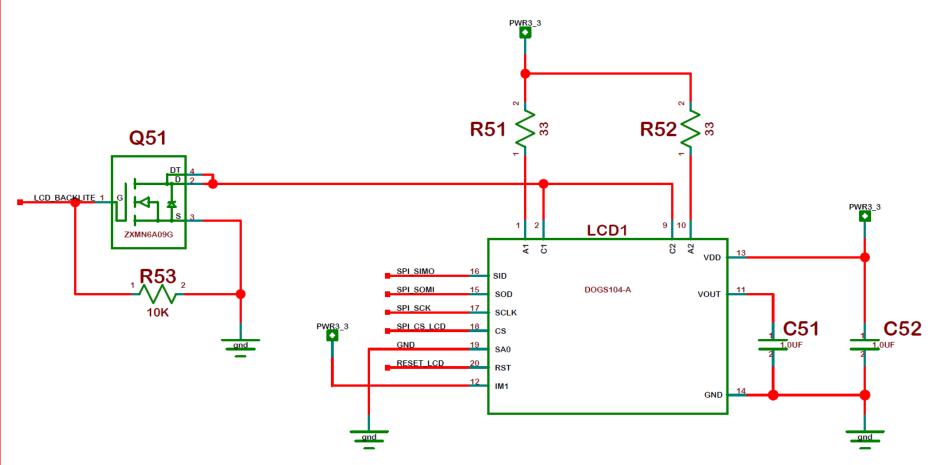


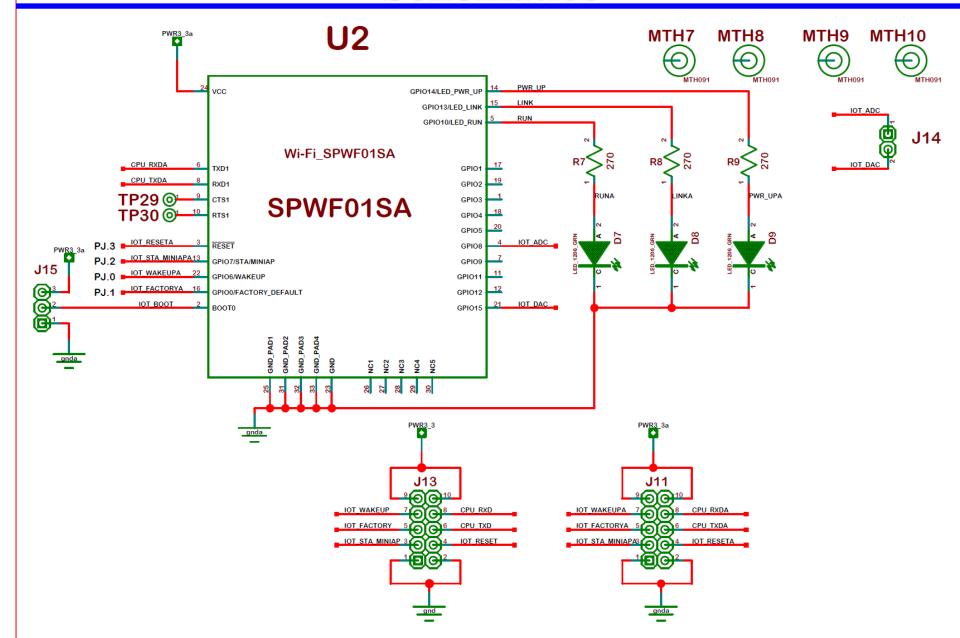


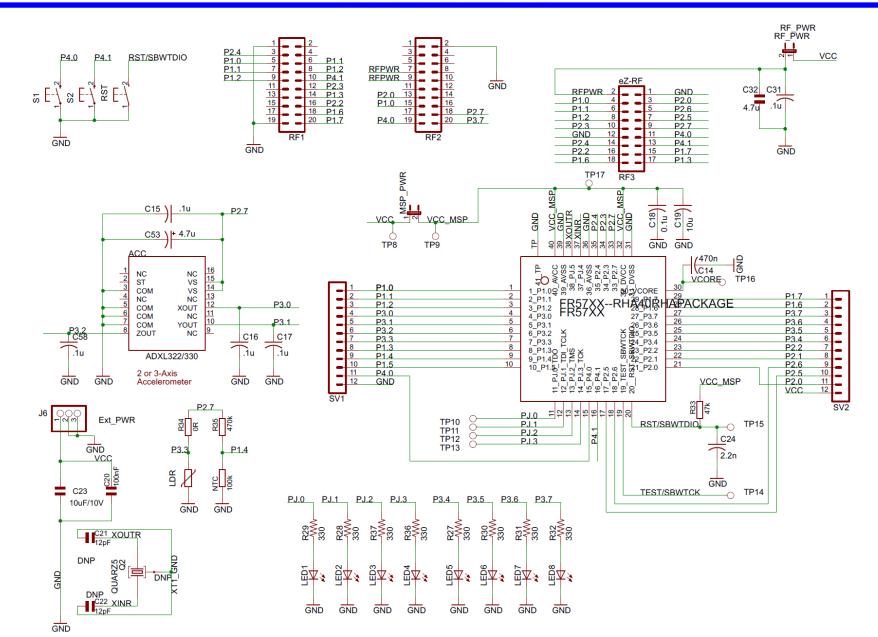
Interconnect











• Project Template –

• Write-up Expectations –