MSP430 SMCLK

From MSP430FR5739_DataSheet pg 85

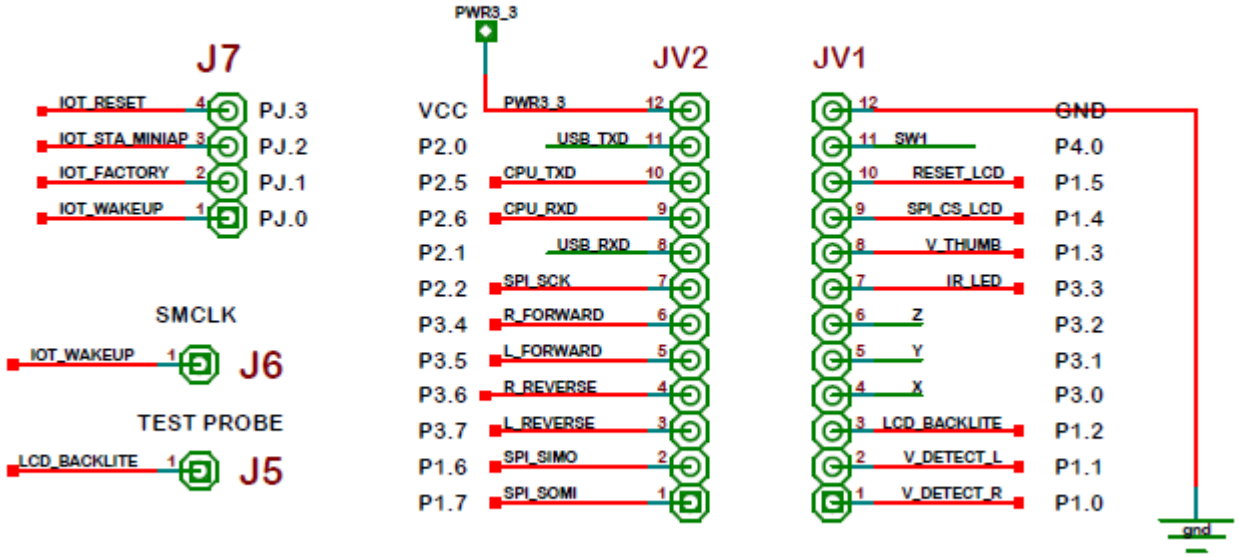
Table 55. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS (1)		
			PJDIR.x	PJSEL1.x	PJSEL0.x
PJ.0/TDO/TB0OUTH/SMCLK/CD6	0	PJ.0 (I/O) (2)	I: 0; O: 1	0	0
		TDO (3)	X	X	X
		TB0OUTH	0	0	1
		SMCLK	1		
		CD6	X	1	1
PJ.1/TDI/TCLK/TB1OUTH/MCLK/CD7	1	PJ.1 (I/O) (2)	I: 0; O: 1	0	0
		TDI/TCLK (3) (4)	X	X	X
		TB1OUTH	0	0	1
		MCLK	1		
		CD7	X	1	1
PJ.2/TMS/TB2OUTH/ACLK/CD8	2	PJ.2 (I/O) (2)	I: 0; O: 1	0	0
		TMS (3) (4)	X	X	X
		TB2OUTH	0	0	1
		ACLK	1		
		CD8	X	1	1
PJ.3/TCK/CD9	3	PJ.3 (I/O) (2)	I: 0; O: 1	0	0
		TCK (3) (4)	X	X	X
		CD9	X	1	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module. JTAG mode selection is made by the SYS module or by the Spy-Bi-Wire four-wire entry sequence. PJSEL1.x and PJSEL0.x have no effect in these cases.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

Schematic to Code

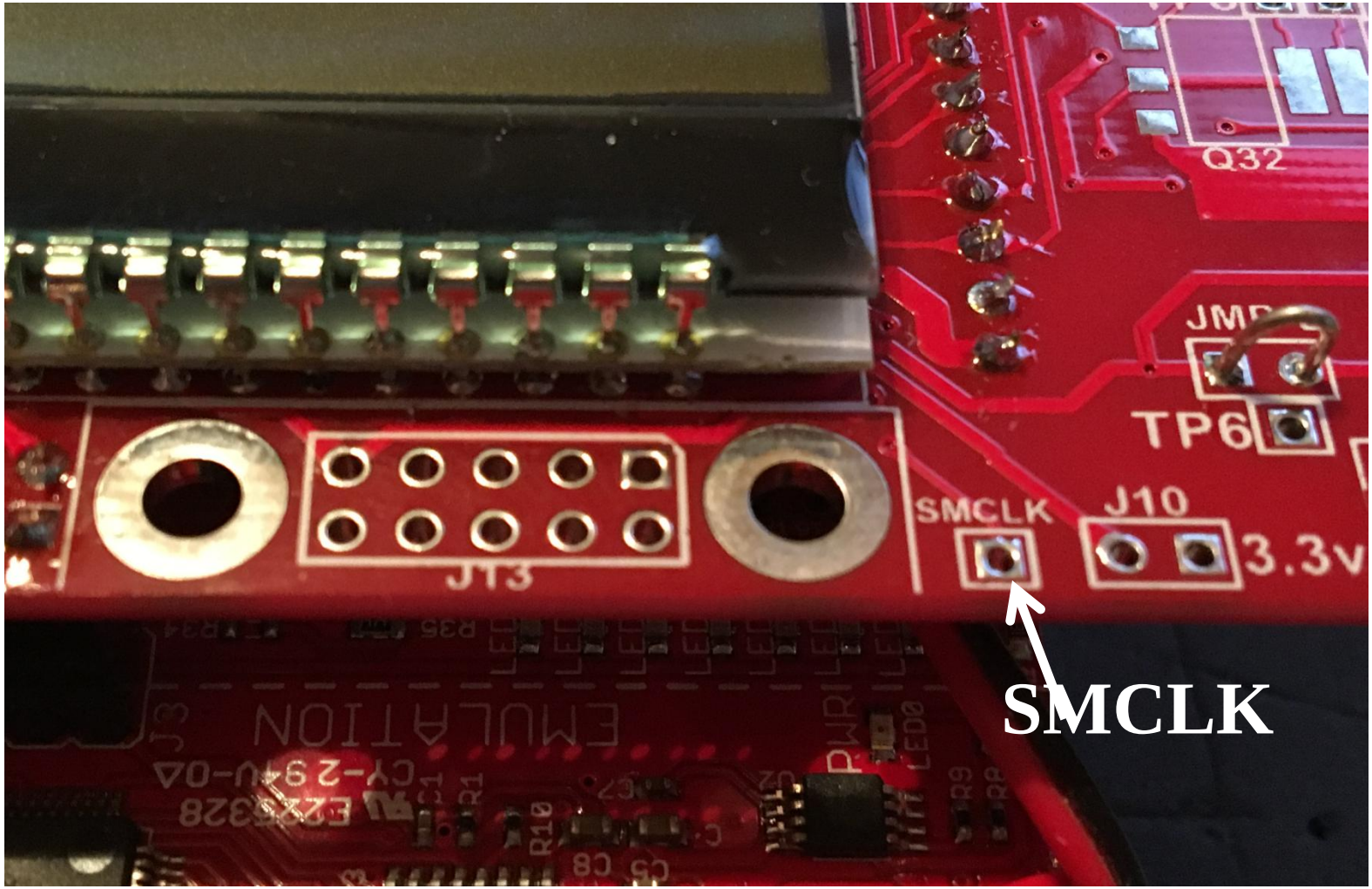
Interconnect




```
// SMCLK_OUT              (0x01) // SMCLK Out signal


  PJSEL0 |= SMCLK_OUT;           // SMCLK_OUT SMCLK Function selected
  PJSEL1 &= ~SMCLK_OUT;          // SMCLK_OUT SMCLK Function selected
  PJDIR |= SMCLK_OUT;            // SMCLK_OUT direction to output
```

Location on the Board



Init Port J

```
void Init_PortJ(char clock_iot){
  PJSEL0 = 0x00;                // Port Pin set as I/0
  PJSEL1 = 0x00;                // Port Pin set as I/0
  PJDIR = 0x00;                 // Set Port Pin direction to input
.
.
.
  if(clock_iot){
[add code for SMCLK selected]
  }else{
[add code for IOT_WAKEUP selected]

  }
.
.
.
}
```