Laborversuch Messdatenerfassung: Analog/Digital- und Digital/Analog-Wandler

DHBW Stuttgart – Laborentwurf: Prof. Dr. Axel Richter

Vorbemerkungen

1) Zur Versuchs-Vorbereitung: Lesen Sie die im Anhang liegenden Dokumente. Sie müssen informiert sein über:
    a. Die in den Versuchen verwendeten AD- und DA-Umsetzungsverfahren,
    b. den Aufbau und die Funktion der verwendeten Bauteile,
    c. Messverfahren der Monotonie, Linearität und Konversionszeit von AD- und DA-Wandlern.

2) Der Laborablauf besteht aus 2 Terminen (je ca. 5 Std.) zur Versuchsdurchführung.

3) Am ersten Labor Tag wird eine kurze Prüfung (15 Min.) zu der zugrundeliegenden Theorie geschrieben. Diese wird benotet und trägt zu 25% zur Gesamtnote der Lehrveranstaltung bei.

4) Achten Sie auf einen übersichtlichen Aufbau auf dem Steckbrett (überlegen Sie sich vor dem Stecken anhand der Schaltskizze die Platzaufteilung etc.). Nutzen Sie möglichst kurze Kabel!

5) Die Funktion jeder Versuchsanordnung wird von einem Betreuer abgenommen, ehe Sie die Messungen beginnen.

6) Beachten Sie das gesonderte Blatt mit Hinweisen zu den Laborberichten bevor Sie anfangen diese zu schreiben.

Versuch 1: Analog/Digital-Converter

Ziel der Messungen (ADC)

- Nichtlinearität über den Gesamtbereich (INL),
- Differentielle Nichtlinearität (DNL) im mittleren Bereich
- Konversionsrate.

Benötigte Geräte

- Netzgerät, Fluke DMM, Oszilloskop für Teil f).

Vorgehen

a) Auf der Seite 24 („Functional Description (Continued)“, Bild 9) finden Sie eine Skizze des benötigten Schaltbildes. Beachten Sie dabei u.a.:
   - Die Clockfrequenz des ADC liege bei ca. 600 kHz.
   - Welche Signale sind auf Digital-Masse, welche auf Analog-Masse zu führen?
   - Der V(+)-Eingang muss mit einem Schutzwiderstand (z.B. 1 kOhm) gegen Überspannungen versehen werden, außerdem mit 100 nF nach Masse gegen Einstreuungen geschützt werden.
   - Die variable Eingangsspannung für den ADC ist vom Netzgerät zu beziehen.
   - Wie messen Sie die Betriebs- und die Eingangsspannung(en) möglichst genau?
   - Wie erkennen Sie das Wandlungsergebnis (Bitmuster) des ADC?
   - Wie hoch ist die anzulegende Versorgungsspannung? Wie ist der Eingangsspannungsbereich für U_{in}?

b) Bauen Sie die Schaltung gemäß Teil a) auf (Versorgungsspannung dabei aus!). Prüfen Sie selbst und lassen Sie den Aufbau vor Einschalten der Versorgungsspannung von einem Betreuer überprüfen.

c) Inbetriebnahme: Legen Sie nun die Spannung(en) an: Generelle Reihenfolge beim Einschalten:
   1) Versorgungsspannung,
   2) Hilfsspannungen (z.B. Referenz)
   3) Signalspannungen (Ausschalten in umgekehrter Reihenfolge!)

   Machen Sie einen kurzen Funktionstest. Entspricht das Ergebnis Ihren Erwartungen?

d) Integrale Nichtlinearität (INL) über den gesamten Bereich:
   Hinweis: alle Spannungen sind mit dem Fluke DMM zu messen, auch V_{cc}!
   - Teilen Sie den Bereich der Eingangsspannung in 16 gleich große Bereiche (Bitmuster?).
   - Fahren Sie jeweils die Bereichsgrenze (d.h. bis Bitmuster gerade umspringt) von unten an und protokollieren Sie die dafür notwendige Eingangsspannung (Tabelle!).
   - Berechnen Sie jeweils die Differenz zur "Idealgeraden" (Verbindungsgerade der Stufenmitten durch den Ursprung!).
   - Erstellen Sie eine graphische Darstellung der Verteilung der Abweichungen von der „Idealgeraden“ als Histogramme (Anzahl als Funktion der Abweichungs-Intervalle).

e) Differentielle Nichtlinearität (DNL):
   - Messen Sie neun symmetrisch um die Bereichsmitte liegende Werte, die jeweils ein Bit (LSB) Abstand voneinander haben, nach dem Verfahren von Teil d).
   - Berechnen Sie die jeweilige Differentielle Nichtlinearität.
   - Erstellen Sie eine graphische Darstellung der gemessenen Treppenfunktion. Zeichnen Sie auch die ideale Treppenfunktion und die Ideal-Gerade ein (geht durch den Ursprung und durch die Mitten der Treppenfunktion).

f) Konversionszeit:
   Messen Sie für eine mittlere Eingangsspannung die tatsächliche Zykluszeit und Frequenz
   - Für die Clock, sowie für die Konversion des ADC.
   - Wie viele Clock-Zyklen werden für eine Konversion benötigt? Vergleich mit Datenblatt!

Versuch 2: Digital/Analog-Converter

Ziel der Messungen (DAC)

- Monotonie,
- Linearität,
- Einschwingzeit.

Benötigte Geräte

- Netzgerät, Fluke DMM, Oszilloskop.

Vorgehen

a) Im Anhang auf der Seite „DA - CONVERTER: LINEARITY, MONOTONICITY“ finden Sie eine Beschreibung zur Messung der Monotonie und der Linearität. Und auf der Seite „Zusammenfassung: Bauteile und Anschlüsse“ finden Sie die Anschlussskizze für den DAC ZN429E.
   - Skizzieren Sie mit den gegebenen Quellen den zur Messung nötigen Schaltungsaufbau, inklusive des Flip-Flops.
   - Welchen Spannungsbereich überdeckt der DAC-Ausgang?
   - Wie ist die V_{ref} zu wählen?
   - Der DAC enthält intern schnelle Schalter. Ein Block-Kondensator könnte evtl. nützlich sein?

b) Bauen Sie die Schaltung gemäß Teil a) auf (Versorgungsspannung dabei aus!). Überprüfen Sie den Aufbau vor Einschalten der Versorgungsspannung nochmals.

c) Monotonie und Nichtlinearität:
   - Messen Sie nach der beschriebenen Methode Vorzeichen und Betrag der Änderung der DAC-Ausgangsspannung pro geändertes Bit.
   - Welche Signale müssen Sie am Oszilloskop vergleichen, um die Monotonie zu prüfen?
   - Ist Ihr Bauteil durchgängig monoton? Welche Nichtlinearität messen Sie?
   - Protokollieren Sie die Werte tabellarisch. Wie groß ist der theoretisch zu erwartende Wert pro LSB?
   - Statt der in der Literatur angegebenen Triggerung des Scope mit dem Q-Ausgang des Flip-Flops könnte auch direkt mit dem Bitsprung des DAC-Ausgangs getriggert werden. Was ist vorzuziehen? Begründung?
   - Wie groß ist der Ausgangswiderstand des DAC? Ist daher bei der Messung etwas zu berücksichtigen?

d) Einschwingverhalten:
   Die bereits aufgebaute Schaltung kann auch zur Untersuchung der Einschwingzeit verwendet werden.
   - Wählen Sie eine hierzu geeignete Einstellung für Funktionsgeneratorfrequenz, Bitsprung (Sprunghöhe) und Scope.
   - Messen Sie die Einschwingzeit: Wann ist der stabile Zustand auf ca. 10%, wann praktisch ganz erreicht? Wie ist die Angabe des Datenblatts?

Datenblatt: Analog/Digital-Wandler

National Semiconductor

November 1999

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

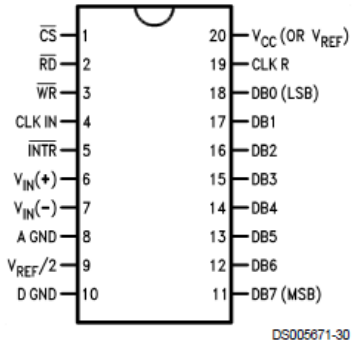
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages



DS005671-30

See Ordering Information

Ordering Information

TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Z-80® is a registered trademark of Zilog Corp.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	−0.3V to +18V
At Other Input and Outputs	−0.3V to (V_{CC}+0.3V)
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0804LCJ	−40°C≤T_A≤+85°C
ADC0801/02/03/05LCN	−40°C≤T_A≤+85°C
ADC0804LCN	0°C≤T_A≤+70°C
ADC0802/04LCWM	0°C≤T_A≤+70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
ADC0802: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±½	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
ADC0804: Total Unadjusted Error (Note 8)	V_{REF}/2=2.500 V_{DC}			±1	LSB
ADC0805: Total Unadjusted Error (Note 8)	V_{REF}/2-No Connection			±1	LSB
V_{REF}/2 Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)	Gnd–0.05		V_{CC}+0.05	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	V_{CC}=5 V_{DC} ±10% Over Allowed V_{IN}(+) and V_{IN}(−) Voltage Range (Note 4)		±1/16	±⅛	LSB

AC Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	f_{CLK}=640 kHz (Note 6)	103		114	μs
T_C	Conversion Time	(Notes 5, 6)	66		73	1/f_{CLK}
f_{CLK}	Clock Frequency Clock Duty Cycle	V_{CC}=5V, (Note 5)	100 40	640	1460 60	kHz %
CR	Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ =0 V_{DC}, f_{CLK}=640 kHz	8770		9708	conv/s
$t_{W(\overline{WR})L}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ =0 V_{DC} (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L=100 pF		135	200	ns
t_{1H}, t_{0H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L=10 pF, R_L=10k (See TRI-STATE Test Circuits)		125	200	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5 V_{DC} and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (1)	Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=5.25 V_{DC}	2.0		15	V_{DC}
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC}=4.75 V_{DC}			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	V_{IN}=5 V_{DC}		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	V_{IN}=0 V_{DC}	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T−	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis (V_T+)−(V_T−)		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	I_O=360 µA V_{CC}=4.75 V_{DC}			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	I_O=−360 µA V_{CC}=4.75 V_{DC}	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT}=1.6 mA, V_{CC}=4.75 V_{DC} I_{OUT}=1.0 mA, V_{CC}=4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−360 µA, V_{CC}=4.75 V_{DC}	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	I_O=−10 µA, V_{CC}=4.75 V_{DC}	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT}=0 V_{DC} V_{OUT}=5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, T_A=25°C	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, T_A=25°C	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCWM	f_{CLK}=640 kHz, $V_{REF}/2$=NC, T_A=25°C and $\overline{CS}$ =5V		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct–especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 4* and section 2.0.

Functional Description (Continued)

±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 2 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 3* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.

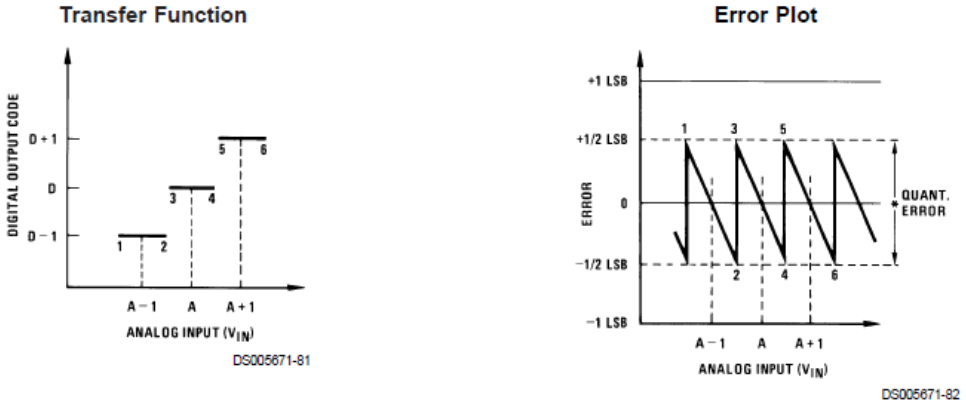


FIGURE 1. Clarifying the Error Specs of an A/D Converter Accuracy=±0 LSB: A Perfect A/D

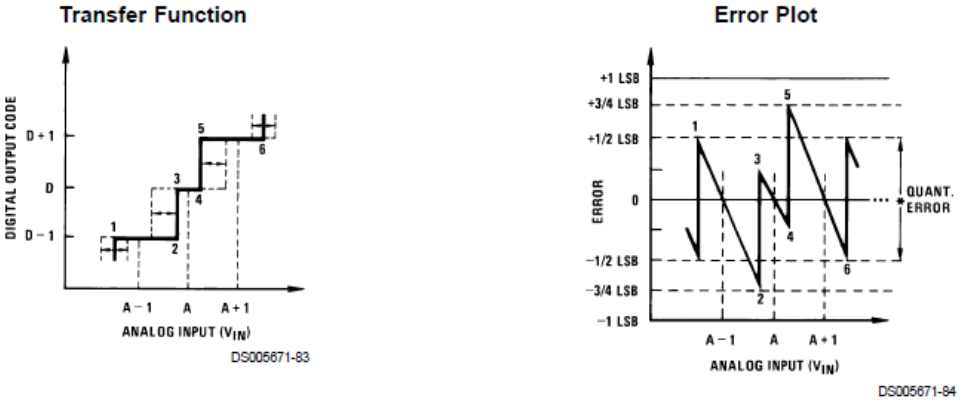
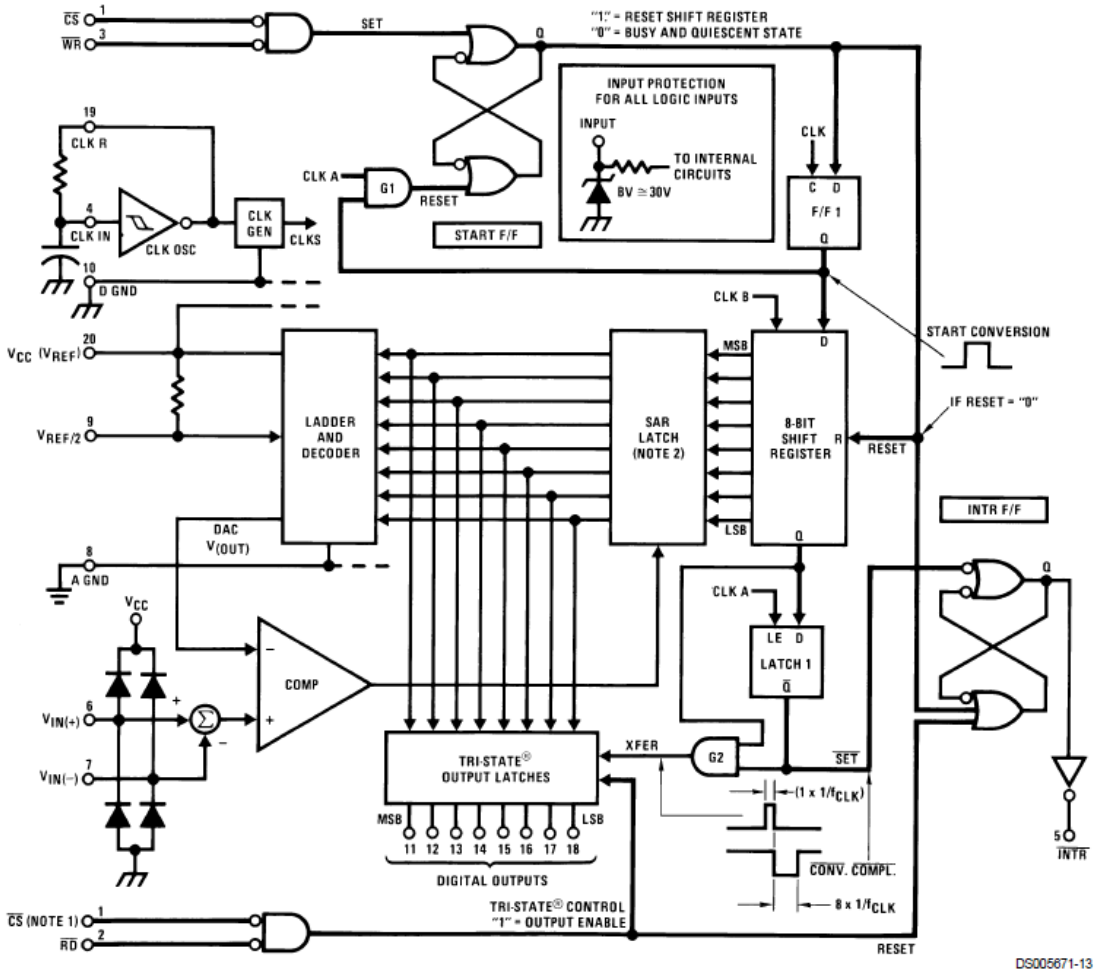


FIGURE 2. Clarifying the Error Specs of an A/D Converter Accuracy=±¼ LSB

Functional Description (Continued)



Note 13: $\overline{CS}$ shown twice for clarity.

Note 14: SAR = Successive Approximation Register.

FIGURE 4. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

Functional Description (Continued)

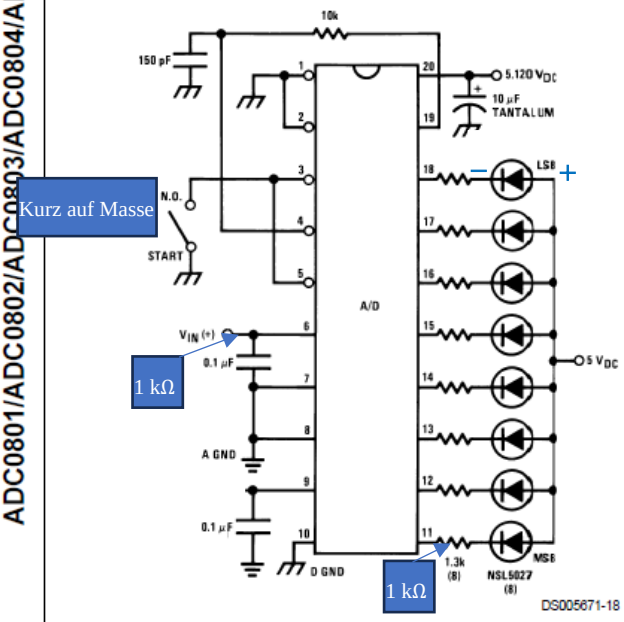
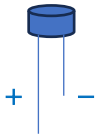


FIGURE 9. Basic A/D Tester



For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis).

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 11*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 12*.

Datenblatt: Digital/Analog-Wandler

DA - CONVERTER: **LINEARITY, MONOTONICITY**
Type: Ferranti ZN 429

1. General

Testing and evaluating of the most significant parameters accuracy and settling time of a DAC requires a lot of time and patience, if all possible outputs and transitions are measured. For a quick conclusion about the device the following shortcuts are possible:

2. Accuracy, nonlinearity

Merely measuring an output level (or even several) does not provide sufficient information. Actually, measuring all possible 2^n levels and computing the nonlinearity is a long and time consuming process. A much shorter way exists to at least insure monotonicity and linearity of a D/A converter. If those factors are verified, then only gain factor remains as a possible source of inaccuracy, normally externally adjustable.
The shortcut requires only n steps for a n-bit DAC and involves comparing the contribution of each bit with the sum of the lower order ones. For example, compare the output of the fourth bit (00001000) with that of all bits "0" except the lower bits (00000111). The difference in outputs is a measure of the linearity. Perfect linearity would produce a step change of 1 LSB. If the difference is greater than zero, monotonicity is assured. If the change is less than 2 LSB's, linearity is within an half LSB, the usual allowable limit.
The eight combinations for testing an 8-bit DAC in this manner are shown below. Performing this test is done on an ac basis and displaying the output on an oscilloscope. By toggling a flipflop and applying one output (Q) to the bit being tested and the other (Q*) to all the lower order bits, the difference can be viewed on an ac coupled oscilloscope.

0000	0001	.....	0000	0000
0000	0010	.....	0000	0001
0000	0100	.....	0000	0011
0000	1000	.....	0000	0111
0001	0000	.....	0000	1111
0010	0000	.....	0001	1111
0100	0000	.....	0011	1111
1000	0000	.....	0111	1111
0000	0000	.....	1111	1111

The high order unused bits are set to "0". Relative phase of the output square must be observed to ascertain, which step is greater, and hence wether the change is greater or less than zero. Internal triggering of the scope can rise confusion, therefore it is more desirable to trigger e.g. from the signal going to the low order bits. Thus, "greater than zero" will always mean, that the first part of the sweep must be less than the second part.

3. Settling time

In general, the settling time has been defined as the time from the change of the digital input until all transitions have sufficiently diminished, so that the output remains within half LSB. Since the situation means measuring some millivolts out of the 10 V range and perhaps transitions in the order of some hundreds nanoseconds, the instrumentation for such tests is not trivial. The scope cannot be used in the dc mode, and the worst case out of the 2^{2n} possible transitions has to be considered.
One might think, that a full scale change (0000 0000 to 1111 1111) would show the worst results. Although this might be so, another test will better verify the settling time.
In digital engineering we have discussed transitions and glitches in connection with the GRAY code. In this regard we had stated that the worst transients, hence perhaps settling time, occur when the digital values go between:

0111 1111
1000 0000

Although this should theoretically change only one LSB worth around the half scale in this case, the intermediate state may be all "0's". Thus, in reality the converter may go from half scale minus one LSB to zero and then back to half scale. Slewing rates as well as small signal bandwith are measured in this supposedly small 1 LSB change.
Note that this requires the same test circuitry as for testing linearity, when performing the check for the MSB. Bandwidth of the oscilloscope has to be considered; a delayed sweep feature of the scope is also helpful.

ZN429E-8 ZN429J-8 ZN429D

INTRODUCTION

The ZN429 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

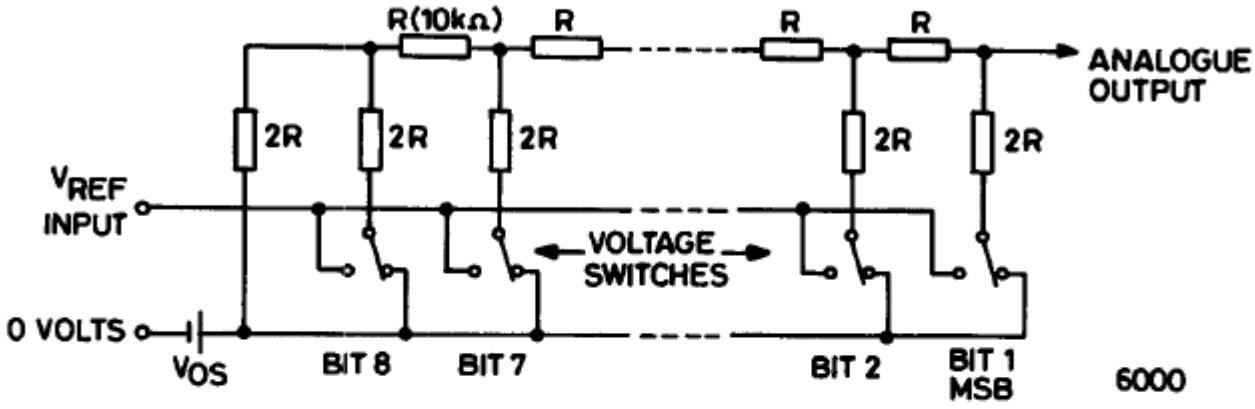


Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN429E-8	0 to +70°C	Plastic D.I.L.
ZN429J-8	−55 to +125°C	Ceramic D.I.L.
ZN429D	0 to +70°C	Plastic SO-14

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Max. voltage, logic and V_{REF} inputs	+5.5V
Storage temperature range	−55 to +125°C

ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified).

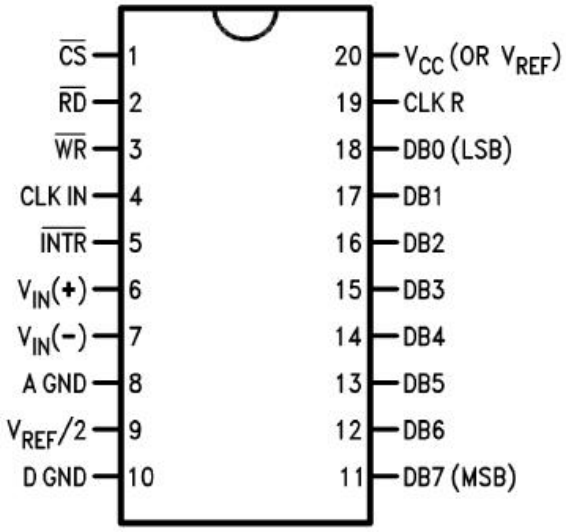
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter						
Resolution		8	–	–	Bits	
Accuracy		8	–	–	Bits	
Non-linearity		–	–	±0.5	LSB	Note 1
Differential non-linearity		–	±0.5	–	LSB	Note 2
Settling time to 0.5LSB		–	1.0	–	μs	1 LSB step
Settling time to 0.5LSB		–	2.0	–	μs	All bits ON to OFF or OFF to ON
Offset voltage						
ZN429J-8	V_{OS}		5.0	8.0	mV	
ZN429E-8, ZN429D		–	3.0	5.0	mV	All bits OFF note 1
V_{OS} temperature co-efficient		–	5	–	μV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. $V_{REF} = 2.56V$
Full-scale temperature coefficient		–	3	–	ppm/°C	Ext. $V_{REF} = 2.560V$
Non-linearity temp. co-efficient		–	7.5	–	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_O	–	10	–	kΩ	
External reference voltage		0	–	3.0	V	
Supply voltage	V_{CC}	4.5	–	5.5	V	
Supply current	I_S	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	V	
Low level input voltage	V_{IL}	–	–	0.7	V	
High level input current	I_{IH}	–	–	10	μA	$V_{CC} = max$, $V_I = 2.4V$
		–	–	100	μA	$V_{CC} = max$, $V_I = 5.5V$
Low level input current	I_{IL}	–	–	−0.18	mA	$V_{CC} = max$, $V_I = 0.3V$

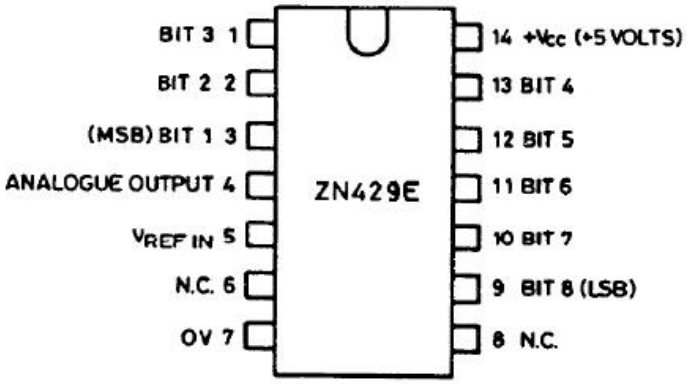
Notes:

1. The ZN429J-8 differs from the ZN429E-8 and the ZN429D in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1LSB over the temperature ranges −55 to 0°C and +70 to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range.

Zusammenfassung: Bauteile und Anschlüsse (inklusive Flip-Flop)

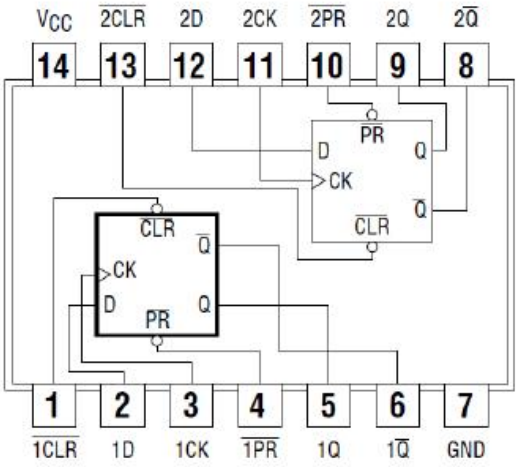
ADC080X
Dual-In-Line and Small Outline (SO) Packages

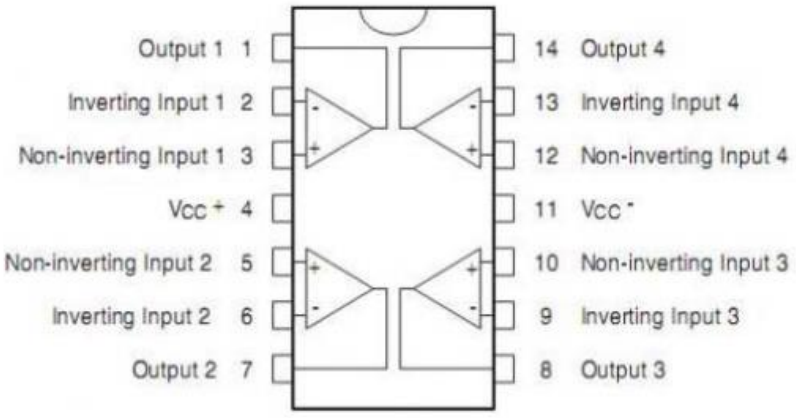




DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET AND CLEAR

74LS74





LM 124, LM324, TL084