Lab work 16042025

Suppose there are 4 processors P1, P2, P3 and P4, and 4 cache units C1, C2, C3 and C4. The processor Pi is physically connected with the cache Ci only.

All four cache units are connected to each other and with the shared RAM through a common bus.

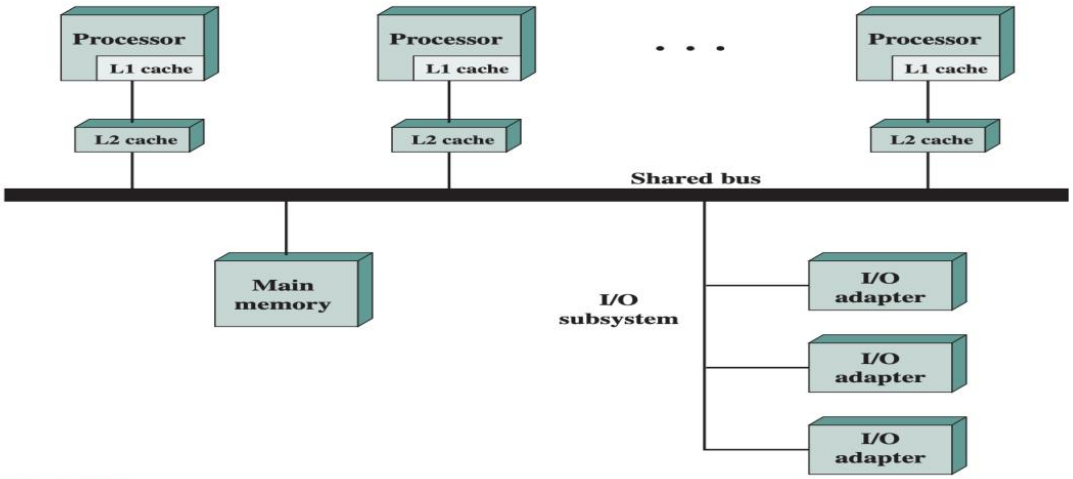


Figure 17.5 Symmetric Multiprocessor Organization

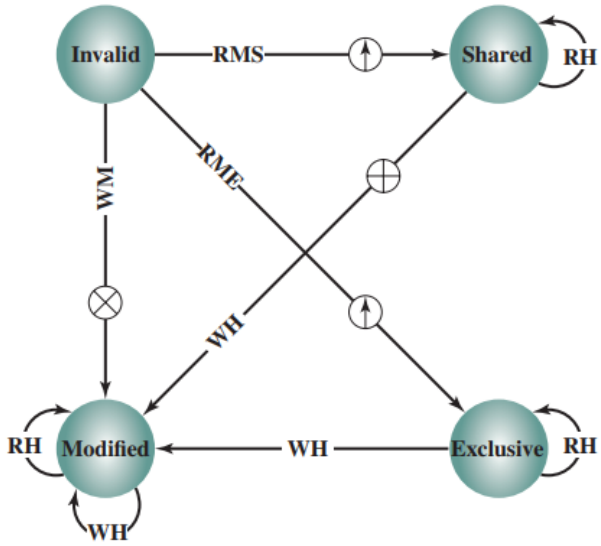
When a processor wants to read from the RAM or write to the RAM, it first checks whether the read/write could be done by working on the connected cache.

Initially all the caches are in the state “INVALID”.

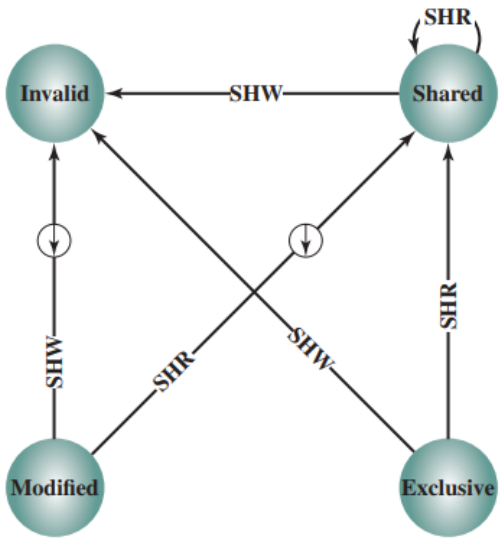
Write a program that takes as input a triple (a,b,c), and outputs the states of C1, C2, C3 and C4.

- a is a member of the set {1,2,3, 4}. For example, a=1 implies that the cache is C1.
- b is member of the set {R,W}. R means that “read” operation has been issued from the corresponding processor. Similarly, W means that “write” operation has been issued from the corresponding processor.
- c is member of the set {0,1}. c=0 means that the program terminates after outputting the states of C1, C2, C3 and C4. c=1 means that program outputs the states of C1, C2, C3 and C4, and waits for another input triple (a,b,c).

The solution will be based on MESI protocol. Use the following state transition diagram.



(a) Line in cache at initiating processor



(b) Line in snooping cache

RH = Read hit
RMS = Read miss, shared
RME = Read miss, exclusive
WH = Write hit
WM = Write miss
SHR = Snoop hit on read
SHW = Snoop hit on write or read-with-intent-to-modify