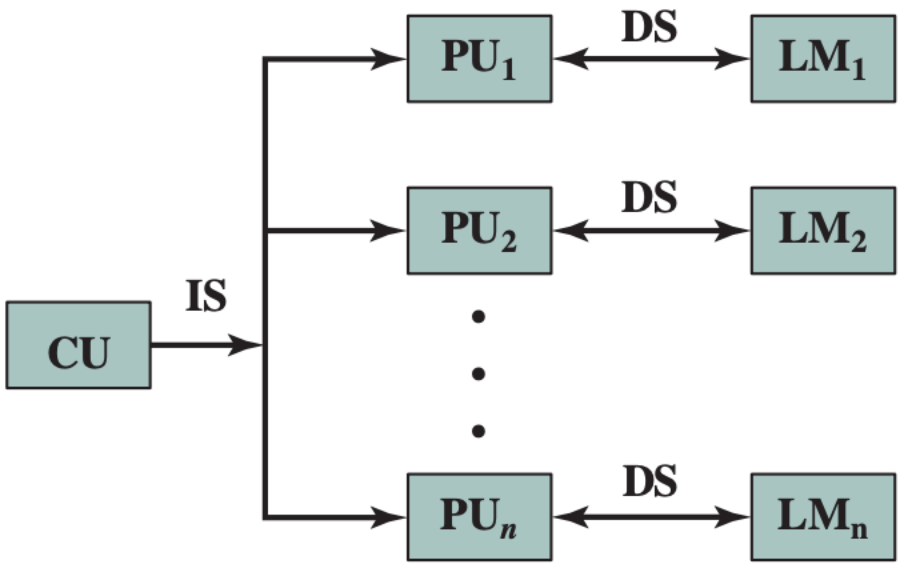
Parallel Processor Architecture

Lecture 07032025

Parallel processor architecture - SISD

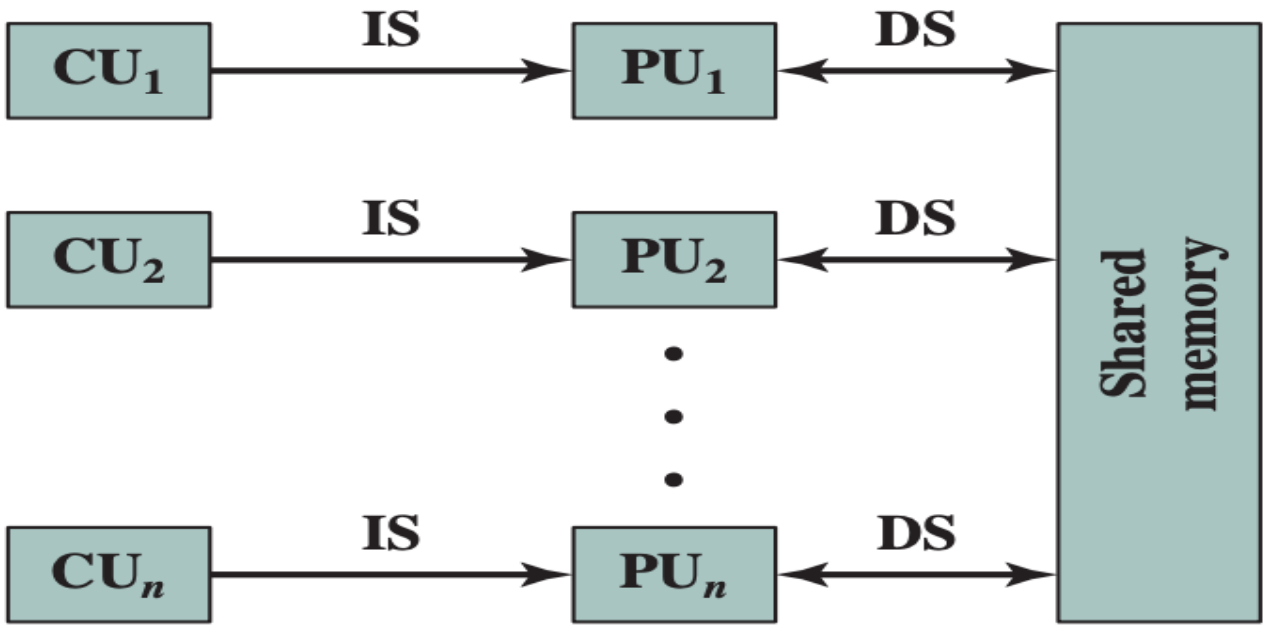
(a) SISD

Parallel processor architecture - SIMD



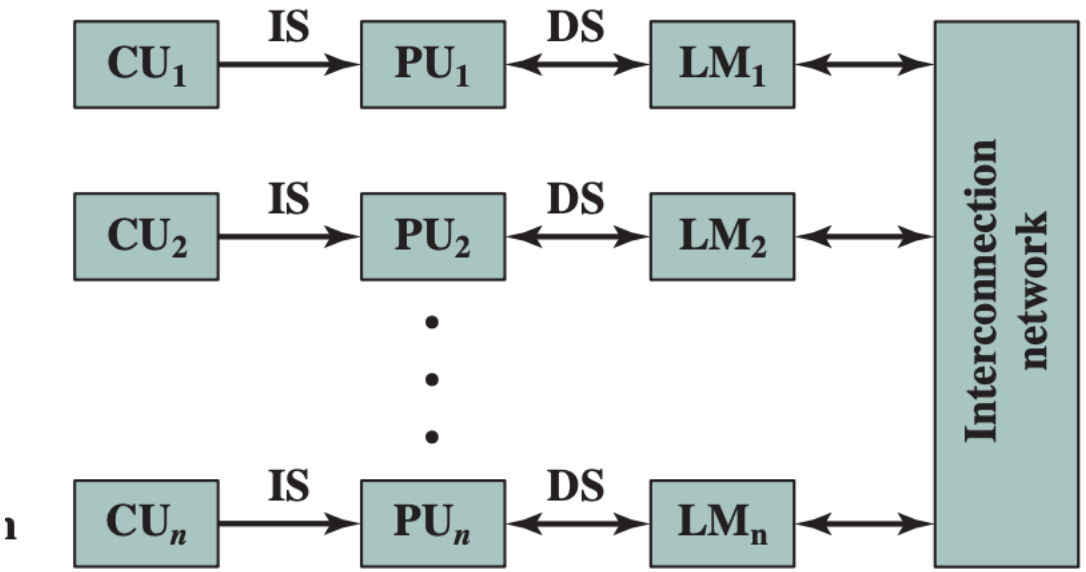
(b) SIMD (with distributed memory)

Parallel processor architecture – MIMD (shared memory)



(c) MIMD (with shared memory)

Parallel processor architecture – MIMD (distributed memory)



(d) MIMD (with distributed memory)

Parallel processor architecture (full landscape)

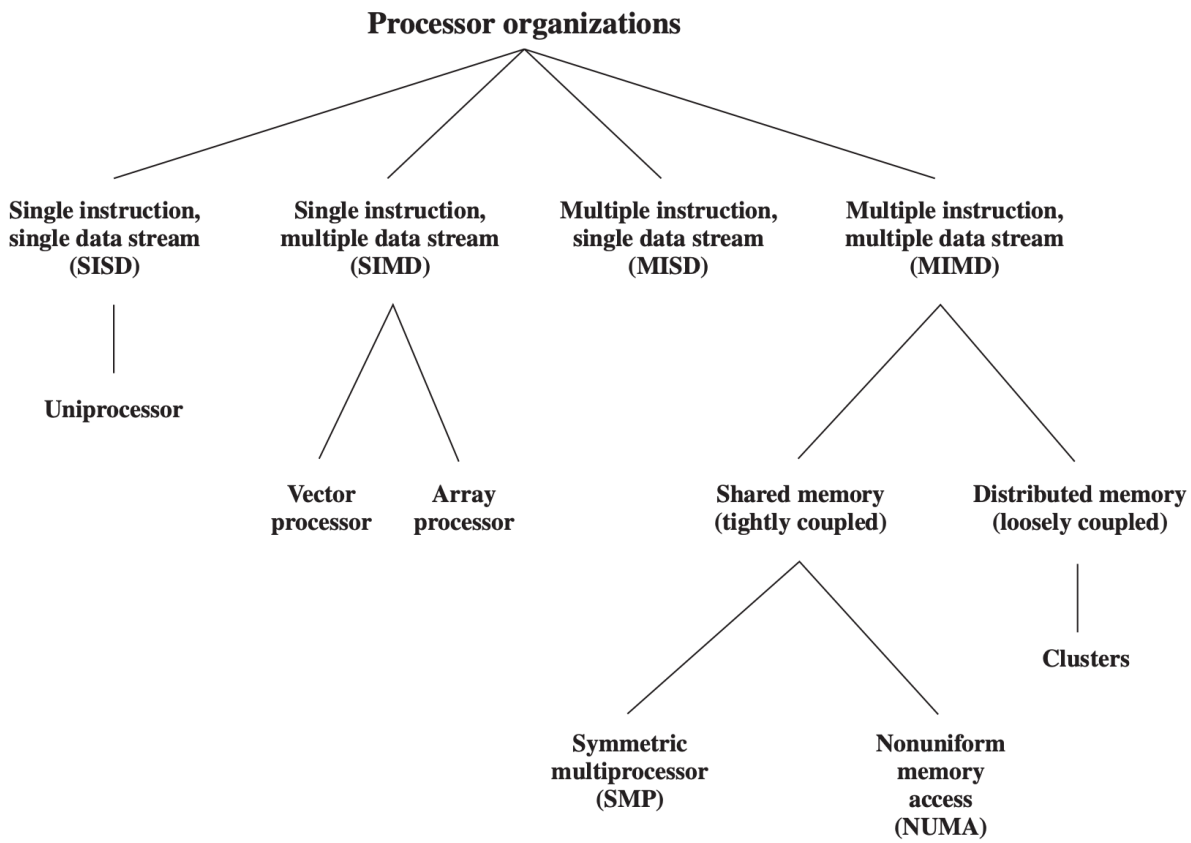


Figure 17.1 A Taxonomy of Parallel Processor Architectures

SMP – Symmetric Multiprocessors

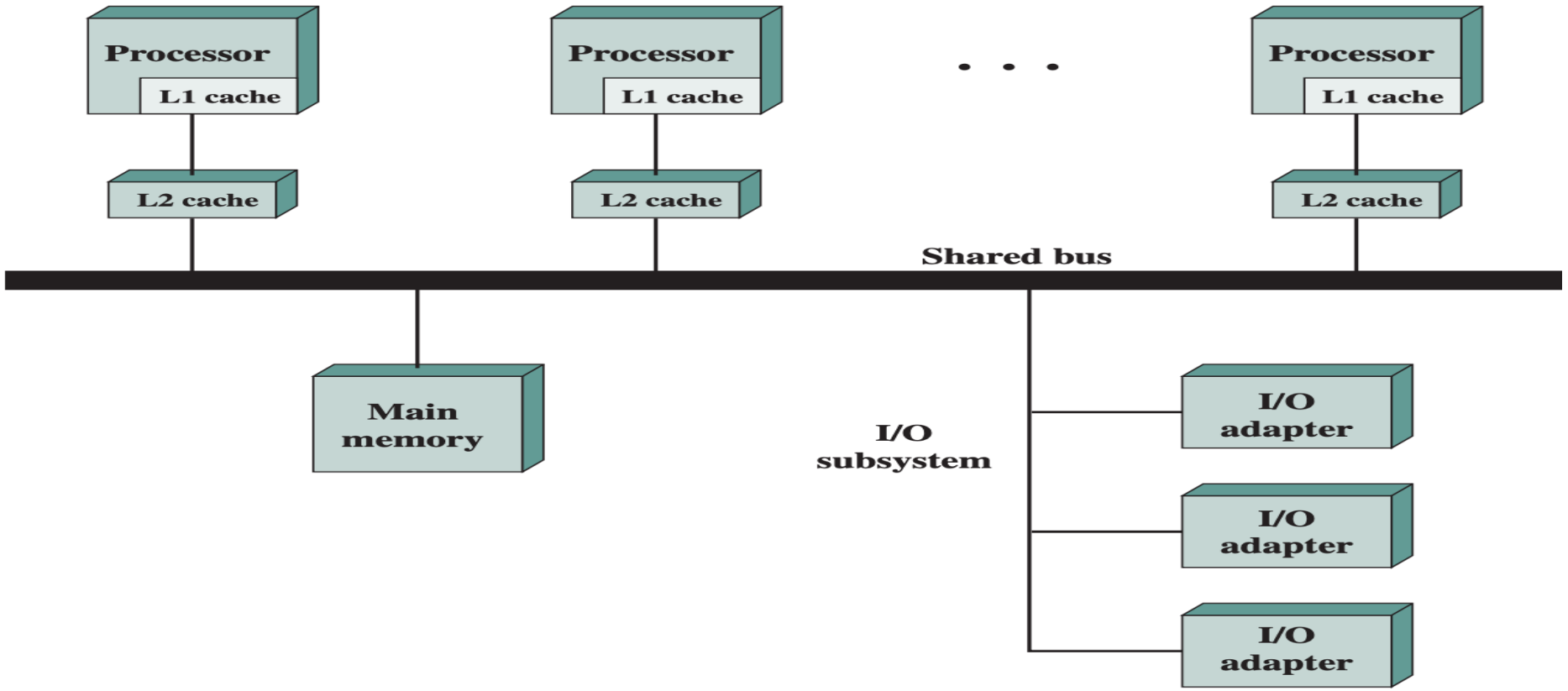


Figure 17.5 Symmetric Multiprocessor Organization

Multiprogramming vs. multiprocessing

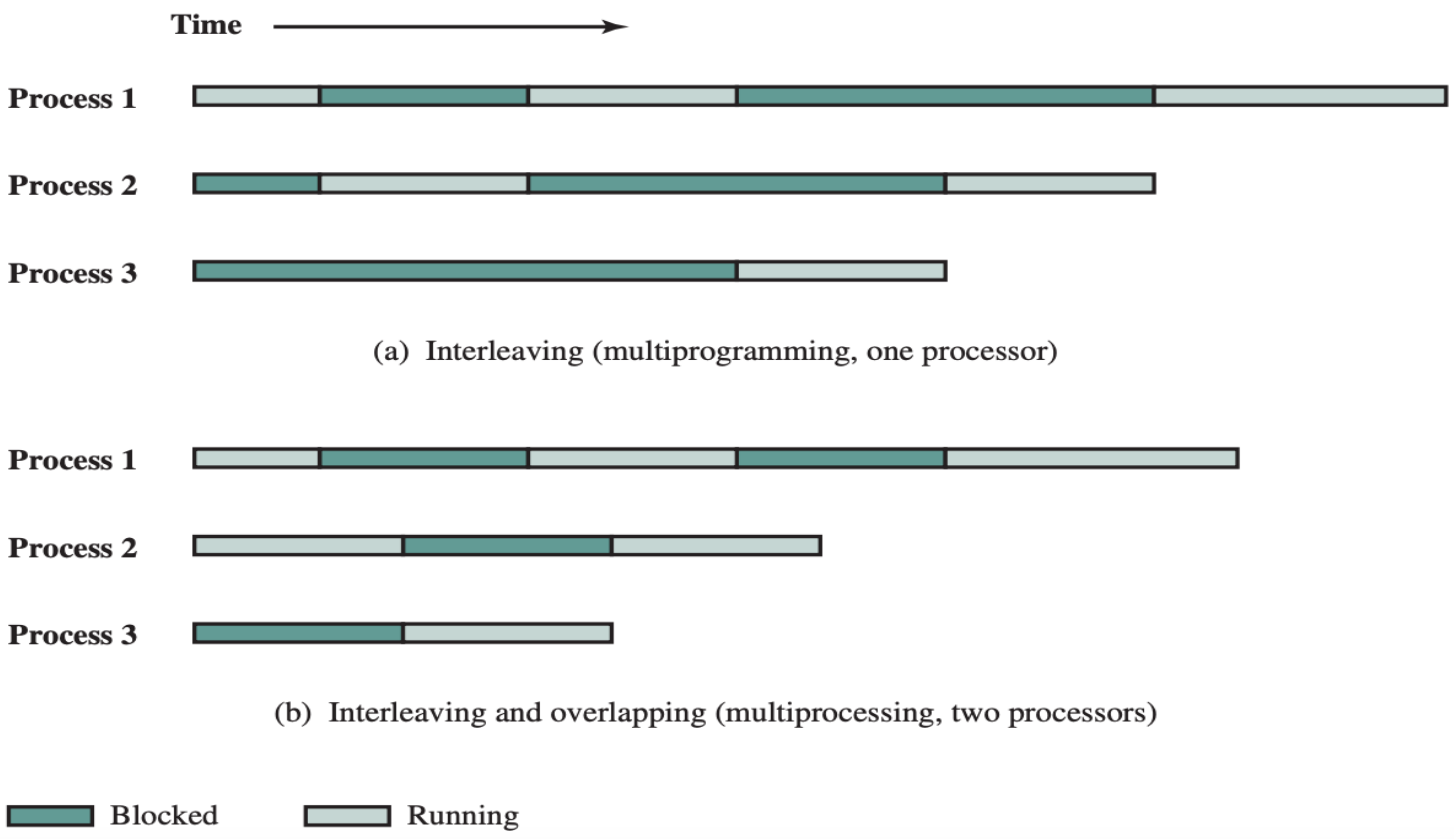


Figure 17.3 Multiprogramming and Multiprocessing

Cache line

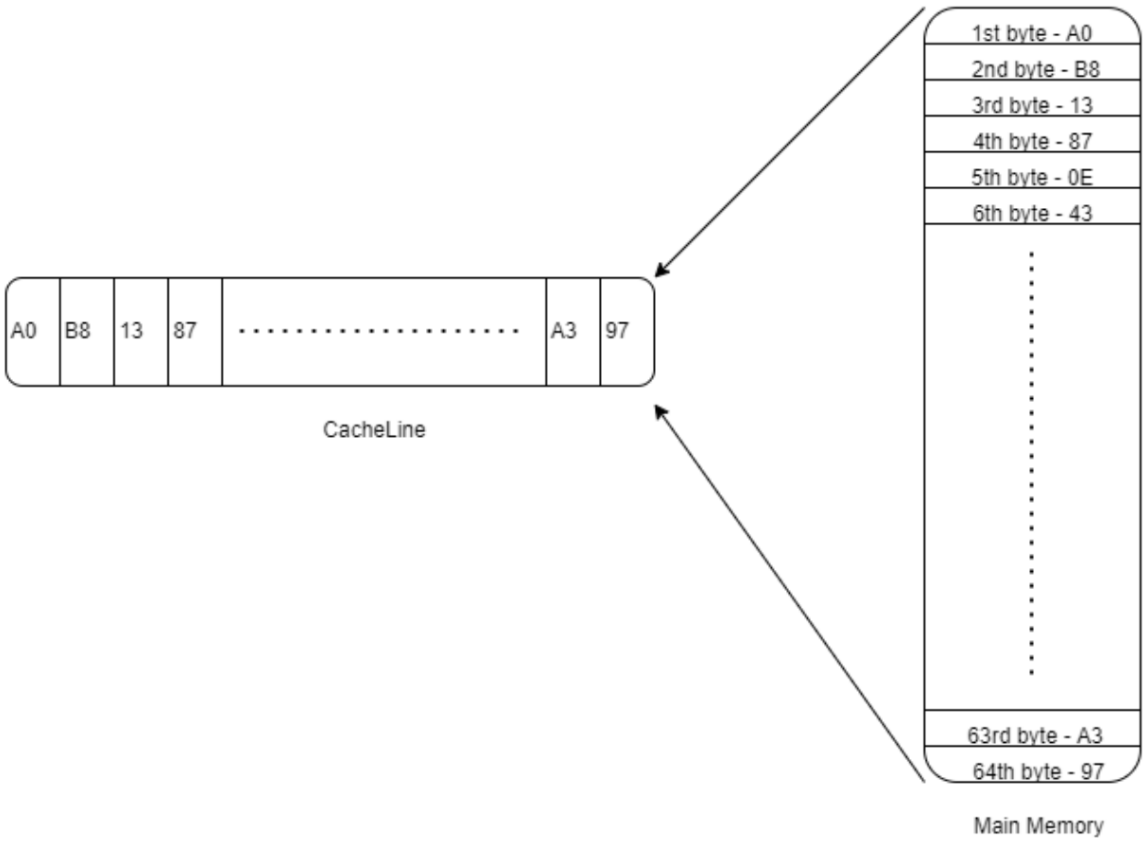
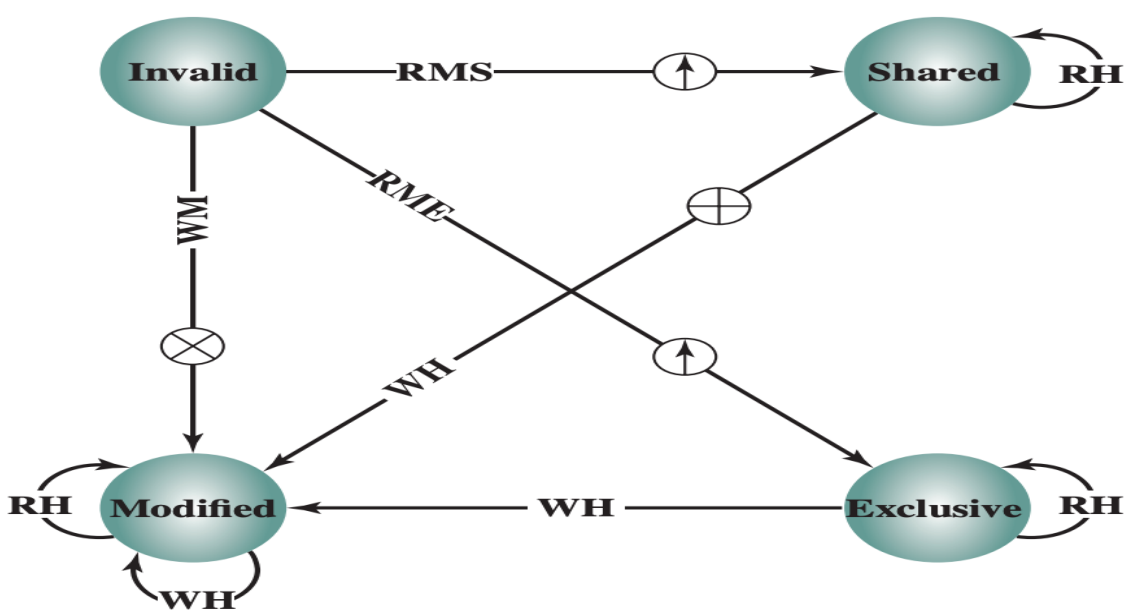

A0
B8
13
87
A3
97
CacheLine
1st byte - A0
2nd byte - B8
3rd byte - 13
4th byte - 87
5th byte - 0E
6th byte - 43
63rd byte - A3
64th byte - 97
Main Memory

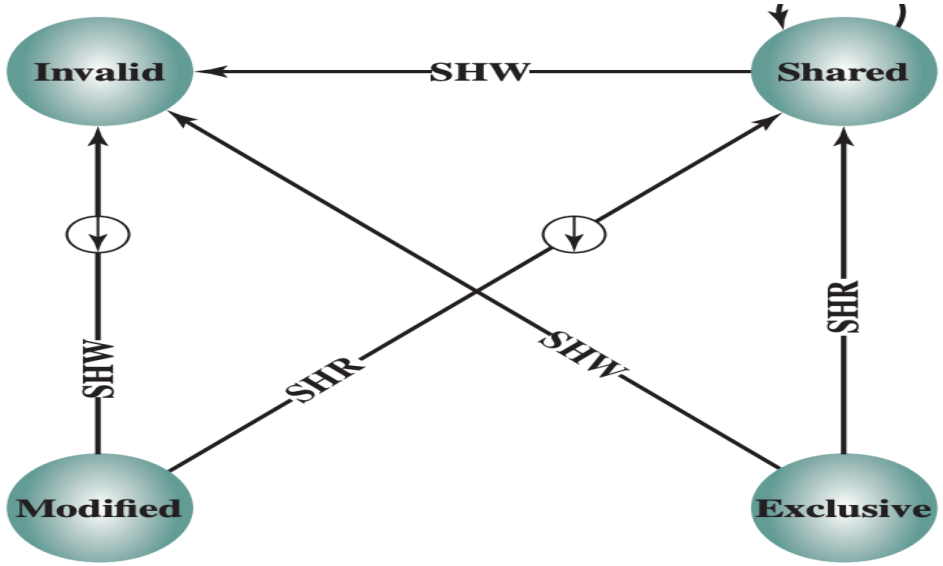
Table 17.1 MESI Cache Line States

	M **Modified**	**E** **Exclusive**	**S** **Shared**	**I** **Invalid**
This cache line valid?	Yes	Yes	Yes	No
The memory copy is …	out of date	valid	valid	—
Copies exist in other caches?	No	No	Maybe	Maybe
A write to this line …	does not go to bus	does not go to bus	goes to bus and updates cache	goes directly to bus

MESI Protocol: State Transitions



(a) Line in cache at initiating processor



(b) Line in snooping cache

RH = Read hit
RMS = Read miss, shared
RME = Read miss, exclusive
WH = Write hit
WM = Write miss
SHR = Snoop hit on read
SHW = Snoop hit on write or read-with-intent-to-modify

Dirty line copyback

Invalidate transaction

Read-with-intent-to-modify

Cache line fill