Development of a Phase Locked Loop (PLL) Systems Interface for RF Transceiver IC

University of Washington, Tacoma

August 2024

I. Project Outline:

This project focused on integrating a Phase Locked Loop (PLL) system with an RF transceiver IC chip. The PLL integration was achieved by connecting two additional main components to the transceiver: a multi-frequency PLL and a microcontroller. The PLL monitors the output frequency of the VCO inside the RF transceiver chip and makes micro-adjustments to the tuning voltage VTUNE to lock the free-running VCO in the transceiver chip. However, as the transceiver chip operates on multiple frequencies, a microcontroller is required to change the frequency the PLL is operating at and may also be used to change frequency band digital selection bits to quickly adjust the transceiver's VCO to operate more precisely anywhere inside its allowable frequency ranges.

As the VCO's output oscillation frequency is locked by the PLL, it allows for precise operation of the entire transceiver chip.

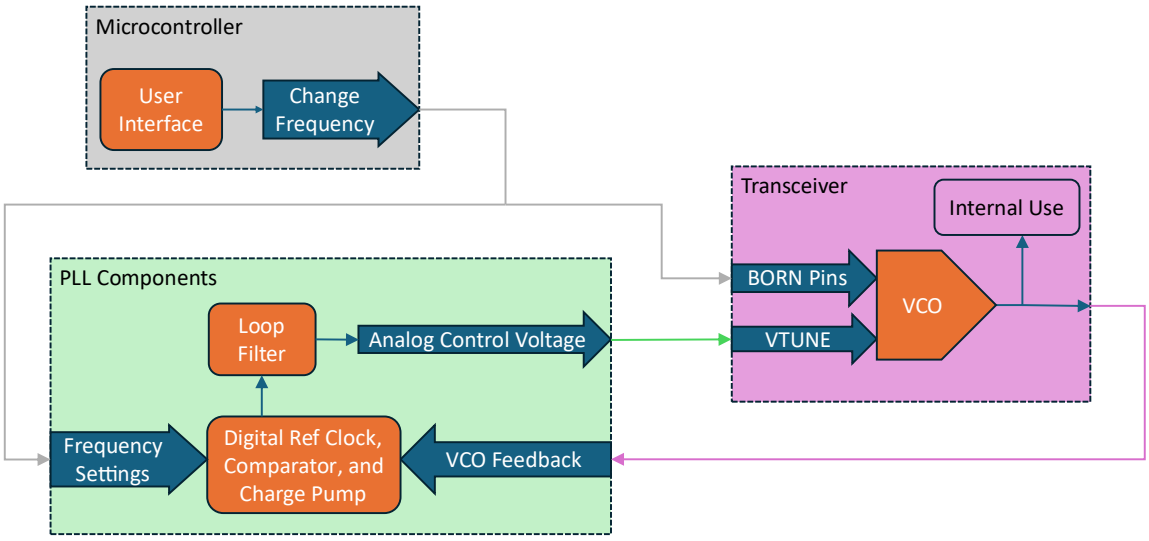

Figure 1: Project Map of Components.

II. Transceiver PCB:

The transceiver IC chip is mounted on a printed circuit board (PCB) and is shown in Figure 2 below. This circuit board allows access to the VTUNE analog voltage header pin to fine tune the VCO's output oscillation frequency within a selected frequency band using a supplied DC voltage. The PCB also provides access to the digital Bit Optimized Reconfigurable Network (BORN) pins which allow selecting between different frequency bands for coarse tuning by using the BORN pins as digital switches.

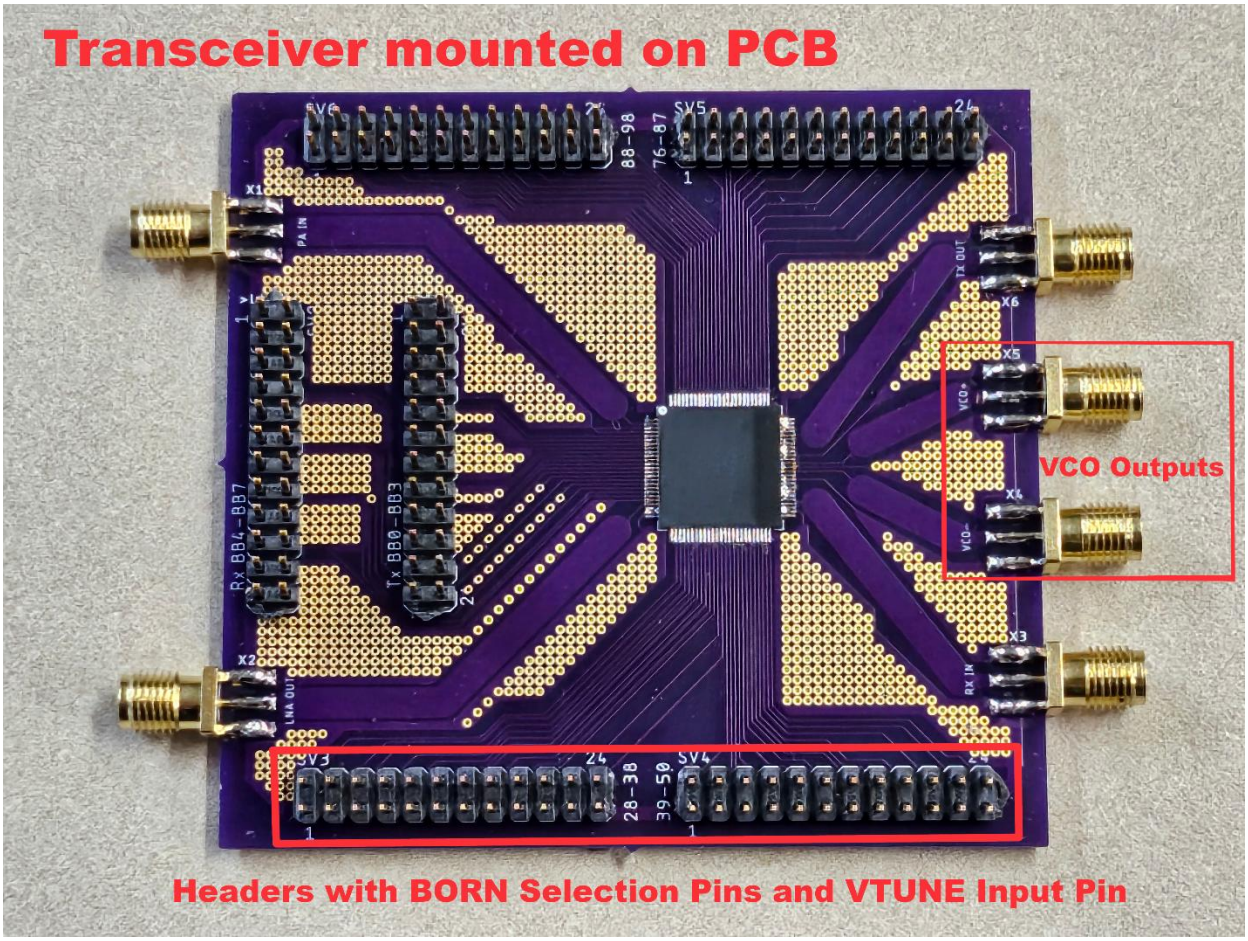

Figure 2: RF Transceiver IC chip.

III. ADF4159 PLL Evaluation Board:

The Analog Devices ADF4159 PLL was selected for implementation, as it is reprogrammable over a 3-wire serial connection to function at all currently supported VCO output frequencies without changes to clock R division settings (allowing very fast performance), while also providing additional coverage for future VCO frequencies up to 13 GHz. The integer and fractional division resolution also allows frequency target selection down to 1 Hz.

A full ADF4159 evaluation board was used in testing which hosts a reference clock, the ADF4159 PLL chip itself (containing both the comparator and charge pump elements), a microcontroller to change PLL settings, an op-amp for the loop filter, as well as empty solder points to add resistors and capacitors to complete the loop filter. As this PLL evaluation board operates over a large range of frequencies and may be used for different purposes, the loop filter resistor and capacitor values must be calculated to optimize performance based on application. After calculating loop filter values and soldering components into place, the evaluation board allowed initial testing of the PLL with the transceiver PCB without any additional circuits, as the evaluation board houses all the additional components required to operate the bare PLL chip.

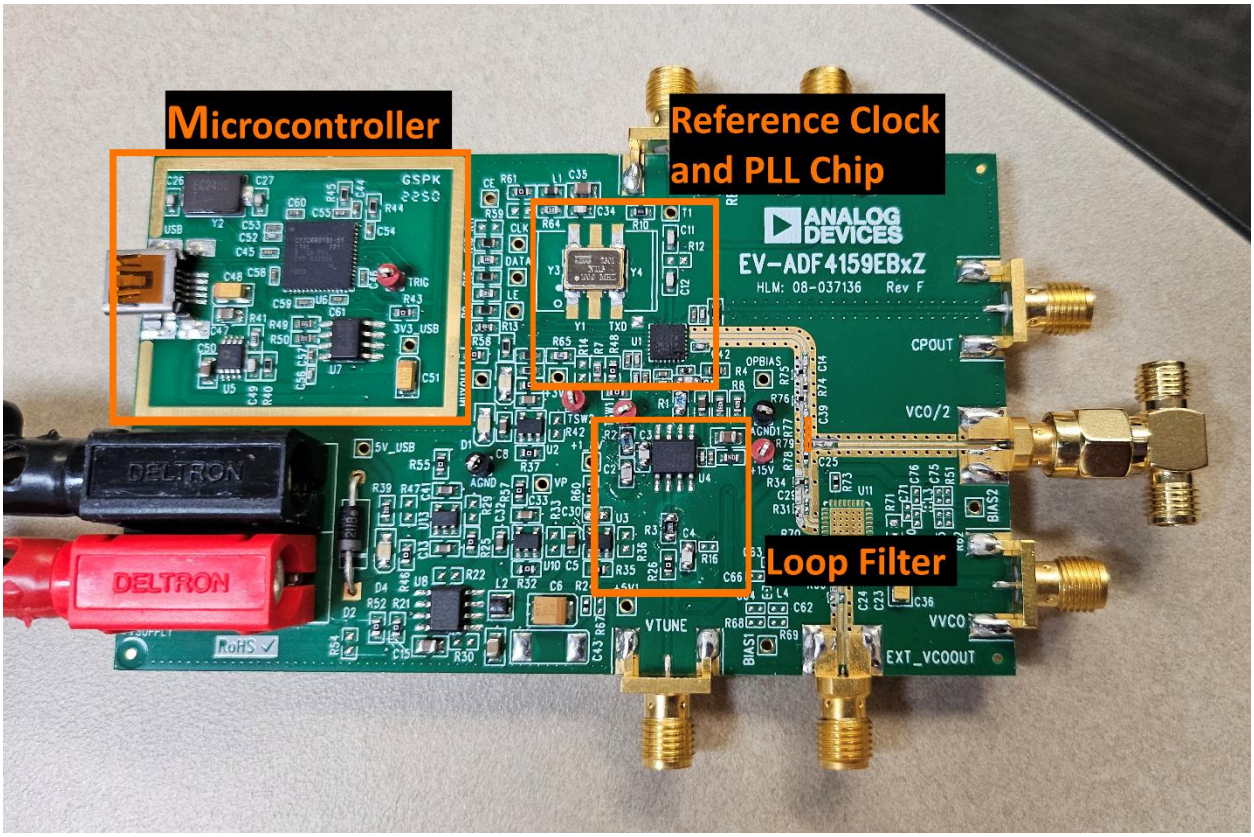

Figure 3: ADF4159 Evaluation Board.

IV. Initial Testing:

The VCO output was connected to the PLL frequency input, the PLL output was connected to the VCO VTUNE input, the PLL's microcontroller was connected to a PC over USB, and power was provided to the system. With this test setup, frequency bands were changed by manually providing power to the BORN digital bit selection pins on the transceiver PCB. Analog Devices evaluation software was used to set the PLL's frequency and other settings using the USB connection from PC to the onboard microcontroller testing one frequency band at a time, and then manually changing to another.

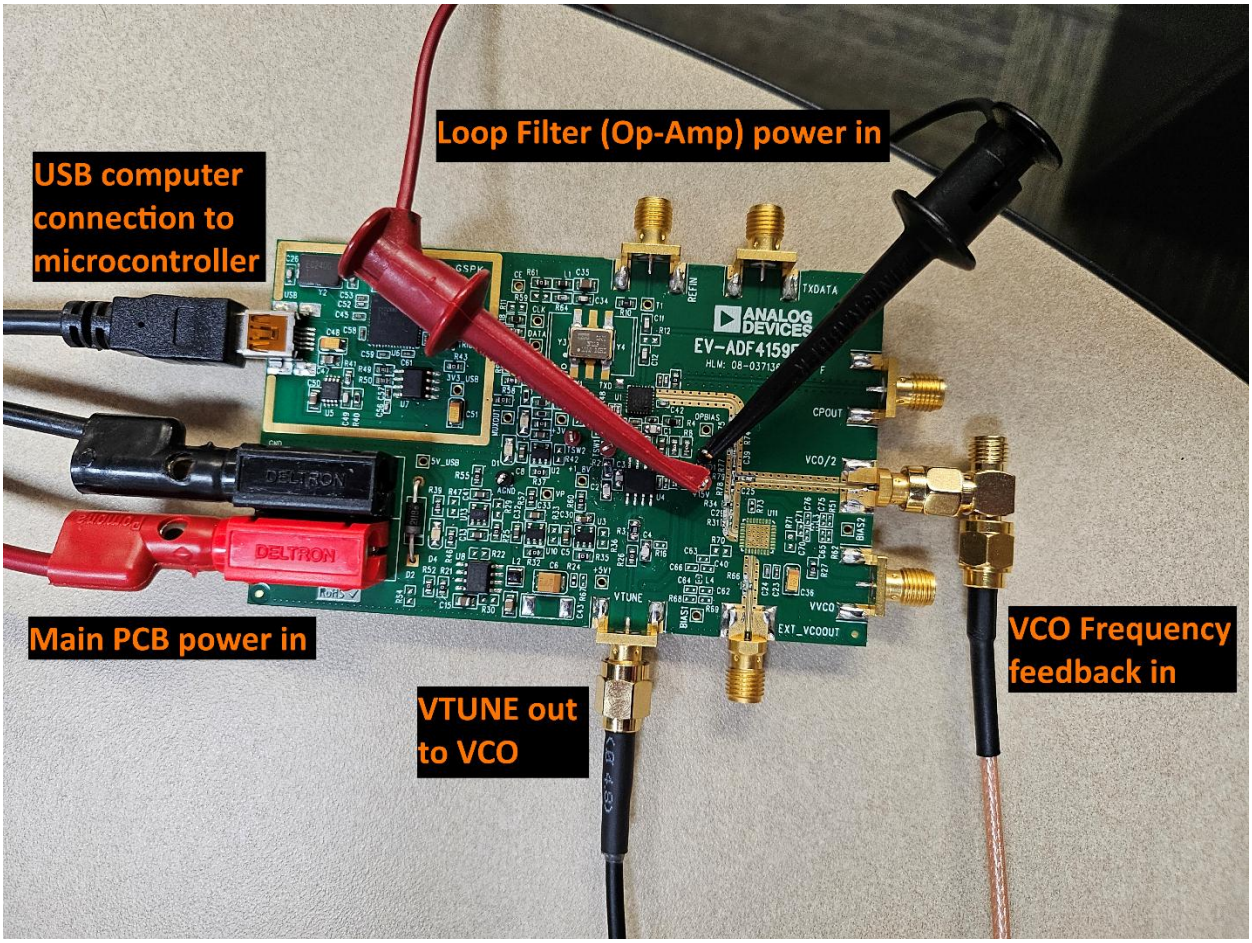

Figure 4: ADF4159 Evaluation Board connected to Transceiver chip on PCB and PC.

The VCO output from the transceiver chip on PCB was connected both to the PLL evaluation board for feedback as well as an oscilloscope for monitoring performance using a T-connector to share the signal between multiple devices. Viewing the VCO frequency output through an oscilloscope set to a fast Fourier transform (FFT) mode, a significant cleanup of the VCO output could be seen when the PLL was enabled, with undesired frequency swing of the output frequency dropping by many orders of magnitude.

First, the VCO was left free running without PLL assistance, and a video of the oscilloscope set to measure the output frequency was recorded. A variation in frequency around 0.4 MHz could be observed over a few seconds in the video. 3 frames of the measured output video were overlayed to create an image representing a simple time-lapse of the VCO output.

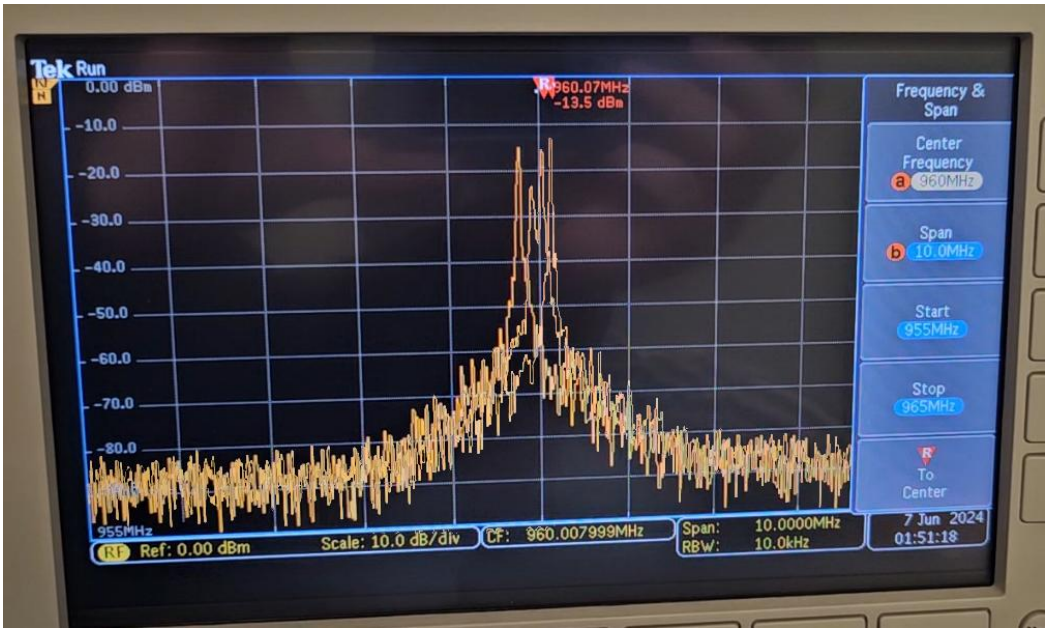

Figure 5: Time lapse representation of VCO output made by overlaying multiple frames of a video.

The PLL was then enabled with the results displayed on the oscilloscope. No variation to the peak frequency was observed at the maximum resolution of the oscilloscope while the PLL was enabled.

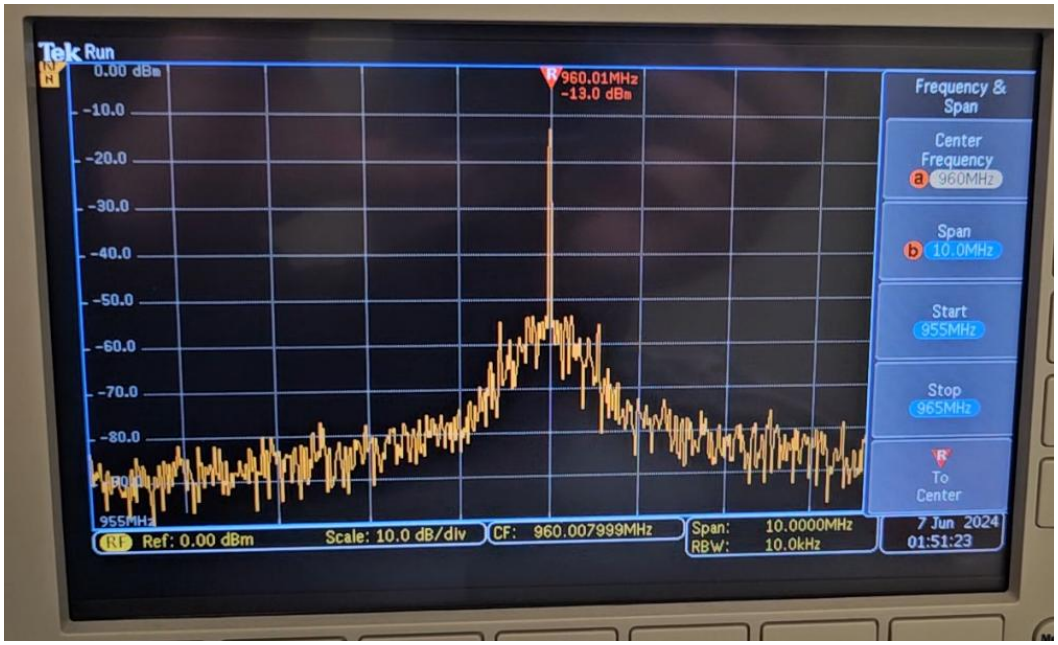

Figure 6: Locked VCO output with PLL enabled.

V. ESP32 Microcontroller Implementation:

After the successful testing of the evaluation board, an ESP32 microcontroller was selected to bypass the evaluation board's built-in microcontroller, and software was written to replace Analog Devices' USB control software wirelessly and to host additional features for laboratory testing. The ESP32 allows for wireless communication over Bluetooth low energy (BLE) or Wi-Fi and rapid prototyping using C++, along with a high clock rate and fast pin switching speeds for digital control signals. Additionally, the processor contains two cores which facilitate multitasking between wireless communication protocols and user programs. These features made the ESP32 ideal to quickly incorporate into the testing environment.

C++ firmware was written for the ESP32 microcontroller, and a companion application to control it over Bluetooth was written in JavaScript using HTML to create the graphic interface for viewing the application in a web browser. Since only a JavaScript enabled web browser is needed, this method of application design allows controlling the ESP32 and PLL over Bluetooth using either a PC or smartphone in the laboratory environment, without needing to make separate applications for each.

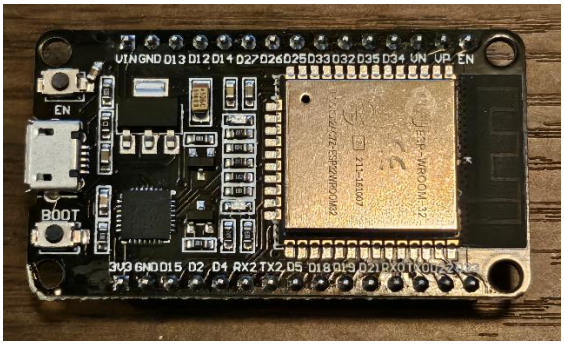

Figure 7: ESP32 Development Board.

The new control software is displayed in Figure 9 and is designed specifically for use in the research and development of Dr. Hamidi's transceiver IC. The software is displayed on a PC or smartphone web browser, allowing the user to connect to the ESP32 over a Bluetooth connection. After connection, the currently set frequency and PLL register values are read from the ESP32 and displayed in the user application. Default values are sent to the BORN pins and PLL registers on powerup of the ESP32. These internal programmable registers control all PLL settings including R division and integer/fractional values (with these settings controlling the VCO's frequency), negative bleed current, ramping, shift keying, and all other settings supported by the ADF4159. The register values are sent over a data/clock/latch 3-wire serial connection, and with fast pin switching options enabled in the control software only 16 µs is required to transmit the 3 registers needed to change the PLL's frequency target. Slower data transmissions may be enabled for easier debugging at lower speed using inexpensive logic analyzers.

Figure 8: PulseView logic analyzer recording of R0, R1, and R2 values transmitting to the PLL in 15.64 µs.

Figure 9: Custom ESP32 interface software displayed on a web browser, in initialization state.

Entering a new frequency target into the user interface drives both the BORN pins as well as the serial data to the PLL, removing the requirement to manually change BORN bits. Any frequency supported by the transceiver on any of its frequency bands may be entered and then immediately observed on the oscilloscope.

Settings to test automatic frequency hopping by driving the PLL and BORN pins with the ESP32 were also written into the user interface. The hopping mode was able to automatically span any smaller portion, or the entire range of frequencies supported by the transceiver, using user defined spacing of frequency jumps. Hopping as fast as 30 µs was achievable using the ESP32 in testing. Hopping at that fast of an interval required the ESP32 to run as quickly as possible by disabling BLE data updates/responses to the user application. The ESP32 is still able to receive new commands over Bluetooth with this BLE return data disabled, with the hopping performance observable on the oscilloscope.

VI. Conclusions:

The PLL implementation using the evaluation board was successful with a significant improvement of VCO oscillation frequency locking, and all benefits on frequency stability using the PLL were retained when implementing the ESP32 microcontroller to bypass the evaluation PCB's onboard microcontroller and software. This means that full use of the ADF4159 is currently possible using a custom PCB and microcontroller instead of relying on the evaluation board, requiring only design work and programming to transition to a tailor-made solution. The ESP32 is also powerful enough to enable additional features in future lab testing beyond PLL manipulation. There are currently plans to send and receive transmissions through the transceiver and to control other digital settings in addition to the BORN pins by expanding the ESP32 programming.

Meanwhile, progress is also being made to develop an in-house replacement for the ADF4159 to explore the feasibility of creating our own PLL solution, potentially using discrete components, a new discrete IC design, or implementation inside the transceiver IC itself. Selecting between these options will depend on further research.

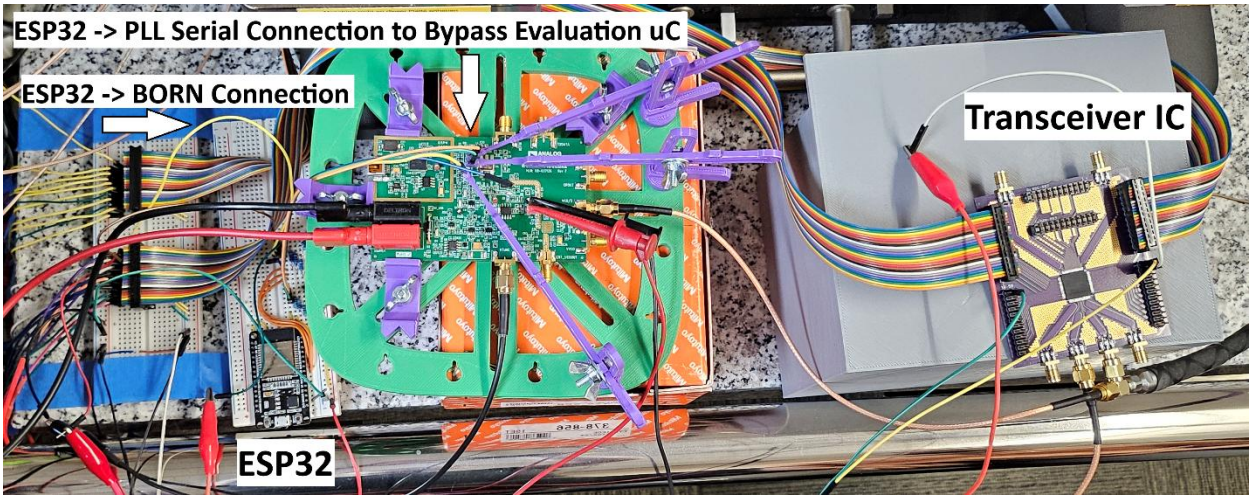

Figure 10: Lab testing setup of ESP32, ADF4159, and Transceiver together.

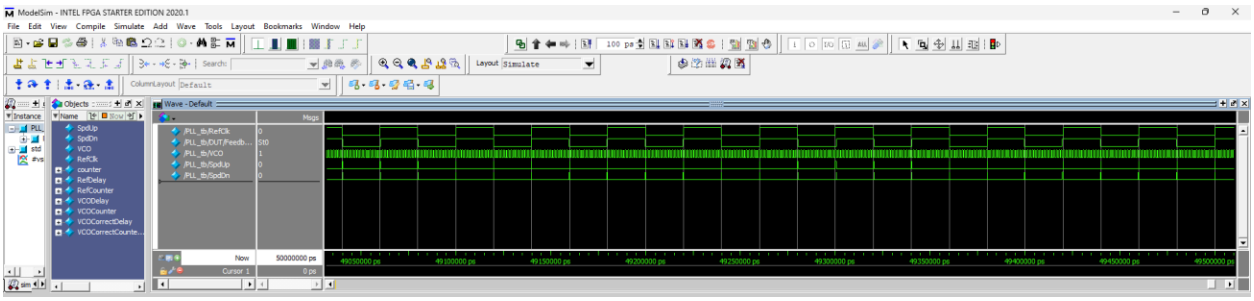

Figure 11: ModelSim simulation of FPGA-driven PLL solution to model feasibility of ADF4159 replacement.

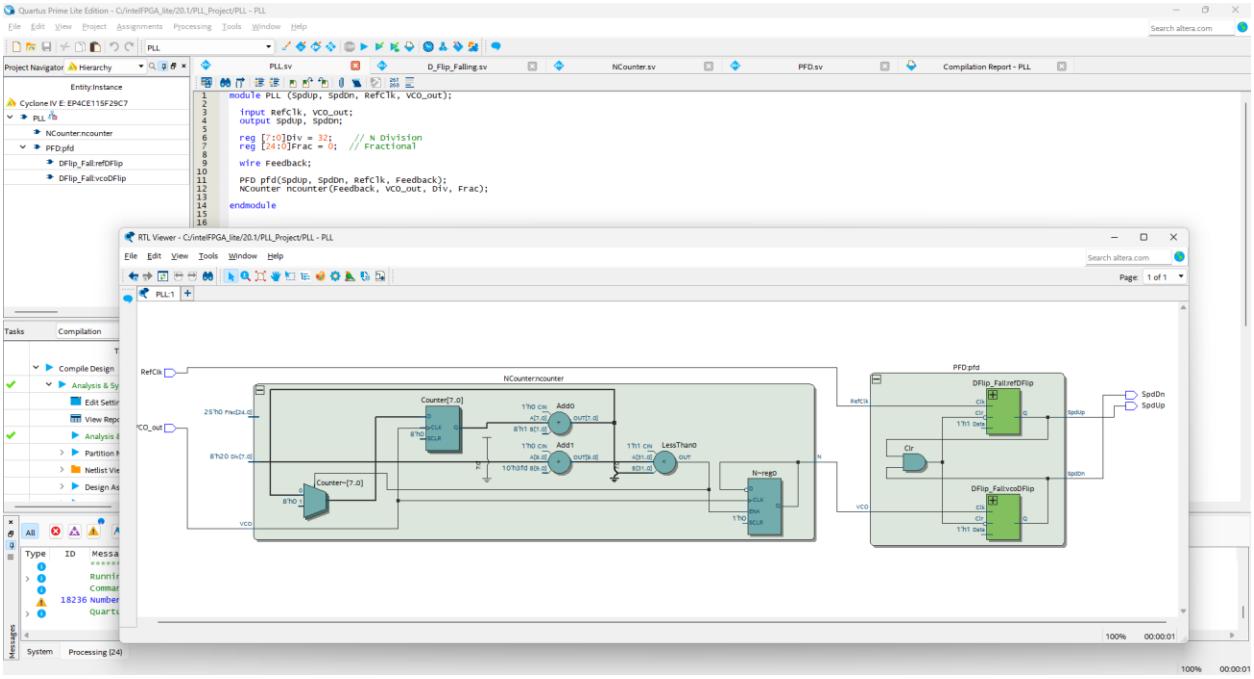

Figure 12: Quartus hardware synthesis to model a PLL on FPGA with a programmable frequency target.

VII. References:

[1] S. B. Hamidi and D. Dawn "A 2-Bit Voltage-Controlled Oscillator (VCO) for Multiband Wireless Applications," IEEE Microwave and Wireless Components Letters, vol. 32, no. 11, pp. 1307-1310, 2022.