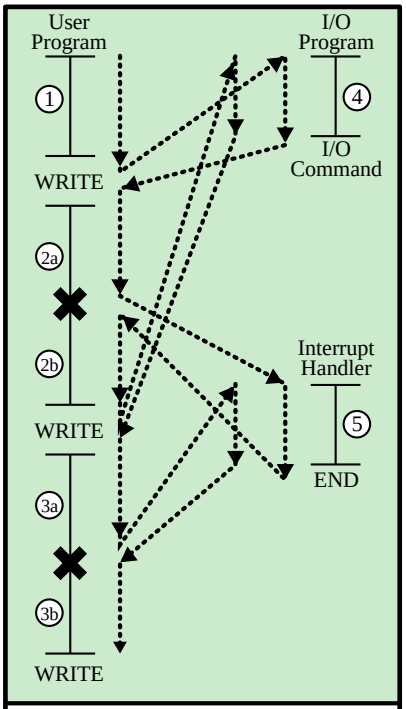
1. Refer to the diagram on the right. What could happen when the I/O operation takes much more time than executing the code segment 2 or 3 of the user program, i.e., the user program reaches the second WRITE call before the I/O operation called by the first one is completed?



(b) Interrupts; short I/O wait

2. What is ***multiprogramming***? How is it different from ***multiprocessing***?

3. Consider a memory system with the following parameters:

Cache access time: 0.1 μs

Memory access time (time needed to load a word into the cache): 1 μs

Suppose we ignore the time required for the processor to determine whether a word is in cache or memory. What is the ***hit ratio*** in order to have an average time to access a word no more than 50% greater than the cache access time?
(Hit ratio: fraction of accesses that are found in the cache)

4. The ***principle of locality*** states that memory references tend to cluster. In the literature, there is a distinction between ***spatial locality*** and ***temporal locality***. Spatial locality refers to the tendency of execution to involve a number of memory locations that are clustered while temporal locality refers to the tendency for a processor to access memory locations that have been used recently.

a) Can you figure out strategies for exploiting spatial locality and temporal locality?

b) Consider the following code:

```
for (i=0; i<20; i++)
     for (j=0; j<10; j++)
          a[i]=a[i]*j;
```

(i) Give one example of the spatial locality in the code.

(ii) Give one example of the temporal locality in the code.

Self-test

Choose the best answer.

1. When an external device becomes ready to be serviced by the processor the device sends a(n) _____ signal to the processor.
   A. access
   B. halt
   C. handler
   D. interrupt

2. Which of the following is the correct sequence of hardware events after the I/O device issues an interrupt signal to the processor?
   (i) Processor loads new PC value based on interrupt
   (ii) Processor finishes execution of current instruction
   (iii) Processor pushes PSW and PC onto control stack
   A. (iii), (ii), (i)
   B. (ii), (i), (iii)
   C. (ii), (iii), (i)
   D. None of the above

3. In a uniprocessor system, multiprogramming increases processor efficiency by:
   A. Increasing processor speed
   B. Taking advantage of time wasted by long wait I/O operations
   C. Disabling all interrupts except those of highest priority
   D. All of the above

4. Which of the following are the benefit of multiprogramming?
   A. Shorter mean response time
   B. Higher resource utilization
   C. Higher throughput
   D. All of the above

5. Which of the following characteristics distinguish the various elements of a memory hierarchy?
   A. Cost
   B. Capacity
   C. Access time
   D. All of the above

6. The unit of data exchanged between cache and main memory is _____ .
   A. block size
   B. map size
   C. word size
   D. slot size