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1  #ifndef _32MC204REGSV1_H_
2  #define _32MC204REGSV1_H_
3  #include <stdint.h>
4
5  #define _IO volatile uint16_t
6
7  #define STATUS_BASE      0x0042
8  #define CORCON_BASE      0x0044
9  #define MODCON_BASE      0x0046
10 #define XMODSRT_BASE     0x0048
11 #define XMODEND_BASE     0x004A
12 #define YMODSRT_BASE     0x004C
13 #define YMODEND_BASE     0x004E
14 #define XBREV_BASE       0x0050
15 #define DISICNT_BASE     0x0052
16
17
18 #define CNEN1_BASE        0x0060
19 #define CNEN2_BASE        0x0062
20 #define CNPU1_BASE        0x0068
21 #define CNPU2_BASE        0x006A
22
23
24
25 #define INTCON1_BASE      0x0080
26 #define INTCON2_BASE      0x0082
27 #define IFS0_BASE         0x0084
28 #define IFS1_BASE         0x0086
29 #define IFS3_BASE         0x008A
30 #define IFS4_BASE         0x008C
31 #define IEC0_BASE         0x0094
32 #define IEC1_BASE         0x0096
33 #define IEC3_BASE         0x009A
34 #define IEC4_BASE         0x009C
35 #define IPC0_BASE         0x00A4
36 #define IPC1_BASE         0x00A6
37 #define IPC2_BASE         0x00A8
38 #define IPC3_BASE         0x00AA
39 #define IPC4_BASE         0x00AC
40 #define IPC5_BASE         0x00AE
41 #define IPC7_BASE         0x00B2
42 #define IPC14_BASE        0x00C0
43 #define IPC15_BASE        0x00C2
44 #define IPC16_BASE        0x00C8
45 #define IPC18_BASE        0x00A4
46 #define INTTREG_BASE      0x00E0
47
48 #define TMR1_BASE         0x0100
49 #define PR1_BASE          0x0102
50 #define T1CON_BASE        0x0104
51 #define TMR2_BASE         0x0106
52 #define TMR3HLD_BASE      0x0108
53 #define TMR3_BASE         0x010A
54 #define PR2_BASE          0x010C
55 #define PR3_BASE          0x010E
56 #define T2CON_BASE        0x0110
57 #define T3CON_BASE        0x0112
58
59 #define IC1BUF_BASE       0x0140
60 #define IC1CON_BASE       0x0142
61 #define IC2BUF_BASE       0x0144
62 #define IC2CON_BASE       0x0146
63 #define IC7BUF_BASE       0x0158
64 #define IC7CON_BASE       0x015A
65 #define IC8BUF_BASE       0x015C
66 #define IC8CON_BASE       0x015E
67
68 #define OC1RS_BASE        0x0180
69 #define OC1R_BASE         0x0182
70 #define OC1CON_BASE       0x0184
71 #define OC2RS_BASE        0x0186
72 #define OC2R_BASE         0x0188
73 #define OC2CON_BASE       0x018A

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74
75 #define P1TCON_BASE      0x01C0
76 #define P1TMR_BASE      0x01C2
77 #define P1TPER_BASE     0x01C4
78 #define P1SECMF_BASE    0x01C6
79 #define PWM1CON1_BASE   0x01C8
80 #define PWM1CON2_BASE   0x01CA
81 #define P1DTCON1_BASE   0x01CC
82 #define P1DTCON2_BASE   0x01CE
83 #define P1FLTACON_BASE  0x01D0
84 #define P1OVDCON_BASE   0x01D4
85 #define P1DC1_BASE      0x01D6
86 #define P1DC2_BASE      0x01D8
87 #define P1DC3_BASE      0x01DA
88
89 #define P2TCON_BASE      0x05C0
90 #define P2TMR_BASE      0x05C2
91 #define P2TPER_BASE     0x05C4
92 #define P2SECMF_BASE    0x05C6
93 #define PWM2CON1_BASE   0x05C8
94 #define PWM2CON2_BASE   0x05CA
95 #define P2DTCON1_BASE   0x05CC
96 #define P2DTCON2_BASE   0x05CE
97 #define P2FLTACON_BASE  0x05D0
98 #define P2OVDCON_BASE   0x05D4
99 #define P2DC1_BASE      0x05D6
100
101 #define QEI1CON_BASE     0x01E0
102 #define DFLT1CON_BASE    0x01E2
103 #define POS1CNT_BASE     0x01E4
104 #define MAX1CNT_BASE     0x01E6
105
106 #define I2C1RCV_BASE     0x0200
107 #define I2C1TRN_BASE     0x0202
108 #define I2C1BRG_BASE     0x0204
109 #define I2C1CON_BASE     0x0206
110 #define I2C1STAT_BASE    0x0208
111 #define I2C1ADD_BASE     0x020A
112 #define I2C1MSK_BASE     0x020C
113
114 #define U1MODE_BASE      0x0220
115 #define U1STA_BASE       0x0222
116 #define U1TXREG_BASE     0x0224
117 #define U1RXREG_BASE     0x0226
118 #define U1BRG_BASE       0x0228
119
120 #define SPI1STAT_BASE    0x0240
121 #define SPI1CON1_BASE    0x0242
122 #define SPI1CON2_BASE    0x0244
123 #define SPI1BUF_BASE     0x0248
124
125 #define ADC1BUF0_BASE    0x0300
126 #define ADC1BUF1_BASE    0x0302
127 #define ADC1BUF2_BASE    0x0304
128 #define ADC1BUF3_BASE    0x0306
129 #define ADC1BUF4_BASE    0x0308
130 #define ADC1BUF5_BASE    0x030A
131 #define ADC1BUF6_BASE    0x030C
132 #define ADC1BUF7_BASE    0x030E
133 #define ADC1BUF8_BASE    0x0310
134 #define ADC1BUF9_BASE    0x0312
135 #define ADC1BUFA_BASE    0x0314
136 #define ADC1BUFB_BASE    0x0316
137 #define ADC1BUFC_BASE    0x0318
138 #define ADC1BUFD_BASE    0x031A
139 #define ADC1BUFE_BASE    0x031C
140 #define ADC1BUFF_BASE    0x031E
141 #define AD1CON1_BASE     0x0320
142 #define AD1CON2_BASE     0x0322
143 #define AD1CON3_BASE     0x0324
144 #define AD1CHS123_BASE   0x0326
145 #define AD1CHS0_BASE     0x0328
146 #define AD1PCFGL_BASE    0x032C

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147 #define AD1CSSL_BASE      0x0330
148
149 #define RPINR0_BASE      0x0680
150 #define RPINR1_BASE      0x0682
151 #define RPINR3_BASE      0x0686
152 #define RPINR7_BASE      0x068E
153 #define RPINR10_BASE     0x0694
154 #define RPINR11_BASE     0x0696
155 #define RPINR12_BASE     0x0698
156 #define RPINR13_BASE     0x069A
157 #define RPINR14_BASE     0x069C
158 #define RPINR15_BASE     0x069E
159 #define RPINR18_BASE     0x06A4
160 #define RPINR20_BASE     0x06A8
161 #define RPINR21_BASE     0x06AA
162
163 #define RPOR0_BASE       0x06C0
164 #define RPOR1_BASE       0x06C2
165 #define RPOR2_BASE       0x06C4
166 #define RPOR3_BASE       0x06C6
167 #define RPOR4_BASE       0x06C8
168 #define RPOR5_BASE       0x06CA
169 #define RPOR6_BASE       0x06CC
170 #define RPOR7_BASE       0x06CE
171 #define RPOR8_BASE       0x06D0
172 #define RPOR9_BASE       0x06D2
173 #define RPOR10_BASE      0x06D4
174 #define RPOR11_BASE      0x06D6
175 #define RPOR12_BASE      0x06D8
176
177 #define TRISA_BASE       0x02C0
178 #define PORTA_BASE       0x02C2
179 #define LATA_BASE        0x02C4
180 #define ODCA_BASE        0x02C6
181
182 #define TRISB_BASE       0x02C8
183 #define PORTB_BASE       0x02CA
184 #define LATB_BASE        0x02CC
185 #define ODCB_BASE        0x02CE
186
187 #define TRISC_BASE       0x02D0
188 #define PORTC_BASE       0x02D2
189 #define LATC_BASE        0x02D4
190 #define ODCC_BASE        0x02D6
191
192 #define RCON_BASE        0x0740
193 #define OSCCON_BASE      0x0742
194 #define CLKDIV_BASE      0x0744
195 #define PLLFBD_BASE      0x0746
196 #define OSCTUN_BASE      0x0748
197
198 #define NVMCON_BASE      0x0760
199 #define NVMKEY_BASE      0x0766
200
201 #define PMD1_BASE        0x0770
202 #define PMD2_BASE        0x0772
203 #define PMD3_BASE        0x0774
204
205 /*****Strukture opisa registara*****/
206 typedef union {
207     struct {
208         _IO C:1;
209         _IO Z:1;
210         _IO OV:1;
211         _IO N:1;
212         _IO RA:1;
213         _IO IPL:3;
214         _IO DC:1;
215         _IO DA:1;
216         _IO SAB:1;
217         _IO OAB:1;
218         _IO SB:1;
219         _IO SA:1;

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220         _IO OB:1;
221         _IO OA:1;
222     };
223     struct {
224         _IO :5;
225         _IO IPL0:1;
226         _IO IPL1:1;
227         _IO IPL2:1;
228     };
229 }STATUSbits;
230
231 #define STATUS      ((STATUSbits*) (STATUS_BASE))
232 /*****
233 typedef union {
234     struct {
235         _IO IFb:1; //Morao sam mu iz 'IF' promijeniti naziv u 'IFb'.
236         _IO RND:1;
237         _IO PSV:1;
238         _IO IPL3:1;
239         _IO ACCSAT:1;
240         _IO SATDW:1;
241         _IO SATB:1;
242         _IO SATA:1;
243         _IO DL:3;
244         _IO EDT:1;
245         _IO US:1;
246     };
247     struct {
248         _IO :8;
249         _IO DL0:1;
250         _IO DL1:1;
251         _IO DL2:1;
252     };
253 }CORCONbits;
254
255 #define CORCON      ((CORCONbits*) (CORCON_BASE))
256 /*****
257 typedef union {
258     struct {
259         _IO XWM:4;
260         _IO YWM:4;
261         _IO BWM:4;
262         _IO :2;
263         _IO YMODEN:1;
264         _IO XMODEN:1;
265     };
266     struct {
267         _IO XWM0:1;
268         _IO XWM1:1;
269         _IO XWM2:1;
270         _IO XWM3:1;
271         _IO YWM0:1;
272         _IO YWM1:1;
273         _IO YWM2:1;
274         _IO YWM3:1;
275         _IO BWM0:1;
276         _IO BWM1:1;
277         _IO BWM2:1;
278         _IO BWM3:1;
279     };
280 }MODCONbits;
281
282 #define MODCON      ((MODCONbits*) (MODCON_BASE))
283 /*****
284 typedef union {
285     struct {
286         _IO XB:15;
287         _IO BREN:1;
288     };
289     struct {
290         _IO XB0:1;
291         _IO XB1:1;
292         _IO XB2:1;

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293         _IO XB3:1;
294         _IO XB4:1;
295         _IO XB5:1;
296         _IO XB6:1;
297         _IO XB7:1;
298         _IO XB8:1;
299         _IO XB9:1;
300         _IO XB10:1;
301         _IO XB11:1;
302         _IO XB12:1;
303         _IO XB13:1;
304         _IO XB14:1;
305     };
306 }XBREVbits;
307
308 #define XBREV      ((XBREVbits*)(XBREV_BASE))
309 /*****
310 //          STRUKTURE ZA KONTROLU CHANGE NOTIFICATION MODULA:
311 //
312 *****/
313 typedef union {
314     struct{
315         _IO CNEN1R:16;
316     };
317     struct{
318         _IO CN0IE:1;
319         _IO CN1IE:1;
320         _IO CN2IE:1;
321         _IO CN3IE:1;
322         _IO CN4IE:1;
323         _IO CN5IE:1;
324         _IO CN6IE:1;
325         _IO CN7IE:1;
326         _IO CN8IE:1;
327         _IO CN9IE:1;
328         _IO CN10IE:1;
329         _IO CN11IE:1;
330         _IO CN12IE:1;
331         _IO CN13IE:1;
332         _IO CN14IE:1;
333         _IO CN15IE:1;
334     };
335 }CNEN1bits;
336
337 #define CNEN1      ((CNEN1bits*)(CNEN1_BASE))
338 /*****
339 typedef union {
340     struct {
341         _IO CNEN2R:15;
342     };
343     struct {
344         _IO CN16IE:1;
345         _IO CN17IE:1;
346         _IO CN18IE:1;
347         _IO CN19IE:1;
348         _IO CN20IE:1;
349         _IO CN21IE:1;
350         _IO CN22IE:1;
351         _IO CN23IE:1;
352         _IO CN24IE:1;
353         _IO CN25IE:1;
354         _IO CN26IE:1;
355         _IO CN27IE:1;
356         _IO CN28IE:1;
357         _IO CN29IE:1;
358         _IO CN30IE:1;
359     };
360 }CNEN2bits;
361
362 #define CNEN2      ((CNEN2bits*)(CNEN2_BASE))
363 /*****
364 typedef union{
365 struct{

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366     _IO CNPU1R:16;
367 };
368 struct{
369     _IO CN0PUE:1;
370     _IO CN1PUE:1;
371     _IO CN2PUE:1;
372     _IO CN3PUE:1;
373     _IO CN4PUE:1;
374     _IO CN5PUE:1;
375     _IO CN6PUE:1;
376     _IO CN8PUE:1;
377     _IO CN9PUE:1;
378     _IO CN10PUE:1;
379     _IO CN11PUE:1;
380     _IO CN12PUE:1;
381     _IO CN13PUE:1;
382     _IO CN14PUE:1;
383     _IO CN15PUE:1;
384 };
385 }CNPU1bits;
386
387 #define CNPU1      ((CNPU1bits*)(CNPU1_BASE))
388 /*****
389 typedef union {
390 struct {
391     _IO CNPU2R:15;
392 };
393 struct {
394     _IO CN16PUE:1;
395     _IO CN17PUE:1;
396     _IO CN18PUE:1;
397     _IO CN19PUE:1;
398     _IO CN20PUE:1;
399     _IO CN21PUE:1;
400     _IO CN22PUE:1;
401     _IO CN23PUE:1;
402     _IO CN24PUE:1;
403     _IO CN25PUE:1;
404     _IO CN26PUE:1;
405     _IO CN27PUE:1;
406     _IO CN28PUE:1;
407     _IO CN29PUE:1;
408     _IO CN30PUE:1;
409 };
410 }CNPU2bits;
411
412 #define CNPU2      ((CNPU2bits*)(CNPU2_BASE))
413 /*****
414 //          STRUKTURE I REGISTR ZA KONTROLU I STATUS PREKIDA:
415 //
416 /*****
417 typedef union{
418 struct {
419     _IO INTCON1R :16;
420 };
421 struct{
422     _IO :1;
423     _IO OSCFAIL:1;
424     _IO STKERR:1;
425     _IO ADDRERR:1;
426     _IO MATHERR:1;
427     _IO :1;
428     _IO DIV0ERR:1;
429     _IO SFTACERR:1;
430     _IO COVTE:1;
431     _IO OVBTE:1;
432     _IO OVATE:1;
433     _IO COVBERR:1;
434     _IO COVAERR:1;
435     _IO OVBERR:1;
436     _IO OVAERR:1;
437     _IO NSTDIS:1;
438 };

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```

439 }INTCON1bits;
440
441 #define INTCON1 ((INTCON1bits*)(INTCON1_BASE))
442 /*****
443 typedef union {
444     struct{
445         _IO INT0EP:1;
446         _IO INT1EP:1;
447         _IO INT2EP:1;
448         _IO :11;
449         _IO DISI:1;
450         _IO ALTIPT:1;
451     };
452 }INTCON2bits;
453
454 #define INTCON2 ((INTCON2bits*)(INTCON2_BASE))
455 /*****
456 typedef union{
457     struct{
458         _IO INT0IF:1;
459         _IO IC1IF:1;
460         _IO OC1IF:1;
461         _IO T1IF:1;
462         _IO :1;
463         _IO IC2IF:1;
464         _IO OC2IF:1;
465         _IO T2IF:1;
466         _IO T3IF:1;
467         _IO SPI1EIF:1;
468         _IO SPI1IF:1;
469         _IO U1RXIF:1;
470         _IO U1TXIF:1;
471         _IO AD1IF:1;
472     };
473 }IFS0bits;
474
475 #define IFS0 ((IFS0bits*)(IFS0_BASE))
476 /*****
477 typedef union {
478     struct {
479         _IO SI2C1IF:1;
480         _IO MI2C1IF:1;
481         _IO :1;
482         _IO CNIF:1;
483         _IO INT1IF:1;
484         _IO :1;
485         _IO IC7IF:1;
486         _IO IC8IF:1;
487         _IO :5;
488         _IO INT2IF:1;
489     };
490     struct {
491         _IO SI2CIF:1;
492     };
493 }IFS1bits;
494
495 #define IFS1 ((IFS1bits*)(IFS1_BASE))
496 /*****
497 typedef union{
498     struct{
499         _IO :9;
500         _IO PWM1IF:1;
501         _IO QE1IF:1;
502         _IO :4;
503         _IO FLTA1IF:1;
504     };
505 }IFS3bits;
506
507 #define IFS3 ((IFS3bits*)(IFS3_BASE))
508 /*****
509 typedef union{
510     struct{
511         _IO :1;

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512         _IO U1EIF:1;
513         _IO :7;
514         _IO PWM2IF:1;
515         _IO FLTA2IF:1;
516     };
517 }IFS4bits;
518
519 #define IFS4      ((IFS4bits*) (IFS4_BASE))
520 /*****
521 typedef union{
522     struct{
523         _IO INTOIE:1;
524         _IO IC1IE:1;
525         _IO OC1IE:1;
526         _IO T1IE:1;
527         _IO :1;
528         _IO IC2IE:1;
529         _IO OC2IE:1;
530         _IO T2IE:1;
531         _IO T3IE:1;
532         _IO SPI1EIE:1;
533         _IO SPI1IE:1;
534         _IO U1RXIE:1;
535         _IO U1TXIE:1;
536         _IO AD1IE:1;
537     };
538 }IEC0bits;
539
540 #define IEC0      ((IEC0bits*) (IEC0_BASE))
541 /*****
542 typedef union {
543     struct {
544         _IO SI2C1IE:1;
545         _IO MI2C1IE:1;
546         _IO :1;
547         _IO CNIE:1;
548         _IO INT1IE:1;
549         _IO :1;
550         _IO IC7IE:1;
551         _IO IC8IE:1;
552         _IO :5;
553         _IO INT2IE:1;
554     };
555     struct {
556         _IO SI2CIE:1;
557     };
558 }IEC1bits;
559
560 #define IEC1      ((IEC1bits*) (IEC1_BASE))
561 /*****
562 typedef union {
563     struct{
564         _IO :9;
565         _IO PWM1IE:1;
566         _IO QE1IE:1;
567         _IO :4;
568         _IO FLTA1IE:1;
569     };
570 }IEC3bits;
571
572 #define IEC3      ((IEC3bits*) (IEC3_BASE))
573 /*****
574 typedef union{
575     struct{
576         _IO :1;
577         _IO U1EIE:1;
578         _IO :7;
579         _IO PWM2IE:1;
580         _IO FLTA2IE:1;
581     };
582 }IEC4bits;
583
584 #define IEC4      ((IEC4bits*) (IEC4_BASE))

```



```

585  /*****
586  typedef union {
587      struct {
588          _IO INT0IP:3;
589          _IO :1;
590          _IO IC1IP:3;
591          _IO :1;
592          _IO OC1IP:3;
593          _IO :1;
594          _IO T1IP:3;
595      };
596      struct {
597          _IO INT0IP0:1;
598          _IO INT0IP1:1;
599          _IO INT0IP2:1;
600          _IO :1;
601          _IO IC1IP0:1;
602          _IO IC1IP1:1;
603          _IO IC1IP2:1;
604          _IO :1;
605          _IO OC1IP0:1;
606          _IO OC1IP1:1;
607          _IO OC1IP2:1;
608          _IO :1;
609          _IO T1IP0:1;
610          _IO T1IP1:1;
611          _IO T1IP2:1;
612      };
613  }IPC0bits;
614
615  #define IPC0 ((IPC0bits*)(IPC0_BASE))
616  /*****
617  typedef union {
618      struct {
619          _IO :4;
620          _IO IC2IP:3;
621          _IO :1;
622          _IO OC2IP:3;
623          _IO :1;
624          _IO T2IP:3;
625      };
626      struct {
627          _IO :4;
628          _IO IC2IP0:1;
629          _IO IC2IP1:1;
630          _IO IC2IP2:1;
631          _IO :1;
632          _IO OC2IP0:1;
633          _IO OC2IP1:1;
634          _IO OC2IP2:1;
635          _IO :1;
636          _IO T2IP0:1;
637          _IO T2IP1:1;
638          _IO T2IP2:1;
639      };
640  }IPC1bits;
641
642  #define IPC1 ((IPC1bits*)(IPC1_BASE))
643  /*****
644  typedef union {
645      struct {
646          _IO T3IP:3;
647          _IO :1;
648          _IO SPI1EIP:3;
649          _IO :1;
650          _IO SPI1IP:3;
651          _IO :1;
652          _IO U1RXIP:3;
653      };
654      struct {
655          _IO T3IP0:1;
656          _IO T3IP1:1;
657          _IO T3IP2:1;

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```

658         _IO :1;
659     _IO SPI1EIP0:1;
660     _IO SPI1EIP1:1;
661     _IO SPI1EIP2:1;
662         _IO :1;
663     _IO SPI1IP0:1;
664     _IO SPI1IP1:1;
665     _IO SPI1IP2:1;
666         _IO :1;
667     _IO U1RXIP0:1;
668     _IO U1RXIP1:1;
669     _IO U1RXIP2:1;
670 };
671 }IPC2bits;
672
673 #define IPC2      ((IPC2bits*)(IPC2_BASE))
674 /*****
675 typedef union {
676     struct {
677         _IO U1TXIP:3;
678         _IO :1;
679         _IO AD1IP:3;
680     };
681     struct {
682         _IO U1TXIP0:1;
683         _IO U1TXIP1:1;
684         _IO U1TXIP2:1;
685         _IO :1;
686         _IO AD1IP0:1;
687         _IO AD1IP1:1;
688         _IO AD1IP2:1;
689     };
690 }IPC3bits;
691
692 #define IPC3      ((IPC3bits*)(IPC3_BASE))
693 /*****
694 typedef union {
695     struct {
696         _IO SI2C1IP:3;
697         _IO :1;
698         _IO MI2C1IP:3;
699         _IO :5;
700         _IO CNIP:3;
701     };
702     struct {
703         _IO SI2C1IP0:1;
704         _IO SI2C1IP1:1;
705         _IO SI2C1IP2:1;
706         _IO :1;
707         _IO MI2C1IP0:1;
708         _IO MI2C1IP1:1;
709         _IO MI2C1IP2:1;
710         _IO :5;
711         _IO CNIP0:1;
712         _IO CNIP1:1;
713         _IO CNIP2:1;
714     };
715 }IPC4bits;
716
717 #define IPC4      ((IPC4bits*)(IPC4_BASE))
718 /*****
719 typedef union {
720     struct {
721         _IO INT1IP:3;
722         _IO :5;
723         _IO IC7IP:3;
724         _IO :1;
725         _IO IC8IP:3;
726     };
727     struct {
728         _IO INT1IP0:1;
729         _IO INT1IP1:1;
730         _IO INT1IP2:1;

```

```

731         _IO :5;
732     _IO IC7IP0:1;
733     _IO IC7IP1:1;
734     _IO IC7IP2:1;
735     _IO :1;
736     _IO IC8IP0:1;
737     _IO IC8IP1:1;
738     _IO IC8IP2:1;
739 };
740 }IPC5bits;
741
742 #define IPC5      ((IPC5bits*)(IPC5_BASE))
743 /*****
744 typedef union {
745     struct {
746         _IO :4;
747         _IO INT2IP:3;
748     };
749     struct {
750         _IO :4;
751         _IO INT2IP0:1;
752         _IO INT2IP1:1;
753         _IO INT2IP2:1;
754     };
755 }IPC7bits;
756
757 #define IPC7      ((IPC7bits*)(IPC7_BASE))
758 /*****
759 typedef union {
760     struct {
761         _IO :4;
762         _IO PWM1IP:3;
763         _IO :1;
764         _IO QEIIP:3;
765     };
766     struct {
767         _IO :4;
768         _IO PWM1IP0:1;
769         _IO PWM1IP1:1;
770         _IO PWM1IP2:1;
771         _IO :1;
772         _IO QEIIP0:1;
773         _IO QEIIP1:1;
774         _IO QEIIP2:1;
775     };
776 }IPC14bits;
777
778 #define IPC14      ((IPC14bits*)(IPC14_BASE))
779 /*****
780 typedef union {
781     struct {
782         _IO :12;
783         _IO FLTA1IP:3;
784     };
785     struct {
786         _IO :12;
787         _IO FLTA1IP0:1;
788         _IO FLTA1IP1:1;
789         _IO FLTA1IP2:1;
790     };
791 }IPC15bits;
792
793 #define IPC15      ((IPC15bits*)(IPC15_BASE))
794 /*****
795 typedef union {
796     struct {
797         _IO :4;
798         _IO U1EIP:3;
799     };
800     struct {
801         _IO :4;
802         _IO U1EIP0:1;
803         _IO U1EIP1:1;

```

```

804         _IO U1EIP2:1;
805     };
806 }IPC16bits;
807
808 #define IPC16      ((IPC16bits*)(IPC16_BASE))
809 /*****
810 typedef union {
811     struct {
812         _IO :4;
813         _IO PWM2IP:3;
814         _IO :1;
815         _IO FLTA2IP:3;
816     };
817     struct {
818         _IO :4;
819         _IO PWM2IP0:1;
820         _IO PWM2IP1:1;
821         _IO PWM2IP2:1;
822         _IO :1;
823         _IO FLTA2IP0:1;
824         _IO FLTA2IP1:1;
825         _IO FLTA2IP2:1;
826     };
827 }IPC18bits;
828
829 #define IPC18      ((IPC18bits*)(IPC18_BASE))
830 /*****
831 typedef union {
832     struct {
833         _IO VECNUM:7;
834         _IO :1;
835         _IO ILR:4;
836     };
837     struct {
838         _IO VECNUM0:1;
839         _IO VECNUM1:1;
840         _IO VECNUM2:1;
841         _IO VECNUM3:1;
842         _IO VECNUM4:1;
843         _IO VECNUM5:1;
844         _IO VECNUM6:1;
845         _IO :1;
846         _IO ILR0:1;
847         _IO ILR1:1;
848         _IO ILR2:1;
849         _IO ILR3:1;
850     };
851 }INTTREGbits;
852
853 #define INTTREG      ((INTTREGbits*)(INTTREG_BASE))
854 /*****
855 //          STRUKTURE I REGISTRI ZA KONTROLU I STATUS TIMER-a:
856 //
857 /*****
858 typedef union {
859     struct {
860         _IO :1;
861         _IO TCS:1;
862         _IO TSYNC:1;
863         _IO :1;
864         _IO TCKPS:2;
865         _IO TGATE:1;
866         _IO :6;
867         _IO TSIDL:1;
868         _IO :1;
869         _IO TON:1;
870     };
871     struct {
872         _IO :4;
873         _IO TCKPS0:1;
874         _IO TCKPS1:1;
875     };
876 }T1CONbits;

```

```

877
878 #define T1CON      ((T1CONbits*)(T1CON_BASE))
879 /*****
880 typedef union {
881     struct {
882         _IO :1;
883         _IO TCS:1;
884         _IO :1;
885         _IO T32:1;
886         _IO TCKPS:2;
887         _IO TGATE:1;
888         _IO :6;
889         _IO TSIDL:1;
890         _IO :1;
891         _IO TON:1;
892     };
893     struct {
894         _IO :4;
895         _IO TCKPS0:1;
896         _IO TCKPS1:1;
897     };
898 }T2CONbits;
899
900 #define T2CON      ((T2CONbits*)(T2CON_BASE))
901 /*****
902 typedef union {
903     struct {
904         _IO :1;
905         _IO TCS:1;
906         _IO :2;
907         _IO TCKPS:2;
908         _IO TGATE:1;
909         _IO :6;
910         _IO TSIDL:1;
911         _IO :1;
912         _IO TON:1;
913     };
914     struct {
915         _IO :4;
916         _IO TCKPS0:1;
917         _IO TCKPS1:1;
918     };
919 }T3CONbits;
920
921 #define T3CON      ((T3CONbits*)(T3CON_BASE))
922 /*****
923 typedef union
924 {
925     struct
926     {
927         _IO TMR1:16;//BUG!!!
928     };
929     }TMR1bits;
930
931 #define TMR1R      ((TMR1bits*)(TMR1_BASE))
932 /*****
933 typedef union
934 {
935     struct
936     {
937         _IO PR1:16;//BUG!!!
938     };
939     }PR1bits;
940
941 #define PR1R       ((PR1bits*)(PR1_BASE))
942 /*****
943 typedef union
944 {
945     struct
946     {
947         _IO TMR2:16;//BUG!!!
948     };
949     }TMR2bits;

```

```

950
951 #define TMR2R      ((TMR2bits*)(TMR2_BASE))
952 /*****
953 typedef union
954 {
955     struct
956     {
957         _IO PR2:16; //BUG!!!
958     };
959     }PR2bits;
960
961 #define PR2R      ((PR2bits*)(PR2_BASE))
962 /*****
963 typedef union
964 {
965     struct
966     {
967         _IO TMR3:16; //BUG!!!
968     };
969     }TMR3bits;
970
971 #define TMR3R      ((TMR3bits*)(TMR3_BASE))
972 /*****
973 typedef union
974 {
975     struct
976     {
977         _IO PR3:16; //BUG!!!
978     };
979     }PR3bits;
980
981 #define PR3R      ((PR3bits*)(PR3_BASE))
982 /*****
983 typedef union
984 {
985     struct
986     {
987         _IO TMR3HLD:16; //BUG!!!
988     };
989     }TMR3HLDbits;
990
991 #define TMR3HLDR      ((TMR3HLDbits*)(TMR3HLD_BASE))
992 /*****
993 //          STRUKTURE I REGISTRI ZA INPUT CAPTURE MODULA:
994 //
995 /*****
996 typedef union
997 {
998     struct
999     {
1000         _IO IC1BUF:16; //BUG!!!
1001     };
1002     }IC1BUFbits;
1003
1004 #define IC1BUFR      ((IC1BUFbits*)(IC1BUF_BASE))
1005 /*****
1006 typedef union {
1007     struct {
1008         _IO ICM:3;
1009         _IO ICBNE:1;
1010         _IO ICOV:1;
1011         _IO ICI:2;
1012         _IO ICTMR:1;
1013         _IO :5;
1014         _IO ICSIDL:1;
1015     };
1016     struct {
1017         _IO ICM0:1;
1018         _IO ICM1:1;
1019         _IO ICM2:1;
1020         _IO :2;
1021         _IO ICI0:1;
1022         _IO ICI1:1;

```

```

1023         };
1024     }IC1CONbits;
1025
1026     #define IC1CON      ((IC1CONbits*)(IC1CON_BASE))
1027     /*****
1028     typedef union
1029     {
1030         struct
1031         {
1032             _IO IC2BUF:16;//BUG!!!
1033         };
1034         }IC2BUFbits;
1035
1036     #define IC2BUFR      ((IC2BUFbits*)(IC2BUF_BASE))
1037     /*****
1038     typedef union {
1039         struct {
1040             _IO ICM:3;
1041             _IO ICBNE:1;
1042             _IO ICOV:1;
1043             _IO ICI:2;
1044             _IO ICTMR:1;
1045             _IO :5;
1046             _IO ICSIDL:1;
1047         };
1048         struct {
1049             _IO ICM0:1;
1050             _IO ICM1:1;
1051             _IO ICM2:1;
1052             _IO :2;
1053             _IO ICI0:1;
1054             _IO ICI1:1;
1055         };
1056     }IC2CONbits;
1057
1058     #define IC2CON      ((IC2CONbits*)(IC2CON_BASE))
1059     /*****
1060     typedef union
1061     {
1062         struct
1063         {
1064             _IO IC7BUF:16;//BUG!!!
1065         };
1066         }IC7BUFbits;
1067
1068     #define IC7BUFR      ((IC7BUFbits*)(IC7BUF_BASE))
1069     /*****
1070     typedef union {
1071         struct {
1072             _IO ICM:3;
1073             _IO ICBNE:1;
1074             _IO ICOV:1;
1075             _IO ICI:2;
1076             _IO ICTMR:1;
1077             _IO :5;
1078             _IO ICSIDL:1;
1079         };
1080         struct {
1081             _IO ICM0:1;
1082             _IO ICM1:1;
1083             _IO ICM2:1;
1084             _IO :2;
1085             _IO ICI0:1;
1086             _IO ICI1:1;
1087         };
1088     }IC7CONbits;
1089
1090     #define IC7CON      ((IC7CONbits*)(IC7CON_BASE))
1091     /*****
1092     typedef union
1093     {
1094         struct
1095         {

```

```

1096     _IO IC8BUF:16;//BUG!!!
1097 };
1098 }IC8BUFbits;
1099
1100 #define IC8BUFR ((IC8BUFbits*)(IC8BUF_BASE))
1101 /*****
1102 typedef union {
1103     struct {
1104         _IO ICM:3;
1105         _IO ICBNE:1;
1106         _IO ICOV:1;
1107         _IO ICI:2;
1108         _IO ICTMR:1;
1109         _IO :5;
1110         _IO ICSIDL:1;
1111     };
1112     struct {
1113         _IO ICM0:1;
1114         _IO ICM1:1;
1115         _IO ICM2:1;
1116         _IO :2;
1117         _IO ICI0:1;
1118         _IO ICI1:1;
1119     };
1120 }IC8CONbits;
1121
1122 #define IC8CON ((IC8CONbits*)(IC8CON_BASE))
1123 /*****
1124 //          STRUKTURE I REGISTRI ZA OUTPUT COMPARE MODUL:
1125 //
1126 /*****
1127 typedef union
1128 {
1129     struct
1130     {
1131         _IO OC1RS:16;//BUG!!!
1132     };
1133 }OC1RSbits;
1134
1135 #define OC1RSR ((OC1RSbits*)(OC1RS_BASE))
1136 /*****
1137 typedef union
1138 {
1139     struct
1140     {
1141         _IO OC1R:16;//BUG!!!
1142     };
1143 }OC1Rbits;
1144
1145 #define OC1RR ((OC1Rbits*)(OC1R_BASE))
1146 /*****
1147 typedef union {
1148     struct {
1149         _IO OCM:3;
1150         _IO OCTSEL:1;
1151         _IO OCFLT:1;
1152         _IO :8;
1153         _IO OCSIDL:1;
1154     };
1155     struct {
1156         _IO OCM0:1;
1157         _IO OCM1:1;
1158         _IO OCM2:1;
1159     };
1160 }OC1CONbits;
1161
1162 #define OC1CON ((OC1CONbits*)(OC1CON_BASE))
1163 /*****
1164 typedef union
1165 {
1166     struct
1167     {
1168         _IO OC2RS:16;//BUG!!!

```



```

1169     };
1170     }OC2RSbits;
1171
1172     #define OC2RSR      ((OC2RSbits*) (OC2RS_BASE))
1173     /*****
1174     typedef union
1175     {
1176         struct
1177         {
1178             _IO OC2R:16; //BUG!!!
1179         };
1180     }OC2Rbits;
1181
1182     #define OC2RR      ((OC2Rbits*) (OC2R_BASE))
1183     /*****
1184     typedef union {
1185         struct {
1186             _IO OCM:3;
1187             _IO OCTSEL:1;
1188             _IO OCFLT:1;
1189             _IO :8;
1190             _IO OCSIDL:1;
1191         };
1192         struct {
1193             _IO OCM0:1;
1194             _IO OCM1:1;
1195             _IO OCM2:1;
1196         };
1197     }OC2CONbits;
1198
1199     #define OC2CON      ((OC2CONbits*) (OC2CON_BASE))
1200     /*****
1201     //          6-IZLAZNI MOTOR CONTROL PWM MODUL:(13 registara)
1202     //          Jos ukupno 111 registara za definisati
1203     /*****
1204     typedef union {
1205         struct {
1206             _IO PTMOD:2;
1207             _IO PTCKPS:2;
1208             _IO PTOPS:4;
1209             _IO :5;
1210             _IO PTSIDL:1;
1211             _IO :1;
1212             _IO PTEN:1;
1213         };
1214         struct {
1215             _IO PTMOD0:1;
1216             _IO PTMOD1:1;
1217             _IO PTCKPS0:1;
1218             _IO PTCKPS1:1;
1219             _IO PTOPS0:1;
1220             _IO PTOPS1:1;
1221             _IO PTOPS2:1;
1222             _IO PTOPS3:1;
1223         };
1224     }P1TCONbits;
1225
1226     #define P1TCON      ((P1TCONbits*) (P1TCON_BASE))
1227     /*****
1228     typedef union
1229     {
1230         struct
1231         {
1232             _IO PTMR:15; //BUG!!!
1233             _IO PTDIR:1;
1234         };
1235     }P1TMRbits;
1236
1237     #define P1TMR      ((P1TMRbits*) (P1TMR_BASE))
1238     /*****
1239     typedef union
1240     {
1241         struct

```

```

1242     {
1243         _IO PTPER:15; //BUG!!!
1244     };
1245     }PlTPERbits;
1246
1247 #define PlTPER      ((PlTPERbits*) (PlTPER_BASE))
1248 /*****
1249 typedef union{
1250     struct{
1251         _IO SEVTCMP:15;
1252         _IO SEVTDIR:1;
1253     };
1254     }PlSECMPbits;
1255
1256 #define PlSECMP      ((PlSECMPbits*) (PlSECMP_BASE))
1257 /*****
1258 typedef union{
1259     struct{
1260         _IO PENL:3;
1261         _IO :1;
1262         _IO PENH:3;
1263         _IO :1;
1264         _IO PMOD:3;
1265     };
1266     struct{
1267         _IO PEN1L:1;
1268         _IO PEN2L:1;
1269         _IO PEN3L:1;
1270         _IO :1;
1271         _IO PEN1H:1;
1272         _IO PEN2H:1;
1273         _IO PEN3H:1;
1274         _IO :1;
1275         _IO PMOD1:1;
1276         _IO PMOD2:1;
1277         _IO PMOD3:1;
1278     };
1279     }PWM1CON1bits;
1280
1281 #define PWM1CON1      ((PWM1CON1bits*) (PWM1CON1_BASE))
1282 /*****
1283
1284 typedef union {
1285     struct {
1286         _IO UDIS:1;
1287         _IO OSYNC:1;
1288         _IO IUE:1;
1289         _IO :5;
1290         _IO SEVOPS:4;
1291     };
1292     struct {
1293         _IO :8;
1294         _IO SEVOPS0:1;
1295         _IO SEVOPS1:1;
1296         _IO SEVOPS2:1;
1297         _IO SEVOPS3:1;
1298     };
1299     }PWM1CON2bits;
1300
1301 #define PWM1CON2      ((PWM1CON2bits*) (PWM1CON2_BASE))
1302 /*****
1303 typedef union {
1304     struct {
1305         _IO DTA:6;
1306         _IO DTAPS:2;
1307         _IO DTB:6;
1308         _IO DTBPS:2;
1309     };
1310     struct {
1311         _IO DTA0:1;
1312         _IO DTA1:1;
1313         _IO DTA2:1;
1314         _IO DTA3:1;

```

```

1315         _IO DTA4:1;
1316         _IO DTA5:1;
1317         _IO DTAPS0:1;
1318         _IO DTAPS1:1;
1319         _IO DTB0:1;
1320         _IO DTB1:1;
1321         _IO DTB2:1;
1322         _IO DTB3:1;
1323         _IO DTB4:1;
1324         _IO DTB5:1;
1325         _IO DTBPS0:1;
1326         _IO DTBPS1:1;
1327     };
1328 }P1DTCON1bits;
1329
1330 #define P1DTCON1    ((P1DTCON1bits*) (P1DTCON1_BASE))
1331 /*****
1332 typedef union{
1333     struct{
1334         _IO DTS1I:1;
1335         _IO DTS1A:1;
1336         _IO DTS2I:1;
1337         _IO DTS2A:1;
1338         _IO DTS3I:1;
1339         _IO DTS3A:1;
1340     };
1341 }P1DTCON2bits;
1342
1343 #define P1DTCON2    ((P1DTCON2bits*) (P1DTCON2_BASE))
1344 /*****
1345 typedef union{
1346 struct{
1347     _IO FAEN1:1;
1348     _IO FAEN2:1;
1349     _IO FAEN3:1;
1350     _IO :4;
1351     _IO FLTAM:1;
1352     _IO FAOV1L:1;
1353     _IO FAOV1H:1;
1354     _IO FAOV2L:1;
1355     _IO FAOV2H:1;
1356     _IO FAOV3L:1;
1357     _IO FAOV3H:1;
1358 };
1359 }P1FLTACONbits;
1360
1361 #define P1FLTACON    ((P1FLTACONbits*) (P1FLTACON_BASE))
1362 /*****
1363 typedef union{
1364 struct{
1365     _IO POUT:6;
1366     _IO :2;
1367     _IO POVD:6;
1368 };
1369 struct{
1370     _IO POUT1L:1;
1371     _IO POUT1H:1;
1372     _IO POUT2L:1;
1373     _IO POUT2H:1;
1374     _IO POUT3L:1;
1375     _IO POUT3H:1;
1376     _IO :2;
1377     _IO POVD1L:1;
1378     _IO POVD1H:1;
1379     _IO POVD2L:1;
1380     _IO POVD2H:1;
1381     _IO POVD3L:1;
1382     _IO POVD3H:1;
1383 };
1384 }P1OVDCONbits;
1385
1386 #define P1OVDCON    ((P1OVDCONbits*) (P1OVDCON_BASE))
1387 /*****

```

```

1388 typedef union
1389 {
1390     struct
1391     {
1392         _IO_PDC:16; //BUG!!!
1393     };
1394 }P1DC1bits;
1395
1396 #define P1DC1 ((P1DC1bits*)(P1DC1_BASE))
1397 /*****
1398 typedef union
1399 {
1400     struct
1401     {
1402         _IO_PDC:16; //BUG!!!
1403     };
1404 }P1DC2bits;
1405
1406 #define P1DC2 ((P1DC2bits*)(P1DC2_BASE))
1407 /*****
1408 typedef union
1409 {
1410     struct
1411     {
1412         _IO_PDC:16; //BUG!!!
1413     };
1414 }P1DC3bits;
1415
1416 #define P1DC3 ((P1DC3bits*)(P1DC3_BASE))
1417 /*****
1418 //          2-IZLAZNI MOTOR CONTROL PWM MODUL:(11 registara)
1419 //
1420 /*****
1421 typedef union {
1422     struct {
1423         _IO_PTMOD:2;
1424         _IO_PTCKPS:2;
1425         _IO_PTOPS:4;
1426         _IO_ :5;
1427         _IO_PTSIDL:1;
1428         _IO_ :1;
1429         _IO_PTEN:1;
1430     };
1431     struct {
1432         _IO_PTMOD0:1;
1433         _IO_PTMOD1:1;
1434         _IO_PTCKPS0:1;
1435         _IO_PTCKPS1:1;
1436         _IO_PTOPS0:1;
1437         _IO_PTOPS1:1;
1438         _IO_PTOPS2:1;
1439         _IO_PTOPS3:1;
1440     };
1441 }P2TCONbits;
1442
1443 #define P2TCON ((P2TCONbits*)(P2TCON_BASE))
1444 /*****
1445 typedef union{
1446     struct{
1447         _IO_PTMR:15;
1448         _IO_PTDIR:1;
1449     };
1450 }P2TMRbits;
1451
1452 #define P2TMR ((P2TMRbits*)(P2TMR_BASE))
1453 /*****
1454 typedef union{
1455     struct{
1456         _IO_PTPER:15;
1457     };
1458 }P2TPERbits;
1459
1460 #define P2TPERR ((P2TPERbits*)(P2TPER_BASE))

```

```

1461  /*****
1462  typedef union{
1463      struct{
1464          _IO SEVTCMP:15;
1465          _IO SEVTDIR:1;
1466      };
1467  }P2SECMpbits;
1468
1469  #define P2SECMp      ((P2SECMpbits*) (P2SECMp_BASE))
1470  /*****
1471  typedef union{
1472      struct{
1473          _IO PEN1L:1;
1474          _IO :3;
1475          _IO PEN1H:1;
1476          _IO :3;
1477          _IO PMOD1:1;
1478      };
1479  }PWM2CON1bits;
1480
1481  #define PWM2CON1      ((PWM2CON1bits*) (PWM2CON1_BASE))
1482  /*****
1483  typedef union {
1484      struct {
1485          _IO UDIS:1;
1486          _IO OSYNC:1;
1487          _IO IUE:1;
1488          _IO :5;
1489          _IO SEVOPS:4;
1490      };
1491      struct {
1492          _IO :8;
1493          _IO SEVOPS0:1;
1494          _IO SEVOPS1:1;
1495          _IO SEVOPS2:1;
1496          _IO SEVOPS3:1;
1497      };
1498  }PWM2CON2bits;
1499
1500  #define PWM2CON2      ((PWM2CON2bits*) (PWM2CON2_BASE))
1501  /*****
1502  typedef union {
1503      struct {
1504          _IO DTA:6;
1505          _IO DTAPS:2;
1506          _IO DTB:6;
1507          _IO DTBPS:2;
1508      };
1509      struct {
1510          _IO DTA0:1;
1511          _IO DTA1:1;
1512          _IO DTA2:1;
1513          _IO DTA3:1;
1514          _IO DTA4:1;
1515          _IO DTA5:1;
1516          _IO DTAPS0:1;
1517          _IO DTAPS1:1;
1518          _IO DTB0:1;
1519          _IO DTB1:1;
1520          _IO DTB2:1;
1521          _IO DTB3:1;
1522          _IO DTB4:1;
1523          _IO DTB5:1;
1524          _IO DTBPS0:1;
1525          _IO DTBPS1:1;
1526      };
1527  }P2DTCON1bits;
1528
1529  #define P2DTCON1      ((P2DTCON1bits*) (P2DTCON1_BASE))
1530  /*****
1531  typedef union{
1532      struct{
1533          _IO DTS1I:1;

```

```

1534     _IO DTS1A:1;
1535 };
1536 }P2DTCON2bits;
1537
1538 #define P2DTCON2 ((P2DTCON2bits*) (P2DTCON2_BASE))
1539 /*****
1540 typedef union{
1541     struct{
1542         _IO FAEN1:1;
1543         _IO :6;
1544         _IO FLTAM:1;
1545         _IO FAOV1L:1;
1546         _IO FAOV1H:1;
1547     };
1548 }P2FLTACONbits;
1549
1550 #define P2FLTACON ((P2FLTACONbits*) (P2FLTACON_BASE))
1551 /*****
1552 typedef union{
1553     struct{
1554         _IO POUT:2;
1555         _IO :6;
1556         _IO POVD:2;
1557     };
1558     struct{
1559         _IO POUT1L:1;
1560         _IO POUT1H:1;
1561         _IO :6;
1562         _IO POVD1L:1;
1563         _IO POVD1H:1;
1564     };
1565 }P2OVDCONbits;
1566
1567 #define P2OVDCON ((P2OVDCONbits*) (P2OVDCON_BASE))
1568 /*****
1569 typedef union
1570 {
1571     struct
1572     {
1573         _IO P2DC1:16; //BUG!!!
1574     };
1575 }P2DC1bits;
1576
1577 #define P2DC1R ((P2DC1bits*) (P2DC1_BASE))
1578 /*****
1579 //          MOTION FEEDBACK MODUL (KVADRATURNI ENKODER):(4 registra)
1580 //
1581 /*****
1582 typedef union {
1583     struct {
1584         _IO UPDN_SRC:1;
1585         _IO TQCS:1;
1586         _IO POSRES:1;
1587         _IO TQCKPS:2;
1588         _IO TQGATE:1;
1589         _IO PCDOU:1;
1590         _IO SWPAB:1;
1591         _IO QEIM:3;
1592         _IO UPDN:1;
1593         _IO INDX:1;
1594         _IO QEISIDL:1;
1595         _IO :1;
1596         _IO CNTERR:1;
1597     };
1598     struct {
1599         _IO :3;
1600         _IO TQCKPS0:1;
1601         _IO TQCKPS1:1;
1602         _IO :3;
1603         _IO QEIM0:1;
1604         _IO QEIM1:1;
1605         _IO QEIM2:1;
1606     };

```

```

1607 }QEILCONbits;
1608
1609 #define QEILCON ((QEILCONbits*)(QEILCON_BASE))
1610 /*****
1611 typedef union {
1612     struct {
1613         _IO :4;
1614         _IO QECK:3;
1615         _IO QEOUT:1;
1616         _IO CEID:1;
1617         _IO IMV:2;
1618     };
1619     struct {
1620         _IO :4;
1621         _IO QECK0:1;
1622         _IO QECK1:1;
1623         _IO QECK2:1;
1624         _IO :2;
1625         _IO IMV0:1;
1626         _IO IMV1:1;
1627     };
1628 }DFLT1CONbits;
1629
1630 #define DFLT1CON ((DFLT1CONbits*)(DFLT1CON_BASE))
1631 /*****
1632 typedef union
1633 {
1634     struct
1635     {
1636         _IO POS1CNT:16;//BUG!!!
1637     };
1638 }POS1CNTbits;
1639
1640 #define POS1CNTR ((POS1CNTbits*)(POS1CNT_BASE))
1641 /*****
1642 typedef union
1643 {
1644     struct
1645     {
1646         _IO MAX1CNT:16;//BUG!!!
1647     };
1648 }MAX1CNTbits;
1649
1650 #define MAX1CNTR ((MAX1CNTbits*)(MAX1CNT_BASE))
1651 /*****
1652 // I2C1 MODUL (2-ZICANI SERIJSKI INTERFEJS):(7 registara)
1653 //
1654 /*****
1655 typedef union
1656 {
1657     struct
1658     {
1659         _IO I2C1RCV:8;//BUG!!!
1660     };
1661 }I2C1RCVbits;
1662
1663 #define I2C1RCVR ((I2C1RCVbits*)(I2C1RCV_BASE))
1664 /*****
1665 typedef union
1666 {
1667     struct
1668     {
1669         _IO I2C1TRN:8;//BUG!!!
1670     };
1671 }I2C1TRNbits;
1672
1673 #define I2C1TRNR ((I2C1TRNbits*)(I2C1TRN_BASE))
1674 /*****
1675 typedef union
1676 {
1677     struct
1678     {
1679         _IO I2C1BRG:9;//BUG!!!

```

```

1680     };
1681     }I2C1BRGbits;
1682
1683 #define I2C1BRGR    ((I2C1BRGbits*)(I2C1BRG_BASE))
1684 /*****
1685 typedef union{
1686     struct{
1687         _IO SEN:1;
1688         _IO RSEN:1;
1689         _IO PEN:1;
1690         _IO RCEN:1;
1691         _IO ACKEN:1;
1692         _IO ACKDT:1;
1693         _IO STREN:1;
1694         _IO GCEN:1;
1695         _IO SMEN:1;
1696         _IO DISSLW:1;
1697         _IO A10M:1;
1698         _IO IPMIEN:1;
1699         _IO SCLREL:1;
1700         _IO I2CSIDL:1;
1701         _IO :1;
1702         _IO I2CEN:1;
1703     };
1704 }I2C1CONbits;
1705
1706 #define I2C1CON    ((I2C1CONbits*)(I2C1CON_BASE))
1707 /*****
1708 typedef union{
1709     struct{
1710         _IO TBF:1;
1711         _IO RBF:1;
1712         _IO R_W:1;
1713         _IO S:1;
1714         _IO P:1;
1715         _IO D_A:1;
1716         _IO I2COV:1;
1717         _IO IWCOL:1;
1718         _IO ADD10:1;
1719         _IO GCSTAT:1;
1720         _IO BCL:1;
1721         _IO :3;
1722         _IO TRSTAT:1;
1723         _IO ACKSTAT:1;
1724     };
1725 }I2C1STATbits;
1726
1727 #define I2C1STAT    ((I2C1STATbits*)(I2C1STAT_BASE))
1728 /*****
1729 typedef union
1730 {
1731     struct
1732     {
1733         _IO I2C1ADD:10; //BUG!!!
1734     };
1735 }I2C1ADDbits;
1736
1737 #define I2C1ADDR    ((I2C1ADDbits*)(I2C1ADD_BASE))
1738 /*****
1739 typedef union
1740 {
1741     struct
1742     {
1743         _IO I2C1MSK:10; //BUG!!!
1744     };
1745 }I2C1MSKbits;
1746
1747 #define I2C1MSKR    ((I2C1MSKbits*)(I2C1MSK_BASE))
1748 /*****
1749 //          USART1 MODUL (SERIJSKI INTERFEJS):(5 registara)
1750 //
1751 /*****
1752 typedef union {

```



```

1753     struct {
1754         _IO STSEL:1;
1755         _IO PDSEL:2;
1756         _IO BRGH:1;
1757         _IO URXINV:1;
1758         _IO ABAUD:1;
1759         _IO LPBACK:1;
1760         _IO WAKE:1;
1761         _IO UEN:2;
1762         _IO :1;
1763         _IO RTSMD:1;
1764         _IO IREN:1;
1765         _IO USIDL:1;
1766         _IO :1;
1767         _IO UARTEN:1;
1768     };
1769     struct {
1770         _IO :1;
1771         _IO PDSEL0:1;
1772         _IO PDSEL1:1;
1773         _IO :5;
1774         _IO UEN0:1;
1775         _IO UEN1:1;
1776     };
1777 }U1MODEbits;
1778
1779 #define U1MODE    ((U1MODEbits*) (U1MODE_BASE))
1780 /*****
1781 typedef union {
1782     struct {
1783         _IO URXDA:1;
1784         _IO OERR:1;
1785         _IO FERR:1;
1786         _IO PERR:1;
1787         _IO RIDLE:1;
1788         _IO ADDEN:1;
1789         _IO URXISEL:2;
1790         _IO TRMT:1;
1791         _IO UTXBF:1;
1792         _IO UTXEN:1;
1793         _IO UTXBRK:1;
1794         _IO :1;
1795         _IO UTXISEL0:1;
1796         _IO UTXINV:1;
1797         _IO UTXISEL1:1;
1798     };
1799     struct {
1800         _IO :6;
1801         _IO URXISEL0:1;
1802         _IO URXISEL1:1;
1803     };
1804 }U1STAbits;
1805
1806 #define U1STA    ((U1STAbits*) (U1STA_BASE))
1807 /*****
1808 typedef union
1809 {
1810     struct
1811     {
1812         _IO U1TXREG:9;//BUG!!!
1813     };
1814     struct
1815     {
1816         _IO UTXREG0:1;
1817         _IO UTXREG1:1;
1818         _IO UTXREG2:1;
1819         _IO UTXREG3:1;
1820         _IO UTXREG4:1;
1821         _IO UTXREG5:1;
1822         _IO UTXREG6:1;
1823         _IO UTXREG7:1;
1824         _IO UTXREG8:1;
1825     };

```

```

1826     }UTXREGbits;
1827
1828 #define UTXREGR      ((UTXREGbits*) (UTXREG_BASE))
1829 /*****
1830 typedef union
1831 {
1832     struct
1833     {
1834         _IO U1RXREG:9; //BUG!!!
1835     };
1836     struct
1837     {
1838         _IO URXREG0:1;
1839         _IO URXREG1:1;
1840         _IO URXREG2:1;
1841         _IO URXREG3:1;
1842         _IO URXREG4:1;
1843         _IO URXREG5:1;
1844         _IO URXREG6:1;
1845         _IO URXREG7:1;
1846         _IO URXREG8:1;
1847     };
1848     }U1RXREGbits;
1849
1850 #define U1RXREGR      ((U1RXREGbits*) (U1RXREG_BASE))
1851 /*****
1852 //          SPI1 MODUL (SERIJSKI INTERFEJS):(4 registra)
1853 //
1854 /*****
1855 typedef union{
1856     struct{
1857         _IO SPIRBF:1;
1858         _IO SPITBF:1;
1859         _IO :4;
1860         _IO SPIROV:1;
1861         _IO :6;
1862         _IO SPISIDL:1;
1863         _IO :1;
1864         _IO SPIEN:1;
1865     };
1866 }SPI1STATbits;
1867
1868 #define SPI1STAT      ((SPI1STATbits*) (SPI1STAT_BASE))
1869 /*****
1870 typedef union {
1871     struct {
1872         _IO PPRE:2;
1873         _IO SPRE:3;
1874         _IO MSTEN:1;
1875         _IO CKP:1;
1876         _IO SSSEN:1;
1877         _IO CKE:1;
1878         _IO SMP:1;
1879         _IO MODE16:1;
1880         _IO DISSDO:1;
1881         _IO DISSCK:1;
1882     };
1883     struct {
1884         _IO PPRE0:1;
1885         _IO PPRE1:1;
1886         _IO SPRE0:1;
1887         _IO SPRE1:1;
1888         _IO SPRE2:1;
1889     };
1890 }SPI1CON1bits;
1891
1892 #define SPI1CON1      ((SPI1CON1bits*) (SPI1CON1_BASE))
1893 /*****
1894 typedef union{
1895     struct{
1896         _IO :1;
1897         _IO FRMDLY:1;
1898         _IO :11;

```

```

1899         _IO FRMPOL:1;
1900         _IO SPIFSD:1;
1901         _IO FRMEN:1;
1902     };
1903 }SPI1CON2bits;
1904
1905 #define SPI1CON2 ((SPI1CON2bits*)(SPI1CON2_BASE))
1906 /*****
1907 typedef union
1908 {
1909     struct
1910     {
1911         _IO SPI1BUF:16;//BUG!!!
1912     };
1913     }SPI1BUFbits;
1914
1915 #define SPI1BUFR ((SPI1BUFbits*)(SPI1BUF_BASE))
1916 /*****
1917 //
1918 //             ADC1 MODUL:
1919 //             (MODUL ANALOGNO-DIGITALNOG PRETVARACA)
1920 /*****
1921 typedef union
1922 {
1923     struct
1924     {
1925         _IO ADCBUF:16;//BUG!!!
1926     };
1927     }ADC1BUF0bits;
1928
1929 #define ADC1BUF0 ((ADC1BUF0bits*)(ADC1BUF0_BASE))
1930 /*****
1931 typedef union
1932 {
1933     struct
1934     {
1935         _IO ADCBUF:16;//BUG!!!
1936     };
1937     }ADC1BUF1bits;
1938
1939 #define ADC1BUF1 ((ADC1BUF1bits*)(ADC1BUF1_BASE))
1940 /*****
1941 typedef union
1942 {
1943     struct
1944     {
1945         _IO ADCBUF:16;//BUG!!!
1946     };
1947     }ADC1BUF2bits;
1948
1949 #define ADC1BUF2 ((ADC1BUF2bits*)(ADC1BUF2_BASE))
1950 /*****
1951 typedef union
1952 {
1953     struct
1954     {
1955         _IO ADCBUF:16;//BUG!!!
1956     };
1957     }ADC1BUF3bits;
1958
1959 #define ADC1BUF3 ((ADC1BUF3bits*)(ADC1BUF3_BASE))
1960 /*****
1961 typedef union
1962 {
1963     struct
1964     {
1965         _IO ADCBUF:16;//BUG!!!
1966     };
1967     }ADC1BUF4bits;
1968
1969 #define ADC1BUF4 ((ADC1BUF4bits*)(ADC1BUF4_BASE))
1970 /*****
1971 typedef union
1972 {

```

```

1972     struct
1973     {
1974         _IO ADCBUF:16;//BUG!!!
1975     };
1976     }ADC1BUF5bits;
1977
1978 #define ADC1BUF5      ((ADC1BUF5bits*) (ADC1BUF5_BASE))
1979 /*****
1980 typedef union
1981 {
1982     struct
1983     {
1984         _IO ADCBUF:16;//BUG!!!
1985     };
1986     }ADC1BUF6bits;
1987
1988 #define ADC1BUF6      ((ADC1BUF6bits*) (ADC1BUF6_BASE))
1989 /*****
1990 typedef union
1991 {
1992     struct
1993     {
1994         _IO ADCBUF:16;//BUG!!!
1995     };
1996     }ADC1BUF7bits;
1997
1998 #define ADC1BUF7      ((ADC1BUF7bits*) (ADC1BUF7_BASE))
1999 /*****
2000 typedef union
2001 {
2002     struct
2003     {
2004         _IO ADCBUF:16;//BUG!!!
2005     };
2006     }ADC1BUF8bits;
2007
2008 #define ADC1BUF8      ((ADC1BUF8bits*) (ADC1BUF8_BASE))
2009 /*****
2010 typedef union
2011 {
2012     struct
2013     {
2014         _IO ADCBUF:16;//BUG!!!
2015     };
2016     }ADC1BUF9bits;
2017
2018 #define ADC1BUF9      ((ADC1BUF9bits*) (ADC1BUF9_BASE))
2019 /*****
2020 typedef union
2021 {
2022     struct
2023     {
2024         _IO ADCBUF:16;//BUG!!!
2025     };
2026     }ADC1BUFAbits;
2027
2028 #define ADC1BUFA      ((ADC1BUFAbits*) (ADC1BUFA_BASE))
2029 /*****
2030 typedef union
2031 {
2032     struct
2033     {
2034         _IO ADCBUF:16;//BUG!!!
2035     };
2036     }ADC1BUFBbits;
2037
2038 #define ADC1BUFB      ((ADC1BUFBbits*) (ADC1BUFB_BASE))
2039 /*****
2040 typedef union
2041 {
2042     struct
2043     {
2044         _IO ADCBUF:16;//BUG!!!

```

```

2045     };
2046     }ADC1BUFCbits;
2047
2048     #define ADC1BUFC      ((ADC1BUFCbits*) (ADC1BUFC_BASE))
2049     /*****
2050     typedef union
2051     {
2052         struct
2053         {
2054             _IO ADCBUF:16; //BUG!!!
2055         };
2056         }ADC1BUFDbits;
2057
2058     #define ADC1BUFD      ((ADC1BUFDbits*) (ADC1BUFD_BASE))
2059     /*****
2060     typedef union
2061     {
2062         struct
2063         {
2064             _IO ADCBUF:16; //BUG!!!
2065         };
2066         }ADC1BUFEbits;
2067
2068     #define ADC1BUFE      ((ADC1BUFEbits*) (ADC1BUFE_BASE))
2069     /*****
2070     typedef union
2071     {
2072         struct
2073         {
2074             _IO ADCBUF:16; //BUG!!!
2075         };
2076         }ADC1BUFFbits;
2077
2078     #define ADC1BUFF      ((ADC1BUFFbits*) (ADC1BUFF_BASE))
2079     /*****
2080     typedef union {
2081         struct{
2082             _IO ADCON1:16; //Zbog brze inicijalizacije periferala.
2083         };
2084         struct {
2085             _IO DONE:1;
2086             _IO SAMP:1;
2087             _IO ASAM:1;
2088             _IO SIMSAM:1;
2089             _IO _IO :1;
2090             _IO SSRC:3;
2091             _IO FORM:2;
2092             _IO AD12B:1;
2093             _IO _IO :2;
2094             _IO ADSIDL:1;
2095             _IO _IO :1;
2096             _IO ADON:1;
2097         };
2098         struct {
2099             _IO _IO :5;
2100             _IO SSRC0:1;
2101             _IO SSRC1:1;
2102             _IO SSRC2:1;
2103             _IO FORM0:1;
2104             _IO FORM1:1;
2105         };
2106     }AD1CON1bits;
2107
2108     #define AD1CON1      ((AD1CON1bits*) (AD1CON1_BASE))
2109     /*****
2110     typedef union {
2111         struct{
2112             _IO ADCON2:16; //Zbog brze inicijalizacije periferala.
2113         };
2114         struct {
2115             _IO ALTS:1;
2116             _IO BUFM:1;
2117             _IO SMPI:4;

```

```

2118         _IO :1;
2119     _IO BUFS:1;
2120     _IO CHPS:2;
2121     _IO CSCNA:1;
2122         _IO :2;
2123     _IO VCFG:3;
2124     };
2125     struct {
2126         _IO :2;
2127     _IO SMPI0:1;
2128     _IO SMPI1:1;
2129     _IO SMPI2:1;
2130     _IO SMPI3:1;
2131         _IO :2;
2132     _IO CHPS0:1;
2133     _IO CHPS1:1;
2134         _IO :3;
2135     _IO VCFG0:1;
2136     _IO VCFG1:1;
2137     _IO VCFG2:1;
2138     };
2139 }AD1CON2bits;
2140
2141 #define AD1CON2 ((AD1CON2bits*) (AD1CON2_BASE))
2142 /*****
2143 typedef union {
2144     struct{
2145         _IO ADCON3:16;//Zbog brze inicijalizacije periferala.
2146     };
2147     struct {
2148         _IO ADCS:8;
2149         _IO SAMC:5;
2150         _IO :2;
2151         _IO ADRC:1;
2152     };
2153     struct {
2154         _IO ADCS0:1;
2155         _IO ADCS1:1;
2156         _IO ADCS2:1;
2157         _IO ADCS3:1;
2158         _IO ADCS4:1;
2159         _IO ADCS5:1;
2160         _IO ADCS6:1;
2161         _IO ADCS7:1;
2162         _IO SAMC0:1;
2163         _IO SAMC1:1;
2164         _IO SAMC2:1;
2165         _IO SAMC3:1;
2166         _IO SAMC4:1;
2167     };
2168 }AD1CON3bits;
2169
2170 #define AD1CON3 ((AD1CON3bits*) (AD1CON3_BASE))
2171 /*****
2172 typedef union {
2173     struct {
2174         _IO CH123SA:1;
2175         _IO CH123NA:2;
2176         _IO :5;
2177         _IO CH123SB:1;
2178         _IO CH123NB:2;
2179     };
2180     struct {
2181         _IO :1;
2182         _IO CH123NA0:1;
2183         _IO CH123NA1:1;
2184         _IO :6;
2185         _IO CH123NB0:1;
2186         _IO CH123NB1:1;
2187     };
2188 }AD1CHS123bits;
2189
2190 #define AD1CHS123 ((AD1CHS123bits*) (AD1CHS123_BASE))

```

```

2191  /*****
2192  typedef union {
2193      struct {
2194          _IO CH0SA:5;
2195          _IO :2;
2196          _IO CH0NA:1;
2197          _IO CH0SB:5;
2198          _IO :2;
2199          _IO CH0NB:1;
2200      };
2201      struct {
2202          _IO CH0SA0:1;
2203          _IO CH0SA1:1;
2204          _IO CH0SA2:1;
2205          _IO CH0SA3:1;
2206          _IO CH0SA4:1;
2207          _IO :3;
2208          _IO CH0SB0:1;
2209          _IO CH0SB1:1;
2210          _IO CH0SB2:1;
2211          _IO CH0SB3:1;
2212          _IO CH0SB4:1;
2213      };
2214  }AD1CHS0bits;
2215
2216  #define AD1CHS0      ((AD1CHS0bits*) (AD1CHS0_BASE))
2217  /*****
2218  typedef union{
2219  struct{
2220      _IO PCFG:9;
2221  };
2222  struct{
2223      _IO PCFG0:1;
2224      _IO PCFG1:1;
2225      _IO PCFG2:1;
2226      _IO PCFG3:1;
2227      _IO PCFG4:1;
2228      _IO PCFG5:1;
2229      _IO PCFG6:1;
2230      _IO PCFG7:1;
2231      _IO PCFG8:1;
2232  };
2233  }AD1PCFGLbits;
2234
2235  #define AD1PCFGL      ((AD1PCFGLbits*) (AD1PCFGL_BASE))
2236  /*****
2237  typedef union{
2238  struct{
2239      _IO CSSL:9;
2240  };
2241  struct{
2242      _IO CSS0:1;
2243      _IO CSS1:1;
2244      _IO CSS2:1;
2245      _IO CSS3:1;
2246      _IO CSS4:1;
2247      _IO CSS5:1;
2248      _IO CSS6:1;
2249      _IO CSS7:1;
2250      _IO CSS8:1;
2251  };
2252  }AD1CSSLbits;
2253
2254  #define AD1CSSL      ((AD1CSSLbits*) (AD1CSSL_BASE))
2255  /*****
2256  //          GPIO (PORT) REGISTRARI(23 registra)
2257  //          (KONTROLA DIGITALNIH I/O PINOVA)
2258  /*****
2259  typedef union{
2260  struct{
2261      _IO TRISL:5;
2262      _IO :2;
2263      _IO TRISH:4;

```

```

2264     };
2265     struct{
2266         _IO TRIS:11;
2267     };
2268     struct{
2269         _IO TRISA0:1;
2270         _IO TRISA1:1;
2271         _IO TRISA2:1;
2272         _IO TRISA3:1;
2273         _IO TRISA4:1;
2274         _IO :2;
2275         _IO TRISA7:1;
2276         _IO TRISA8:1;
2277         _IO TRISA9:1;
2278         _IO TRISA10:1;
2279     };
2280 }TRISAbits;
2281
2282 #define TRISA    ((TRISAbits*)(TRISA_BASE))
2283 /*****
2284 typedef union{
2285     struct{
2286         _IO PORTAL:5;
2287         _IO :2;
2288         _IO PORTAH:4;
2289     };
2290     struct{
2291         _IO PORTAR:16;
2292     };
2293     struct{
2294         _IO RA0:1;
2295         _IO RA1:1;
2296         _IO RA2:1;
2297         _IO RA3:1;
2298         _IO RA4:1;
2299         _IO :2;
2300         _IO RA7:1;
2301         _IO RA8:1;
2302         _IO RA9:1;
2303         _IO RA10:1;
2304     };
2305 }PORTAbits;
2306
2307 #define PORTA    ((PORTAbits*)(PORTA_BASE))
2308 /*****
2309 typedef union{
2310     struct{
2311         _IO GPOAL:5;
2312         _IO :2;
2313         _IO GPOAH:4;
2314     };
2315     struct{
2316         _IO GPOA:16;
2317     };
2318     struct{
2319         _IO LATA0:1;
2320         _IO LATA1:1;
2321         _IO LATA2:1;
2322         _IO LATA3:1;
2323         _IO LATA4:1;
2324         _IO :2;
2325         _IO LATA7:1;
2326         _IO LATA8:1;
2327         _IO LATA9:1;
2328         _IO LATA10:1;
2329     };
2330     struct{
2331         _IO LA0:1;
2332         _IO LA1:1;
2333         _IO LA2:1;
2334         _IO LA3:1;
2335         _IO LA4:1;
2336         _IO :2;

```



```

2337         _IO LA7:1;
2338         _IO LA8:1;
2339         _IO LA9:1;
2340         _IO LA10:1;
2341     };
2342 }LATAbits;
2343
2344 #define LATA    ((LATAbits*)(LATA_BASE))
2345 /*****
2346 typedef union{
2347     struct{
2348         _IO ODCAL:5;
2349         _IO :2;
2350         _IO ODCAH:4;
2351     };
2352     struct{
2353         _IO ODCAR:16;
2354     };
2355     struct{
2356         _IO ODCA0:1;
2357         _IO ODCA1:1;
2358         _IO ODCA2:1;
2359         _IO ODCA3:1;
2360         _IO ODCA4:1;
2361         _IO :2;
2362         _IO ODCA7:1;
2363         _IO ODCA8:1;
2364         _IO ODCA9:1;
2365         _IO ODCA10:1;
2366     };
2367 }ODCAbits;
2368
2369 #define ODCA    ((ODCAbits*)(ODCA_BASE))
2370 /*****
2371 typedef union{
2372     struct{
2373         _IO TRIS:16;
2374     };
2375     struct{
2376         _IO TRISB0:1;
2377         _IO TRISB1:1;
2378         _IO TRISB2:1;
2379         _IO TRISB3:1;
2380         _IO TRISB4:1;
2381         _IO TRISB5:1;
2382         _IO TRISB6:1;
2383         _IO TRISB7:1;
2384         _IO TRISB8:1;
2385         _IO TRISB9:1;
2386         _IO TRISB10:1;
2387         _IO TRISB11:1;
2388         _IO TRISB12:1;
2389         _IO TRISB13:1;
2390         _IO TRISB14:1;
2391         _IO TRISB15:1;
2392     };
2393 }TRISBbits;
2394
2395 #define TRISB    ((TRISBbits*)(TRISB_BASE))
2396 /*****
2397 typedef union{
2398     struct{
2399         _IO PORT:16;
2400     };
2401     struct{
2402         _IO RB0:1;
2403         _IO RB1:1;
2404         _IO RB2:1;
2405         _IO RB3:1;
2406         _IO RB4:1;
2407         _IO RB5:1;
2408         _IO RB6:1;
2409         _IO RB7:1;

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```

2410         _IO RB8:1;
2411         _IO RB9:1;
2412         _IO RB10:1;
2413         _IO RB11:1;
2414         _IO RB12:1;
2415         _IO RB13:1;
2416         _IO RB14:1;
2417         _IO RB15:1;
2418     };
2419 }PORTBbits;
2420
2421 #define PORTB    ((PORTBbits*) (PORTB_BASE))
2422 /*****
2423 typedef union{
2424     struct{
2425         _IO LAT:16;
2426     };
2427     struct{
2428         _IO LB0:1;
2429         _IO LB1:1;
2430         _IO LB2:1;
2431         _IO LB3:1;
2432         _IO LB4:1;
2433         _IO LB5:1;
2434         _IO LB6:1;
2435         _IO LB7:1;
2436         _IO LB8:1;
2437         _IO LB9:1;
2438         _IO LB10:1;
2439         _IO LB11:1;
2440         _IO LB12:1;
2441         _IO LB13:1;
2442         _IO LB14:1;
2443         _IO LB15:1;
2444     };
2445     struct{
2446         _IO LATB0:1;
2447         _IO LATB1:1;
2448         _IO LATB2:1;
2449         _IO LATB3:1;
2450         _IO LATB4:1;
2451         _IO LATB5:1;
2452         _IO LATB6:1;
2453         _IO LATB7:1;
2454         _IO LATB8:1;
2455         _IO LATB9:1;
2456         _IO LATB10:1;
2457         _IO LATB11:1;
2458         _IO LATB12:1;
2459         _IO LATB13:1;
2460         _IO LATB14:1;
2461         _IO LATB15:1;
2462     };
2463 }LATBbits;
2464
2465 #define LATB    ((LATBbits*) (LATB_BASE))
2466 /*****
2467 typedef union{
2468     struct{
2469         _IO ODCBR:16;
2470     };
2471     struct{
2472         _IO ODCB0:1;
2473         _IO ODCB1:1;
2474         _IO ODCB2:1;
2475         _IO ODCB3:1;
2476         _IO ODCB4:1;
2477         _IO ODCB5:1;
2478         _IO ODCB6:1;
2479         _IO ODCB7:1;
2480         _IO ODCB8:1;
2481         _IO ODCB9:1;
2482         _IO ODCB10:1;

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2483         _IO ODCB11:1;
2484         _IO ODCB12:1;
2485         _IO ODCB13:1;
2486         _IO ODCB14:1;
2487         _IO ODCB15:1;
2488     };
2489 }ODCBbits;
2490
2491 #define ODCB      ((ODCBbits*)(ODCB_BASE))
2492 /*****
2493 typedef union{
2494     struct{
2495         _IO TRIS:10;
2496     };
2497     struct{
2498         _IO TRISC0:1;
2499         _IO TRISC1:1;
2500         _IO TRISC2:1;
2501         _IO TRISC3:1;
2502         _IO TRISC4:1;
2503         _IO TRISC5:1;
2504         _IO TRISC6:1;
2505         _IO TRISC7:1;
2506         _IO TRISC8:1;
2507         _IO TRISC9:1;
2508     };
2509 }TRISCbits;
2510
2511 #define TRISC      ((TRISCbits*)(TRISC_BASE))
2512 /*****
2513 typedef union{
2514     struct{
2515         _IO PORTCR:10;
2516     };
2517     struct{
2518         _IO RC0:1;
2519         _IO RC1:1;
2520         _IO RC2:1;
2521         _IO RC3:1;
2522         _IO RC4:1;
2523         _IO RC6:1;
2524         _IO RC7:1;
2525         _IO RC8:1;
2526         _IO RC9:1;
2527     };
2528 }PORTCbits;
2529
2530 #define PORTC      ((PORTCbits*)(PORTC_BASE))
2531 /*****
2532 typedef union{
2533     struct{
2534         _IO LAT:10;
2535     };
2536     struct{
2537         _IO LC0:1;
2538         _IO LC1:1;
2539         _IO LC2:1;
2540         _IO LC3:1;
2541         _IO LC4:1;
2542         _IO LC5:1;
2543         _IO LC6:1;
2544         _IO LC7:1;
2545         _IO LC8:1;
2546         _IO LC9:1;
2547     };
2548     struct{
2549         _IO LATC0:1;
2550         _IO LATC1:1;
2551         _IO LATC2:1;
2552         _IO LATC3:1;
2553         _IO LATC4:1;
2554         _IO LATC5:1;
2555         _IO LATC6:1;

```

```

2556     _IO LATC7:1;
2557     _IO LATC8:1;
2558     _IO LATC9:1;
2559     };
2560 }LATCbits;
2561
2562 #define LATC ((LATCbits*) (LATC_BASE))
2563 /*****
2564 typedef union{
2565     struct{
2566         _IO ODCCR:10;
2567     };
2568     struct{
2569         _IO ODCC0:1;
2570         _IO ODCC1:1;
2571         _IO ODCC2:1;
2572         _IO ODCC3:1;
2573         _IO ODCC4:1;
2574         _IO ODCC5:1;
2575         _IO ODCC6:1;
2576         _IO ODCC7:1;
2577         _IO ODCC8:1;
2578         _IO ODCC9:1;
2579     };
2580 }ODCCbits;
2581
2582 #define ODCC ((ODCCbits*) (ODCC_BASE))
2583 /*****
2584 //          REGISTRIRANJE ULAZNIH PINOVA ZA PERIFERALE:(13 registara)
2585 //          (INUT PIN REMAPPING)
2586 /*****
2587 typedef union {
2588     struct {
2589         _IO :8;
2590         _IO INT1R:5;
2591     };
2592     struct {
2593         _IO :8;
2594         _IO INT1R0:1;
2595         _IO INT1R1:1;
2596         _IO INT1R2:1;
2597         _IO INT1R3:1;
2598         _IO INT1R4:1;
2599     };
2600 }RPINR0bits;
2601
2602 #define RPINR0 ((RPINR0bits*) (RPINR0_BASE))
2603 /*****
2604 typedef union {
2605     struct {
2606         _IO INT2R:5;
2607     };
2608     struct {
2609         _IO INT2R0:1;
2610         _IO INT2R1:1;
2611         _IO INT2R2:1;
2612         _IO INT2R3:1;
2613         _IO INT2R4:1;
2614     };
2615 }RPINR1bits;
2616
2617 #define RPINR1 ((RPINR1bits*) (RPINR1_BASE))
2618 /*****
2619 typedef union {
2620     struct {
2621         _IO T2CKR:5;
2622         _IO :3;
2623         _IO T3CKR:5;
2624     };
2625     struct {
2626         _IO T2CKR0:1;
2627         _IO T2CKR1:1;
2628         _IO T2CKR2:1;

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```

2629         _IO T2CKR3:1;
2630         _IO T2CKR4:1;
2631         _IO :3;
2632         _IO T3CKR0:1;
2633         _IO T3CKR1:1;
2634         _IO T3CKR2:1;
2635         _IO T3CKR3:1;
2636         _IO T3CKR4:1;
2637     };
2638 }RPINR3bits;
2639
2640 #define RPINR3      ((RPINR3bits*) (RPINR3_BASE))
2641 /*****
2642 typedef union {
2643     struct {
2644         _IO IC1R:5;
2645         _IO :3;
2646         _IO IC2R:5;
2647     };
2648     struct {
2649         _IO IC1R0:1;
2650         _IO IC1R1:1;
2651         _IO IC1R2:1;
2652         _IO IC1R3:1;
2653         _IO IC1R4:1;
2654         _IO :3;
2655         _IO IC2R0:1;
2656         _IO IC2R1:1;
2657         _IO IC2R2:1;
2658         _IO IC2R3:1;
2659         _IO IC2R4:1;
2660     };
2661 }RPINR7bits;
2662
2663 #define RPINR7      ((RPINR7bits*) (RPINR7_BASE))
2664 /*****
2665 typedef union {
2666     struct {
2667         _IO IC7R:5;
2668         _IO :3;
2669         _IO IC8R:5;
2670     };
2671     struct {
2672         _IO IC7R0:1;
2673         _IO IC7R1:1;
2674         _IO IC7R2:1;
2675         _IO IC7R3:1;
2676         _IO IC7R4:1;
2677         _IO :3;
2678         _IO IC8R0:1;
2679         _IO IC8R1:1;
2680         _IO IC8R2:1;
2681         _IO IC8R3:1;
2682         _IO IC8R4:1;
2683     };
2684 }RPINR10bits;
2685
2686 #define RPINR10     ((RPINR10bits*) (RPINR10_BASE))
2687 /*****
2688 typedef union {
2689     struct {
2690         _IO OCFAR:5;
2691     };
2692     struct {
2693         _IO OCFAR0:1;
2694         _IO OCFAR1:1;
2695         _IO OCFAR2:1;
2696         _IO OCFAR3:1;
2697         _IO OCFAR4:1;
2698     };
2699 }RPINR11bits;
2700
2701 #define RPINR11     ((RPINR11bits*) (RPINR11_BASE))

```

```

2702  /*****
2703  typedef union {
2704      struct {
2705          _IO FLTA1R:5;
2706      };
2707      struct {
2708          _IO FLTA1R0:1;
2709          _IO FLTA1R1:1;
2710          _IO FLTA1R2:1;
2711          _IO FLTA1R3:1;
2712          _IO FLTA1R4:1;
2713      };
2714  }RPINR12bits;
2715
2716  #define RPINR12    ((RPINR12bits*) (RPINR12_BASE))
2717  /*****
2718  typedef union {
2719      struct {
2720          _IO FLTA2R:5;
2721      };
2722      struct {
2723          _IO FLTA2R0:1;
2724          _IO FLTA2R1:1;
2725          _IO FLTA2R2:1;
2726          _IO FLTA2R3:1;
2727          _IO FLTA2R4:1;
2728      };
2729  }RPINR13bits;
2730
2731  #define RPINR13    ((RPINR13bits*) (RPINR13_BASE))
2732  /*****
2733  typedef union {
2734      struct {
2735          _IO QEA1R:5;
2736          _IO :3;
2737          _IO QEB1R:5;
2738      };
2739      struct {
2740          _IO QEA1R0:1;
2741          _IO QEA1R1:1;
2742          _IO QEA1R2:1;
2743          _IO QEA1R3:1;
2744          _IO QEA1R4:1;
2745          _IO :3;
2746          _IO QEB1R0:1;
2747          _IO QEB1R1:1;
2748          _IO QEB1R2:1;
2749          _IO QEB1R3:1;
2750          _IO QEB1R4:1;
2751      };
2752  }RPINR14bits;
2753
2754  #define RPINR14    ((RPINR14bits*) (RPINR14_BASE))
2755  /*****
2756  typedef union {
2757      struct {
2758          _IO INDX1R:5;
2759      };
2760      struct {
2761          _IO INDX1R0:1;
2762          _IO INDX1R1:1;
2763          _IO INDX1R2:1;
2764          _IO INDX1R3:1;
2765          _IO INDX1R4:1;
2766      };
2767  }RPINR15bits;
2768
2769  #define RPINR15    ((RPINR15bits*) (RPINR15_BASE))
2770  /*****
2771  typedef union {
2772      struct {
2773          _IO U1RXR:5;
2774          _IO :3;

```

```

2775         _IO U1CTSR:5;
2776     };
2777     struct {
2778         _IO U1RXR0:1;
2779         _IO U1RXR1:1;
2780         _IO U1RXR2:1;
2781         _IO U1RXR3:1;
2782         _IO U1RXR4:1;
2783         _IO :3;
2784         _IO U1CTSR0:1;
2785         _IO U1CTSR1:1;
2786         _IO U1CTSR2:1;
2787         _IO U1CTSR3:1;
2788         _IO U1CTSR4:1;
2789     };
2790 }RPINR18bits;
2791
2792 #define RPINR18      ((RPINR18bits*) (RPINR18_BASE))
2793 /*****
2794 typedef union {
2795     struct {
2796         _IO SDI1R:5;
2797         _IO :3;
2798         _IO SCK1R:5;
2799     };
2800     struct {
2801         _IO SDI1R0:1;
2802         _IO SDI1R1:1;
2803         _IO SDI1R2:1;
2804         _IO SDI1R3:1;
2805         _IO SDI1R4:1;
2806         _IO :3;
2807         _IO SCK1R0:1;
2808         _IO SCK1R1:1;
2809         _IO SCK1R2:1;
2810         _IO SCK1R3:1;
2811         _IO SCK1R4:1;
2812     };
2813 }RPINR20bits;
2814
2815 #define RPINR20      ((RPINR20bits*) (RPINR20_BASE))
2816 /*****
2817 typedef union {
2818     struct {
2819         _IO SS1R:5;
2820     };
2821     struct {
2822         _IO SS1R0:1;
2823         _IO SS1R1:1;
2824         _IO SS1R2:1;
2825         _IO SS1R3:1;
2826         _IO SS1R4:1;
2827     };
2828 }RPINR21bits;
2829
2830 #define RPINR21      ((RPINR21bits*) (RPINR21_BASE))
2831 /*****
2832 //          REGISTRI REMAPIRANJA IZLAZNIH PINOVA ZA PERIFERALE:(13 registara)
2833 //          (OUTPUT PIN REMAPPING)
2834 /*****
2835 typedef union {
2836     struct {
2837         _IO RP0R:5;
2838         _IO :3;
2839         _IO RP1R:5;
2840     };
2841     struct {
2842         _IO RP0R0:1;
2843         _IO RP0R1:1;
2844         _IO RP0R2:1;
2845         _IO RP0R3:1;
2846         _IO RP0R4:1;
2847         _IO :3;

```

```

2848         _IO RP1R0:1;
2849         _IO RP1R1:1;
2850         _IO RP1R2:1;
2851         _IO RP1R3:1;
2852         _IO RP1R4:1;
2853     };
2854 }RPOR0bits;
2855
2856 #define RPOR0    ((RPOR0bits*) (RPOR0_BASE))
2857 /*****
2858 typedef union {
2859     struct {
2860         _IO RP2R:5;
2861         _IO :3;
2862         _IO RP3R:5;
2863     };
2864     struct {
2865         _IO RP2R0:1;
2866         _IO RP2R1:1;
2867         _IO RP2R2:1;
2868         _IO RP2R3:1;
2869         _IO RP2R4:1;
2870         _IO :3;
2871         _IO RP3R0:1;
2872         _IO RP3R1:1;
2873         _IO RP3R2:1;
2874         _IO RP3R3:1;
2875         _IO RP3R4:1;
2876     };
2877 }RPOR1bits;
2878
2879 #define RPOR1    ((RPOR1bits*) (RPOR1_BASE))
2880 /*****
2881 typedef union {
2882     struct {
2883         _IO RP4R:5;
2884         _IO :3;
2885         _IO RP5R:5;
2886     };
2887     struct {
2888         _IO RP4R0:1;
2889         _IO RP4R1:1;
2890         _IO RP4R2:1;
2891         _IO RP4R3:1;
2892         _IO RP4R4:1;
2893         _IO :3;
2894         _IO RP5R0:1;
2895         _IO RP5R1:1;
2896         _IO RP5R2:1;
2897         _IO RP5R3:1;
2898         _IO RP5R4:1;
2899     };
2900 }RPOR2bits;
2901
2902 #define RPOR2    ((RPOR2bits*) (RPOR2_BASE))
2903 /*****
2904 typedef union {
2905     struct {
2906         _IO RP6R:5;
2907         _IO :3;
2908         _IO RP7R:5;
2909     };
2910     struct {
2911         _IO RP6R0:1;
2912         _IO RP6R1:1;
2913         _IO RP6R2:1;
2914         _IO RP6R3:1;
2915         _IO RP6R4:1;
2916         _IO :3;
2917         _IO RP7R0:1;
2918         _IO RP7R1:1;
2919         _IO RP7R2:1;
2920         _IO RP7R3:1;

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```

2921         _IO RP7R4:1;
2922     };
2923 }RPOR3bits;
2924
2925 #define RPOR3      ((RPOR3bits*) (RPOR3_BASE))
2926 /*****
2927 typedef union {
2928     struct {
2929         _IO RP8R:5;
2930         _IO :3;
2931         _IO RP9R:5;
2932     };
2933     struct {
2934         _IO RP8R0:1;
2935         _IO RP8R1:1;
2936         _IO RP8R2:1;
2937         _IO RP8R3:1;
2938         _IO RP8R4:1;
2939         _IO :3;
2940         _IO RP9R0:1;
2941         _IO RP9R1:1;
2942         _IO RP9R2:1;
2943         _IO RP9R3:1;
2944         _IO RP9R4:1;
2945     };
2946 }RPOR4bits;
2947
2948 #define RPOR4      ((RPOR4bits*) (RPOR4_BASE))
2949 /*****
2950 typedef union {
2951     struct {
2952         _IO RP10R:5;
2953         _IO :3;
2954         _IO RP11R:5;
2955     };
2956     struct {
2957         _IO RP10R0:1;
2958         _IO RP10R1:1;
2959         _IO RP10R2:1;
2960         _IO RP10R3:1;
2961         _IO RP10R4:1;
2962         _IO :3;
2963         _IO RP11R0:1;
2964         _IO RP11R1:1;
2965         _IO RP11R2:1;
2966         _IO RP11R3:1;
2967         _IO RP11R4:1;
2968     };
2969 }RPOR5bits;
2970
2971 #define RPOR5      ((RPOR5bits*) (RPOR5_BASE))
2972 /*****
2973 typedef union {
2974     struct {
2975         _IO RP12R:5;
2976         _IO :3;
2977         _IO RP13R:5;
2978     };
2979     struct {
2980         _IO RP12R0:1;
2981         _IO RP12R1:1;
2982         _IO RP12R2:1;
2983         _IO RP12R3:1;
2984         _IO RP12R4:1;
2985         _IO :3;
2986         _IO RP13R0:1;
2987         _IO RP13R1:1;
2988         _IO RP13R2:1;
2989         _IO RP13R3:1;
2990         _IO RP13R4:1;
2991     };
2992 }RPOR6bits;
2993

```

```

2994 #define RPOR6      ((RPOR6bits*) (RPOR6_BASE))
2995 /*****
2996 typedef union {
2997     struct {
2998         _IO RP14R:5;
2999         _IO :3;
3000         _IO RP15R:5;
3001     };
3002     struct {
3003         _IO RP14R0:1;
3004         _IO RP14R1:1;
3005         _IO RP14R2:1;
3006         _IO RP14R3:1;
3007         _IO RP14R4:1;
3008         _IO :3;
3009         _IO RP15R0:1;
3010         _IO RP15R1:1;
3011         _IO RP15R2:1;
3012         _IO RP15R3:1;
3013         _IO RP15R4:1;
3014     };
3015 }RPOR7bits;
3016
3017 #define RPOR7      ((RPOR7bits*) (RPOR7_BASE))
3018 /*****
3019 typedef union {
3020     struct {
3021         _IO RP16R:5;
3022         _IO :3;
3023         _IO RP17R:5;
3024     };
3025     struct {
3026         _IO RP16R0:1;
3027         _IO RP16R1:1;
3028         _IO RP16R2:1;
3029         _IO RP16R3:1;
3030         _IO RP16R4:1;
3031         _IO :3;
3032         _IO RP17R0:1;
3033         _IO RP17R1:1;
3034         _IO RP17R2:1;
3035         _IO RP17R3:1;
3036         _IO RP17R4:1;
3037     };
3038 }RPOR8bits;
3039
3040 #define RPOR8      ((RPOR8bits*) (RPOR8_BASE))
3041 /*****
3042 typedef union {
3043     struct {
3044         _IO RP18R:5;
3045         _IO :3;
3046         _IO RP19R:5;
3047     };
3048     struct {
3049         _IO RP18R0:1;
3050         _IO RP18R1:1;
3051         _IO RP18R2:1;
3052         _IO RP18R3:1;
3053         _IO RP18R4:1;
3054         _IO :3;
3055         _IO RP19R0:1;
3056         _IO RP19R1:1;
3057         _IO RP19R2:1;
3058         _IO RP19R3:1;
3059         _IO RP19R4:1;
3060     };
3061 }RPOR9bits;
3062
3063 #define RPOR9      ((RPOR9bits*) (RPOR9_BASE))
3064 /*****
3065 typedef union {
3066     struct {

```

```

3067         _IO RP20R:5;
3068         _IO :3;
3069         _IO RP21R:5;
3070     };
3071     struct {
3072         _IO RP20R0:1;
3073         _IO RP20R1:1;
3074         _IO RP20R2:1;
3075         _IO RP20R3:1;
3076         _IO RP20R4:1;
3077         _IO :3;
3078         _IO RP21R0:1;
3079         _IO RP21R1:1;
3080         _IO RP21R2:1;
3081         _IO RP21R3:1;
3082         _IO RP21R4:1;
3083     };
3084 }RPOR10bits;
3085
3086 #define RPOR10 ((RPOR10bits*) (RPOR10_BASE))
3087 /*****
3088 typedef union {
3089     struct {
3090         _IO RP22R:5;
3091         _IO :3;
3092         _IO RP23R:5;
3093     };
3094     struct {
3095         _IO RP22R0:1;
3096         _IO RP22R1:1;
3097         _IO RP22R2:1;
3098         _IO RP22R3:1;
3099         _IO RP22R4:1;
3100         _IO :3;
3101         _IO RP23R0:1;
3102         _IO RP23R1:1;
3103         _IO RP23R2:1;
3104         _IO RP23R3:1;
3105         _IO RP23R4:1;
3106     };
3107 }RPOR11bits;
3108
3109 #define RPOR11 ((RPOR11bits*) (RPOR11_BASE))
3110 /*****
3111 typedef union {
3112     struct {
3113         _IO RP24R:5;
3114         _IO :3;
3115         _IO RP25R:5;
3116     };
3117     struct {
3118         _IO RP24R0:1;
3119         _IO RP24R1:1;
3120         _IO RP24R2:1;
3121         _IO RP24R3:1;
3122         _IO RP24R4:1;
3123         _IO :3;
3124         _IO RP25R0:1;
3125         _IO RP25R1:1;
3126         _IO RP25R2:1;
3127         _IO RP25R3:1;
3128         _IO RP25R4:1;
3129     };
3130 }RPOR12bits;
3131
3132 #define RPOR12 ((RPOR12bits*) (RPOR12_BASE))
3133 /*****
3134 //             REGISTRİ KONTROLE SISTEMA:
3135 //
3136 /*****
3137 typedef union{
3138     struct{
3139         _IO POR:1;

```

```

3140         _IO BOR:1;
3141         _IO IDLE:1;
3142         _IO SLEEP:1;
3143         _IO WDTO:1;
3144         _IO SWDTEN:1;
3145         _IO SWR:1;
3146         _IO EXTR:1;
3147         _IO VREGS:1;
3148         _IO CM:1;
3149         _IO :4;
3150         _IO IOPUWR:1;
3151         _IO TRAPR:1;
3152     };
3153 }RCONbits;
3154
3155 #define RCON ((RCONbits*)(RCON_BASE))
3156 /*****
3157 typedef union {
3158     struct {
3159         _IO OSWEN:1;
3160         _IO LPOSCEN:1;
3161         _IO :1;
3162         _IO CF:1;
3163         _IO :1;
3164         _IO LOCK:1;
3165         _IO IOLOCK:1;
3166         _IO CLKLOCK:1;
3167         _IO NOSC:3;
3168         _IO :1;
3169         _IO COSC:3;
3170     };
3171     struct {
3172         _IO :8;
3173         _IO NOSC0:1;
3174         _IO NOSC1:1;
3175         _IO NOSC2:1;
3176         _IO :1;
3177         _IO COSC0:1;
3178         _IO COSC1:1;
3179         _IO COSC2:1;
3180     };
3181 }OSCCONbits;
3182
3183 #define OSCCON ((OSCCONbits*)(OSCCON_BASE))
3184 /*****
3185 typedef union {
3186     struct {
3187         _IO PLLPRE:5;
3188         _IO :1;
3189         _IO PLLPOST:2;
3190         _IO FRCDIV:3;
3191         _IO DOZEN:1;
3192         _IO DOZE:3;
3193         _IO ROI:1;
3194     };
3195     struct {
3196         _IO PLLPRE0:1;
3197         _IO PLLPRE1:1;
3198         _IO PLLPRE2:1;
3199         _IO PLLPRE3:1;
3200         _IO PLLPRE4:1;
3201         _IO :1;
3202         _IO PLLPOST0:1;
3203         _IO PLLPOST1:1;
3204         _IO FRCDIV0:1;
3205         _IO FRCDIV1:1;
3206         _IO FRCDIV2:1;
3207         _IO :1;
3208         _IO DOZE0:1;
3209         _IO DOZE1:1;
3210         _IO DOZE2:1;
3211     };
3212 }CLKDIVbits;

```

```

3213 #define CLKDIV      ((CLKDIVbits*)(CLKDIV_BASE))
3214 /*****
3215
3216 typedef union {
3217     struct {
3218         _IO PLLDIV:9;
3219     };
3220     struct {
3221         _IO PLLDIV0:1;
3222         _IO PLLDIV1:1;
3223         _IO PLLDIV2:1;
3224         _IO PLLDIV3:1;
3225         _IO PLLDIV4:1;
3226         _IO PLLDIV5:1;
3227         _IO PLLDIV6:1;
3228         _IO PLLDIV7:1;
3229         _IO PLLDIV8:1;
3230     };
3231 }PLLFBDbits;
3232
3233 #define PLLFBD      ((PLLFBDbits*)(PLLFBD_BASE))
3234 /*****
3235
3236 typedef union {
3237     struct {
3238         _IO TUN:6;
3239     };
3240     struct {
3241         _IO TUN0:1;
3242         _IO TUN1:1;
3243         _IO TUN2:1;
3244         _IO TUN3:1;
3245         _IO TUN4:1;
3246         _IO TUN5:1;
3247     };
3248 }OSCTUNbits;
3249
3250 #define OSCTUN      ((OSCTUNbits*)(OSCTUN_BASE))
3251 /*****
3252 //
3253 //          NVM KONTROLNI REGISTR: (2 registra)
3254 //
3255 /*****
3256 typedef union {
3257     struct {
3258         _IO NVMOP:4;
3259         _IO _IO :2;
3260         _IO ERASE:1;
3261         _IO _IO :6;
3262         _IO WRERR:1;
3263         _IO WREN:1;
3264         _IO WR:1;
3265     };
3266     struct {
3267         _IO NVMOP0:1;
3268         _IO NVMOP1:1;
3269         _IO NVMOP2:1;
3270         _IO NVMOP3:1;
3271     };
3272 }NVMCONbits;
3273
3274 #define NVMCON      ((NVMCONbits*)(NVMCON_BASE))
3275 /*****
3276
3277 typedef union
3278 {
3279     struct
3280     {
3281         _IO NVMKEYR:8;//BUG!!!
3282     };
3283 }NVMKEYbits;
3284
3285 #define NVMKEY      ((NVMKEYbits*)(NVMKEY_BASE))
3286 /*****
3287 //
3288 //          PMD KONTROLNI REGISTR: (3 registra)
3289 //          (ONEMOGUCAVANJE MODULA PERIFERALA)

```

```

3286  /*****
3287  typedef union {
3288      struct {
3289          _IO AD1MD:1;
3290          _IO :2;
3291          _IO SPI1MD:1;
3292          _IO :1;
3293          _IO U1MD:1;
3294          _IO :1;
3295          _IO I2C1MD:1;
3296          _IO :1;
3297          _IO PWM1MD:1;
3298          _IO QE1MD:1;
3299          _IO T1MD:1;
3300          _IO T2MD:1;
3301          _IO T3MD:1;
3302      };
3303  }PMD1bits;
3304
3305  #define PMD1 ((PMD1bits*)(PMD1_BASE))
3306  /*****
3307  typedef union {
3308      struct {
3309          _IO OC1MD:1;
3310          _IO OC2MD:1;
3311          _IO :6;
3312          _IO IC1MD:1;
3313          _IO IC2MD:1;
3314          _IO :4;
3315          _IO IC7MD:1;
3316          _IO IC8MD:1;
3317      };
3318  }PMD2bits;
3319
3320  #define PMD2 ((PMD2bits*)(PMD2_BASE))
3321  /*****
3322  typedef union {
3323      struct {
3324          _IO :4;
3325          _IO PWM2MD:1;
3326      };
3327  }PMD3bits;
3328
3329  #define PMD3 ((PMD3bits*)(PMD3_BASE))
3330  /*****
3331  #endif
3332

```