# UNIVERSITY OF TECHNOLOGY-VNU-HCM

## Falcuty of Electrical-Electronis


# COMPUTER ARCHITECTURE-MILESTONE

Design a 32 bit single-cycle cpu RISC-V

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Group: ca120


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## I. FEATURE LIST.

- Review basic concepts of sequential logic and Finite State Machine (FSM) design.
- Implement a simple vending machine using System Verilog.
- Practice simulation and waveform analysis to verify system functionality.

## II. PROBLEM STATEMENT.

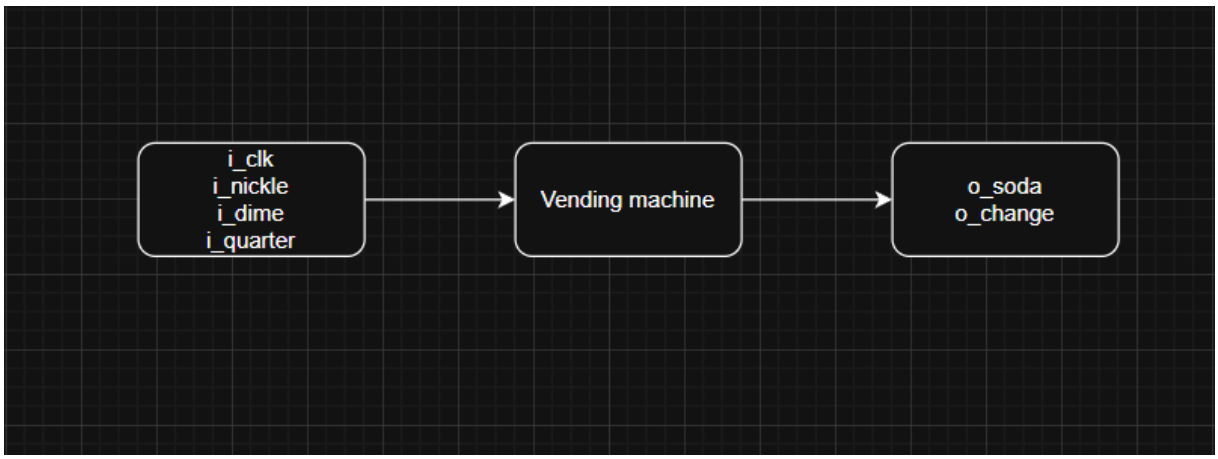
**Design a vending machine with the following requirements:**

- Accepts coins: ¢5 (nickel), ¢10 (dime), ¢25 (quarter).
- Only one coin is accepted per clock cycle.
- When the total amount of money inserted is **≥ ¢20**, the machine should:
  **Dispense a soda** (o_soda = 1)
  **Return change** (o_change), encoded as a 3-bit value:

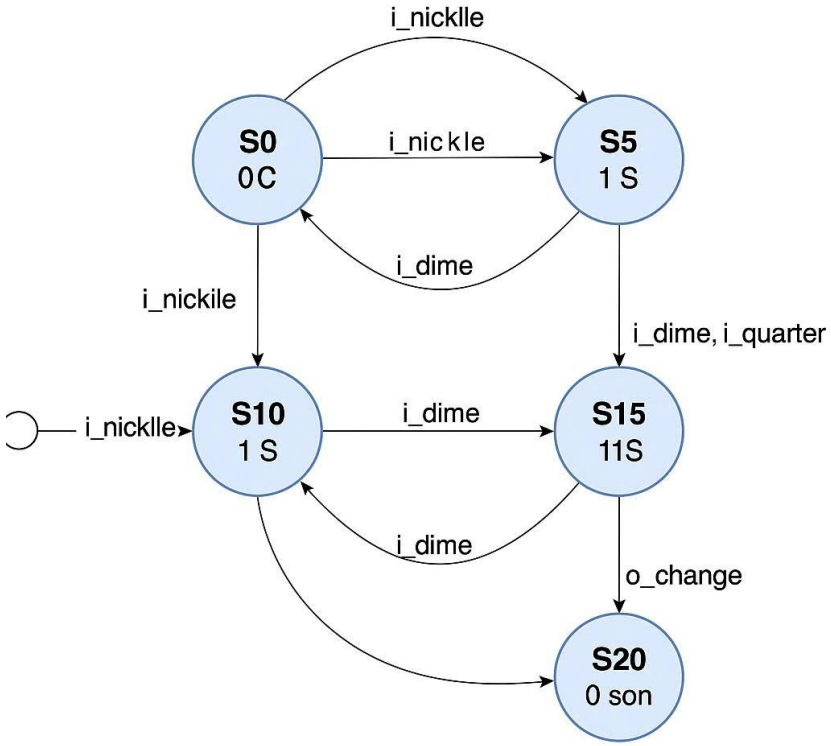
| o_change Value | Change Amount |
|---|---|
| 000 | ¢0 |
| 001 | ¢5 |
| 010 | ¢10 |
| 011 | ¢15 |
| 100 | ¢20 |

## III. SYSTEM DESIGN.

### 3.1. Block diagram



### 3.2. FSM state diagram

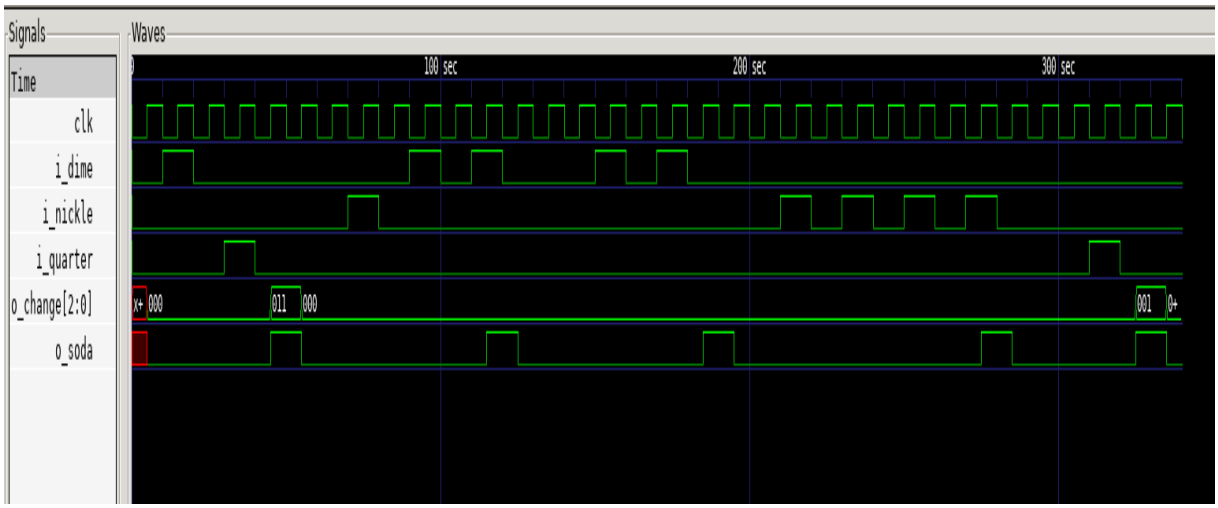



## IV. SIMULATION.

### 4.1. Test cases

| Test | Sequence | Total | Expected Result |
|---|---|---|---|
| 1 | dime + quarter | ¢35 | `o_soda = 1`, `o_change = 011` (¢15) |
| 2 | 4 × nickel | ¢20 | `o_soda = 1`, `o_change = 000` (no change) |
| 3 | 2 × dime | ¢20 | `o_soda = 1`, `o_change = 000` |
| 4 | 1 × quarter | ¢25 | `o_soda = 1`, `o_change = 001` (¢5) |

### 4.2. Waveform




## V. EVALUATION.

- The vending machine works correctly according to the specifications.
- FSM transitions and outputs are verified to be accurate.
- Edge cases (exactly 20¢, extra change, multiple coin sequences) are handled correctly.
- Clean and modular Verilog code, easy to expand or modify.