DC Analysis of Transistor Circuits

DC analysis procedure:

For DC analysis, knowledge of mode of operation of the transistor is required. Sometimes Guess to Start!

- Assume transistor in forward-active mode,

  $V_{BE} = V_{BE}$ (on), I_B>0 and I_C=βI_B.
- If analysis proves I_B<0 and V_{CE}<V_{CE} *(sat)* then assumption is wrong, restart.

$$I_C / I_B < \beta$$

Biased in Saturation mode (both forward bias)

$$\frac{I_C}{I_B} \equiv \beta_{\text{Forced}} \qquad \beta_{\text{Forced}} < \beta$$

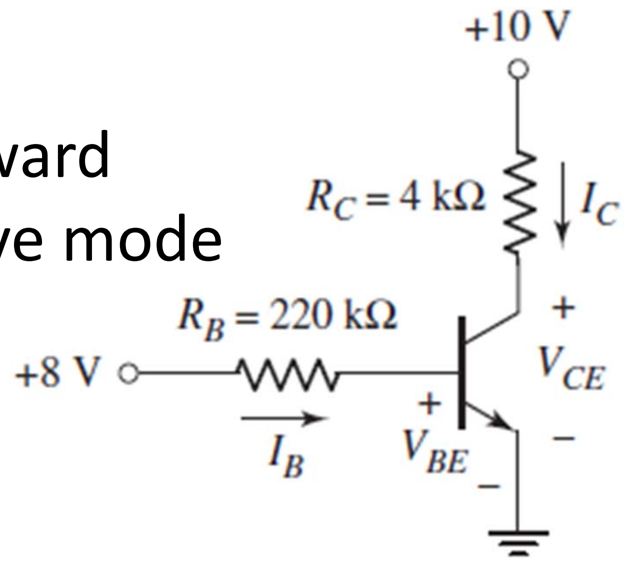
Example (tutorial):

$$I_B = \frac{V_{BB} - V_{BE}(\mathrm{on})}{R_B}$$

Forward active mode

$$I_C = \beta I_B$$

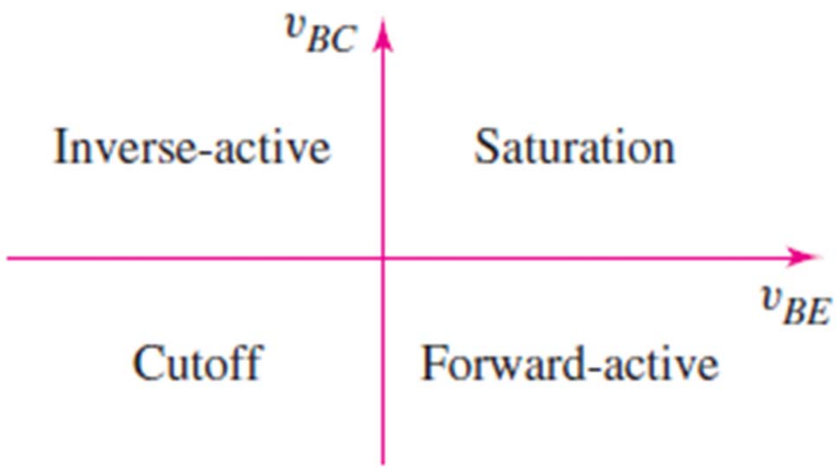
given



$$V_{CE} = V_{CC} - I_C R_C$$ → Negative (<V_{CE}(Sat))

$$I_C = I_C(\mathrm{sat}) = \frac{V_{CC} - V_{CE}(\mathrm{sat})}{R_C}$$ → given $\frac{I_C}{I_B} < \beta$

4 modes



Inverse-active mode:

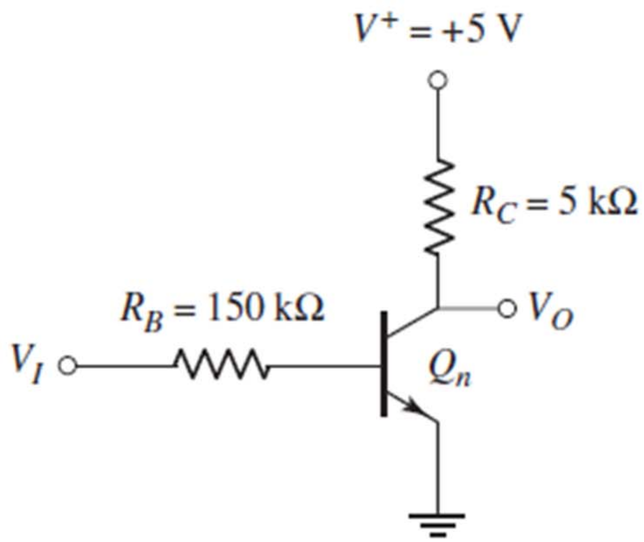
B–E junction is reverse biased and the B–C junction is forward biased.

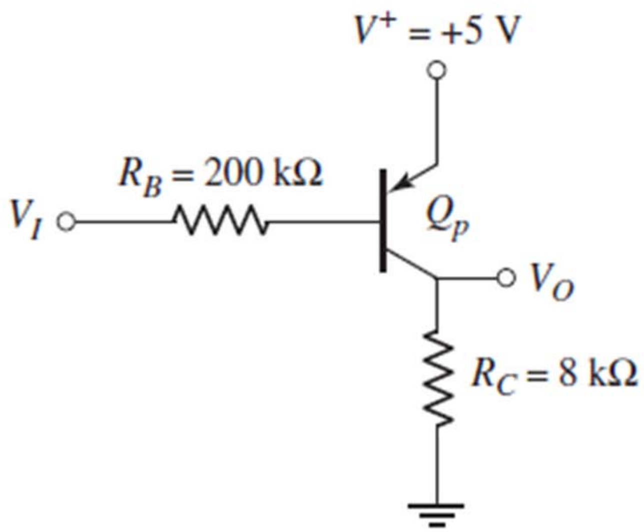
- The transistor is operating “upside down”, emitter acting as a collector and collector as an emitter
- Transistors are not electrically & physically symmetrical, so it will have significantly smaller β
- BJTs have very low saturation voltage (mV)
- App: Digital Electronics Circuit

Piecewise linear model ←→ Ebers-Moll model

Voltage Transfer Characteristics:

Output voltage versus input voltage





$$V_{BE}(on) = 0.7V, \beta = 120,$$
$$V_{CE}(sat) = 0.2V, V_A \to \infty$$

$$V_{EB}(on) = 0.7V, \beta = 80,$$
$$V_{EC}(sat) = 0.2V, V_A \to \infty$$

NPN

$$I_B = \frac{V_I - 0.7}{R_B}$$

$V_I \leq 0.7\ \text{V}$, $\quad I_B = I_C = 0.$ $\quad V_O = V^+ = 5\ \text{V}.$

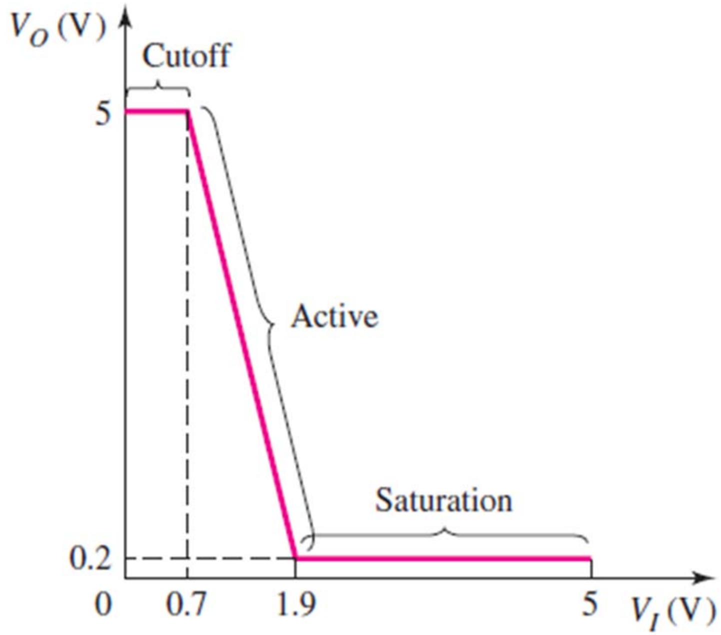
$V_I > 0.7\ \text{V}$

$$I_C = \beta I_B = \frac{\beta(V_I - 0.7)}{R_B}$$

$$V_O = 5 - I_C R_C = 5 - \frac{\beta(V_I - 0.7)R_C}{R_B}$$

$\boldsymbol{V_O = V_{CE}}$ $\quad V_O = 0.2\ \text{V}$ $\quad V_I = 1.9\ \text{V}.$

$V_I \geq 1.9\ \text{V}$ $\quad V_O = 0.2\ \text{V}.$



PNP

$$4.3 \le V_I \qquad I_B = I_C = 0 \qquad V_O = 0$$

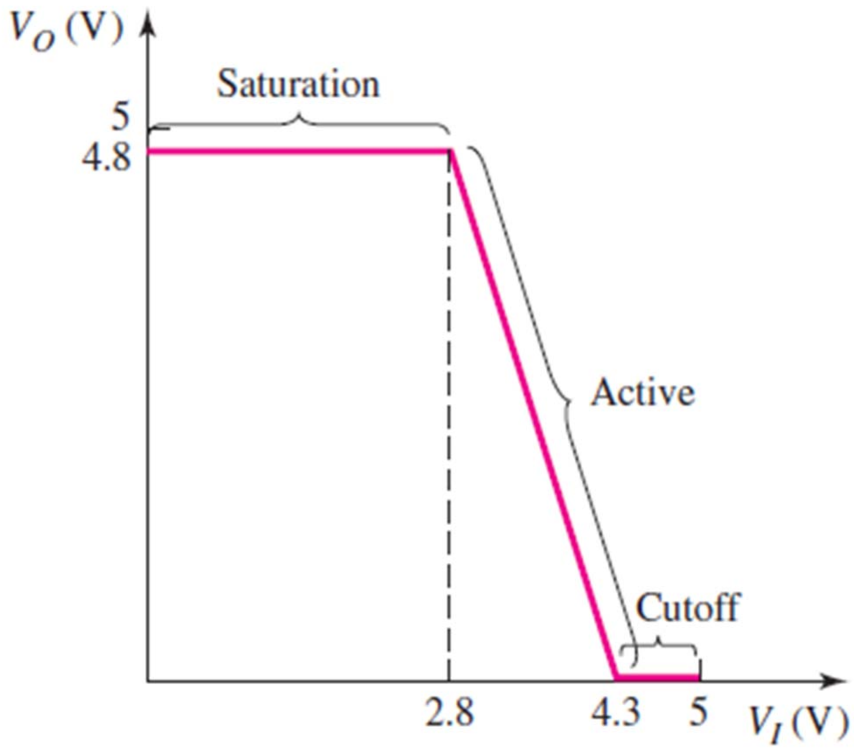
$$V_I < 4.3 \text{ V} \qquad I_B = \frac{(5-0.7)-V_I}{R_B} \qquad I_C = \beta I_B = \beta\left[\frac{(5-0.7)-V_I}{R_B}\right]$$

$$V_O = I_C R_C = \beta R_C\left[\frac{(5-0.7)-V_I}{R_B}\right]$$

$$V^+ - V_O = V_{EC} \qquad V_O = 4.8\text{ V} \qquad V_I = 2.8\text{ V}$$

$$V_I \leq 2.8\text{ V}$$

$$V_O = 4.8\text{ V}$$

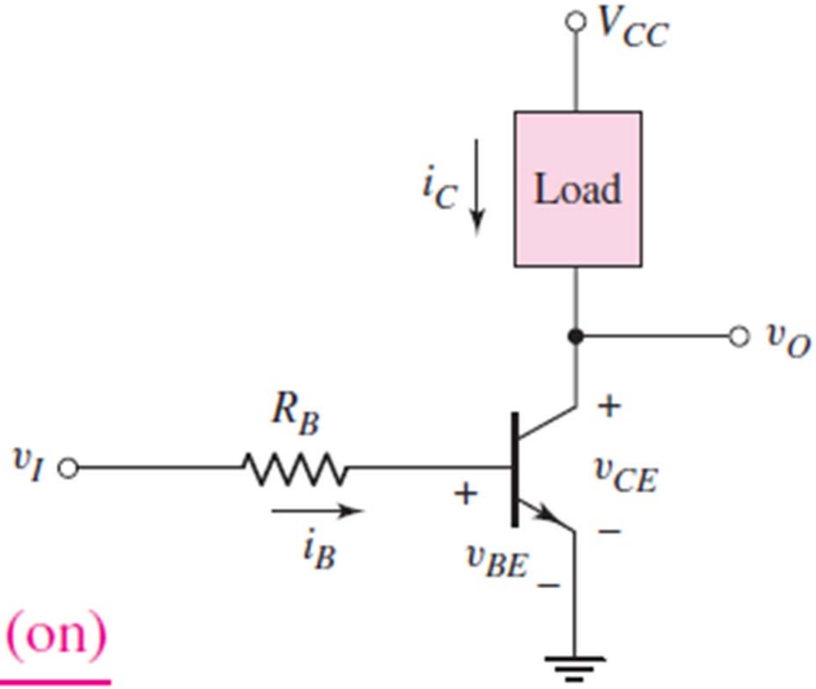


Voltage transfer characteristics are determined by finding the range of input voltage values that biases the transistor in cut off, the forward-active mode, or the saturation mode.

Basic Transistor Applications

Switch:

Inverter



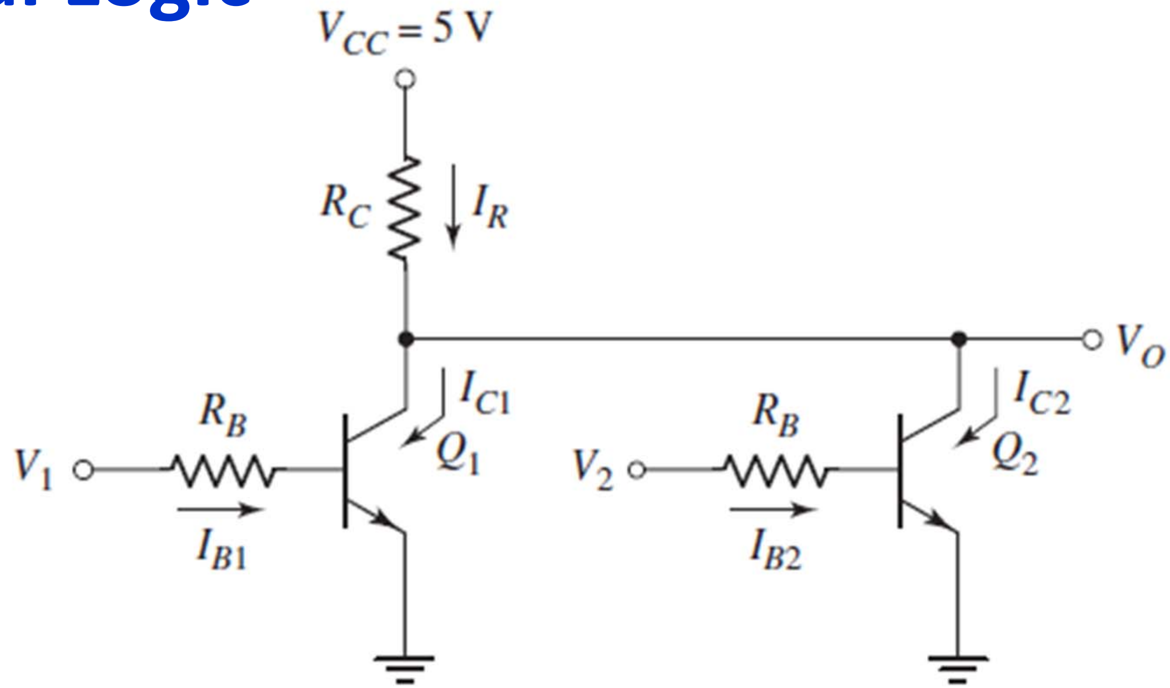
$$i_B \cong \frac{v_I - V_{BE}(\text{on})}{R_B}$$

$v_I < V_{BE}(\text{on})$ $\qquad$ $i_B = i_C = 0$ $\qquad$ $v_O = V_{CC}$

$v_I = V_{CC}$ $\qquad$ $\boldsymbol{\frac{R_B}{R_C} < \beta \rightarrow saturation\ mode}$

$$i_C = I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C} \qquad v_O = V_{CE}(\text{sat})$$

Digital Logic



$$V_1 = 0, V_2 = 0 \rightarrow V_O = 5V, both\ cut\ off$$

$$V_1 = 5, V_2 = 0 \rightarrow V_O = 0.2V, Q1\ saturation\ Q2\ cut\ off$$

$$V_1 = 0, V_2 = 5 \rightarrow V_O = 0.2V, Q2\ saturation\ Q1\ cut\ off$$

$$V_1 = 5, V_2 = 5 \rightarrow V_O = 0.2V, Q1\ saturation\ Q2saturation$$

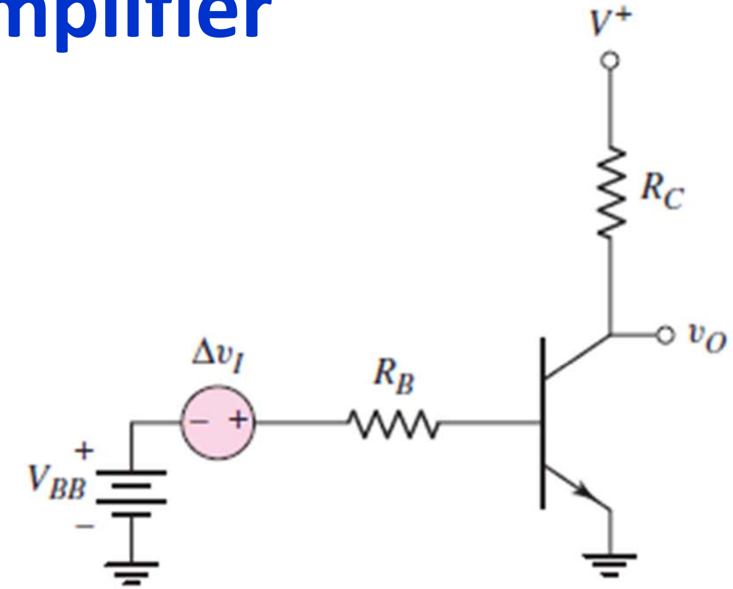
Positive logic system - NOR logic function

- Bipolar transistor circuits can be configured to perform logic functions
- Logic circuits must be designed to minimize or eliminate such loading effects

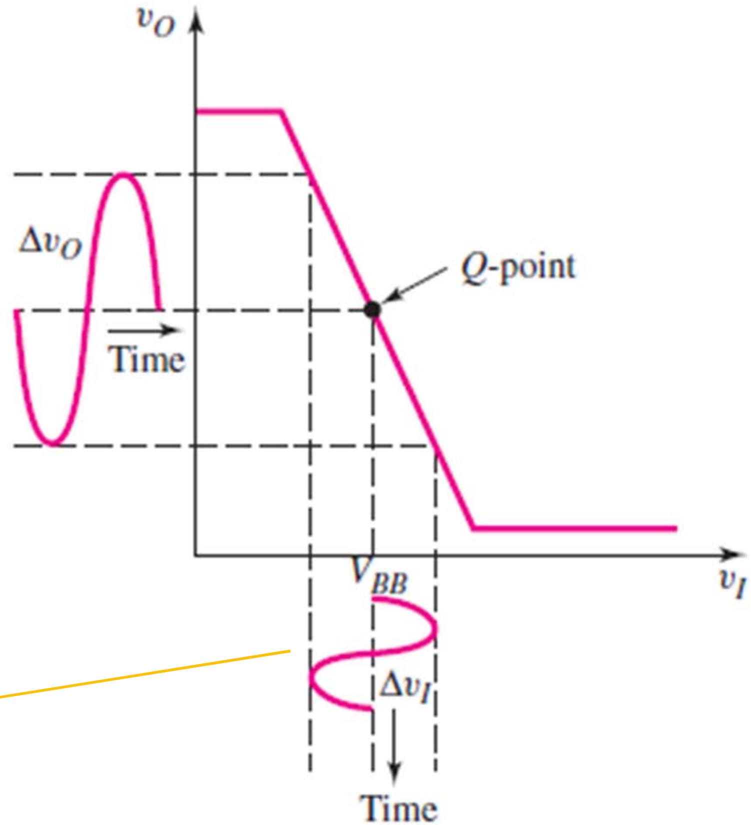
The bipolar NOR logic circuit response

V_1 (V)	V_2 (V)	V_O (V)
0	0	5
5	0	0.2
0	5	0.2
5	5	0.2

Amplifier



In forward active region

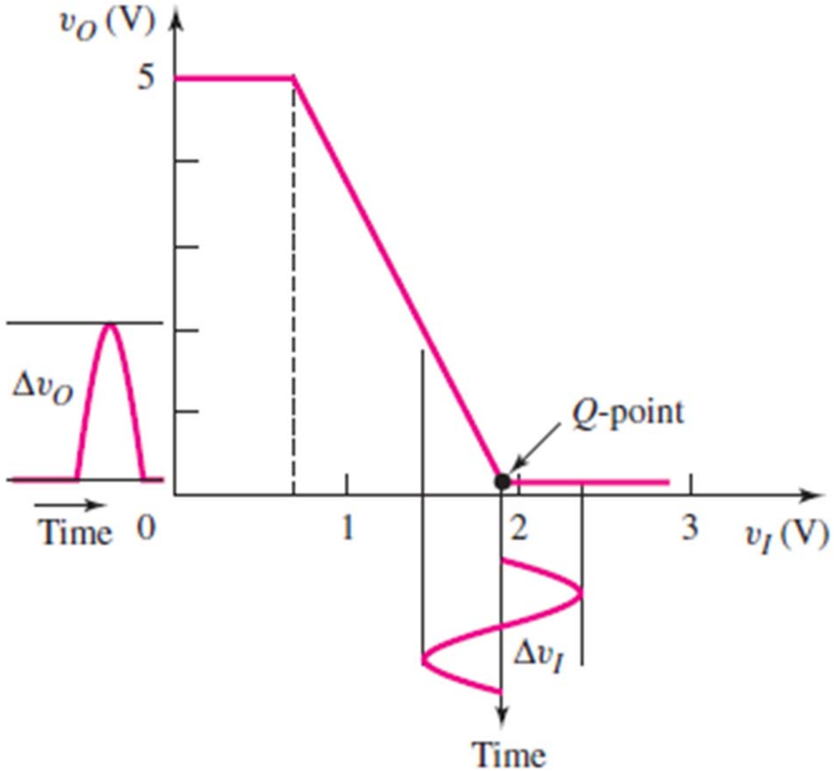


$$v_O = V^+ - I_C R_C = V^+ - \frac{\beta(V_{BB} + \Delta v_I - 0.7)}{R_B} R_C$$

$$V_O + \Delta v_O = V^+ - \frac{\beta(V_{BB} - 0.7)}{R_B} R_C - \frac{\beta \Delta v_I}{R_B} R_C$$

Therefore, the bipolar inverter circuit with proper biasing can be used to amplify a time-varying signal.

Improper DC biasing:



There are many schemes for properly biasing the transistor for analog or amplifier applications