CVC Open Core Arguments and Simulation Results

Below are CVC simulation times for various Verilog designs from the open cores project that you can run with OSS CVC. If you suspect that some change in your OSS CVC binary has caused loss of speed, you can compare your simulation times to these times that were run on an Intel i5 2500k 3.3 Ghz processor.

To run the benchmarks, cd into the selected benchmark directory then run "cvc64 [maybe some options] -f run.flist". If you run cvc instead of cvc64, your memory use will be smaller and for older X86 processors cvc is faster than cvc64. Use the +verbose option to see simulation times, sizes and other design statistics.

Designs are from www.opencores.com with minor modifications so that they are easy to run out of the box.

Designs and Simulation Times

DESIGN NAME	CVC OPTIONS	TIME (seconds)
usb1.1	-O	2.5
m68k (Verilator benchmark)	-O +nbaopt	10.3
ata	-O	17.8
ac97	-O +nbaopt +2state	39.2
can	-O	5.5
sha1	-O +2state	0.9
ethernet	-O	113.7
generic_fifos	-O +nbaopt	100.4
wb_dma	-O +nbaopt +2state	788.3

For example to run the usb11 open core design with CVC:

```
%cd usb11
%cvc64 +verbose -f run.flist
%cvcsim
```

All example design source directories have a 'run.flist' standard Verilog -f option argument that contains the list of files needed to run the simulation. A 'cvc.log' file is also present in the top level of the directory. It contains expected simulation results and times.

You can see OSS CVC's performance compared to other simulators on one design by visiting Verilator benchmarks page.