%A	counter	Ready Q	main	state	comment	T1	state	comment
	0	T1					Ready	
0	0	T1	A1	Run	LD		Ready	
	0				interrupt			
0	0	main		Ready		B1	Run	LD
1	0	main		Ready		B2	Run	ADD
1	1	main		Ready		B3	Run	ST
1	1	main		Ready		B1	Run	LD
2	1	main		Ready		B2	Run	ADD
2	2	main		Ready		B3	Run	ST
2	2	main		Ready		B1	Run	LD
3	2	main		Ready		B2	Run	ADD
0					interrupt			
2	3	T1	A2	Run	ADD		Ready	
2	2	T1	A3	Run	ST		Ready	
2	2	T1	A1	Run	LD		Ready	
4	2	T1	A2	Run	ADD		Ready	
4	4	T1	A3	Run	ST		Ready	
4	4	T1	A1	Run	LD		Ready	
6	4	T1	A2	Run	ADD		Ready	
6	6	T1	A3	Run	ST		Ready	
6	6	T1	A1	Run	LD		Ready	
8	6	T1	A2	Run	ADD		Ready	
8	8	T1	A3	Run	ST		Ready	
3	2				interrupt			
3	3	main		Ready		B3	Run	ST
3	3	main		Ready		B1	Run	LD
4	3	main		Ready		B2	Run	ADD

4	4	main		Ready		B3	Run	ST