%A         counter         Ready Q         main         state         comment         T1         state         comment           0         T1         A1         Run         LD         Ready         —           0         0         T1         A1         Run         LD         Ready         —           0         0         main         Ready         —         B1         Run         LD           1         0         main         Ready         —         B2         Run         ADD           1         1         main         Ready         —         B3         Run         ST           1         1         main         Ready         —         B3         Run         ADD           2         1         main         Ready         —         B2         Run         ADD           2         1         main         Ready         —         B3         Run         ST           2         2         main         Ready         —         B1         Run         ADD           3         2         main         Ready         —         B2         Run         ADD		T	T	Γ	T	T	Γ	1	T
0         0         T1         A1         Run         LD         Ready           0         0         main         Ready         B1         Run         LD           1         0         main         Ready         B2         Run         ADD           1         1         main         Ready         B3         Run         ST           1         1         main         Ready         B1         Run         LD           2         1         main         Ready         B2         Run         ADD           2         2         main         Ready         B3         Run         ST           2         2         main         Ready         B1         Run         ADD           3         2         main         Ready         B2         Run         ADD           4         2         main         Ready         B2         Run         ADD           4         2         main         Ready         Ready         Ready         Ready           2         3         T1         A2         Run         ADD         Ready           2         2         T1 <td< th=""><th>%<b>A</b></th><th>counter</th><th>Ready Q</th><th>main</th><th>state</th><th>comment</th><th>T1</th><th>state</th><th>comment</th></td<>	% <b>A</b>	counter	Ready Q	main	state	comment	T1	state	comment
0         main         Ready         B1         Run         LD           1         0         main         Ready         B2         Run         ADD           1         1         main         Ready         B3         Run         ST           1         1         main         Ready         B1         Run         LD           2         1         main         Ready         B2         Run         ADD           2         2         main         Ready         B3         Run         ST           2         2         main         Ready         B3         Run         ADD           3         2         main         Ready         B1         Run         LD           3         2         main         Ready         B2         Run         ADD           0         1         1         A2         Run         ADD         Ready		0	T1					Ready	
0         0         main         Ready         B1         Run         LD           1         0         main         Ready         B2         Run         ADD           1         1         main         Ready         B3         Run         ST           1         1         main         Ready         B2         Run         ADD           2         1         main         Ready         B3         Run         ST           2         2         main         Ready         B1         Run         ADD           3         2         main         Ready         B2         Run         ADD           3         2         main         Ready         B2         Run         ADD           4         2         main         Ready         B2         Run         ADD           4         2         main         Ready         Ready         Ready         Ready           5         2         main         Ready         Ready         Ready         Ready           2         3         71         A2         Run         ADD         Ready           4         2         71	0	0	T1	A1	Run	LD		Ready	
1         0         main         Ready         B2         Run         ADD           1         1         main         Ready         B3         Run         ST           1         1         main         Ready         B1         Run         ADD           2         1         main         Ready         B3         Run         ST           2         2         main         Ready         B3         Run         ST           2         2         main         Ready         B2         Run         ADD           3         2         main         Ready         B2         Run         ADD           4         2         main         Ready         B2         Run         ADD           4         2         main         Ready         B2         Run         ADD           4         2         main         Ready         Ready         Ready         Ready           2         3         71         A2         Run         ADD         Ready         Ready           2         71         A3         Run         ST         Ready         Ready           4         4		0				interrupt			
1         1         main         Ready         B3         Run         ST           1         1         main         Ready         B1         Run         LD           2         1         main         Ready         B2         Run         ADD           2         2         main         Ready         B1         Run         LD           3         2         main         Ready         B2         Run         ADD           0         Interrupt         B2         Run         ADD           1         A2         Run         ADD         Ready           2         3         T1         A2         Run         ADD         Ready           2         3         T1         A2         Run         ADD         Ready           2         2         T1         A3         Run         ST         Ready           4         2         T1         A2         Run         ADD         Ready           4         4         T1         A3         Run         ST         Ready           4         4         T1         A2         Run         ADD         Ready <tr< th=""><th>0</th><th>0</th><th>main</th><th></th><th>Ready</th><th></th><th>В1</th><th>Run</th><th>LD</th></tr<>	0	0	main		Ready		В1	Run	LD
1         1         main         Ready         B1         Run         LD           2         1         main         Ready         B2         Run         ADD           2         2         main         Ready         B3         Run         ST           2         2         main         Ready         B1         Run         LD           3         2         main         Ready         B2         Run         ADD           0	1	0	main		Ready		В2	Run	ADD
2       1       main       Ready       B2       Run       ADD         2       2       main       Ready       B3       Run       ST         2       2       main       Ready       B1       Run       LD         3       2       main       Ready       B2       Run       ADD         0       Interrupt       Interrupt	1	1	main		Ready		В3	Run	ST
2         2         main         Ready         B3         Run         ST           2         2         main         Ready         B1         Run         LD           3         2         main         Ready         B2         Run         ADD           0         Interrupt         2         Run         ADD         Ready           2         3         T1         A2         Run         ADD         Ready           2         2         T1         A3         Run         ST         Ready           4         2         T1         A2         Run         ADD         Ready           4         4         T1         A3         Run         ST         Ready           4         4         T1         A1         Run         LD         Ready           6         4         T1         A2         Run         ADD         Ready           6         6         T1         A3         Run         ST         Ready           8         6         T1         A2         Run         ADD         Ready           8         6         T1         A3         Ru	1	1	main		Ready		В1	Run	LD
2       2       main       Ready       B1       Run       LD         3       2       main       Ready       B2       Run       ADD         0       Interrupt	2	1	main		Ready		B2	Run	ADD
3       2       main       Ready       B2       Run       ADD         0       Interrupt       Interrupt         2       3       T1       A2       Run       ADD       Ready         2       2       T1       A3       Run       ST       Ready         4       2       T1       A2       Run       ADD       Ready         4       4       T1       A3       Run       ST       Ready         4       4       T1       A2       Run       ADD       Ready         6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         8       8       T1       A3       Run       ST       Ready         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD </th <th>2</th> <th>2</th> <th>main</th> <th></th> <th>Ready</th> <th></th> <th>В3</th> <th>Run</th> <th>ST</th>	2	2	main		Ready		В3	Run	ST
0         interrupt           2         3         T1         A2         Run         ADD         Ready           2         2         T1         A3         Run         ST         Ready           2         2         T1         A1         Run         LD         Ready           4         2         T1         A2         Run         ADD         Ready           4         4         T1         A3         Run         ST         Ready           6         4         T1         A2         Run         ADD         Ready           6         6         T1         A3         Run         ST         Ready           6         6         T1         A1         Run         LD         Ready           8         6         T1         A2         Run         ADD         Ready           8         8         T1         A3         Run         ST         Ready           3         2         interrupt         B3         Run         ST           3         3         main         Ready         B1         Run         LD	2	2	main		Ready		B1	Run	LD
2         3         T1         A2         Run         ADD         Ready           2         2         T1         A3         Run         ST         Ready           2         2         T1         A1         Run         LD         Ready           4         2         T1         A2         Run         ADD         Ready           4         4         T1         A1         Run         LD         Ready           6         4         T1         A2         Run         ADD         Ready           6         6         T1         A3         Run         ST         Ready           6         6         T1         A1         Run         LD         Ready           8         6         T1         A2         Run         ADD         Ready           8         8         T1         A3         Run         ST         Ready           8         8         T1         A3         Run         ST         Ready           3         2         interrupt         Interrupt         B3         Run         ST           3         3         main         Ready	3	2	main		Ready		B2	Run	ADD
2         2         T1         A3         Run         ST         Ready           2         2         T1         A1         Run         LD         Ready           4         2         T1         A2         Run         ADD         Ready           4         4         T1         A3         Run         ST         Ready           6         4         T1         A2         Run         ADD         Ready           6         6         T1         A3         Run         ST         Ready           8         6         T1         A2         Run         ADD         Ready           8         8         T1         A3         Run         ST         Ready           8         8         T1         A3         Run         ST         Ready           3         2         interrupt         Interrupt         B3         Run         ST           3         3         main         Ready         B1         Run         LD	0					interrupt			
2       2       T1       A1       Run       LD       Ready         4       2       T1       A2       Run       ADD       Ready         4       4       T1       A3       Run       ST       Ready         6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         6       6       T1       A1       Run       LD       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	2	3	T1	A2	Run	ADD		Ready	
4       2       T1       A2       Run       ADD       Ready         4       4       T1       A3       Run       ST       Ready         4       4       T1       A1       Run       LD       Ready         6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	2	2	T1	А3	Run	ST		Ready	
4       4       T1       A3       Run       ST       Ready         4       4       T1       A1       Run       LD       Ready         6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         6       6       T1       A1       Run       LD       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	2	2	T1	A1	Run	LD		Ready	
4       4       T1       A1       Run       LD       Ready         6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         6       6       T1       A1       Run       LD       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	4	2	T1	A2	Run	ADD		Ready	
6       4       T1       A2       Run       ADD       Ready         6       6       T1       A3       Run       ST       Ready         6       6       T1       A1       Run       LD       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	4	4	T1	А3	Run	ST		Ready	
6         6         T1         A3         Run         ST         Ready           6         6         T1         A1         Run         LD         Ready           8         6         T1         A2         Run         ADD         Ready           8         8         T1         A3         Run         ST         Ready           3         2         interrupt         Interrupt         B3         Run         ST           3         3         main         Ready         B1         Run         LD	4	4	T1	A1	Run	LD		Ready	
6       6       T1       A1       Run       LD       Ready         8       6       T1       A2       Run       ADD       Ready         8       8       T1       A3       Run       ST       Ready         3       2       interrupt         3       3       main       Ready       B3       Run       ST         3       3       main       Ready       B1       Run       LD	6	4	T1	A2	Run	ADD		Ready	
8         6         T1         A2         Run         ADD         Ready           8         8         T1         A3         Run         ST         Ready           3         2         interrupt         Interrupt         ST           3         3         main         Ready         B3         Run         ST           3         3         main         Ready         B1         Run         LD	6	6	T1	А3	Run	ST		Ready	
8         8         T1         A3         Run         ST         Ready           3         2         interrupt         Interrupt         B3         Run         ST           3         3         main         Ready         B1         Run         LD	6	6	T1	A1	Run	LD		Ready	
3 2 interrupt  3 3 main Ready B3 Run ST  3 3 main Ready B1 Run LD	8	6	T1	A2	Run	ADD		Ready	
3 3 main Ready B3 Run ST  3 3 main Ready B1 Run LD	8	8	T1	А3	Run	ST		Ready	
3 3 main Ready B1 Run LD	3	2				interrupt			
	3	3	main		Ready		В3	Run	ST
4 3 main Ready B2 Run ADD	3	3	main		Ready		B1	Run	LD
	4	3	main		Ready		B2	Run	ADD

4 4 main Ready B3 Run ST