6-bit Fully Differential Current Steering DAC

MIXED SIGNAL DESIGN(EC441) TERM PROJECT REPORT

Submitted in partial fulfilment of the requirements for the degree of

BACHELOR OF TECHNOLOGY IN ELECTRONICS AND COMMUNICATION ENGINEERING

by

Keerthi Bhushan M(211EC226)
Sanganabasu M Herur(211EC245)

Department of ELECTRONICS AND COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA (NITK)
SURATHKAL, MANGALORE - 575 025

ABSTRACT

This project involves the design and analysis of a 6-bit fully differential current steering Digital-to-Analog Converter (DAC) tailored to meet specific performance criteria. The DAC was designed for a 180 nm process with a 1.8 V analog supply and a full-scale output voltage of 1.6 V (peak-to-peak). The design process was divided into two main stages. In the first stage, the DAC was implemented using ideal current sources, and its output transfer characteristics were evaluated.

In the second stage, a practical implementation was achieved using PMOS current sources and a row-column decoder (2:3-to-8 priority decoder) to control the DAC's output based on digital input. The design utilized current mirroring with MOSFETs to generate the required analog output. The transfer characteristics were plotted, and Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were calculated using a Python script developed for this purpose. Furthermore, the effects of random mismatches in the width of unit transistors, with deviations of 0.1% and 1%, were analysed to evaluate the impact on INL and DNL. Simulations were performed using LTspice, and the results demonstrated compliance with the design specifications, providing insights into the trade-offs and limitations of the DAC architecture.

INTRODUCTION

Digital-to-Analog Converters (DACs) play a critical role in modern electronic systems, facilitating the interface between digital processors and analog signal domains. Among various DAC architectures, the current steering DAC is widely employed due to its high-speed operation and ability to deliver precise output with minimal power consumption. This project focuses on designing a 6-bit fully differential current steering DAC to meet stringent performance specifications, including high linearity, low power consumption, and robust operation under process variations.

The design process is divided into two stages. The first stage involves implementing the DAC using ideal current sources to evaluate its theoretical performance. The second stage transitions to a practical implementation using PMOS current sources, current mirroring techniques, and a row-column decoding mechanism for digital-to-analog conversion. A 2:3-to-8 priority decoder controls the row-column switching logic, determining the analog output corresponding to the digital input.

To evaluate the DAC's performance, metrics such as Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were calculated. Simulations were conducted using LTspice, while Python scripting was utilized for INL and DNL computation. Additionally, the impact of random mismatches in the dimensions of unit transistors on DAC performance was analysed, providing insights into design robustness.

This report outlines the methodology, simulation results, and conclusions drawn from the design process, highlighting the challenges and trade-offs encountered in the realization of a high-performance DAC.

PROBLEM STATEMENT

Design a 6-bit fully differential current steering DAC for the following specifications.

Process: 180 nm

Analog supply: 1.8 V

Full scale voltage (pk-to-pk): 1.6 V

Analog input range: 0 - 1.6 V

INL (MAX): 0.5 LSB DNL (MAX) : 0.5 LSB

Maximum static power drawn from the supply < 1 mW

Step-1: Design the DAC using ideal current sources. Plot the transfer characteristic.

Step-2: (a) Design the DAC using PMOS current sources along with the row-column decoder. Plot - transfer characteristics, INL and DNL

(b) In the circuit designed above, introduce random mismatch in the width of the unit transistors of the current source such that the max deviation is 0.1%. Plot the transfer characteristic, INL and DNL.

(c) Repeat (b) for maximum deviation of 1%

IMPLEMENTATION AND METHDOLOGY

The design and analysis of the 6-bit fully differential current steering DAC were carried out in two stages:

Step 1: Ideal Current Sources Implementation

The DAC was initially designed using ideal current sources to verify the concept and establish a baseline performance. A row-column decoder, specifically a 2:3-to-8 priority decoder, was employed to control the switching of rows and columns, which determines the analog output corresponding to a given digital input. This setup was simulated in the LTspice environment to plot the output transfer characteristics. The output waveform confirmed the linearity and accuracy of the DAC design at this idealized stage.

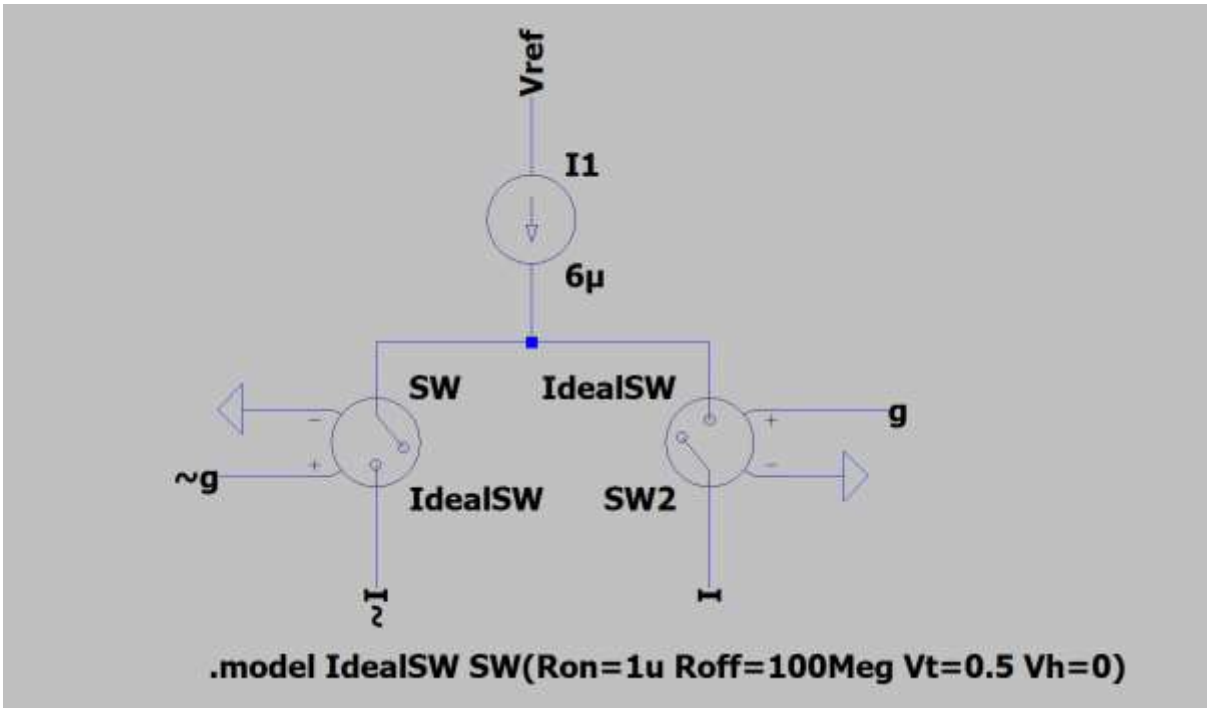


Figure 1: Ideal Current Source

Step 2: PMOS Current Sources Implementation

In the second stage, the DAC was practically implemented using PMOS current sources. The current sources were designed using current mirror circuits to ensure consistency in output current across all bits. The row-column decoder logic remained unchanged from the previous stage, allowing seamless transition to a more practical design.

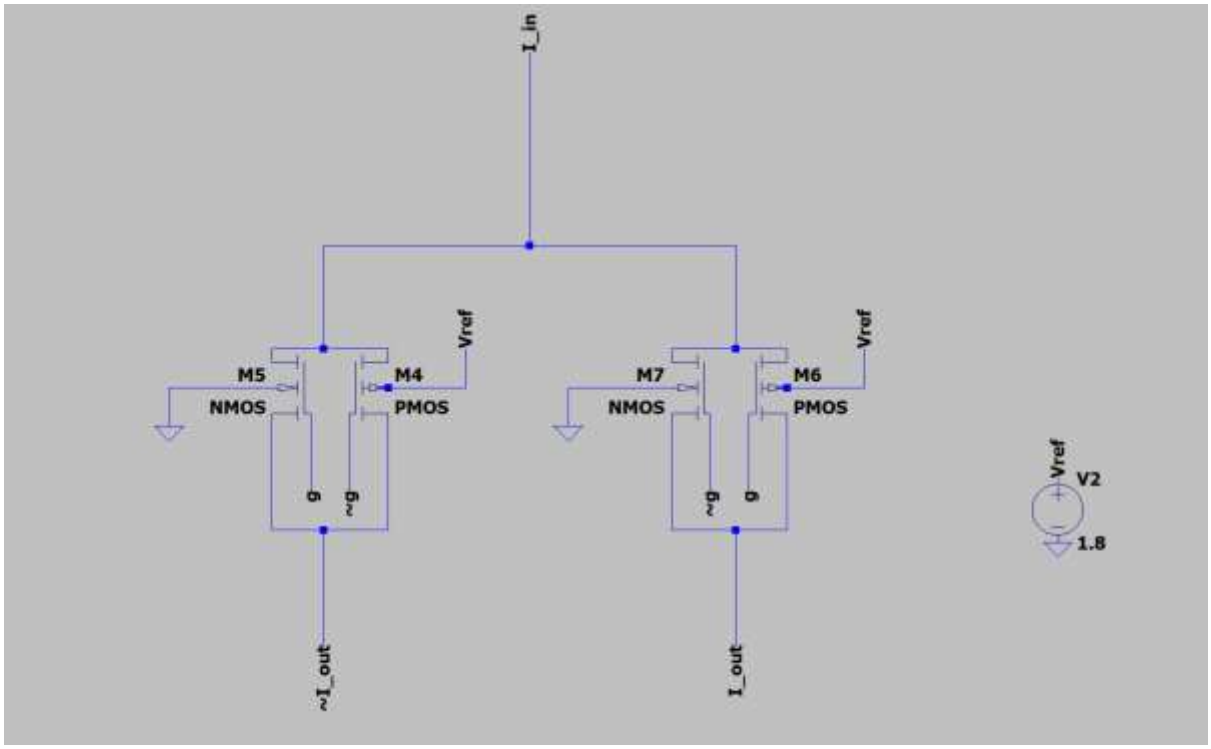


Figure 2: Non-Ideal Current Source

Step 3: Row-Column Decoder Implementation

The row-column decoder for the 6-bit fully differential current steering DAC is implemented using two 3:8 priority decoders. In this configuration, one decoder is designated to control the rows, while the other controls the columns. The inputs to the decoders are the most significant bit (MSB) and the least significant bit (LSB) of the 6-bit digital input signal. The MSB is fed into the row decoder, which selects one of the eight rows based on the value of the MSB, and similarly, the LSB is fed into the column decoder, which selects one of the eight columns. Each output of the decoders is connected to a corresponding current source, with the row and column outputs determining which current source is activated to produce the appropriate analog output voltage.

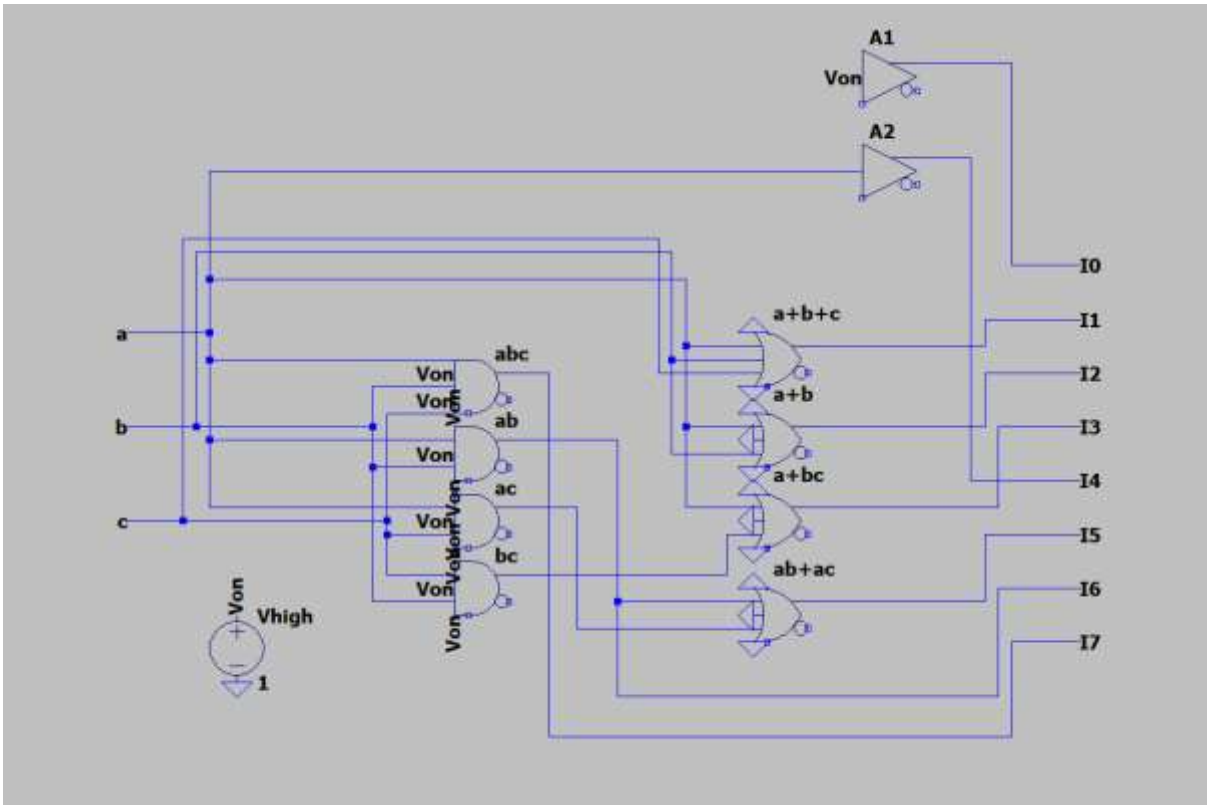


Figure 3: Row-Column Decoder

Step 4: Logic for realization of Unit Cell

The logic for the realization of the unit cell in the 6-bit fully differential current steering DAC is based on the interaction between the row and column values. Let the row value be denoted as i and the column value as j. To select the appropriate current source, we perform an OR operation between i+1 and j. The output of this OR gate is then passed to an AND gate along with the row input i. The output of this AND gate determines the selection of the current source. The output from the cell select subblock consists of two signals: bit b and its complement b bar. These signals are then fed as inputs to the differential current source block, enabling it to steer the current based on the decoded row and column values. This logic ensures that the correct current source is activated for each combination of the digital input bits, facilitating precise control of the DAC's analog output.

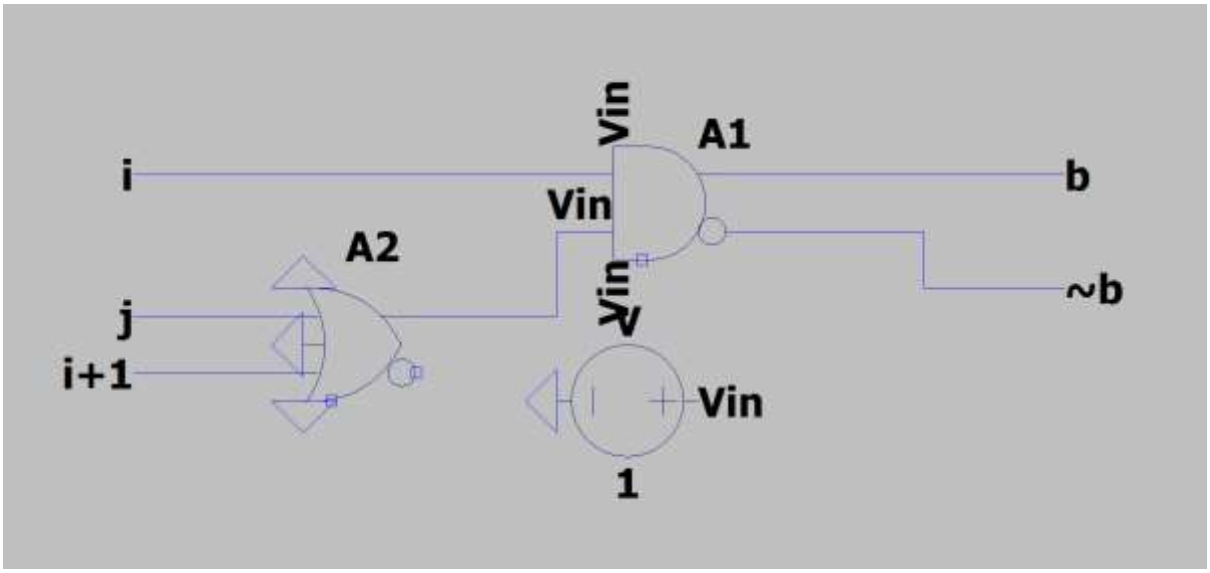


Figure 4: Logic for Realisation of Unit Cell

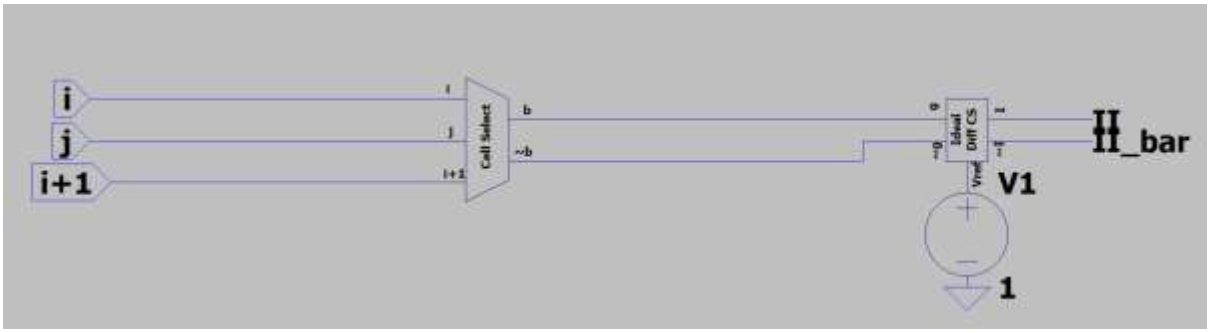


Figure 5: Combination of Cell Select and Differential Current Source block

Step 5: Block diagram of Final DAC Implementation

The final implementation of the 6-bit fully differential current steering DAC integrates the row-column decoder along with ideal or non-ideal differential current source blocks at each matrix cell. The row-column decoder, as described earlier, controls the selection of rows and columns based on the MSB and LSB of the digital input. For each combination of row and column, an ideal or non-ideal differential current source block is inserted at the corresponding matrix cell. The differential current source is responsible for generating the appropriate current based on the selected digital input value. In the non-ideal case, variations in the current source performance, such as mismatch in transistor widths, are considered to assess the impact on the DAC's linearity. The total output current is measured differentially by using two load resistances connected across the differential output. This differential measurement ensures that the DAC produces the correct analog output voltage corresponding to the input digital code, allowing for accurate voltage conversion. The overall design ensures that the DAC meets the required specifications for linearity, power consumption, and output range, while also providing the necessary flexibility to account for non-ideal effects in the current source performance.

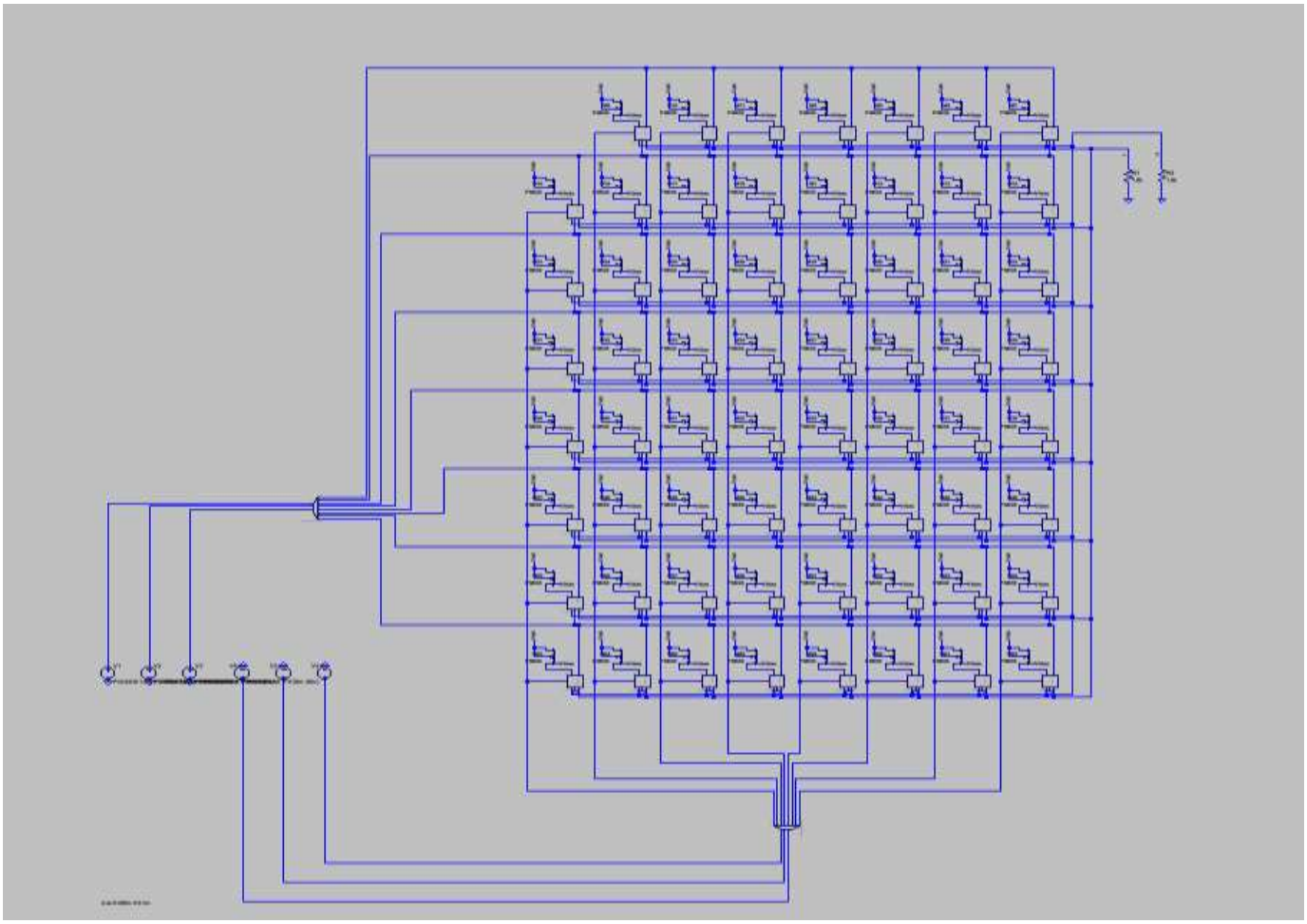


Figure 4: Final DAC implementation

Sub-steps:

1. **Transfer Characteristics**
   The DAC's output transfer characteristics were simulated, and the voltage levels were extracted from the LTspice output. These characteristics were then analyzed to ensure compliance with the expected design specifications.

2. **INL and DNL Calculation**
   To evaluate the DAC's linearity, the Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) were calculated. A Python script was developed for this purpose, which processed the voltage data from the output waveform. The results confirmed that the INL and DNL were within the specified limits of 0.5 LSB.

3. **Mismatch Analysis**
   To assess the impact of process variations, random mismatches were introduced in the width of the unit transistors of the PMOS current sources:

   - **0.1% Deviation**: The design was simulated with a maximum deviation of 0.1% in transistor widths. The transfer characteristics, INL, and DNL were plotted and analyzed.
   - **1% Deviation**: The simulation was repeated with a maximum deviation of 1% in transistor widths. The plots revealed the effects of increased mismatch on linearity and overall performance.

Simulation Tools

The design and simulations were carried out using the LTspice simulator for circuit modeling and waveform analysis. Python was used to automate the calculation of INL and DNL values, ensuring precision and efficiency in the analysis.

SIMULATION RESULTS

1. Transfer Characteristics plot:

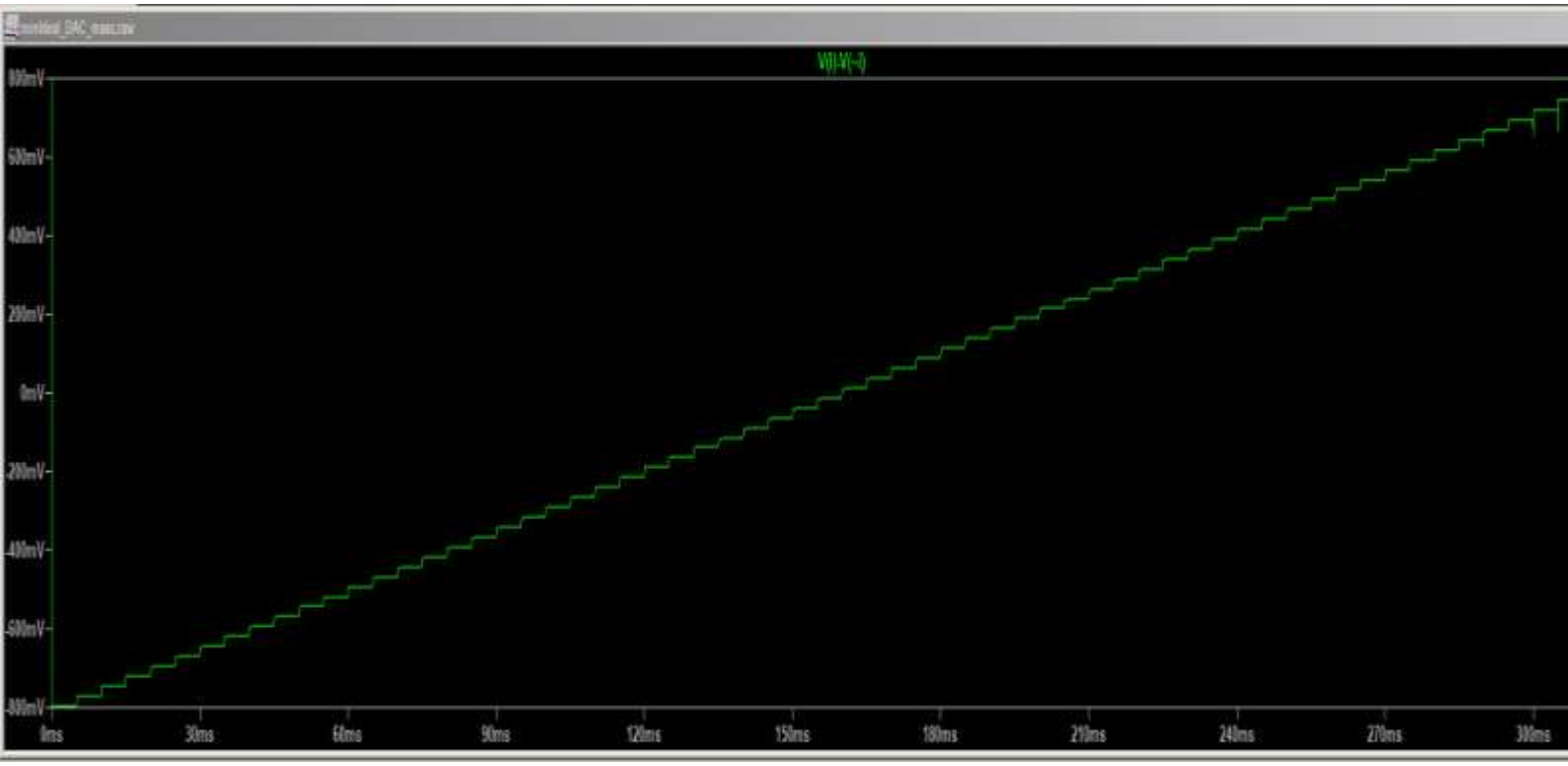
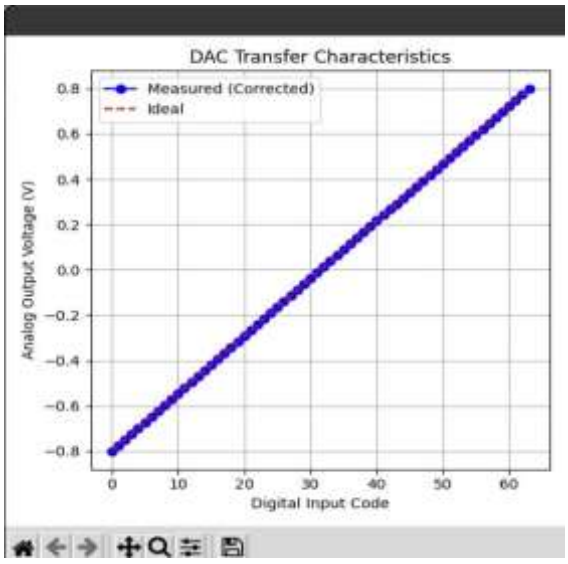
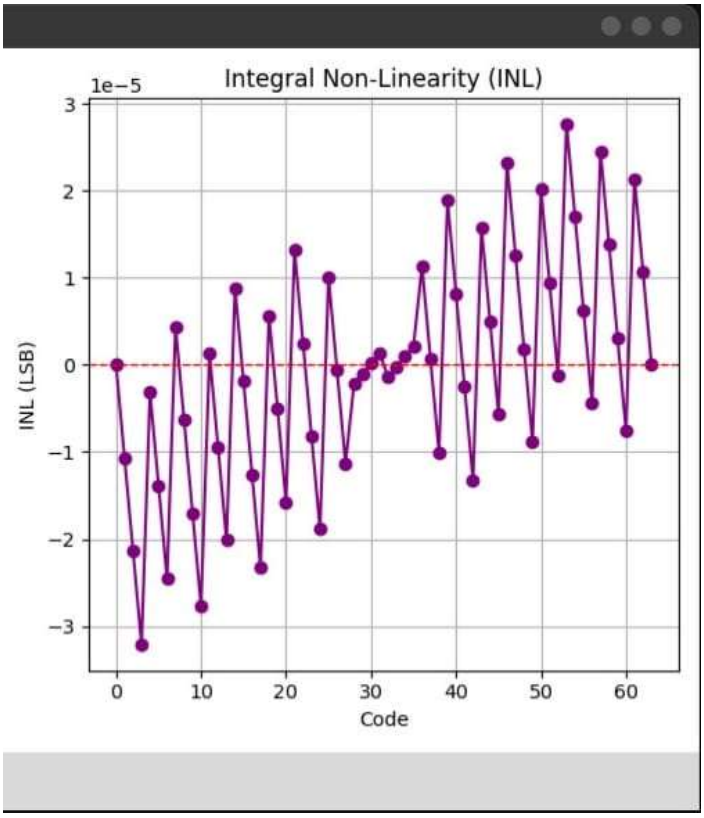
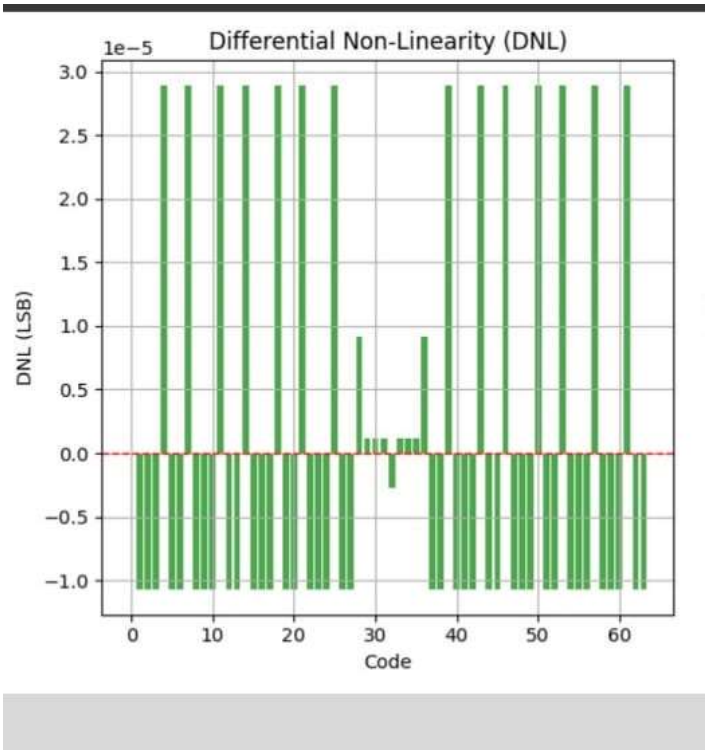


Figure 5: Transfer Characteristics plot



2. INL and DNL plot:





CONCLUSION

The design and analysis of a 6-bit fully differential current steering DAC were successfully completed, meeting the specified performance criteria. The project began with an idealized implementation using ideal current sources, providing a foundational understanding of the DAC's behaviour and establishing a baseline for its transfer characteristics.

Transitioning to a practical design, PMOS current sources were employed in conjunction with a row-column decoder to generate the required analog output. Simulations confirmed that the DAC adhered to the specified limits for Integral Non-Linearity (INL) and Differential Non-Linearity (DNL), ensuring the desired accuracy and linearity. A Python script was developed to automate the computation of INL and DNL, improving the efficiency and accuracy of the analysis.

To evaluate robustness under process variations, random mismatches in the width of unit transistors were introduced with deviations of 0.1% and 1%. These analyses demonstrated the impact of mismatches on DAC performance, emphasizing the importance of precision in current source design to maintain linearity and reduce non-idealities.

Overall, the project achieved its objectives, providing valuable insights into the design challenges and trade-offs in current steering DAC architectures. The systematic approach adopted in this project highlights the significance of simulation tools and analytical methods in ensuring compliance with stringent design specifications.