# TRIBHUVAN UNIVERSITY

## INSTITUTE OF ENGINEERING

## CENTRAL CAMPUS PULCHOWK

## DEPARTMENT OF ELECTRICAL ENGINEERING

**LALITPUR, NEPAL**

A

FINAL YEAR PROJECT REPORT

ON

# "DESIGN AND FABRICATION OF SHUNT ACTIVE POWER FILTER USING DIGITAL NOTCH FILTER"

(In partial fulfillment of B.E. in Electrical Engineering)

**EE755**


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November 2014

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This undersigned certify that they have read, and recommended to the Institute of Engineering a final year project work entitled **"DESIGN AND FABRICATION OF SHUNT ACTIVE POWER FILTER USING DIGITAL NOTCH FILTER**" submitted by **Rupak Mahat, Saroj Prasad Khanal, Saroj Twanabasu** and **Sulav Adhikari** in partial fulfilment of the requirements for the Bachelor's degree in Electrical Engineering.

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# COPYRIGHT

# ACKNOWLEDGEMENT

At first, our humble gratitude goes to our project supervisors **Assoc. Prof. Dr. Netra Prasad Gyawali** and **Er. Hari Prasad Rimal** for guiding us throughout this project. Their valuable advice, suggestions, instructive guidance and cooperative supervision has been one of the motivating factors for the successful completion of the project with ease.

We would like to express our honor to the Department of Electrical Engineering for providing us the opportunity to do a final year project on the topic of interest.

We would also like to thank **Assoc. Prof. Dr. Nava Raj Karki,** Head of Department, for his support with provision of the lab facilities and other electrical equipment required for the project. We would also like to thank our respected **Prof. Dr. Indraman Tamrakar** for initiative guidance of the project.

At last, we'd like to thank to all our teachers, colleagues and seniors especially to **Mr. Rojan Bhattrai**, for their support throughout the project.

# ABSTRACT

This project report presents a single phase shunt active power filter (APF) which automatically adapts to changes in the network and load fluctuations in electrical systems to mitigate power quality problems by the use of digital notch filter control strategy. The power stage of the APF is based on an inverter, with battery in dc side, and a filter inductor in the ac side. It can be used for the compensation of harmonic components of current drawn by the non-linear load. Shunt active power filter operates as a current source injecting the current harmonics drawn by the load and letting the source to supply only the fundamental component.

In this project, we have used RL circuit with 6H inductance in series with 30 ohm resistance connected across a rectifier for the purpose of non-linear load and is powered by 7V ac through autotransformer from grid. Likewise, we have modelled analog notch filter into digital form and designed a digital notch filter using a microcontroller and finally required current is injected by inverter with supply of 12V dc to the grid through an interfacing transformer with 75mH inductance and 3.8 ohm.

First of all we have modelled the overall system in the MATLAB Simulink. And then for the hardware fabrication we first designed the overall circuit in the Proteus. And finally we fabricated the system in the PCB.

In MATLAB simulation, we found that the THD of the system is improved from 34.63% to 5.07% after the use of the system. Also after the fabrication of the hardware of the system, the THD improved from 45% to 10% in hardware implementation.

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# LIST OF ACRONYMS

| | |
|---|---|
| AC | Alternating Current |
| APF | Active Power Filter |
| BJT | Bipolar Junction Transistor |
| CRO | Cathode Ray Oscilloscope |
| CT | Current Transformer |
| DC | Direct Current |
| DSP | Digital Signal Processor |
| GND | Ground |
| Hz | Hertz |
| I/O | Input/output |
| IC | Integrated Circuit |
| IGBT | Insulated-Gate Bipolar Transistor |
| KVL | Kirchhoff's Voltage Law |
| mA | milliAmpere |
| mH | milliHenry |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect Transistor |
| Op-Amp | Operational Amplifier |
| PCB | Printed Circuit Board |
| Q-factor | Quality Factor |
| RL | Resistive-Inductive |

| | |
|---|---|
| μF | Micro Farad |
| V | Volt |

# 1. INTRODUCTION

## 1.1. Background

The growing number of power electronics-based (non-linear) loads have produced deterioration in the power quality by introduction of harmonics in the network voltages. At the same time, many equipment are quite sensitive to the deviations from the ideal sinusoidal line voltage when exposed to such disturbances.

The presence of harmonics in the power lines results in greater power losses in distribution, interference problems in communication systems and, sometimes, in operation failures of electronic equipment, which are more sensitive since they include microelectronic control systems, which work with very low energy levels. Because of these problems, the issue of the power quality delivered to the end consumers is of great concern.

Harmonic distortion has traditionally been dealt with the use of passive LC filters. However, the application of passive filters for harmonic reduction may result in parallel resonances with the network impedance, over compensation of reactive power at fundamental frequency, and poor flexibility for dynamic compensation of different frequency harmonic components.

The increased severity of power quality in power networks has attracted the attention of power engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipment, generally known as active filters, are also called active power line conditioners, and are able to compensate current and voltage harmonics, reactive power, regulate terminal voltage, suppress flicker, and to improve voltage balance in three-phase systems. The advantage of active filtering is that it automatically adapts to changes in the network and load fluctuations. They can compensate for several harmonic orders, and are not affected by major changes in network characteristics, eliminating the risk of resonance between the filter and network impedance.

Our project finds its application in the various industries, power line conditioner, converter stations, etc. for the purpose of improving power quality, reducing overheating of the transformers and reducing interference with neighboring electronic appliance.

## 1.2. Objective and Scope

The objective of the project is to design and fabricate single phase shunt active power filter using digital notch filter.

To achieve the objective of the project, first of all, simulation model of the proposed system is designed in MATLAB Simulink. After successful simulation, hardware simulation model is developed in PROTEUS using microcontroller programming in Atmel Studio. Subsequently, hardware model is tested in breadboard with suitable components followed by required debugging. And finally PCB of the system is fabricated.

# 2. METHODOLOGY

The whole project work consists of simulation, software and hardware works. First of all we performed literature review of the shunt active power filter and developed our own strategy to meet our project objective. After general planning of strategy, we developed the simulation model of the APF in MATLAB Simulink. And we developed hardware simulation model of the system in PROTEUS along with microcontroller programming in Atmel Studio. Then, after selection of suitable hardware components, we performed testing and debugging of our planned hardware system in breadboard. Finally, with successful working in breadboard, we fabricated PCB.

## 2.1. Proposed System Layout

The shunt active power filter is used for compensation of harmonic components of current drawn by the non-linear load. Shunt active power filter operates as a current source injecting the harmonic components drawn by the load.

In our scheme, as in *Fig.2.1*, the load current $I_L$ is sensed by using Hall Effect current transformer which exactly gives the output voltage as the exact replica of the scaled input current and is then fed to microcontroller unit through Analog to Digital Converter (ADC). Microcontroller is used for the digital implementation of notch filter to obtain total harmonic components which is to be injected to the power circuit through hysteresis band current controlled inverter via suitable interfacing inductor. Since all the harmonics components of the current $I_0$ is supplied by the Shunt APF, the current drawn from the AC source $I_s$ is only fundamental component of that drawn by the load [1].

Here,

$$I_s = I_L - I_0$$

Where $I_S$ = Source current

$I_L$ = Load current

$I_0$ = Injected current by Shunt APF

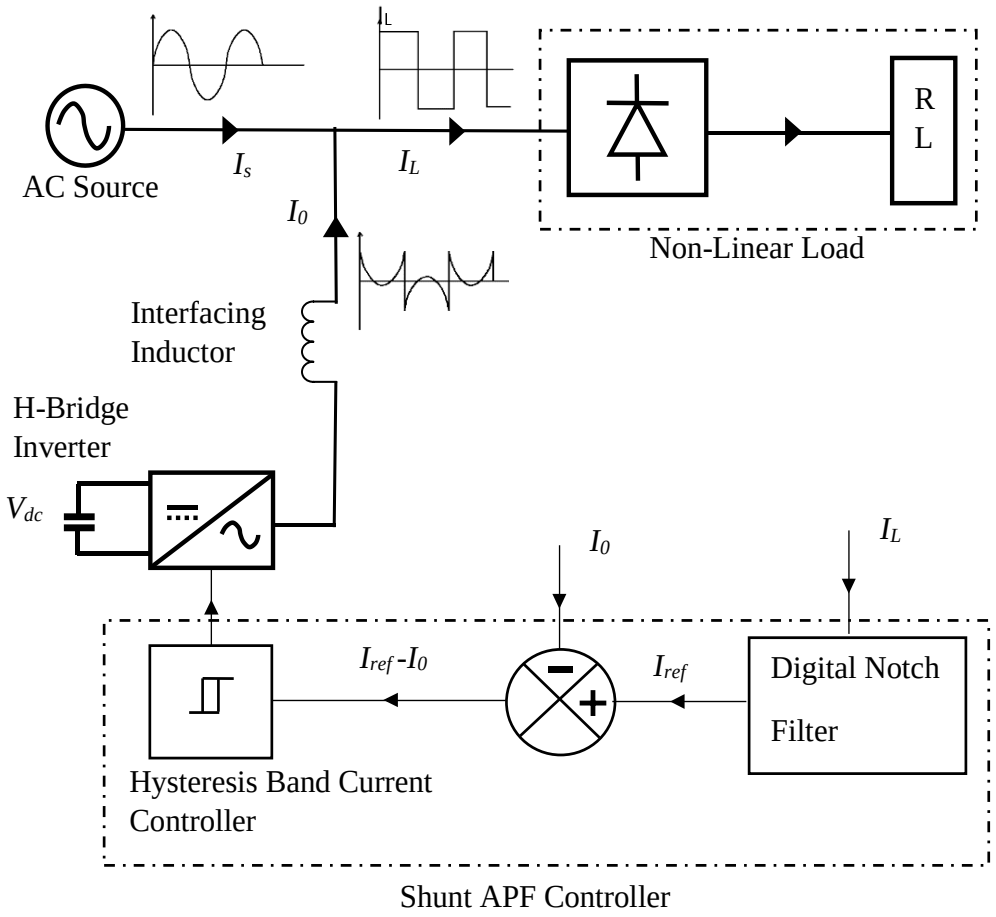



*Fig. 2.1 Overall Implementation of Proposed Scheme*

The theory behind each of the blocks used in the overall system are explained below in detail:

### 2.1.1. Introduction to Loads

There is generally two types of load namely linear loads and non-linear loads. Linear loads draw load current which has waveform exactly similar to that of voltage. So, if the supplied voltage is composed of only fundamental component then the load current drawn will also contain only fundamental component as in the *Fig. 2.2 (b)*. But for the same voltage, non-linear load draws the load current with fundamental component along with harmonics component as in the *Fig. 2.2 (c).* This deviation from a perfect sine wave can be represented by harmonics sinusoidal components having a frequency that is an integral multiple of the fundamental frequency. This is illustrated in the *Fig. 2.2 (a)*. To quantify the distortion, the term total harmonic distortion (THD) is used. The term expresses the distortion as a percentage of the fundamental (pure sine) of voltage and current waveforms.

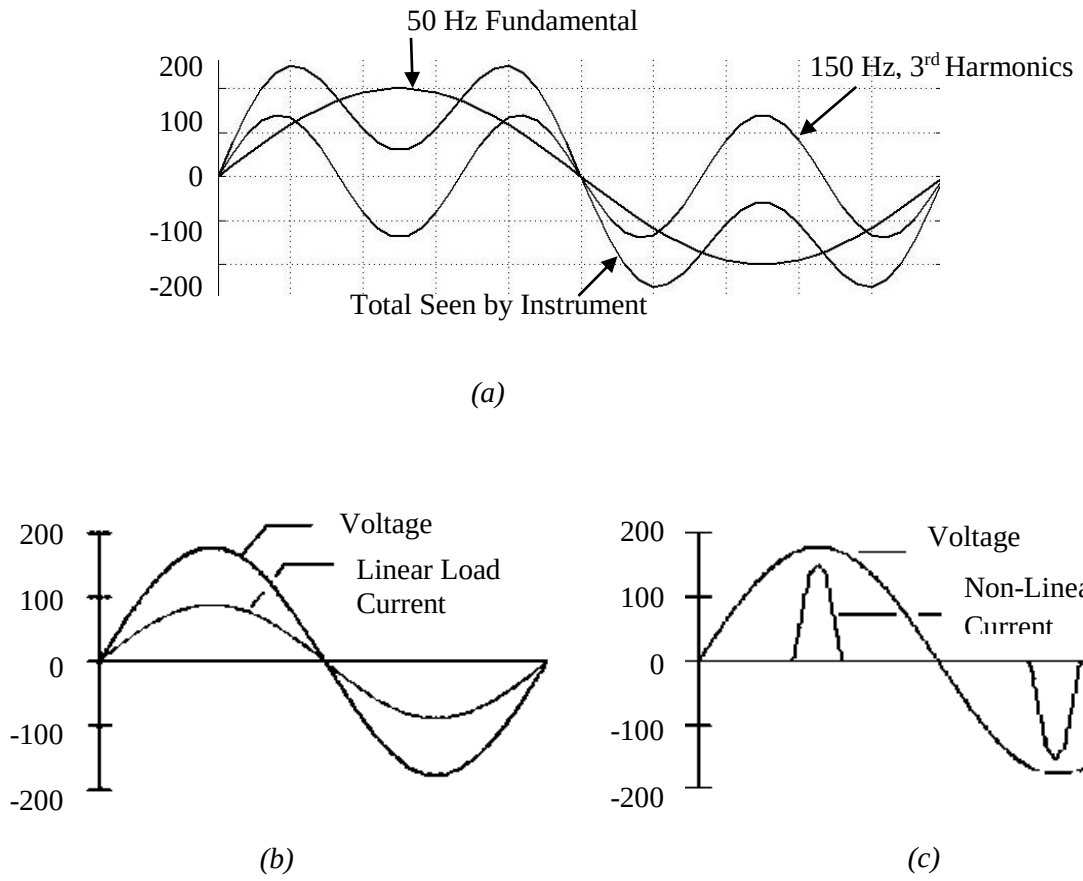



*Fig. 2.2 Characteristics of (a) Harmonic Sine Waves (b) Linear Load (c)Non-linear Load*

### 2.1.2. Digital Notch Filter

In signal processing, signals are often encountered that contain unwanted information, such as random noise or interference, or there is a need to selectively extract a signal of interest merged with several other signals. Filters are used in these situations to separate the signals of interest from others [3].

Filters can be analog or digital. Analog filters use electronic circuits made from components, such as resistors, capacitors, inductors and so forth, to produce the required filtering effect. At all stages, the signal being filtered is an electrical voltage or current, which is the direct analogue of the physical quantity (e.g., a sound or video signal or transducer output) involved. A digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. The processor may be a general purpose computing machine, such as a PIC18 microcontroller, AVR microcontrollers, FPGAs or a specialized Digital Signal Processor (DSP) chip [3].

The approach for the design of the digital notch filter in our project is explained as below:

a. Mathematical Modeling

A band stop filter (or band rejection filter) is a filter that passes most frequencies unaltered but attenuates those in a specific range to a very low level. Notch filter is a band stop filter with a narrow stop band (high Q-factor) [4].

Notch filter can be realized by simple passive components (R, L and C) by the arrangement as shown in the *Fig. 2.3* .In the figure, the parameters L and C are tuned with a cutoff frequency $\omega_c$ so that the path impedance along L-C becomes zero. Thus, the $\omega_c$ frequency components are attenuated highly and all frequency components other than $\omega_c$ are passed unaltered.

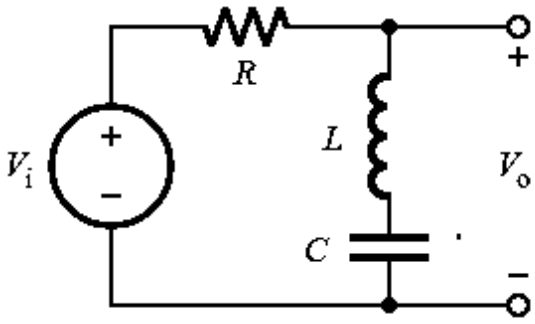



*Fig. 2.3 Realization of Notch Filter using Passive Filter*

Mathematically, $V_0 = 0\ V\ for\ f = 50\ Hz$

$\therefore\ X_L - X_C = 0$

Where, $X_L = \omega L$ And, $Xc = 1/\omega C$ Thus, $\omega = \frac{1}{\sqrt{LC}} = \omega_C$

Using KVL in s-domain,

$$\frac{V_o}{V_i} = \frac{Ls + \frac{1}{Cs}}{R + Ls + \frac{1}{Cs}}$$

$$or, \frac{V_o}{V_i} = \frac{LCs^2 + 1}{LCs^2 + RCs + 1}$$

$$or, \frac{V_0}{V_i} = \frac{s^2 + \frac{1}{LC}}{s^2 + \frac{Rs}{L} + \frac{1}{LC}}$$

$$\therefore\ G(S) = \frac{V_0}{V_i} = \frac{s^2 + \omega_C^2}{s^2 + \beta s + \omega_C^2}$$

Where, $\omega_C$= the cutoff or notch frequency (rad/sec), $\beta$=width of the notch (rad/sec).

For $f_C = 50Hz$, $\omega_C = 2\pi f_c = 2 * 3.14 * 50 = 314\, rad/sec$, the transfer function becomes,

$$G(s) = \frac{s^2 + 314^2}{s^2 + 25s + 314^2}$$

The relation between Q (quality factor) and β (notch width) is obtained as,

$$\frac{\omega_C}{Q} = \beta$$

Here, $\beta = 25$, $\omega_C = 314$

$$\therefore\ Q = 12.56$$

Thus, the Q-factor of the implemented notch filter is 12.56.

The bode plot consisting of magnitude and phase the obtained transfer function is shown in the *Fig. 2.4.* The magnitude plot shows that the only fundamental frequency is highly attenuated by the filter and other pass unaltered. Also in the phase plot shows that the phase of frequencies of our concern are altered.

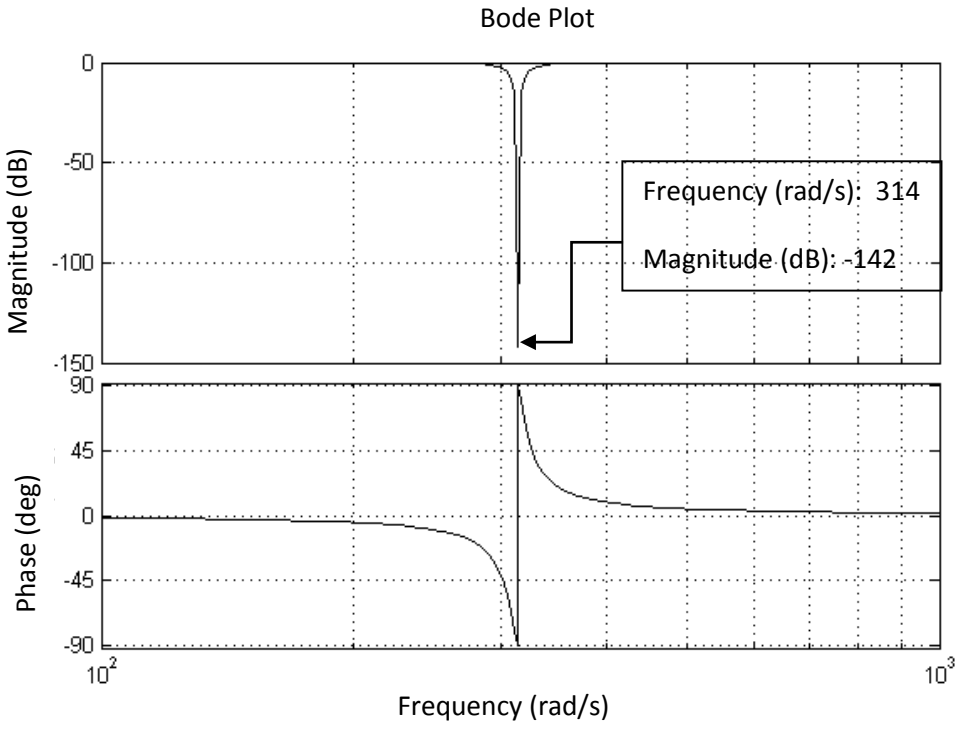



*Fig. 2.4 Bode Plot of G(s) of notch Filter with the cutoff frequency 50Hz*

b. Digital Filter Implementation

Sampling is the process of sensing the analog values at discrete time intervals. Quantization is the process of converting the sensed analog voltage to discrete values. Note that with quantization, the signal values are approximated to a finite set of values. The value obtained after sampling and quantization is referred to as Sample Value. Is it necessary to convert all instantaneous values of an analog signal to numbers? If the answer is yes, this is an impossible task. Fortunately the answer is no, provided the signal satisfies certain conditions. The Nyquist Sampling theorem states this condition.

According to this theorem, if the signal has frequency components only up to a frequency of F Hz, then the signal must be sampled at 2F times/sec or more to prevent loss of signal information. After sampling and quantization, the signal is in the form of a sequence of numbers. The *Fig. 2.5* shows the phenomenon [3].

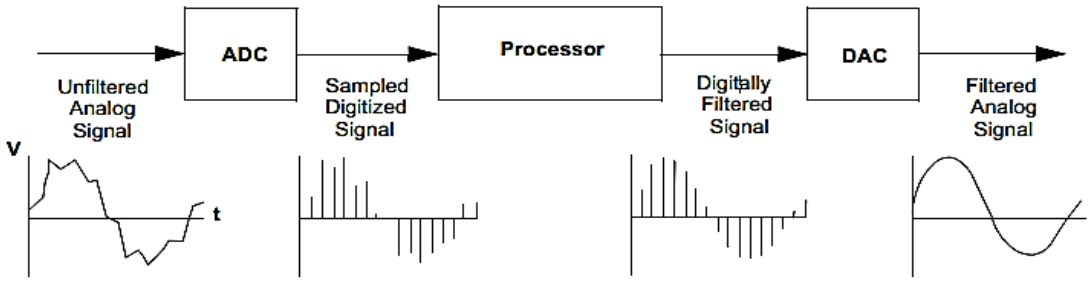



*Fig. 2.5 Signal Processing Using Digital Filter*

The common method of designing a filter is as follows. The transfer function G(S) of an analog filter is derived for the required specifications. This transfer function is then converted to Z domain G(Z), which represents the Z transform of the transfer function of the desired digital filter. The conversion from S domain to Z domain can be done by any of the following methods:

• Impulse Invariant

• Step Invariant

• Bilinear Transformation

• Matched Z

The bilinear transformation (also known as Tustin's method) is used in digital signal processing and discrete-time control theory to transform continuous-time system representations to discrete-time and vice versa. Bilinear transformation technique is used in the conversion in which ‘s’ in the continuous transfer function is substituted

with the 'z' expression as shown below, to create the transfer function of the digital filter,

$$s = \frac{2(z-1)}{T(z+1)}$$

Where, T= sampling period satisfying the Nyquist Criteria [3].

The continuous transfer function is:

$$G(s) = \frac{s^2 + 314^2}{s^2 + 25s + 314^2}$$

Now, for bilinear transformation, let's take sampling frequency of 5000 Hz and then substituting $s = \frac{2(z-1)}{T(z+1)}$ at T=1/5000 sec,

$$G(z) = \frac{0.9975 - 1.9911z^{-1} + 0.9975z^{-2}}{1.0000 - 1.9911z^{-1} + 0.9950z^{-2}} = \frac{Y(z)}{X(z)}$$

After some manipulation,

$$Y(z) = 0.9975X(z) - 1.9911z^{-1}X(z) + 0.9975z^{-2}X(z) + 1.9911z^{-1}Y(z) - 0.9950z^{-2}Y(z)$$

Taking Inverse Z-transform, the required difference equation is:

$$\therefore \boldsymbol{y(k) = 0.9975x(k) - 1.9911x(k-1) + 0.9975x(k-2) + 1.9911y(k-1) - 0.9950y(k-2)}$$

Where, $k$ =n*T, n=0, 1, 2, 3 …

$y(k)$ = output at $k^{th}$ instant

$y(k-1)$ = output at $(k-1)^{th}$ instant

$y(k-2)$ = output at $(k-2)^{th}$ instant

$x(k)$ = input at $k^{th}$ instant

$x(k-1)$ = input at $(k-1)^{th}$ instant

$x(k-2)$ = input at $(k-2)^{th}$ instant

So, we can see that output at an instant depends upon input at the instant, previous inputs and previous outputs.

### 2.1.3. Hysteresis Band Current Control Scheme

It is an instantaneous feedback current control method in which a band is created around a reference current. The reference current is the required current that is expected to be injected ideally. The hysteresis band provides boundary around reference within which the injected current is made to fluctuate as in the *Fig. 2.6*. This is achieved by controlling the gate signal of the inverter.

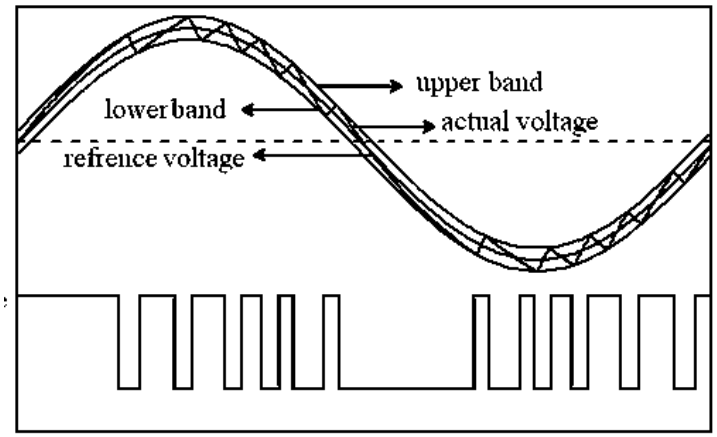



*Fig. 2.6 Hysteresis Band Current Control Scheme*

A comparator is used to compare the value of actual signal and the reference signal to give gate signal as output. Normally, to control the value of some signal, one of the approach is: to use a single threshold value i.e. with no band around the reference signal. In that case, as the actual signal crosses the reference signal, the output gate signal varies as shown in *Fig* 2.7 *A*. Another approach is to create an upper and lower threshold around the reference signal, thus obtained output gate signal is as shown in the *Fig. 2.7* as B. The signal B has less oscillation than compare to A.

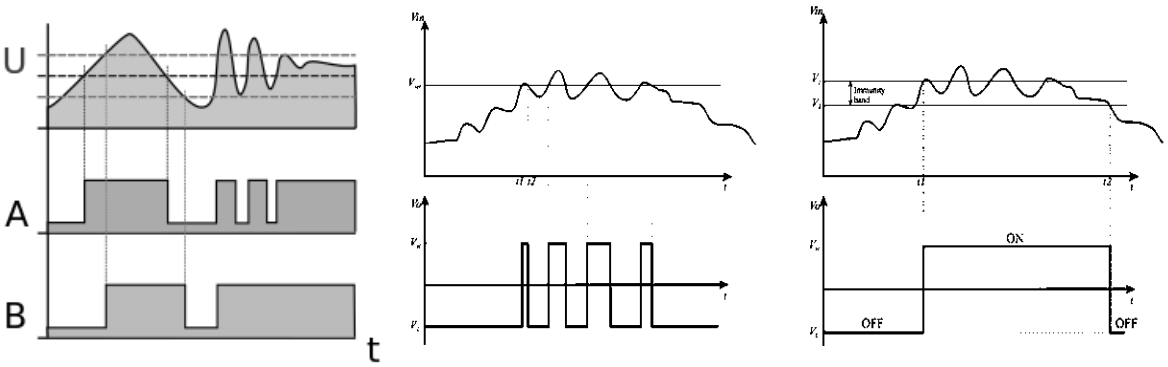



*Fig. 2.7 Comparator Output Signal with Single and Double Threshold*

### 2.1.4. H-Bridge Inverter

Four switches are used in two-leg full bridge inverter (H-Bridge inverter) as shown in *Fig. 2.8.* Here, $S_{1+}$ and $S_{2-}$ form one pair and remaining form the other. The configuration is maintained in such a way that one pair is OFF when another pair is ON using NOT gate. When the first pair is ON, the voltage at output is positive resulting rise in the inverter current. And reversely, when the second pair is ON, the voltage at the output of inverter is negative causing fall in the inverter current. A constant dc supply from a battery is fed to the inverter [2].

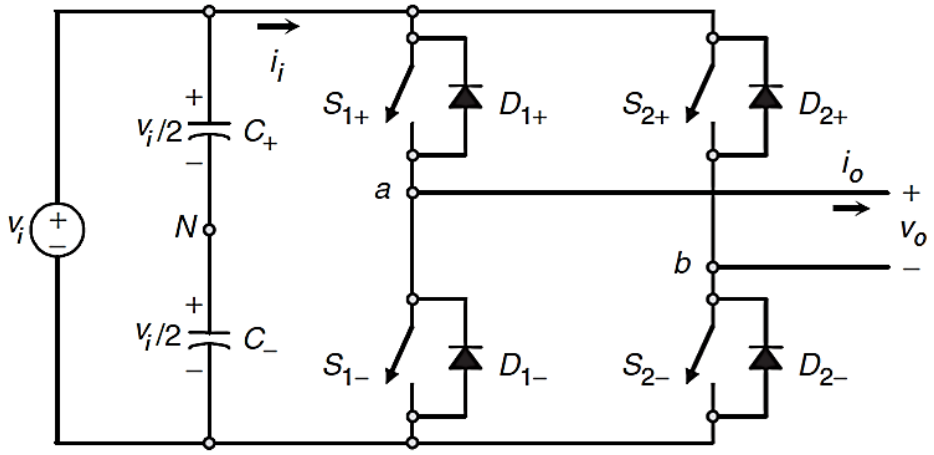



*Fig. 2.8 H-bridge Inverter*

## 2.2. MATLAB Simulation Study

MATLAB is a technical computing environment for high performance numeric computation and visualization. It is a technical computing language developed by The MathWorks Inc. MATLAB integrates numerical analysis, matrix computation, signal processing, and graphics into an easy-to-use environment. The name MATLAB stands for Matrix Laboratory.

Simulink is a software package inside the MATLAB. Simulink and MATLAB form a package that serves as a tool for modeling dynamic systems. Simulink provides graphical user interface (GUI) that is used in building block diagrams, performing simulations, as well as analyzing results. Simulink includes a comprehensive block library of sinks, sources, linear and nonlinear components, connectors etc. Simulink provides the facility of customizing and creating our own blocks. Using scopes and other display blocks the simulation result can be observed and analyzed. In addition, the parameters of the model developed can be changed and observed immediately for 'what if' exploration [5].

### 2.2.1. Load Modelling

The non-linear load is modeled in MATLAB/Simulink as show in the *Fig. 2.9*. It consists of a thyristor bridge fired at an angle of $30^0$ from pulse generator. The dc output of the bridge is fed to a RL load with resistance of 10 ohm and inductance of 100mH.

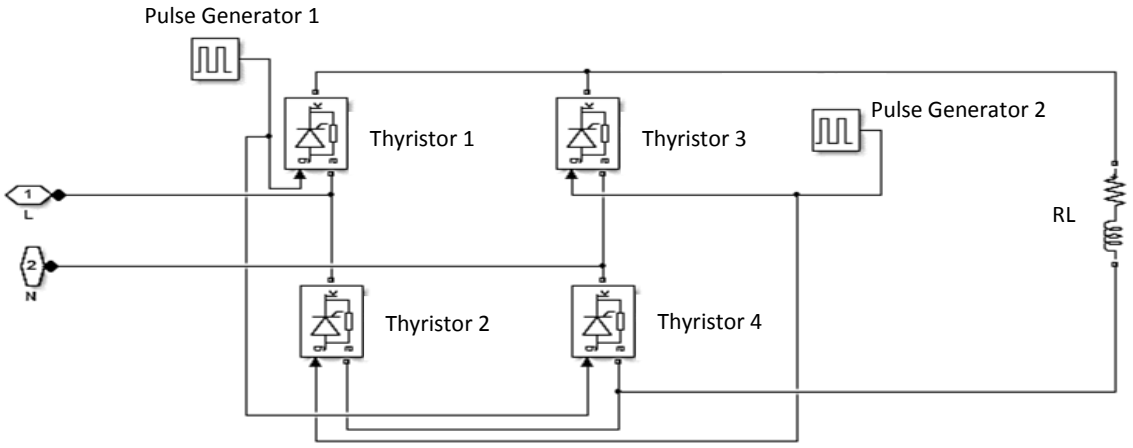



*Fig. 2.9 Simulation model of non-linear load in MATLAB/Simulink®*

### 2.2.2. Hysteresis Band Current Controller

The block in *Fig. 2.10* generates the gate signals for the inverter controlling the switching pattern of the IGBTs so as to generate the required current. The instantaneous injected current from the inverter ($I_0$) and reference current generated ($I_{ref}$) is supplied as input in the block and accordingly hysteresis band of the current is created. The block checks if injected current from inverter is within the limit of the band and produces corresponding output signal.

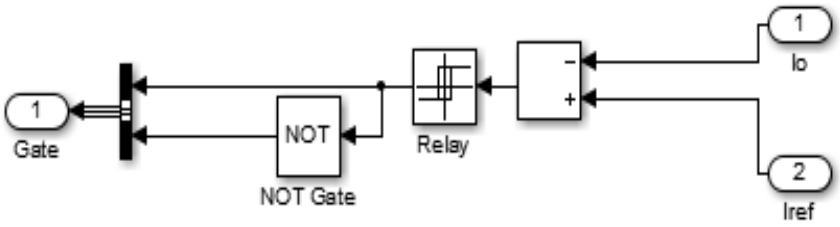



*Fig. 2.10 Simulation Model of Hysteresis Band Current Controller in MATLAB /Simulink®*

The difference of the reference current ($I_{ref}$) and the injected current ($I_0$) is fed to the relay. The relay is configured with the switch ON point as 0.1 and switch OFF point as -0.1. Hence, the relay creates a hysteresis band and checks if the injected current is within the band. Thus, the relay generates gate signals in following pattern:

When $I_{ref} - I_0 \leq -0.1$, output of relay=1

When $I_{ref} - I_0 \geq 0.1$, output of relay =0

### 2.2.3. H-Bridge Inverter

Four IGBTs are used in two-leg full bridge inverter (H-Bridge inverter) as shown in *Fig. 2.9.* Here, IGBT_1 and IGBT_3 form one pair and remaining form the other pair and the IGBT switching pattern are shown in the *Table 2.1.*

*Table 2.1 Truth Table for IGBT switching*

| Gate Signal | IGBT | State | $V_o$ |
|---|---|---|---|
| 1 | IGBT_1 and IGBT_3 | ON | $+V_c$ |
| | IGBT_2 and IGBT_4 | OFF | |
| 0 | IGBT_1 and IGBT_3 | OFF | $-V_c$ |
| | IGBT_2 and IGBT_4 | ON | |

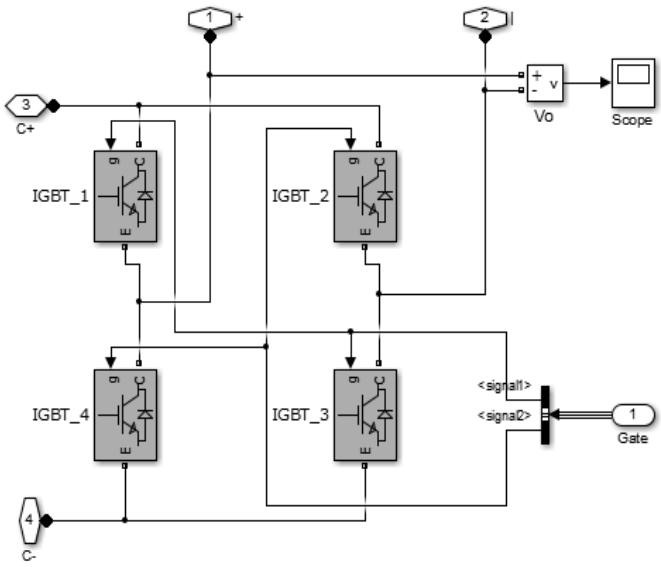



*Fig 2.9 Simulation Model of H-Bridge Inverter in MATLAB/Simulink®*

# 3. SIMULATION RESULTS

All the building blocks of Simulink as explained in previous section are integrated as in *Fig. 3.1* to form overall APF system. The scheme consist of generator modeled as an AC voltage source of 220V, 50Hz with the resistance of 0.002 ohm and inductance of 20mH which is supplying a non-linear load which is a thyristor bridge fired at an angle of $30^0$. The dc output of the bridge is fed to a RL load with resistance of 10 ohm and inductance of 100mH. The sensed load current is fed to shunt active power filter portion and output of the Inverter, with dc supply of 330V, is fed into the grid through an interfacing inductor with inductance of 1mH and resistance of 0.5 ohm. Then the simulation is performed with the parameters.

After the simulation, *Fig. 3.2* shows the waveforms of load current drawn by non-linear load, source current after compensation and reference current generated by notch filter respectively in *(a), (b)* and *(c).* Likewise, *Fig. 3.3* shows the waveforms of injected current by APF, inverter output voltage for one cycle and zoomed view of inverter output voltage respectively in *(a), (b)* and *(c).* Also, *Fig. 3.4* shows the waveform of transient response of compensated source current, source voltage and source current after compensation respectively in *(a)* and *(b).*

The harmonic distortion problem can be dealt efficiently with the FFT analysis tool in MATLAB®. This tool helps to analyze the signal by the measurements of Sampling time, DC components, fundamental component and THD. For the FFT analysis in the simulation, we took 1 microsecond as sampling time resulting 20000 samples per cycle.

The result of FFT analysis of load current and compensated source current are shown in *Fig. 3.5*. In the load current we observed fundamental component of 20.72A peak and DC component of 0.02157A resulting 34.63% THD. Whereas in the compensated source current, we observed fundamental component of 188A peak, DC component of 0.0517A and 34.63% THD.

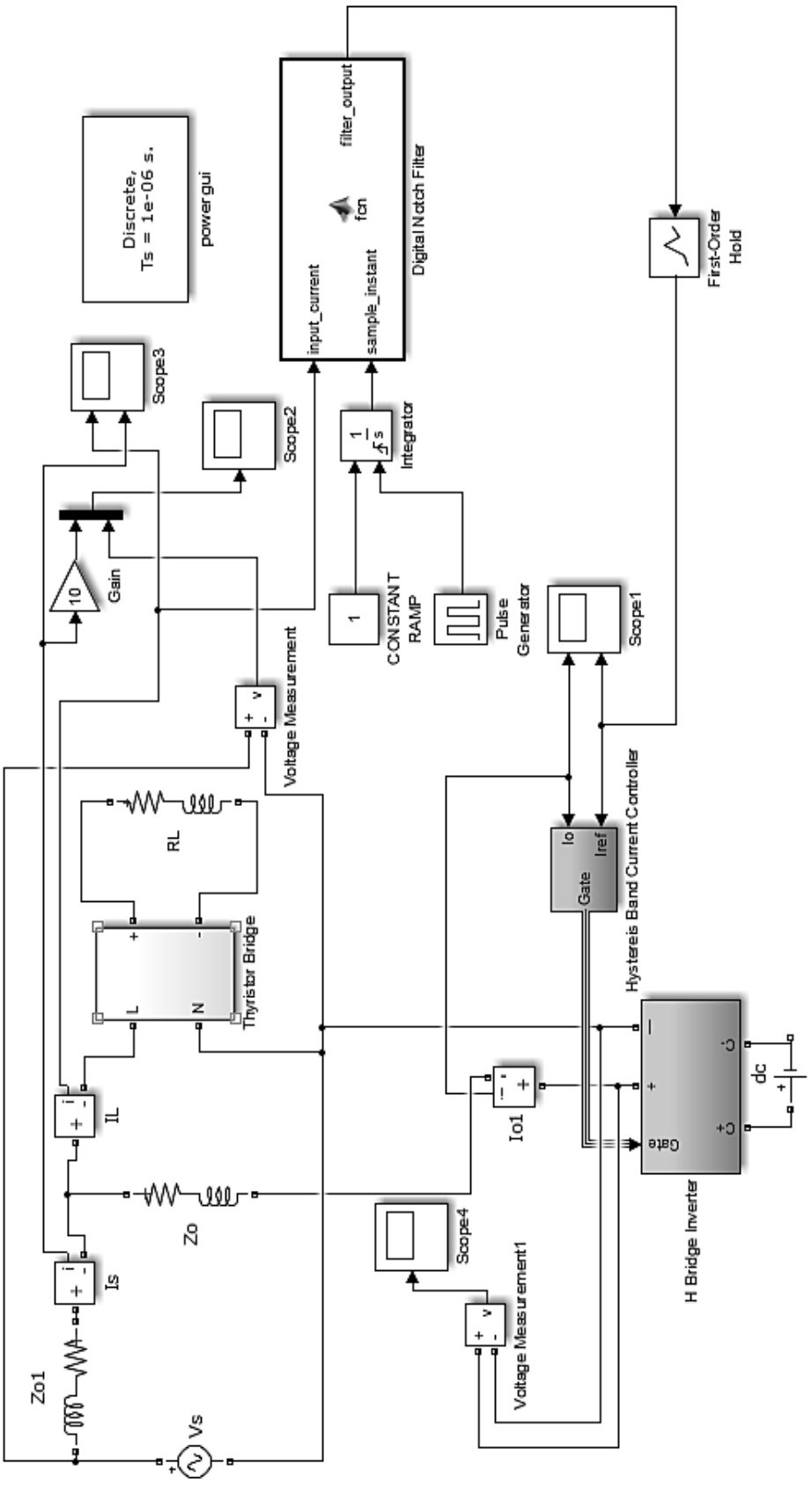
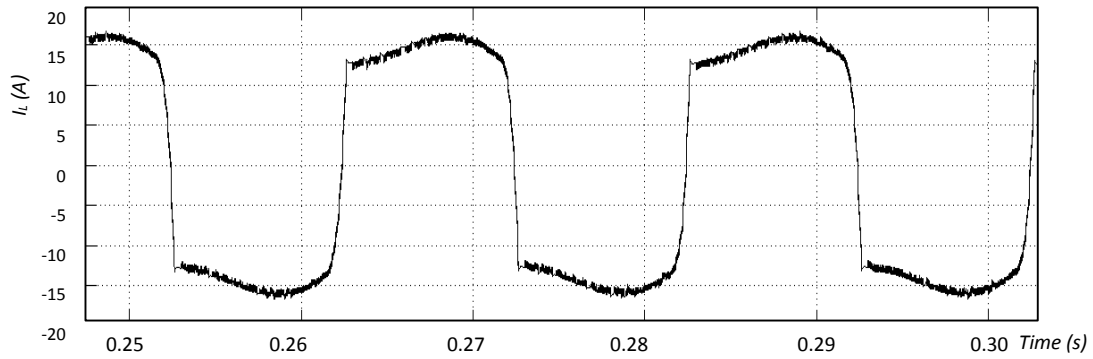
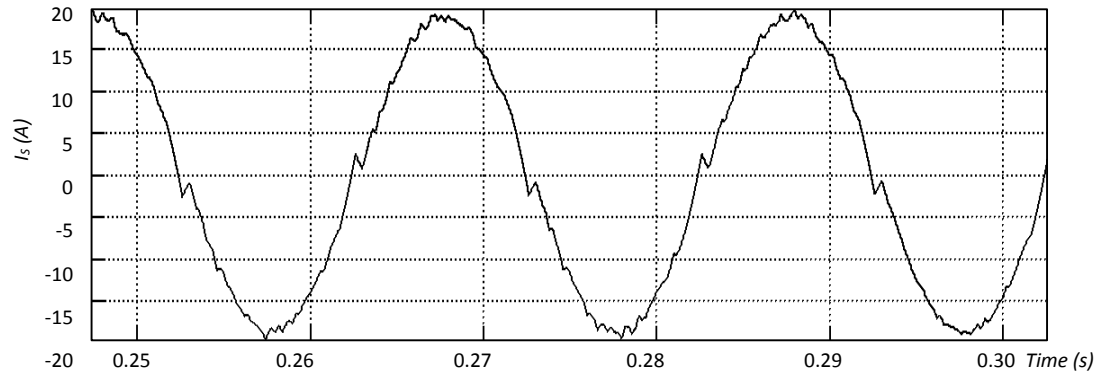


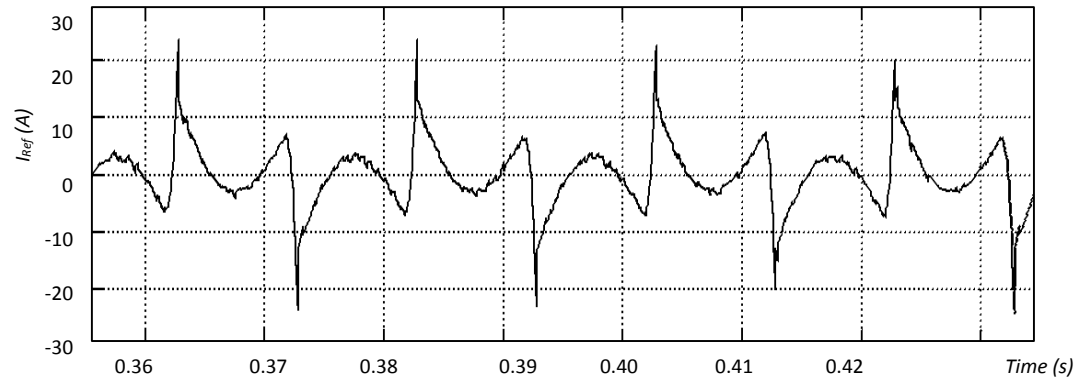

*Fig. 3.1 Overall Simulation Model of APF in MATLAB/Simulink®*




*(a)*




*(b)*




*(c)*

*Fig. 3.2 Waveforms of currents (a) Load Current drawn by non-linear load (b) Source current after compensation (c) Reference current generated by notch filter*

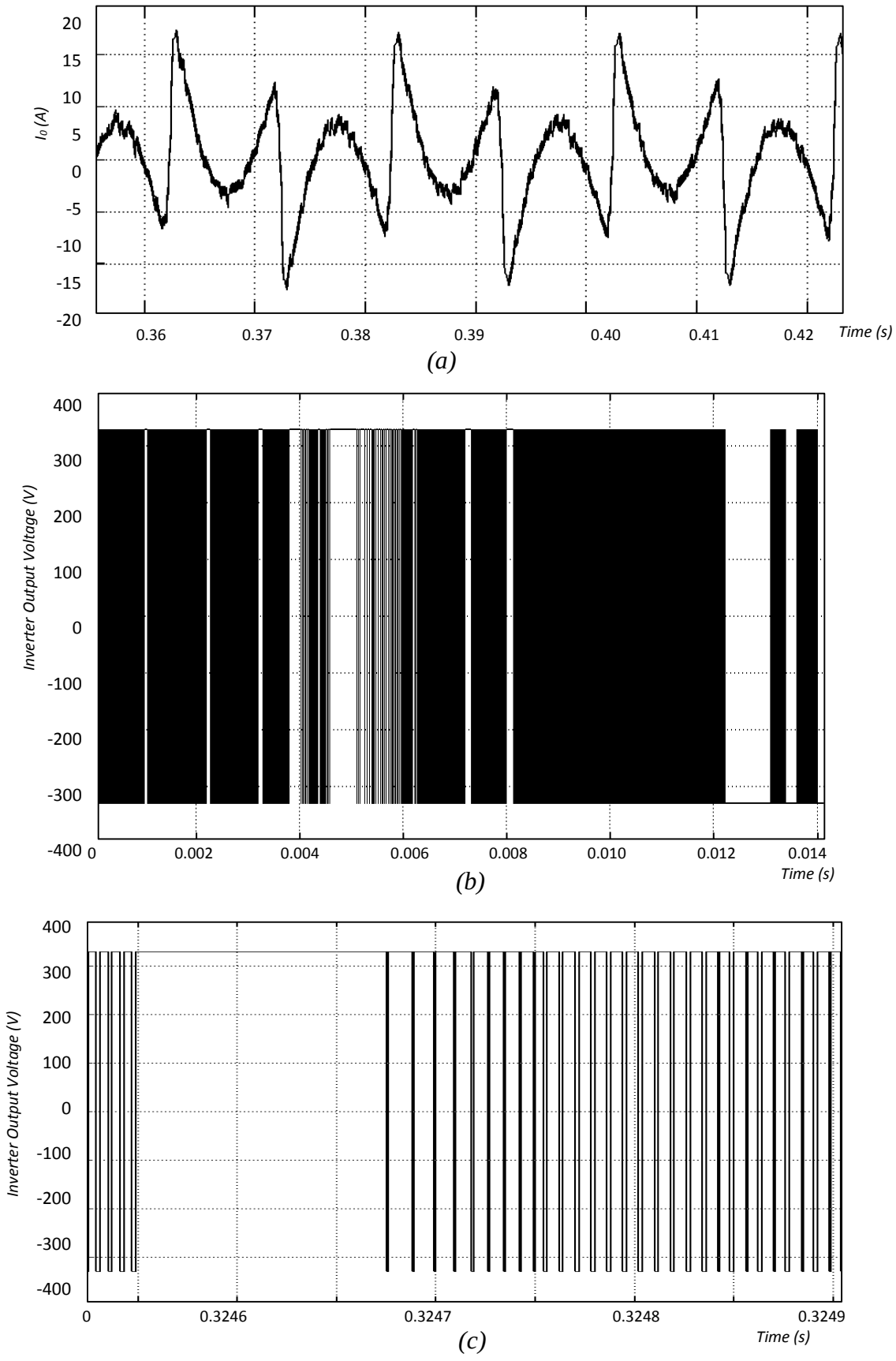
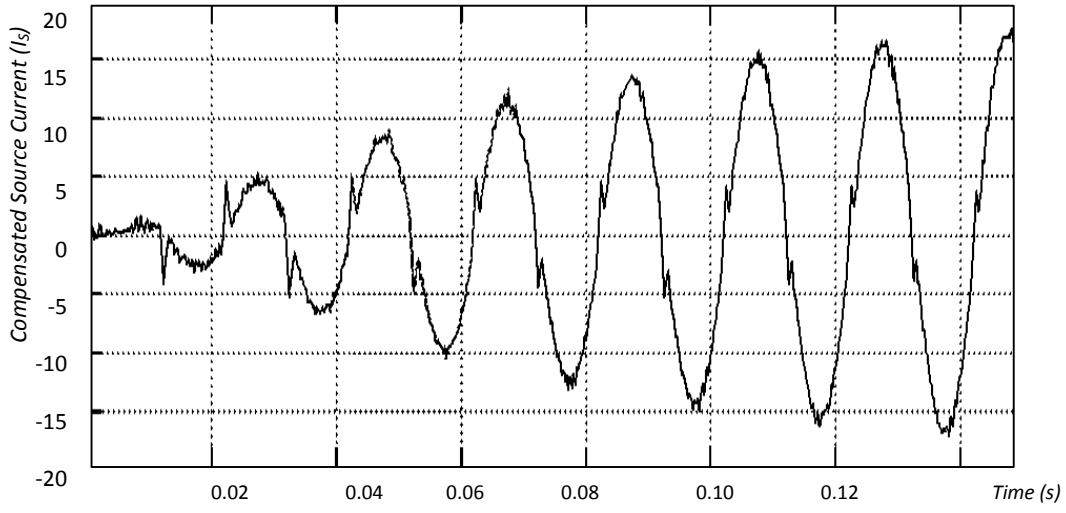
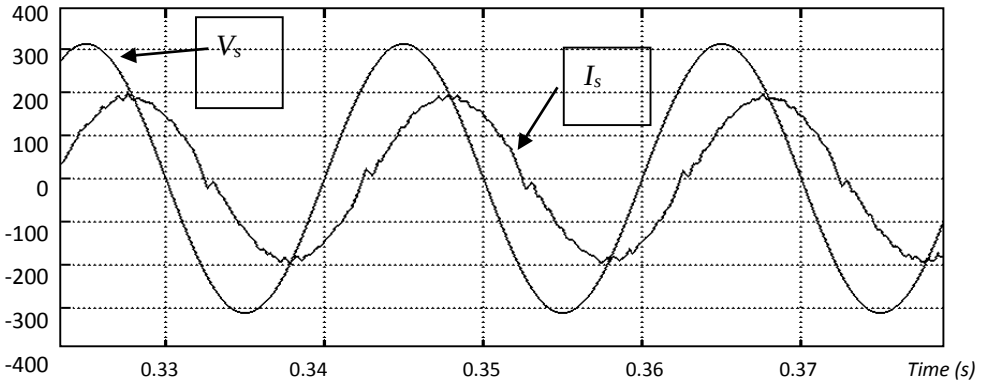



*Fig. 3.3 Waveform of (a) Injected current by APF (b) Inverter Output Voltage for one cycle (c) Zoomed view of inverter output Voltage*

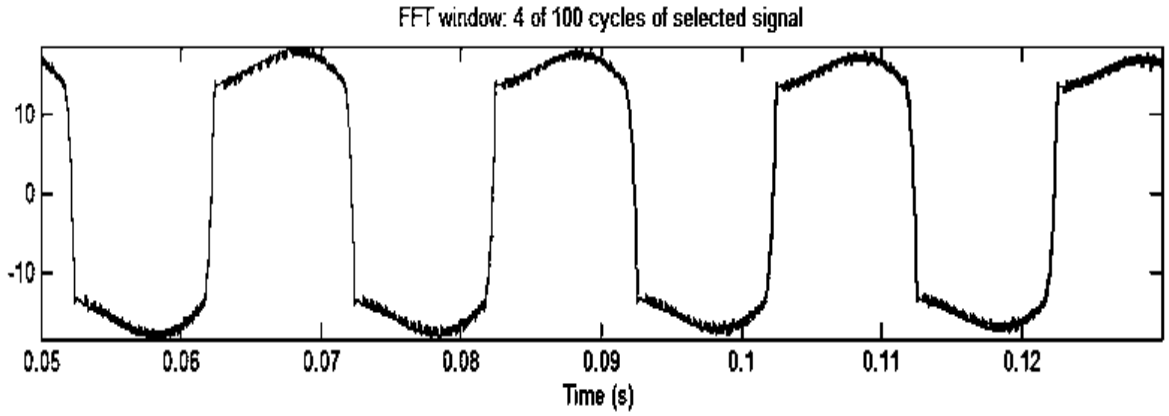



*(a)*



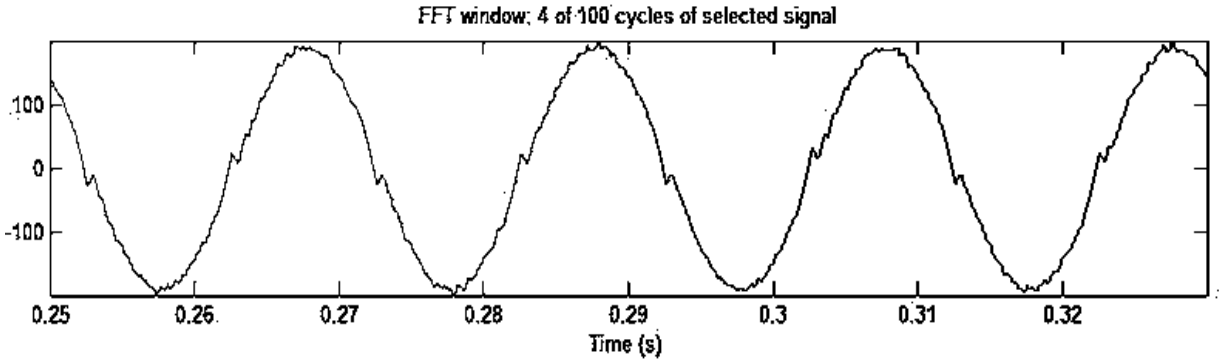

*(b)*

*Fig. 3.4 Waveform of (a) Transient response of compensated source current (b) Source voltage and source current after compensation*




| | |
|---|---|
| Sampling time | = 1e-06 s |
| Samples per cycle | = 20000 |
| DC component | = 0.02157 |
| Fundamental | = 20.72 peak (14.65 rms) |
| THD | = 34.63 % |

*(a)*




| | |
|---|---|
| Sampling time | = 1e-06 s |
| Samples per cycle | = 20000 |
| DC component | = 0.05717 |
| Fundamental | = 188 peak (132.9 rms) |
| THD | = 5.07 % |

*(b)*

*Fig. 3.5 FFT analysis of (a) Load current (b) Compensated Source current*

# 4. HARDWARE IMPLEMENTATION

The main hardware parts that were used in our hardware fabrication of our proposed single phase Shunt APF are explained below:

## 4.1. Non-Linear Load

In hardware, the non-linear load is modelled with a RL load with inductance (L) = 6 H and resistance (R) =30 ohm, fed through the output of full-wave bridge rectifier and 7V AC from auto-transformer is supplied to the rectifier. *Fig. 4.1* shows the schematic in PROTEUS. The simulation result showing current waveform of non-linear load is observed in Oscilloscope of PROTEUS as in the *Fig 4.2.* In actual hardware, *Fig 4.3* shows the current waveform of non-linear load on CRO.

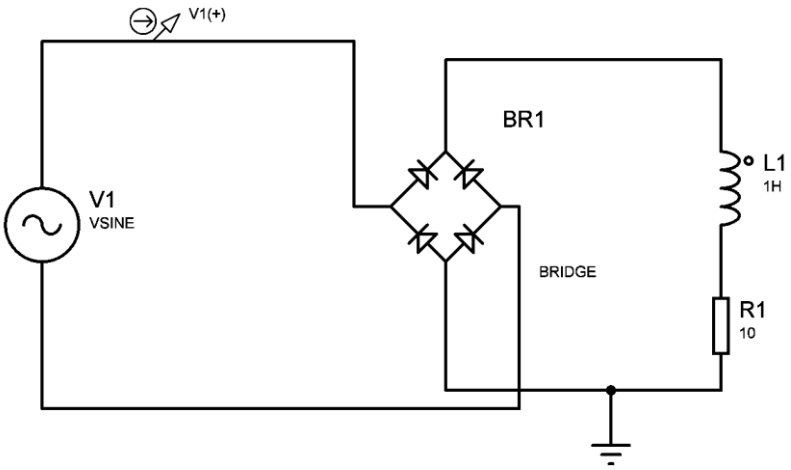



*Fig. 4.1 Simulation model of Non-Linear load in Proteus®*

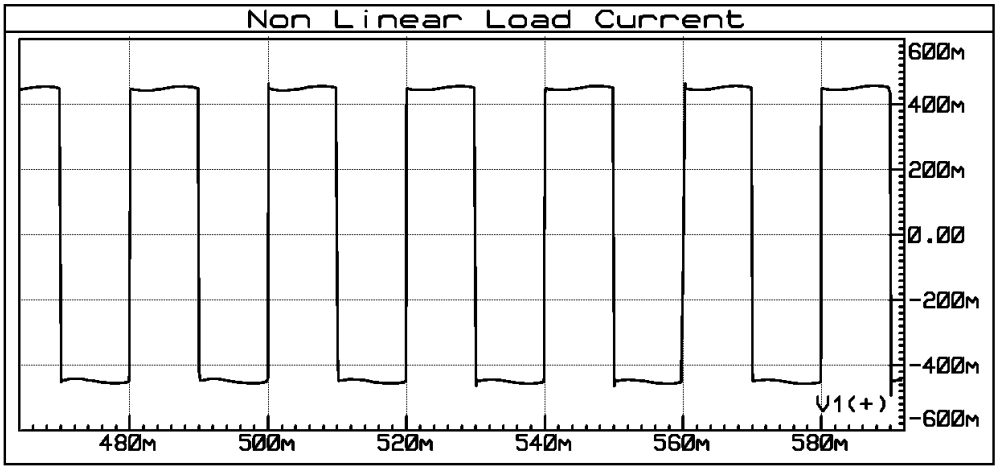



*Fig. 4.2 Current Waveform of Non-Linear load in Proteus®*

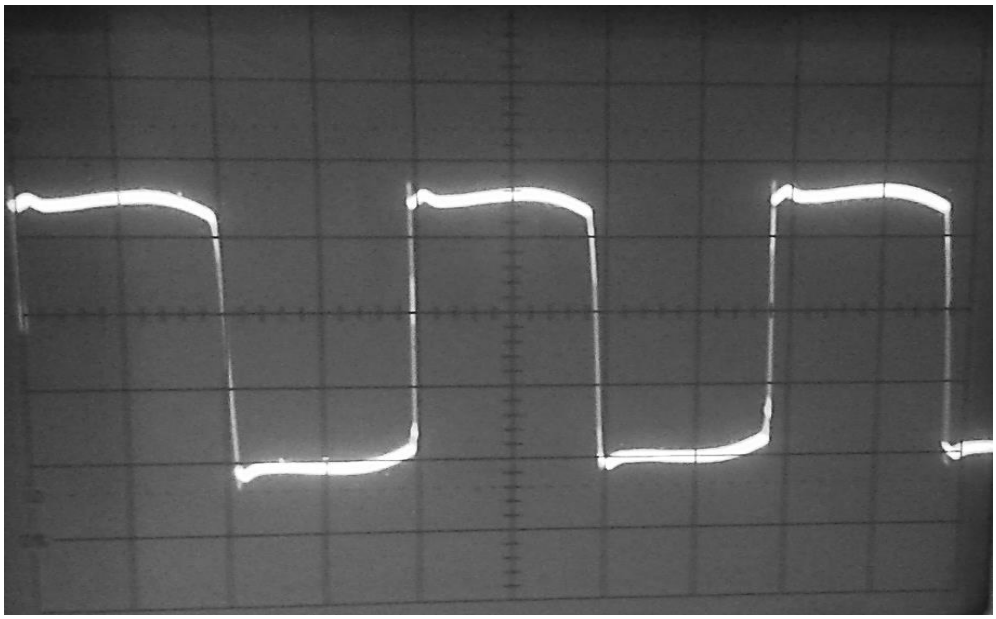


*Fig. 4.3 Current Waveform of Non-Linear load in actual hardware on CRO*

## 4.2. Offset (Clamper) Circuits

Input to the microcontroller must be within 0V to 5V. But the input signal x(t) will be an AC signal within the range of -2.5V to +2.5V. So the input signal x(t) must be converted to the range of 0 to 5V by using positive offset circuit. Similarly, the output of microcontroller and DAC will be in the range of 0V to 5V which has to be converted again to the initial range of -2.5V to 2.5V. These are achieved by using offset circuit as shown in the *Fig. 4.4.* Simulation on PROTEUS of the hardware model gives the the result as in the *Fig. 4.5 (a).* In actual hardware implemention, the output on CRO is as in the *Fig. 4.5 (b)* showing the positive clamping of sine wave.

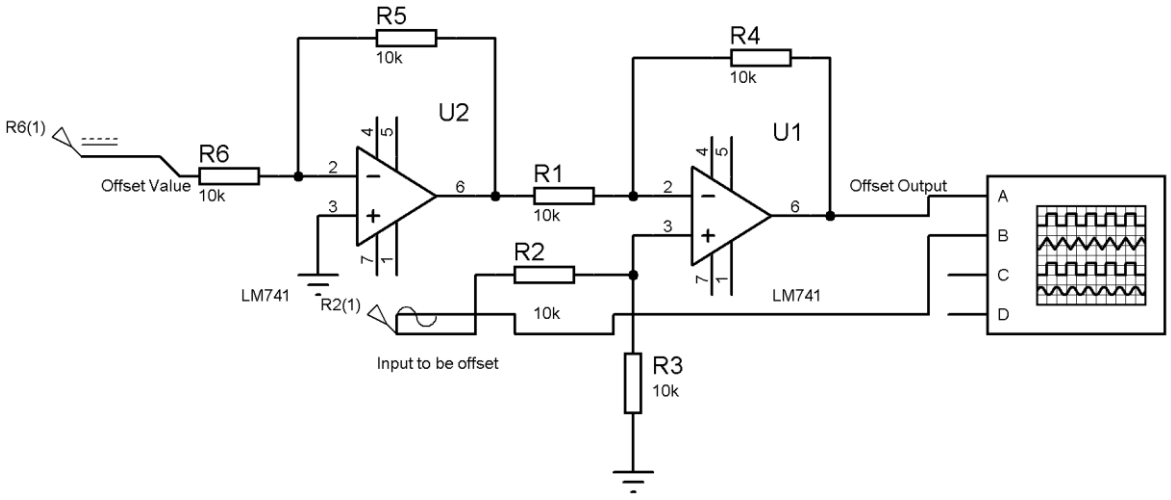
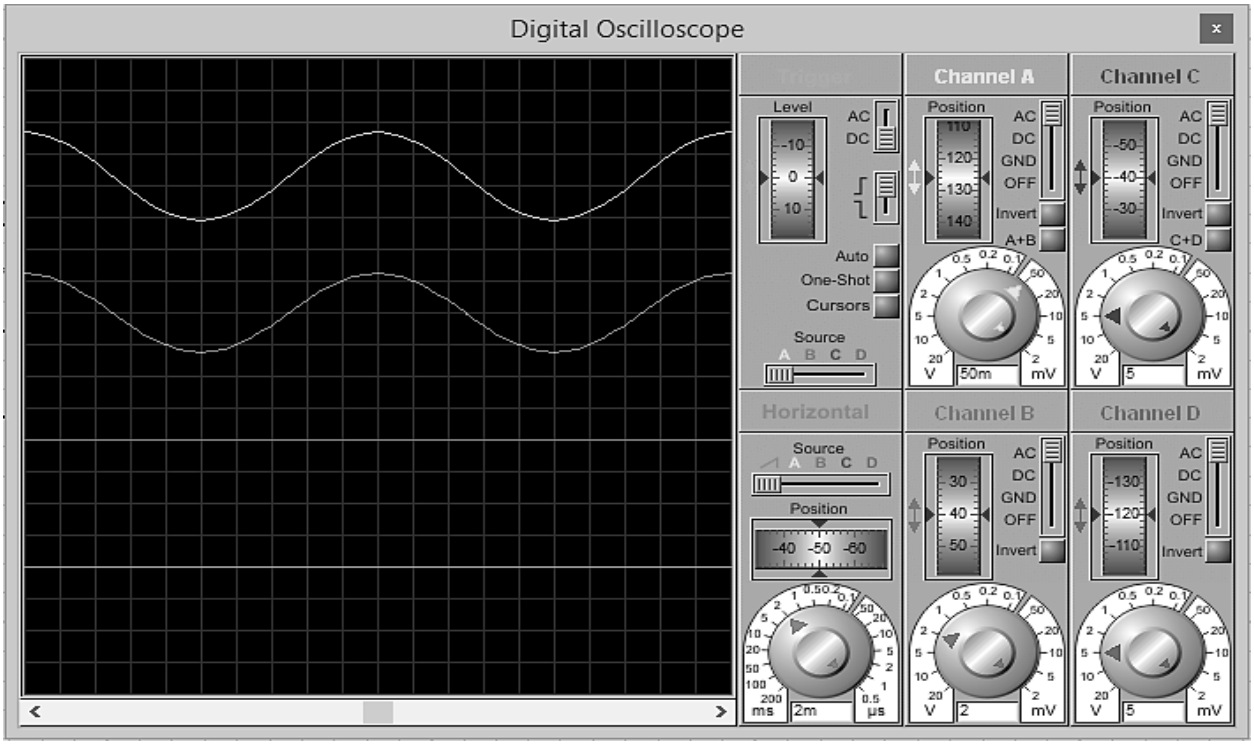
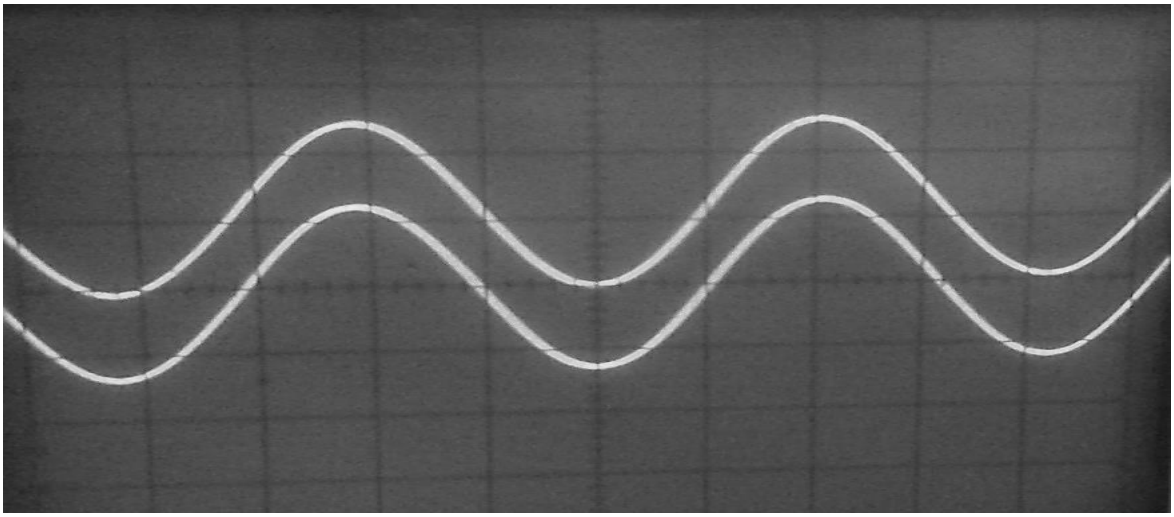



*Fig. 4.4 Simulation model of Positive Offset Circuit in Proteus®*




*(a)*



*(b)*

*Fig. 4.5 Waveform of positive clamping of sine wave (a) in oscilloscope in Proteus® (b) on CRO in actual hardware*

## 4.3. Notch Filter

Notch filter is digitally implemented by using the difference equation:

$$y(k) = 0.9975x(k) - 1.9911x(k-1) + 0.9975x(k-2) + 1.9911y(k-1) - 0.9950y(k-2)$$

which is implemented in AVR ATmega8 microcontroller. To begin with, input load current is sensed through Hall Effect CT and fed to the ADC. Then, the output of ADC is x(k) which is digital input load current. This x(k) is fed to the digital notch filter whose output is y(k). Here, x(k) is the digital input signal to the filter with fundamental frequency component and harmonic components but y(k) is the digital output signal from the filter with only harmonic components. Then, the output digital signal y(k) is then converted into analog signal y(t) with DAC circuit. The implementaion of digital notch filter in PROTEUS is as shown in the *Fig. 4.6*. The simulation of this module in PROTEUS is visualized in Oscilloscope as shown in the *Fig. 4.7(a)* which shows the response of notch filter. In actual hardware, the response of noctch filter obtained in CRO is as in the *Fig. 4.7(b).*

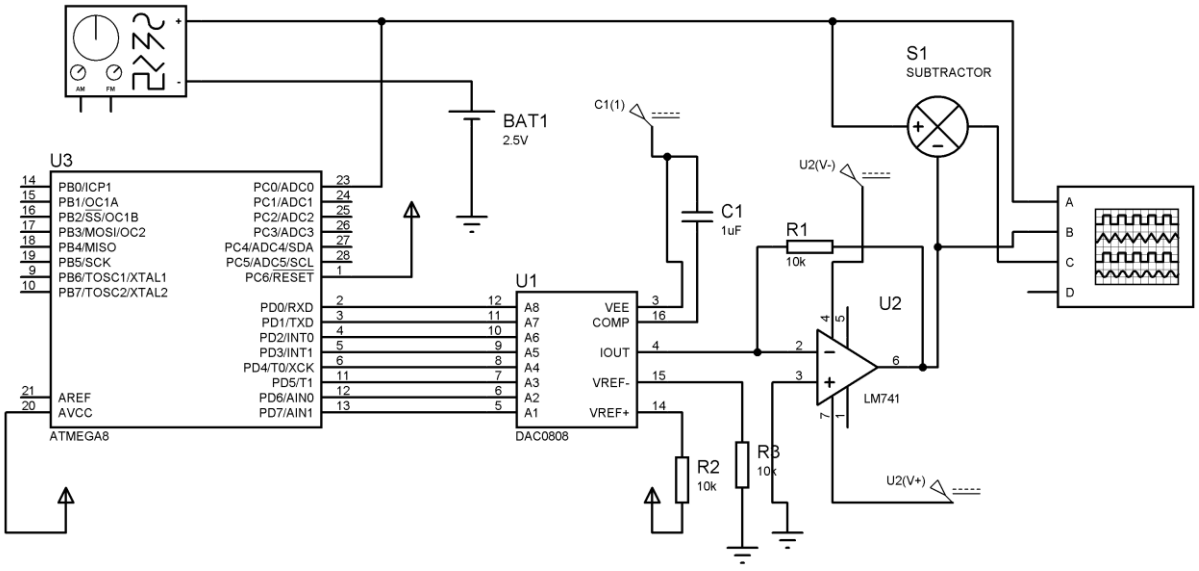
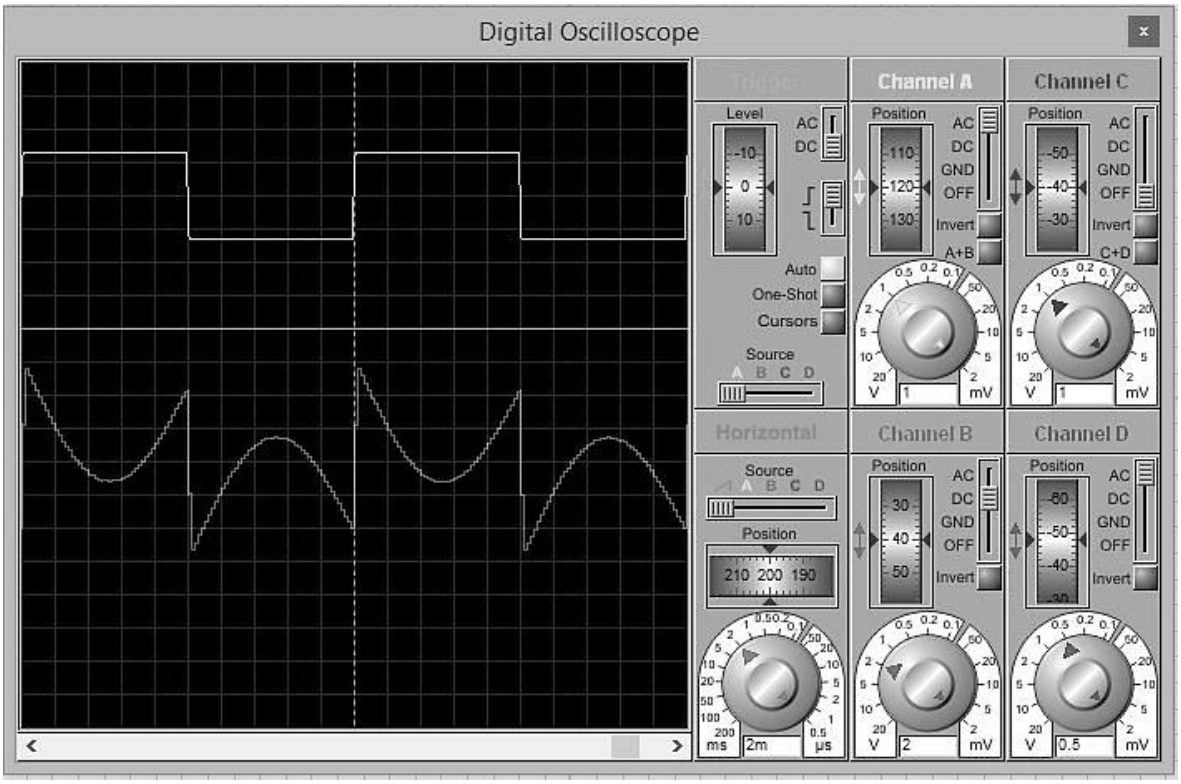
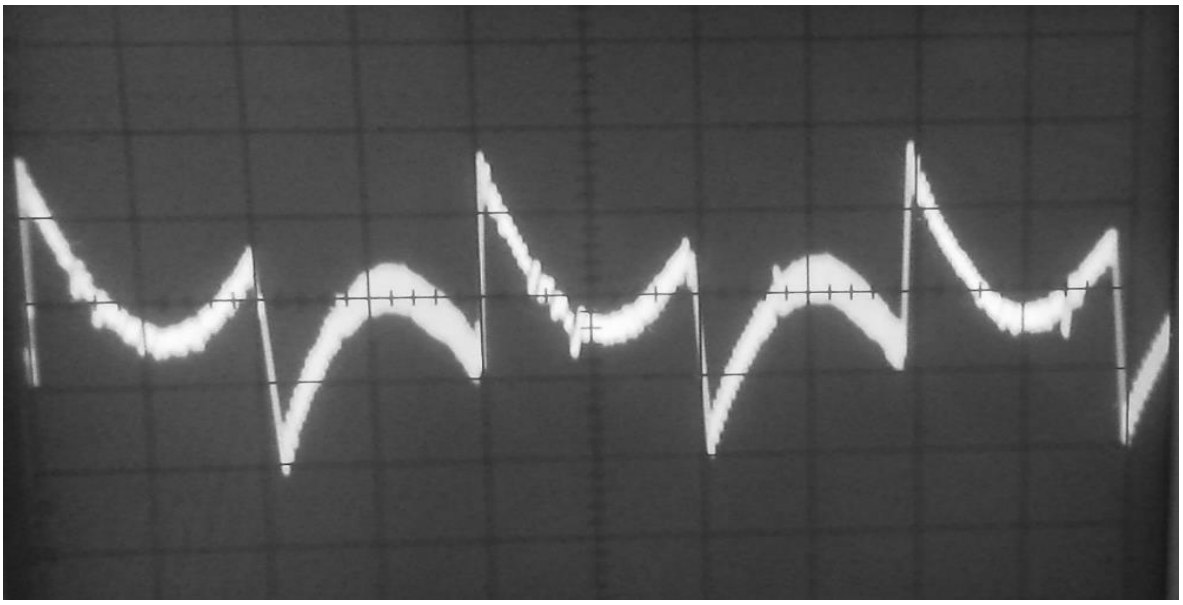



*Fig. 4.6 Simulation model of Digital Notch Filter on ATmega8 in Proteus®*




*(a)*



*(b)*

*Fig. 4.7 Response of Notch Filter (a) in oscilloscope in Proteus® (b) on CRO in actual hardware*

### 4.3.1. Microcontroller: Atmel AVR ATmega8

A microcontroller (sometimes abbreviated µC, uC or MCU) is a small computer on a single IC containing a processor core, memory, and programmable I/O peripherals. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications.

Microcontrollers are used in automatically controlled products and devices, such as automobile engine control systems, implantable medical devices, remote controls, office machines, appliances, power tools, toys and other embedded systems. With its small size and increased flexibility it is finding its application in more and more devices and processes.

In this project, Atmel AVR ATmega8, as in the *Fig. 4.8*, microcontroller has been used for the purpose of implementing the notch filter in digital form to obtain harmonics components contained in the power circuit current.

The AVR is a modified Harvard architecture 8-bit RISC single chip microcontroller which was developed by Atmel in 1996. The AVR was one of the first microcontroller families to use on-chip flash memory for program storage, as opposed to one-time programmable ROM, EPROM, or EEPROM used by other microcontrollers at the time.

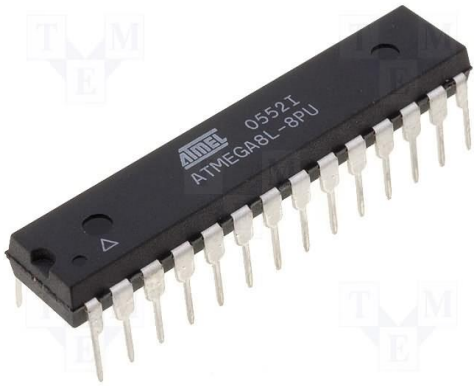



*Fig. 4.8 Atmel AVR ATmega8 IC*

The Atmel AVR ATmega8 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega8 achieves throughputs approaching 1 MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The Atmel AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit

(ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The general Pin Configuration of Atmel AVR ATmega8 is as shown in *Fig. 4.9.*

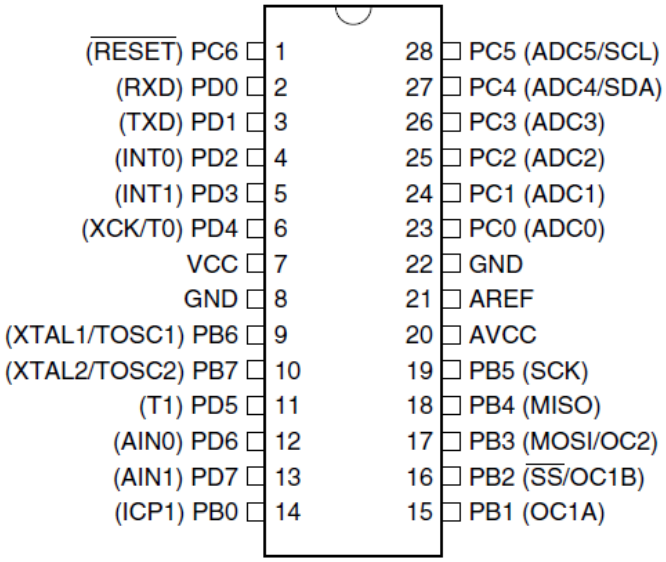



*Fig. 4.9 Atmel AVR ATmega8 Pin Configuration*

## 4.4. DAC

DAC stands for digital to analog converter. It is used to convert the digital 1 (+5 volt) and 0 (0 volt) data into analog values. The reference wave is generated in the digital circuit using the inputs and mathematics, which is then communicated with the DAC chip which converts the digital data into corresponding analog values. In this way, the reference signal is generated. Here, the DAC chip used is DAC 0808 as in the *Fig. 4.10,* which is an 8 bit DAC i.e. it takes 8 bit digital data as input and can take $2^8$ different states each representing a different analog value. It is a parallel DAC, so it requires 8


*Fig. 4.10 DAC0808 IC*

data lines from the microcontroller to its input. The output of DAC 0808 is in current form, hence an op-amp is used to convert it into corresponding voltage form. *Fig. 4.11* shows the hardware model of DAC in PROTEUS. For the verification we have used digital input 10000000(128 decimal) whose analog output is 2.5V as shown in *Fig 4.12*.

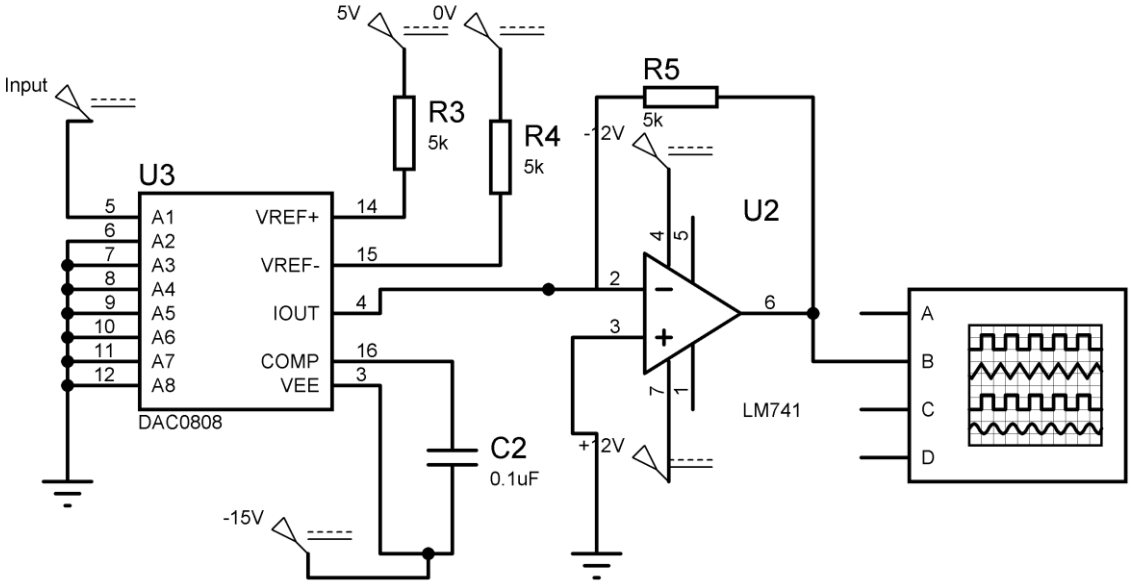



*Fig. 4.11 DAC in Proteus®*

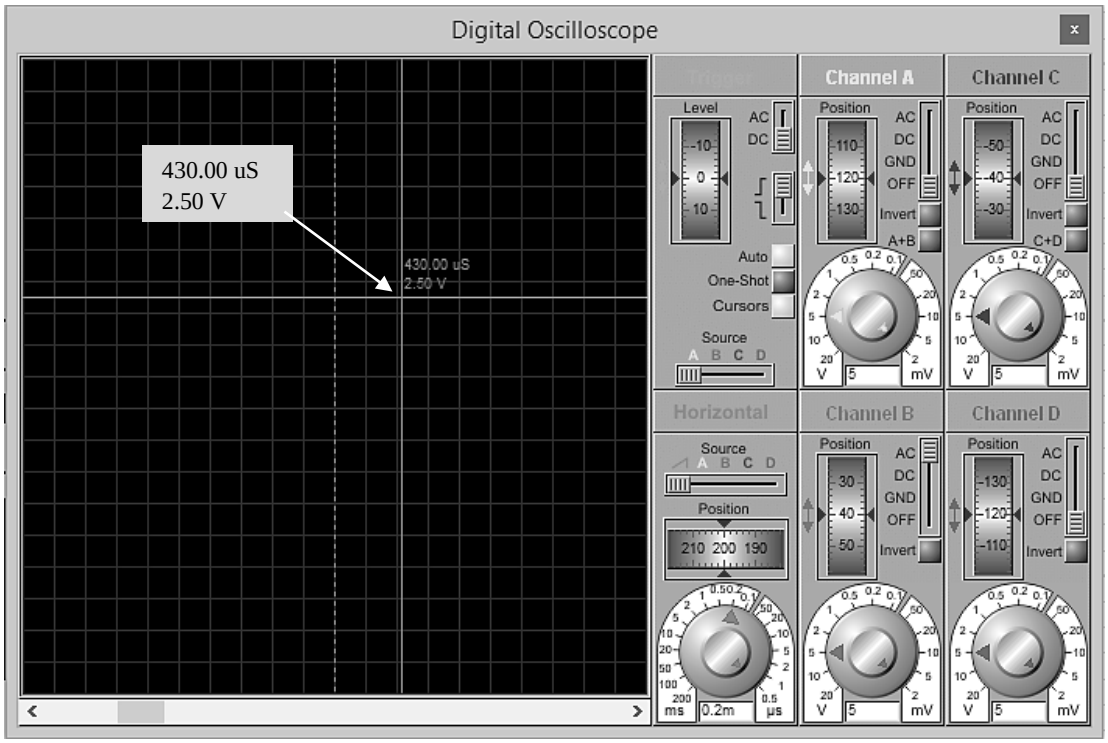



*Fig. 4.12 Output of DAC when digital input is 10000000 i.e. 128 in Proteus® Oscilloscope*

## 4.5. Hysteresis Band Current Controller (Schmitt Trigger)

It is a circuit or system with positive feedback and loop gain greater than 1. It is called "trigger" because the output retains its value until changes sufficiently to trigger a change. In the non-inverting configuration, when the input is higher than a certain chosen threshold, the output is high. When the input is below a different (lower) chosen threshold, the output is low, and when the input is between the two levels, the output retains its value. This dual threshold action is called hysteresis and implies that the Schmitt trigger possesses memory and can act as a bi-stable circuit (latch or flip-flop). There are two threshold values in Schmitt trigger which are formed by adding certain value to create upper threshold and subtracting same value to create lower threshold. In this way a band is created around the reference signal in Schmitt trigger called as hysteresis band. Thus, Schmitt trigger can be used to create a hysteresis band around the reference signal and compare the actual signal such that the output changes its state only when actual signal try to cross the band around the reference signal if the output signal can control the actual signal behavior. This can be done if output is used as a gate signal for the inverter which controls the actual current through inverter. Thus, Schmitt trigger is of great help to create hysteresis band and gate signal for the inverter. *Fig. 4.13* shows the circuit diagram for hysteresis band and gate signal generator. It is the main part of the system where the reference current and the actual current waveform

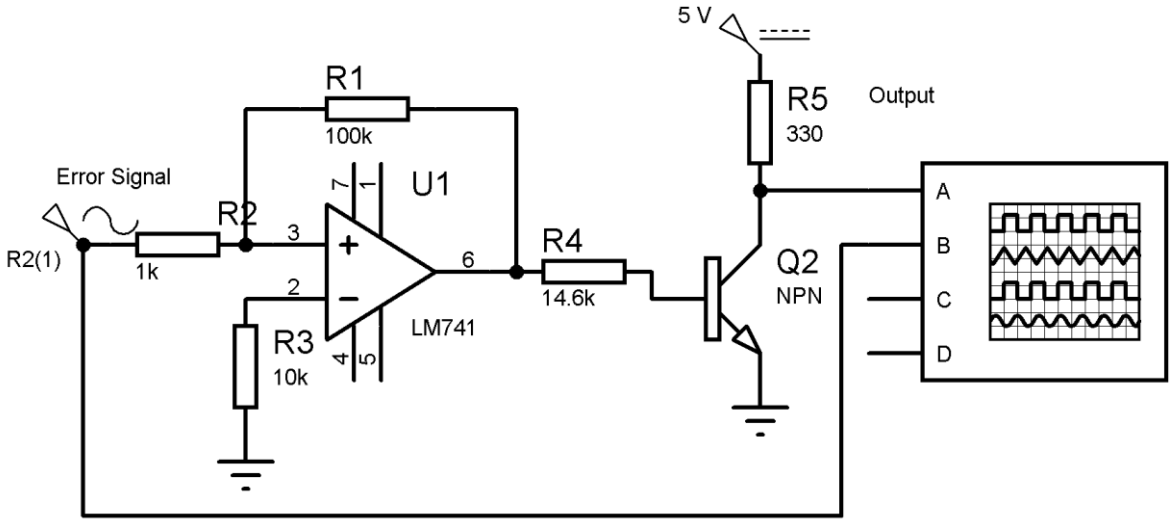
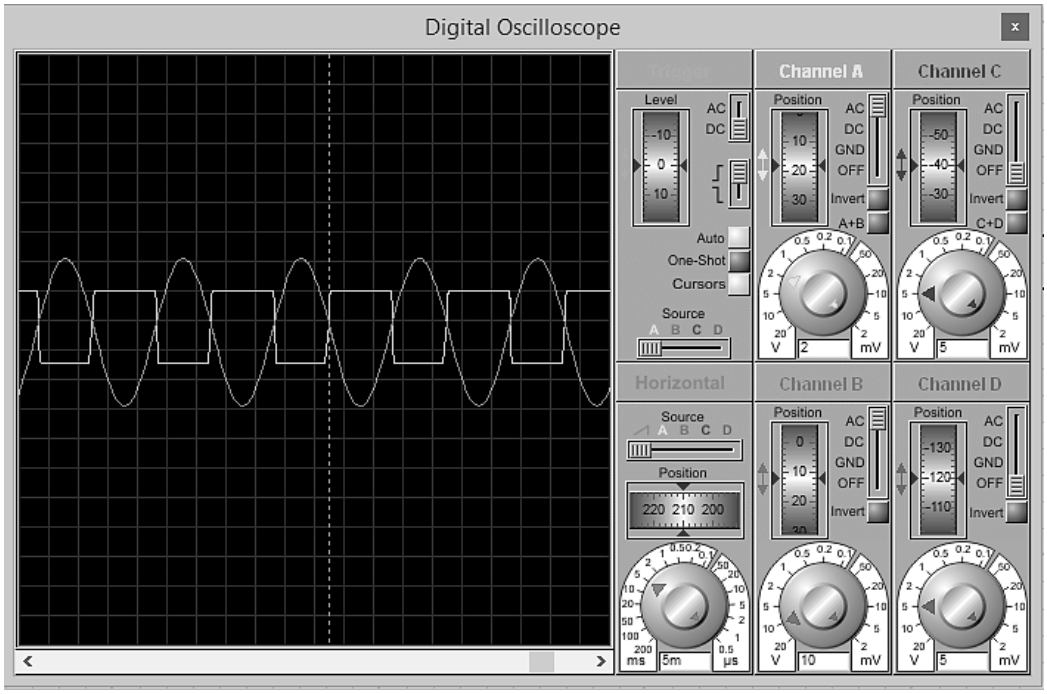


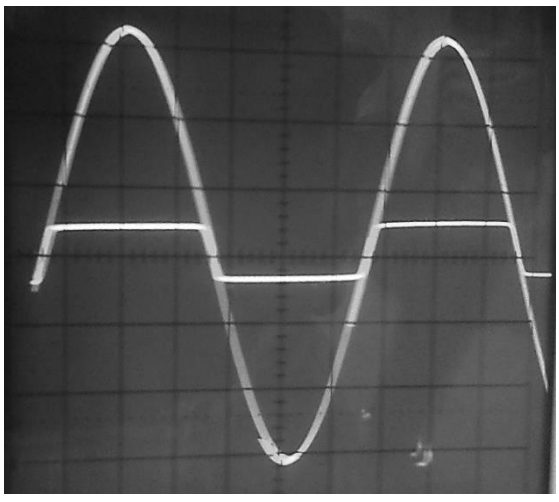

*Fig. 4.13 Schmitt Trigger in Proteus®*

are compared in order to generate the gate signal for the inverter. It consists of a subtractor in series with non-inverting Schmitt Trigger circuit configuration. The subtractor subtracts the actual current from the reference current. This error (subtracted value) is the input to the Schmitt Trigger. The reference of the Schmitt Trigger is set to

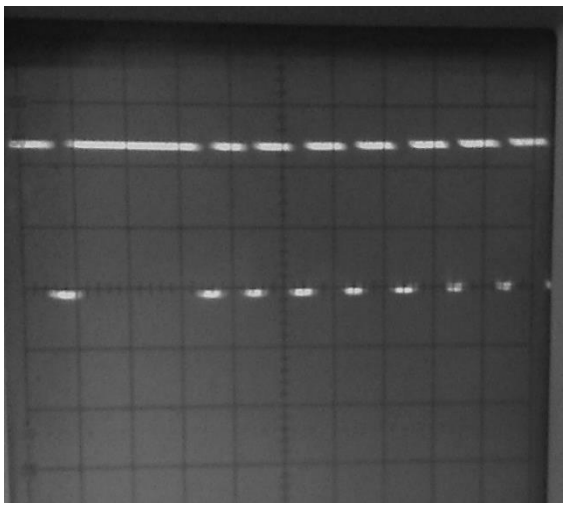
ground. Hence, it creates a band around the ground axis. Hence, as the error crosses the band, the output gate switch signal switches its state which acts as the gate signal to the inverter. *Fig. 4.14(a)* shows the simulation result of Schmitt Trigger (Inverting Type) output for a sinusoidal test signal in Proteus® Oscilloscope. In actual hardware, *Fig. 4.14(b)* shows response of Schmitt Trigger (Non-Inverting Type) for a sinusoidal test signal. *Fig. 4.14(c)* shows the actual response of Schmitt Trigger output for interter gate signal.




*(a)*



*(b)*



*(c)*

*Fig. 4.14 Schmitt Trigger output for a sinusoidal test signal (a) Inverting Type in Proteus® Oscilloscope (b)Non-Inverting Type output in CRO (c) Actual Schmitt Trigger output for Inverter gate signal in CRO*

## 4.6. H-Bridge Inverter

The inverter converts the DC power into AC power. The H-bridge inverter uses four MOSFETs as its switches in this circuit. MOSFETs are switched using a MOSFET driver IC IR2110. The driver converts the digital gate signal into required gate voltages of the MOSFETs. The gate signal is obtained from the hysteresis generator block. The above circuit clearly shows the driver IC and the H-bridge inverter using constant dc source. If the MOSFETs of the same leg of the H-bridge gate turned ON at the same instant, it creates a short circuit. Thus, in order to prevent this condition, the signal to the lower MOSFET is the inverted signal to the higher MOSFET using the NOT gate as shown in *Fig. 4.16* in the next page.

### 4.6.1. MOSFETs (IRF540)

MOSFET is a type of transistor used for amplifying or switching electronic signals. The gate of MOSFET is insulated from the channel by a silicon dioxide layer. It is voltage controlled device i.e. a certain voltage applied in the gate turns on the MOSFET and it allows the flow of current from drain to source otherwise it acts like a huge impedance and stops the flow of current. Thus, MOSFET can be used as switch in the inverter. It has lower switching loss than BJT. But it has higher power loss than BJT. IGBT has lower switching loss as well as lower power loss. Considering the cost and unavailability in Nepalese market, MOSFET is the best option for our project. A typical MOSFET IC and its representation is shown in the *Fig. 4.15.*

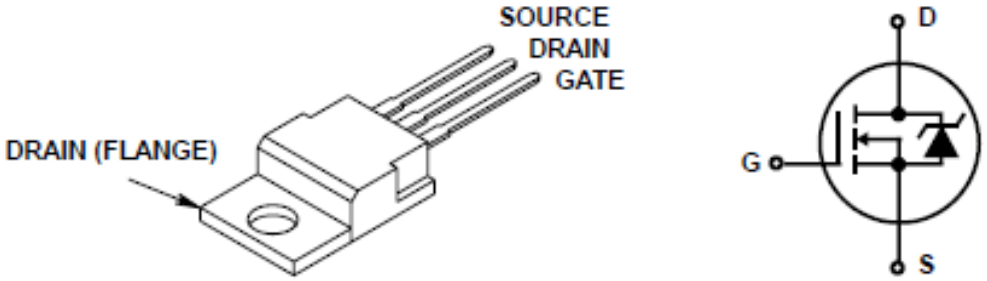



*Fig. 4.15 IRF540 IC and MOSFET's Symbol*

In this section, two pairs of MOSFETs are used to construct a single phase H-bridge inverter. The MOSFET gate requires a voltage of about +12 volts with respect to source in order to turn on. Thus, in order to drive the MOSFET a special driver IC is to be used which maintain this value using a bootstrap capacitor.

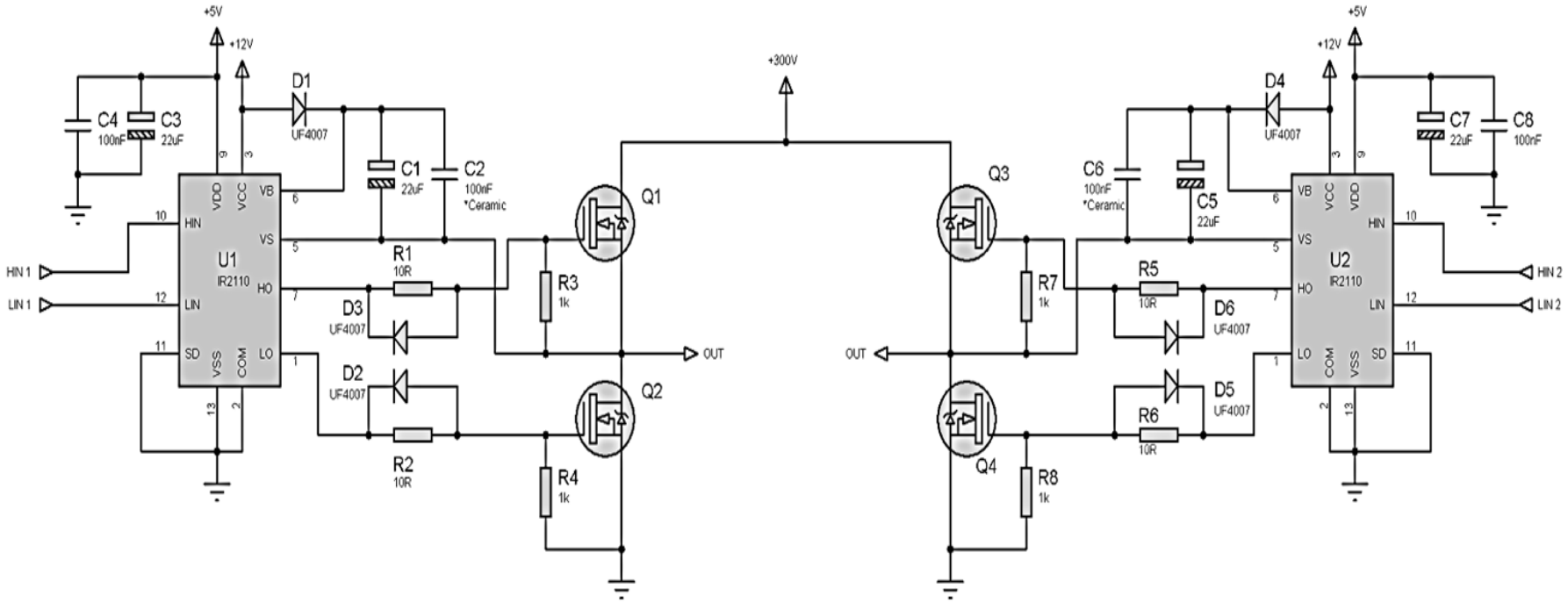



*Fig. 4.16 H-Bridge Inverter with MOSFET Drivers*

### 4.6.2. Gate Driver IC (IR2110)


*Fig. 4.17 IR2110 IC*

In case of single phase H-bridge inverter, two pairs of MOSFET are used where each pair represents high side MOSFETs and low side MOSFETs. The source terminals of low side MOSFETs are grounded. So it is not difficult to create a voltage of 12 volt across gate and source terminals. But in case of high side MOSFETs, the source terminals are not grounded which creates difficulty in creating 12 volt across gate and source to turn the high side MOSFETs on. Thus, for this purpose, a particular type of driver IC is to be used. Among several driver IC, IR2110 as in *Fig. 4.17.* It is one of the famous driver IC found in the market. It requires to be powered to 12 or 15 volt to switch the MOSFET on and off. It can easily control low and high side MOSFET. It only requires a digital 0/5 volt signal as input and it creates the required voltage across gate of MOSFET to turn it on and off. One driver IC is made to control 1 high and 1 low side MOSFET i.e. 1 leg of the bridge. In order to create 12 volt or more in the gate of high side MOSFET with respect to source it uses a bootstrap capacitor. While high side is off, the bootstrap capacitor get charged to the supply voltage, and during turning on process this capacitor is made to get connected across gate and source thus creating the required voltage to turn it on. The capacitor value is to be chosen to suit the time of on state since its charge decreases with time. For fast operation, i.e. short on time period, small value capacitor is enough but for slow switching, high value may be necessary. In this way, driver IC provides easy control over the switching action of MOSFET using simple digital signals. In actual hardware, the inverter output voltage obtained in CRO is shown in *Fig. 4.18.*

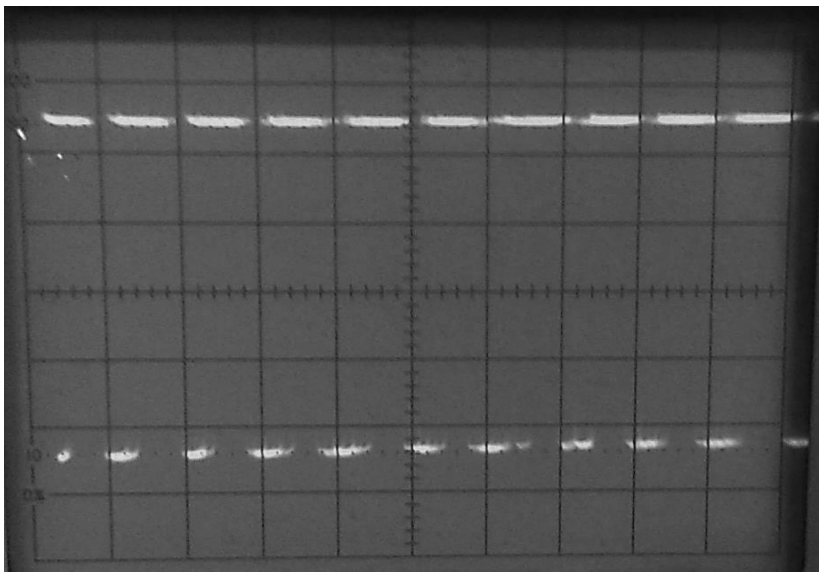


*Fig. 4.18 Inverter output voltage in CRO*

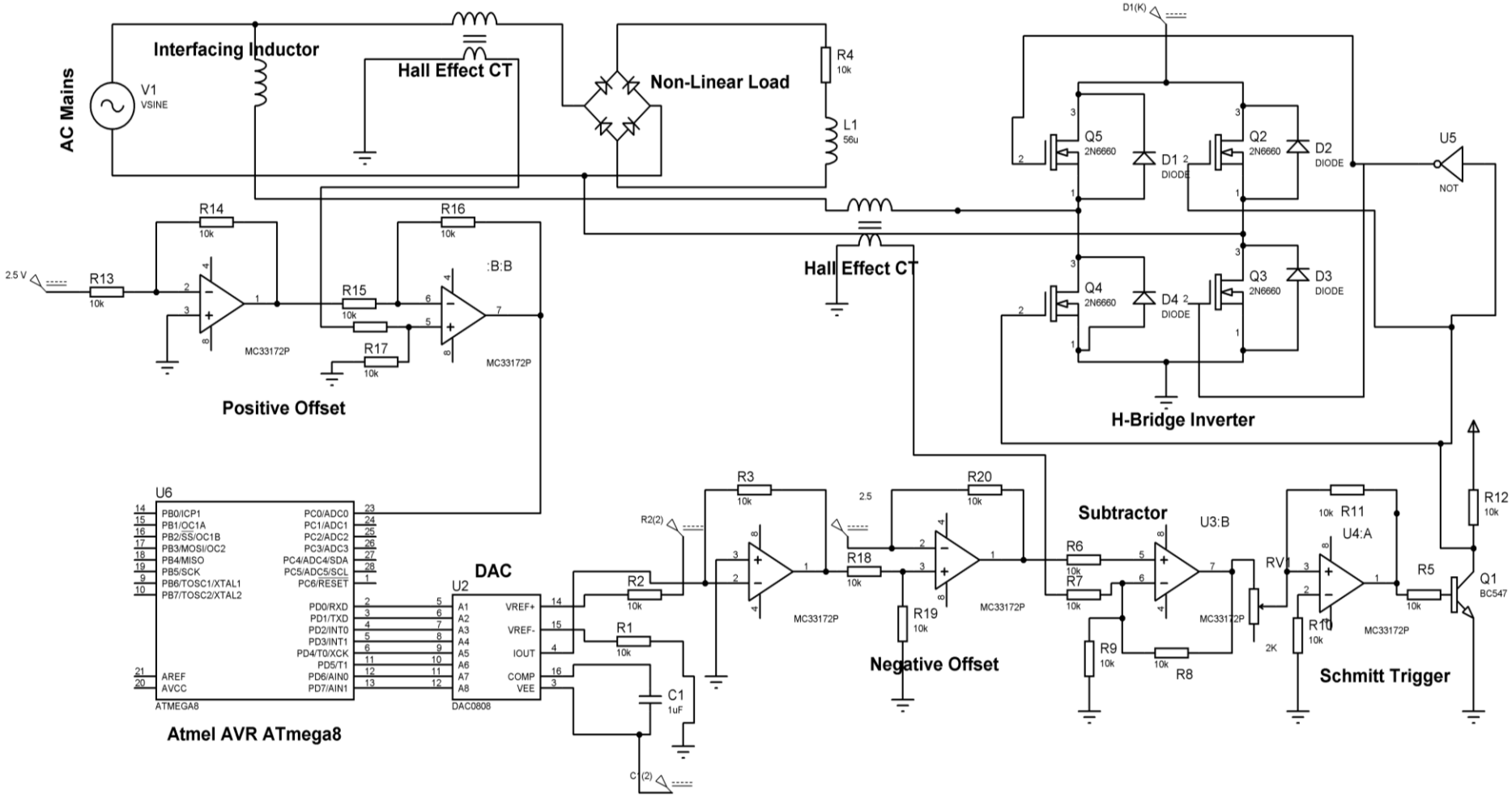



*Fig. 4.19 Overall hardware circuits in Proteus®*

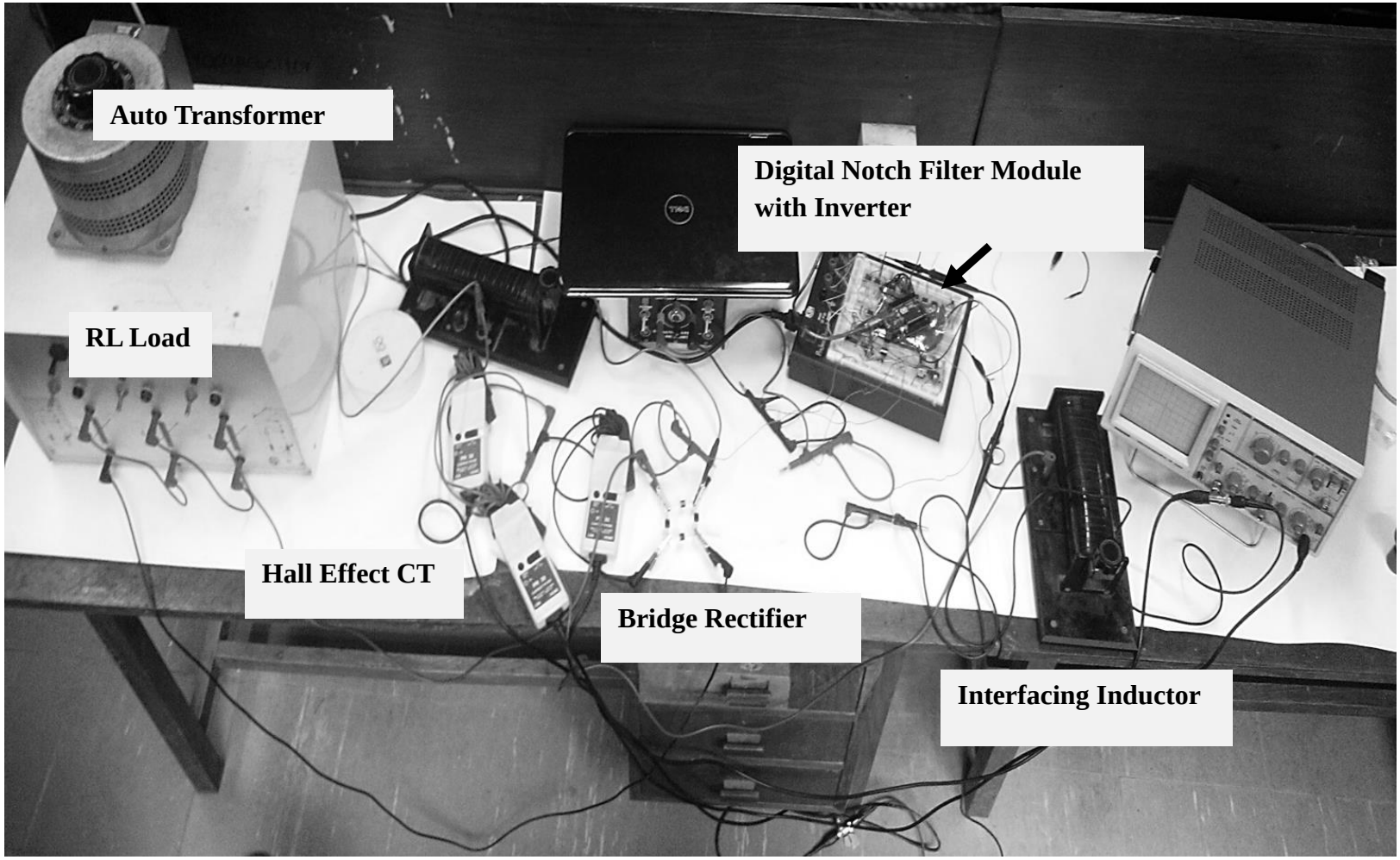



*Fig. 4.20 Overall hardware (In this demonstration, electronic prototyping board (Arduino Uno R3) was used instead of ATmega8 microcontroller)*

## 4.7. Overall Hardware Results

The complete model of the APF was implemented on the hardware as shown in the *Fig. 4.19* with H-Bridge Inverter using MOSFETs instead of IGBTs and Schmitt Trigger circuit as Hysteresis band current controller. Also glimpse of overall hardware for demonstration in shown in *Fig. 4.20* in previous page. A RL load with inductance (L) = 6 H and resistance (R) =30 ohm, fed through the output of full-wave bridge rectifier was used as nonlinear load and 7V ac from auto-transformer was supplied to the rectifier. The digital notch filter implemented on ATmega8 microprocessor, gave total current harmonics as output which was then fed to the hysteresis band current controller consisting of Schmitt trigger with the band of 5%, as reference current. Hysteresis band current controller produced a switching signal to the inverter with constant dc supply of +12V which finally injected the reference current to the grid through interfacing inductor of inductance 75mH and resistance 3.8 ohm. The implementation of this hardware scheme improved the source current THD from 45% to 10%. In the CRO, the waveform of compensated source current is as shown in the *Fig. 4.21*. Likewise, *Fig. 4.22* shows the load current with compensated source current and load current.

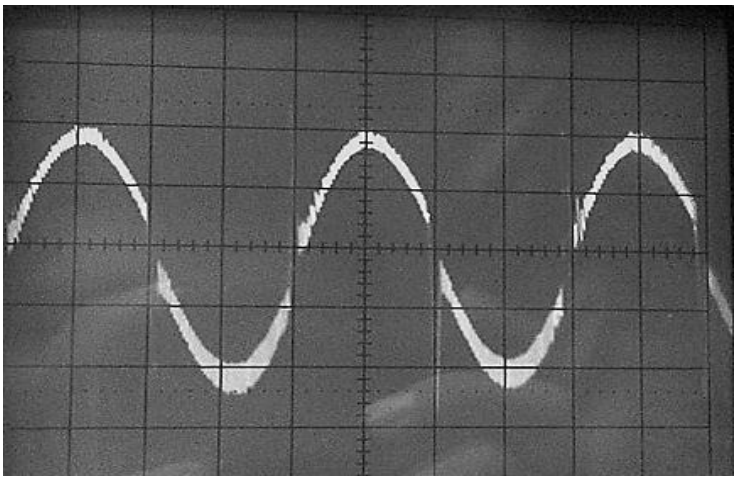


*Fig. 4.21 Compensated source current ($I_S$) by the Shunt APF with a series inductor filter*

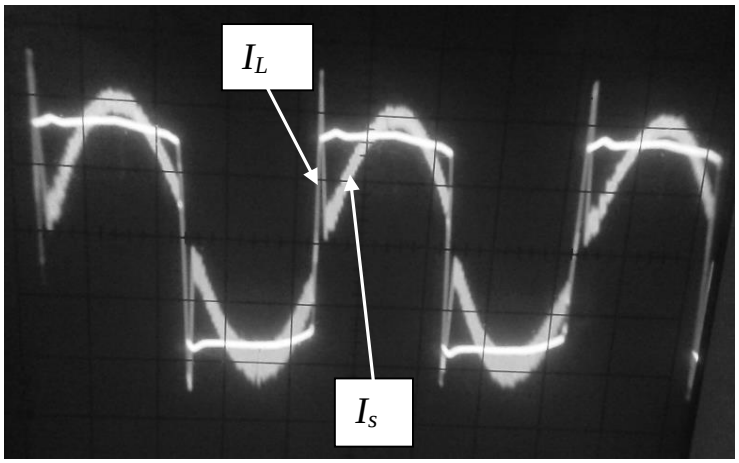



*Fig. 4.22 Load current ($I_L$) and Compensated Source current ($I_S$) by the Shunt APF*

# 5. CONCLUSION

Due to increasing application of power electronics-based (non-linear) loads, the issue of the power quality delivered to the end consumers is of great concern in an electrical power system. Traditionally, power quality problem issues have been dealt with passive LC Filters. To overcome the various drawbacks, active power filters has been developed which provides dynamic and adjustable solutions to the power quality problems. Shunt active power filter is one of the widely used flexible active power line conditioner and its design and fabrication in our project was our objective.

The MATLAB simulation results of our designed system shows its effectiveness and flexibility in improving power quality. In our design, the combination of digital notch filter along with hysteresis band current controller acts as main control part for operation of the APF.

Digital notch filter facilitates us to obtain overall harmonics component in the load current which is reference current that is to be supplied by inverter. Schmitt Trigger has been proved to be a successful circuit in hardware for hysteresis band current control method in which the actual current is tracked within hysteresis band around the reference current. And this combination has served our purpose very well in both simulation and hardware.

The simulation results show the improvement of the source current THD from 34.63% to 5.07% by the implementation of the proposed scheme of shunt active power filter. Also after hardware implementation, we observed source current THD improvement from 45% to 10%. Moreover, its response is instantaneous and adaptive in nature.

So, we can conclude that the design and fabrication of the single phase shunt APF was done successfully by using digital notch filter along with hysteresis band current controller.

# REFERENCES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[4] Phillip A. Regalia, P. P. Vaidyanathan, "The Digital All-Pass Filter: A Versatile Signal Processing Building Block", Proceedings Of The IEEE, Vol. 76, No. 1, January 1988

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# APPENDIX – I

## MATLAB Commands Used

The MATLAB commands that were used for the simulation of the system model are shown below:

### Bode Plot

```
>>bode ([1 0 314^2],[1 25 314^2]),grid
```

### Bilinear Transformation

```
>>[A B]=bilinear([1 0 314^2],[1 25 314^2]),5000)
A =
    0.9975   -1.9911    0.9975
B =
1.0      -1.9911    0.9950
```

### Digital Notch Filter

```
function filter_output = fcn(input_current,sample_instant)
        persistent x_t1 y_t1 y_t2 y_t x_t2;
             x_t1 = 0;
         end
         if isempty(x_t2)
             x_t2 = 0;
         end
         if isempty(y_t1)
             y_t1 = 0;
         end
         if isempty(y_t)
             y_t = 0;
         end
         if isempty(y_t2)
             y_t2 = 0;
         end
        if (sample_instant == 0)
```

```
            y_t = (0.9975*x_t2-
            1.9911*x_t1+0.9975*input_current-
            0.9950*y_t2+1.9911*y_t1);
            y_t2 = y_t1;
            y_t1 = y_t;
            x_t2 = x_t1;
            x_t1 = input_current;
        end
        filter_output = y_t;
end
```

# APPENDIX-II

## AVR ATmega8 Source Code on Atmel Studio®

```
#include <avr/io.h>
#include <avr/interrupt.h>
long int xn,xn_1=0,xn_2=0, yn_=0,yn_1=0,yn_2=0,
ytemp1,ytemp2,ytemp3;
ISR (TIMER1_COMPA_vect)
{
      ADCSRA|=(1<<ADEN)|(1<<ADSC);
      while(ADCSRA &(1<<ADSC));
      xn=ADCH;
      xn=(xn<<8);
      ytemp1=(16343*xn_2 -32622*xn_1 +16343*xn -16302*yn_2
      +32622*yn_1);
      /*Scaled by multiplying factor 2^14*/
      ytemp1=(ytemp1>>14);
      ytemp2=ytemp1;
      PORTD=(ytemp1>>8);
      xn_2=xn_1;
      xn_1=xn;
      yn_2=yn_1;
      yn_1=ytemp2;
}

int main(void)
{
      DDRD=0XFF;  //port D as output.
      sei();
      TCCR1B|=(1<< WGM12)|(1 << CS11)|(1 << CS10);
      //PS=64 & CTC mode
      OCR1A = 49;
      // initialize compare value
      TIMSK |= (1 << OCIE1A); // enable compare interrupt
      ADCSRA|=((1<<ADEN)|(1<<ADPS1)|(1<<ADPS0));
```

```
        //enable ADC n Prescalar to 8
        ADCSRA&=~((1<<ADPS2)|(1<<ADIE));
        //adc interrupt disable ADMUX|=((1<<REFS0)|(1<<ADLAR));
        /*AVcc with external capacitor at  AREF//left justified
        result*/
        ADMUX&=~((1<<MUX3)|(1<<MUX2)|(1<<MUX1)|(1<<MUX0));
        /*Channel select PC0 PIN 23*/
        /*after initialization it is recommended to get "dummy
        reading" so that to test ADC*/
        ADCSRA|=(1<<ADSC);
        while(ADCSRA & (1<<ADSC));
        ADCSRA&=~(1<<ADEN);
        while(1)
        {
        }
}
```