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Team Number: 8	Implementation of R-2R Ladder using Operational Amplifier
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Team Members:

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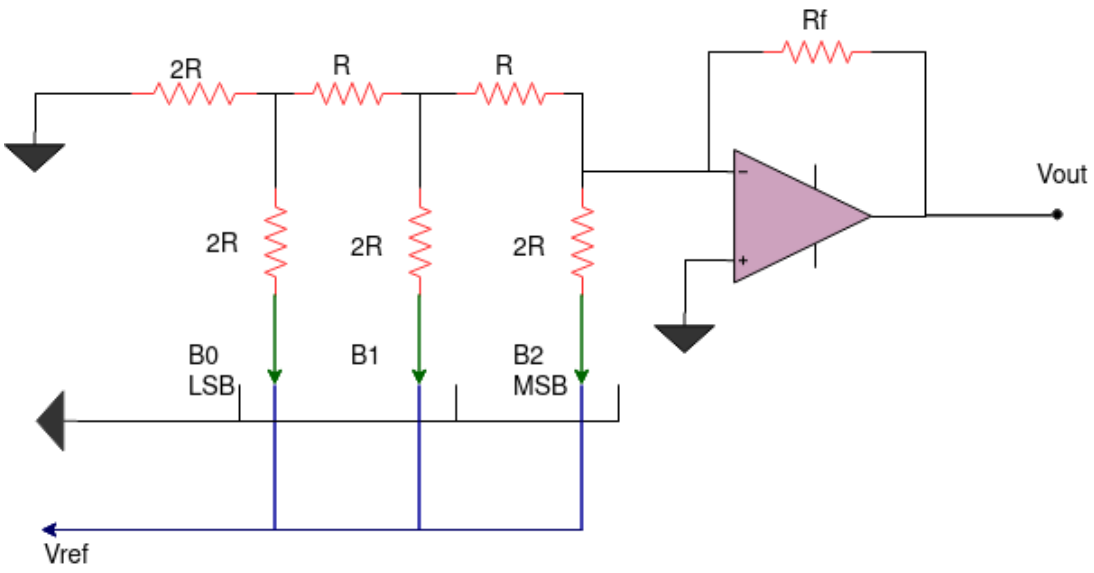
Objective:

To implement the R-2R ladder using OpAmp with cadence virtuoso- 64 software.

Software Required:

Cadence Virtuoso, gpdk180

THEORY:



The binary-weighted DAC is appropriate for DACs with low resolving power. This is because it requires a wide range of precise resistors to perform error-free operations for high-order DACs. It is impossible to maintain the accuracy of the weighted DACs and is expensive. This leads to the R-2R ladder technique, which implements only two resistors for DAC functionality for every digital bit.

The R-2R configuration is a simple arrangement that consists of parallel and series resistors connected in cascaded form to an operational amplifier. We can use an operational amplifier in inverting or non-inverting form, depending on the polarity of the output voltage that we want to get from the DAC. R-2R ladder resistors act as voltage dividers along with the entire network, with the output voltage dependent on the input voltages.

Procedure:

i) Launch Cadence

1. Create a Folder: Go to your desktop and create a new folder with your reg. no. as the folder name.

2. Open Terminal: Navigate into the folder you just created. Right-click inside the folder and select the option to open a terminal here.

3. Switch to C Shell: In the terminal window, type `csh` and press Enter.

4. Source the Environment File: Next, type `source /cad/cshrc` and press Enter.

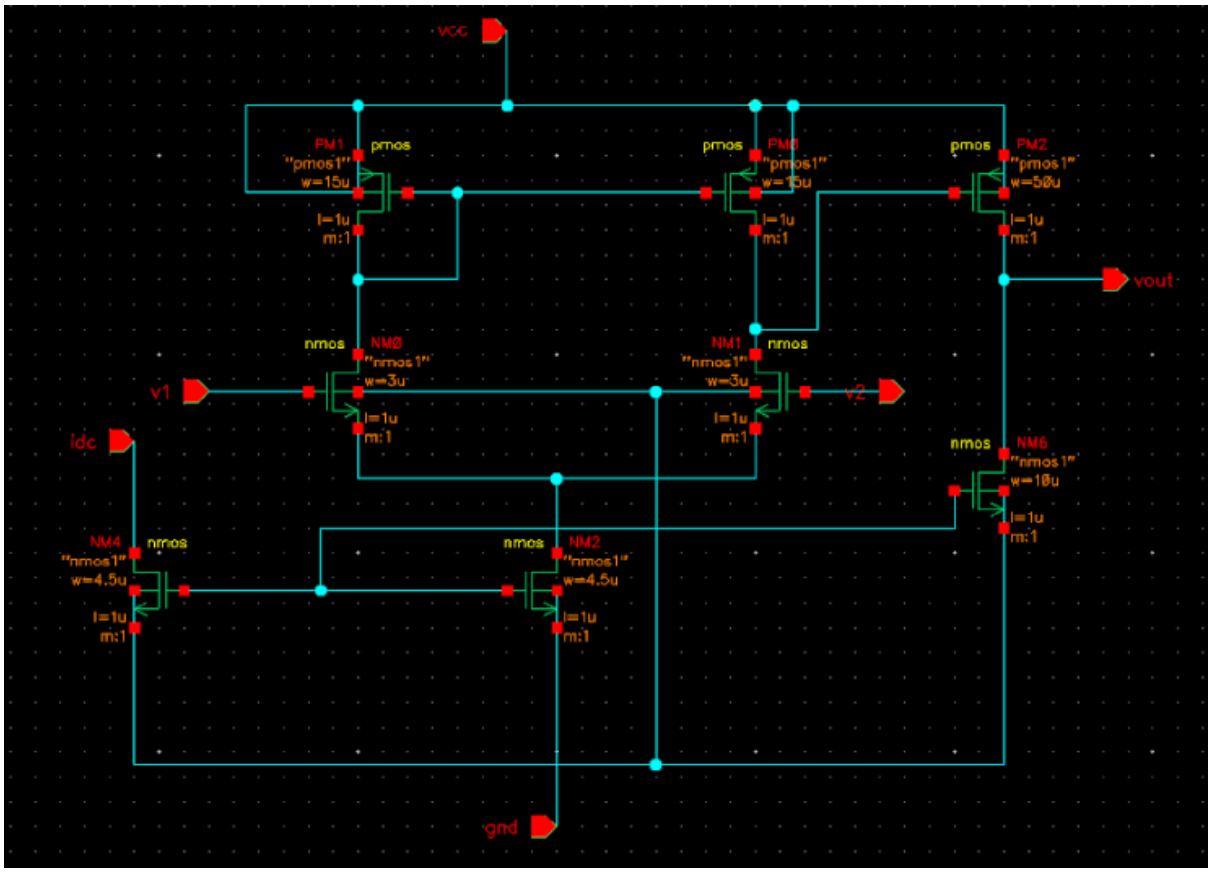
5. Launch Virtuoso: Finally, type `virtuoso &` and press Enter to launch the Cadence Virtuoso software.

ii) Virtuoso:

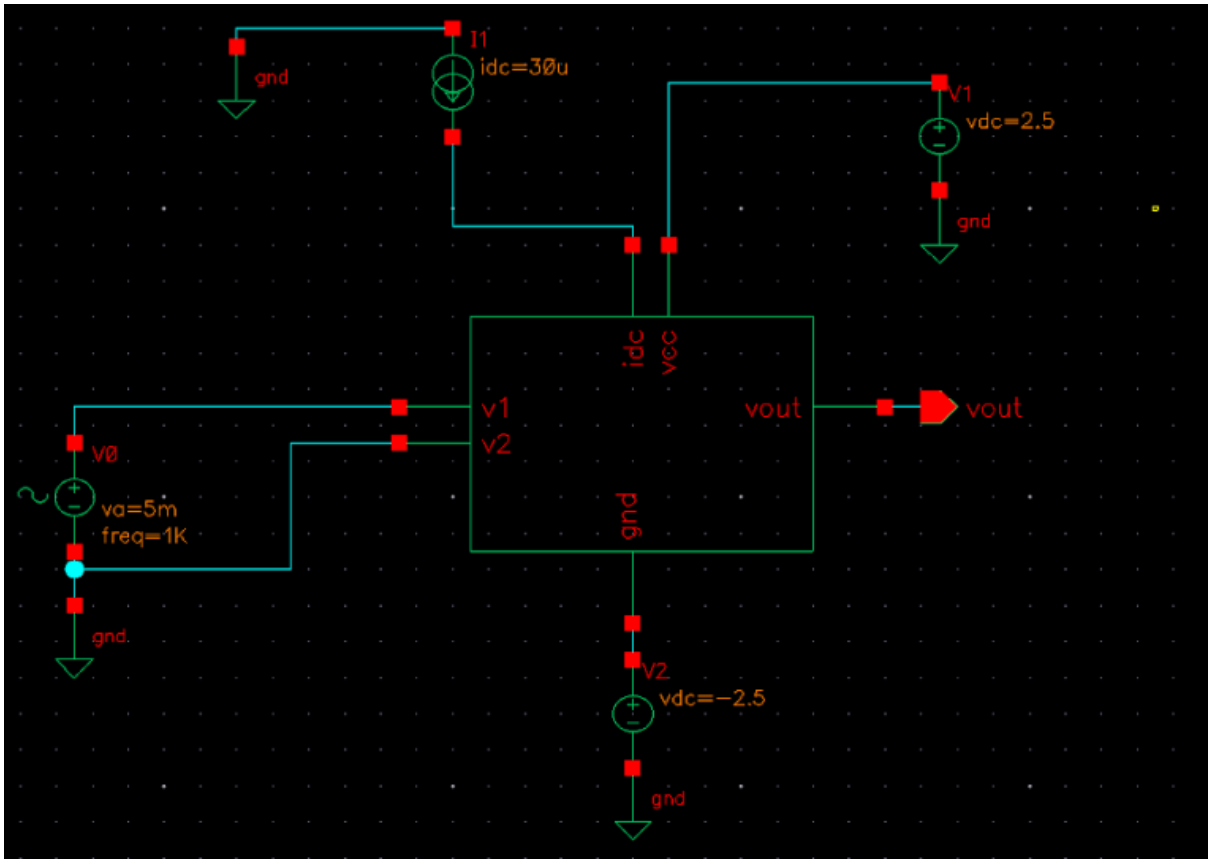
• Open schematic window in virtuoso.
• Draw the circuit diagram required using components from different libraries.
•Use NOT symbol created previously.
• Set the Vdc value as V=1.8V. Save project and check for errors.
• Go to launch > ADE L > Stimuli and enter the following :
• One value = 1.8
• Zero value = 0
• Rise time = 1n
• Fall time = 1n
• Period = 100n
• Bit pattern = I0:1000; I1:0100; I2:0010; I3:0001; S1:0011; S0:0101.
• In Analysis, choose trans analysis and give stop time as 800n.
• Select outputs to be plotted.
• Run the project and observe the timing diagram.

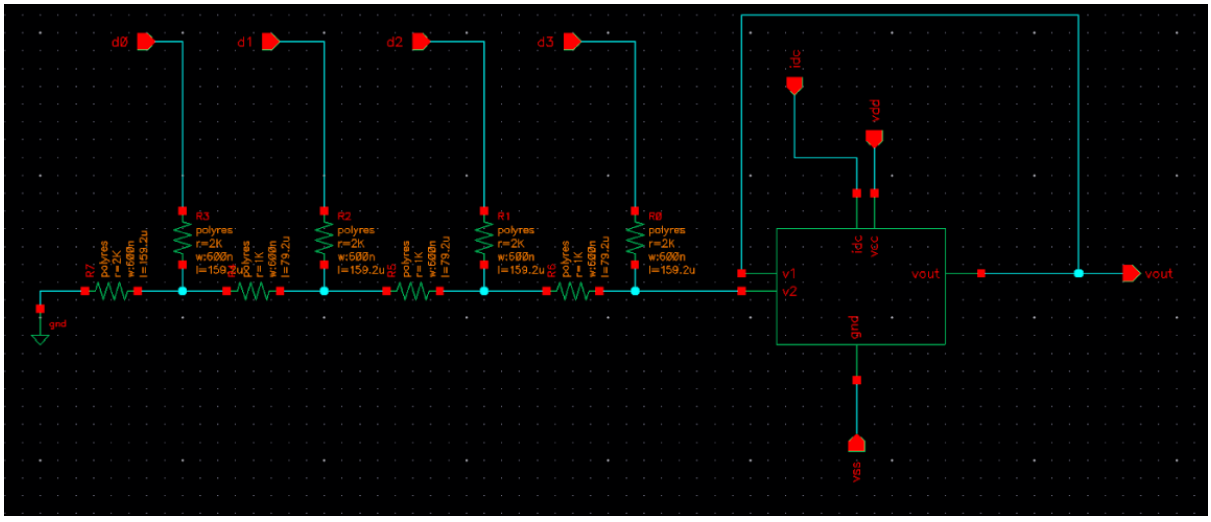
SCHEMATIC:

Two-stage differential OpAmp

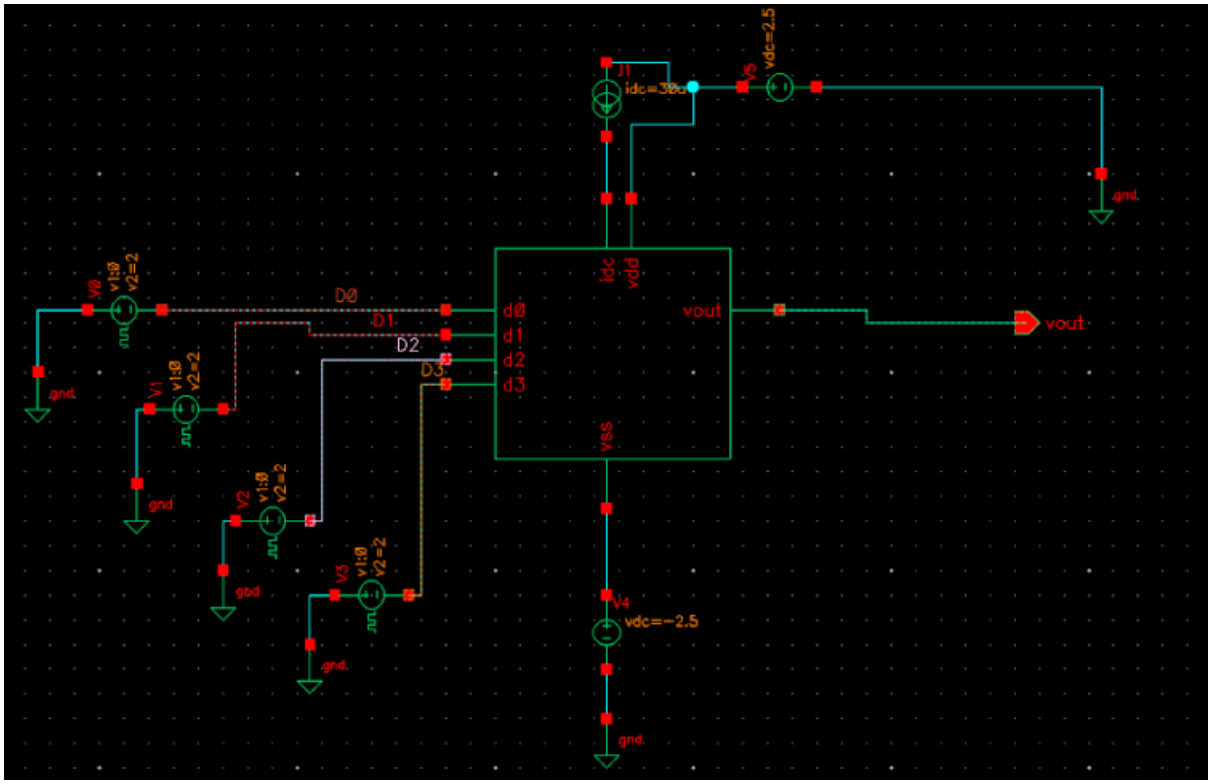


R-2R Ladder using OpAmp

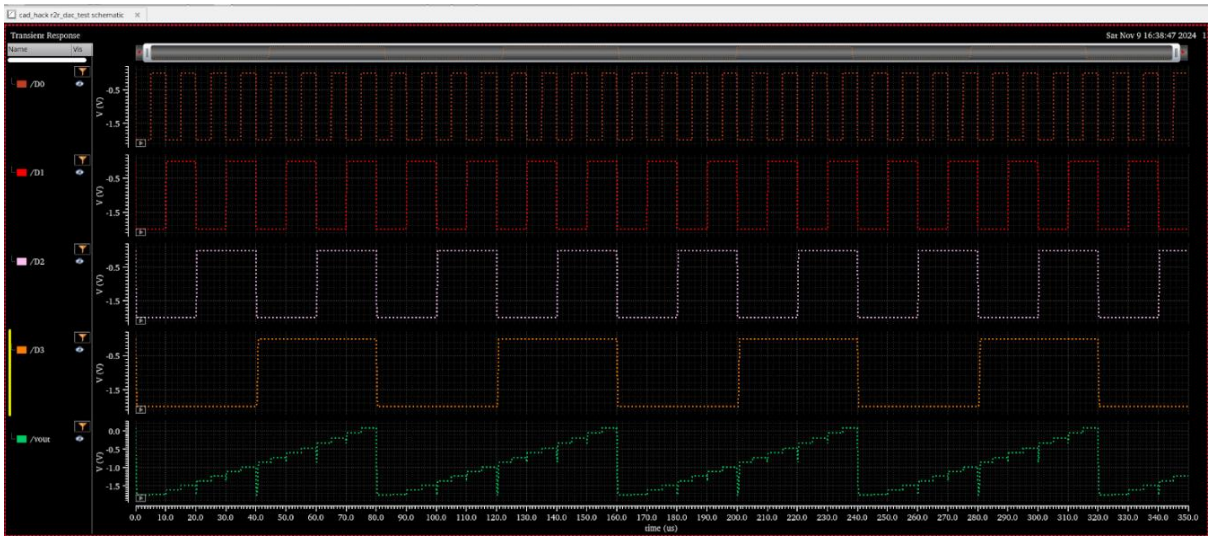




DAC Using R-2R Ladder



OUTPUT:



RESULT:

Hence, DAC using R-2R ladder was designed and verified successfully.