A Noval 13-Level Inverter Topology with Reduced Components Count and Build-in Self-Balancing Capability for EV Applications

***Abstract*— A new dual T-type 13-level inverter topology is developed in our project.**

The traditional multilevel inverter topologies, such as neutral point clamped, flying capacitor, T-type and cascaded H-bridge inverters employs more no of switches, gate drivers and diodes to produce the 13-level output. In our proposed inverter topology, there are no additional circuits to equalize the voltage of capacitors present in each pole. Hence the reduction in number of switches, driver circuits, modulation strategies and balancing circuits leads to reduction of cost and power losses in the proposed topology, makes it much more suitable for EV applications. The proposed topology performance was simulated and efficiency and THD performance parameters verified with experimental results.

***Index Terms*—High efficiency, multilevel inverter (MLI), nearest level modulation (NLM), total harmonic distortion (THD).**

I. INTRODUCTION

MULTILEVEL inverters (MLIs) are today an attractive alternative to conventional two-level inverters (TLIs) in medium voltage electrical power transmission and high-speed drives. MLI topologies in general feature a reduced distortion of output ac voltages and currents than TLI operating at the same switching frequency, as well as lower voltage gradients, lower switching stresses and lower switching power losses. Furthermore, MLI is effective in reducing transient overvoltage at the terminals of motor windings, harmonic losses in the cables, common mode disturbance currents and power losses on grid side sine-filters. On the other hand, MLI requires a higher number of power switches than conventional TLI, although with lower voltage ratings. This is a key disadvantage of MLI topologies because the higher the number of power switches, the higher the cost and circuital complexity. Progress in semiconductor technology led to availability of low-cost.

High-power switches, making possible the realization of very efficient MLI based on traditional topologies, such as neutral point clamped (NPC), T-type, flying capacitor (FC), cascaded H- bridge (CHB), modular multilevel inverter, or their derivatives. On any kind of MLI the smaller the amount of output voltage levels, the higher the output voltage and current total harmonic distortions (THD) indexes achieved for a given switching frequency. Therefore, on simpler and cheaper MLI, operating at low switching frequency and with a small number of output voltage levels, quite high THD occurs, leading to additional power losses and torque oscillations in the case of electric motor drives. Several possible solutions have been proposed to improve the output current THD_i on MLI. Among them, line reactors and tuned harmonic filters are simple passive measures, which gained popularity because of the low cost, even if they are poorly flexible and could generate resonance issues. Active techniques based on the injection of suitable current harmonics by auxiliary converters are more expensive but provide an effective harmonic attenuation, as well as some additional functions such as power factor correction. MLI can also benefit from high switching frequency pulse width modulation (PWM) strategies, although at the cost of increased switching losses. MLI using open-end winding configurations have been recently also developed, where the ac machine is fed by two separate power converters sharing the load, to improve the harmonic content of phase voltages and currents. Such an approach produces a lower stator current distortion than conventional MLI topologies switching at the fundamental frequency, while requiring less power switches than PWM multilevel inverters featuring the same THD.

A distinct disadvantage of MLI over TLI is that the more output voltage levels, the more power switches are required. Hence, a large effort has been exerted in last years to develop special topologies with a reduced power switch count.

Among them, 13-levels topologies have been developed to reduce the 24 power switches per pole required on conventional 13-levels NPC, T-Type and FC inverters. A 13-level inverter has been presented using only nine power switches per pole. However, ten isolated dc power sources are required, achieving only limited benefits in terms of complexity of the system, cost, and size. Other reduced switch count 13-level inverters have been proposed in and featuring respectively 14, 13, 11, and 16 power switches per pole, while a 13-Level Switched-Capacitor Inverter with a single dc source has been proposed in featuring 3 capacitors and 15 power switches per pole. In this case, a suitable capacitor voltage control strategy is necessary to balance the capacitor voltages. An envelope type modular inverter has been proposed featuring only ten power switches per pole, although requiring four isolated dc power sources.

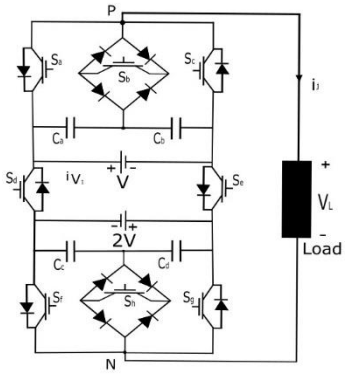

Fig. 1. Pole of the 13-LDT topology.

Finally, a 13-level inverter with self-balanced switched-capacitor has been investigated in consisting of two series connected 7-level modules, requiring 16 power switches per pole.

This article presents a novel asymmetrical 13-level dual T-type (13-LDT) inverter topology featuring only eight power switches per pole, and two isolated power sources, thus requiring less power switches, gate drivers, and diodes, than 13-level inverters based on traditional and previously developed reduced switch count topologies. A key feature of the proposed topology is that it does not need any additional circuit to stabilize the voltage of the four capacitors equipping each pole, leading to a reduction of circuital complexity and cost. A detailed analysis of the proposed topology is provided in the article, as well as a comparison with standard and reduced switch count 13-level configurations. As confirmed by simulation and experimental tests, the proposed 13-LDT inverter operated at low switching frequency according to the nearest level modulation (NLM) technique, achieves high efficiency and low output voltage THDs.

II. The Proposed 13-LDT Topology

A pole of the proposed 13-LDT topology encompasses eight switches, as shown in Fig.1. It consists of two three-level T-type sections, two isolated dc voltage sources V, $2V$, four capacitors C_a, C_b, C_c, C_d and two switches S_d and S_e. Each T-type section includes two bidirectional switches S_b and S_g which consist of an IGBT embedded in a diode bridge. This configuration has the advantage of reducing the complexity of the system and its cost compared to common-collector or common-emitter solutions. The disadvantage is that three devices are conducting whenever the switch is turned on. In this article, it was decided to minimize the cost since the losses are already low thanks to a low frequency modulation. For the safe operation of the proposed structure,

the couples of switches (S_a, S_b), (S_a, S_c), (S_b, S_c), (S_d, S_e), (S_f, S_g), (S_f, S_h), and (S_g, S_h) are operated with a suitable dead time to prevent short-circuiting of the dc voltage sources.

If the ratio between the voltage sources changes, the number of output voltage levels varies from 9 to 17.

TABLE I
13-LDT Inverter Pole Switching Configurations

SC	S_a	S_b	S_c	S_d	S_e	S_f	S_g	S_h	Vo
1	1	0	0	0	1	1	0	0	3V
2	0	1	0	0	1	1	0	0	2.5V
3	0	0	1	0	1	1	0	0	2V
4	1	0	0	0	1	0	1	0	
5	0	1	0	0	1	0	1	0	1.5V
6	1	0	0	0	1	0	0	1	V
7	0	0	1	0	1	0	1	0	
8	0	1	0	0	1	0	0	1	0.5V
9	0	0	1	0	1	0	0	1	0
10	1	0	0	1	0	1	0	0	
11	0	1	0	1	0	1	0	0	-0.5V
12	0	0	1	1	0	1	0	0	-V
13	1	0	0	1	0	0	1	0	
14	0	1	0	1	0	0	1	0	-1.5V
15	1	0	0	1	0	0	0	1	-2V
16	0	0	1	1	0	0	1	0	
17	0	1	0	1	0	0	0	1	-2.5V
18	0	0	1	1	0	0	0	1	-3V

More specifically, for the voltage ratio equal to 1/1, 2/1 and 3/1, the corresponding voltage levels generated by the inverter at its output are respectively, 9, 13, and 17. However, by increasing the voltage ratio, the voltage stress on power switches S_f, S_g, and S_h increases, generating an uneven power losses distribution. A good tradeoff between THD, distribution of power losses and number of output voltage levels is achieved by considering 13 voltage levels. Thus, the two dc voltage sources are set at V and $2V$, and C_a, C_b, C_c, C_d voltages are set respectively at $0.5V$, $0.5V$, V, V. Table I and Fig. 2 deal with 13-LDT pole switching configurations and corresponding output voltage V_o. Redundant switching combi- nations exist, named as: 3-4, 6-7, 9-10, 12-13, and 15-16, which generates same output voltage.

Switches S_d and S_e are operated at the fundamental frequency, to determine the polarity of the output voltage V_o. When S_d is OFF and S_e is ON, the output voltage V_o is positive. Otherwise, the output voltage is negative. Zero-voltage level is obtained by turning on S_c, S_e, S_h or S_a, S_d, S_f.

Pole modules can be connected according to a wye, or an open-end winding configuration, to realize a 13-LDT three-phase inverter, as shown in Fig. 3.

Several multilevel modulation techniques have been developed with the goal to achieve the lowest possible THD. They can be divided into two categories, low switching frequency modulation techniques and high frequency PWM. In general, low switching frequency modulation techniques face output voltage THD issues by increasing the number of output voltage levels, while the use of high frequency PWM techniques yield to an increase of the switching frequency; some hybrid approaches have been also presented in the literature. The low switching frequency modulation techniques feature a quite low number of switching events per period of the output

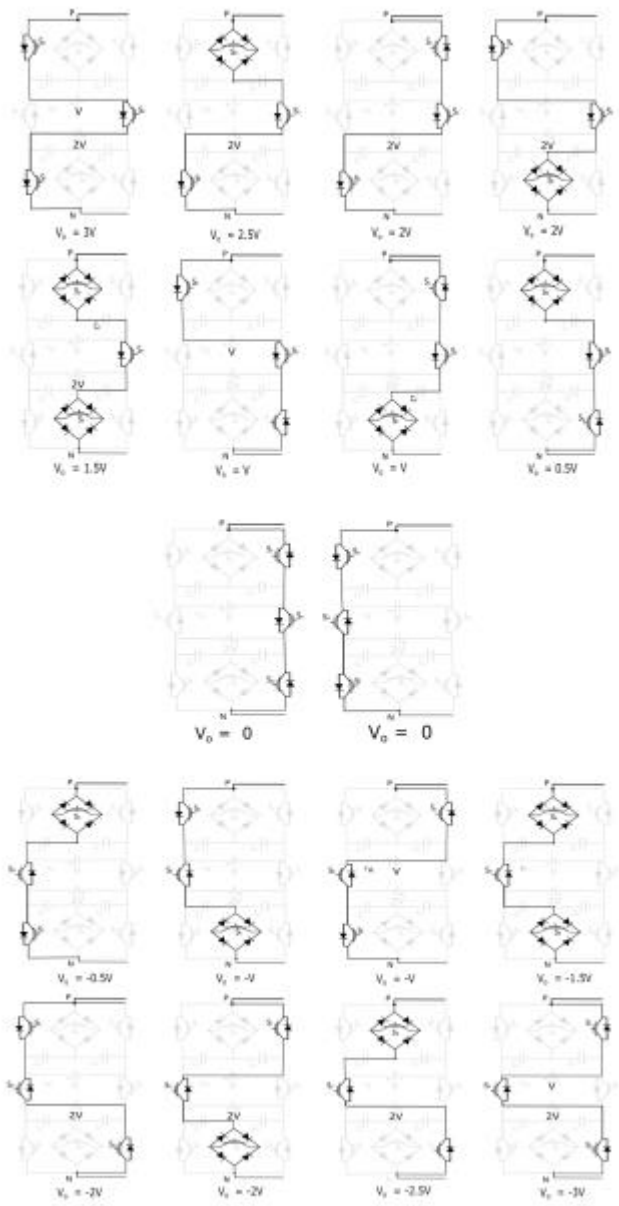

Fig. 2. 13-LDT inverter pole switching configurations.

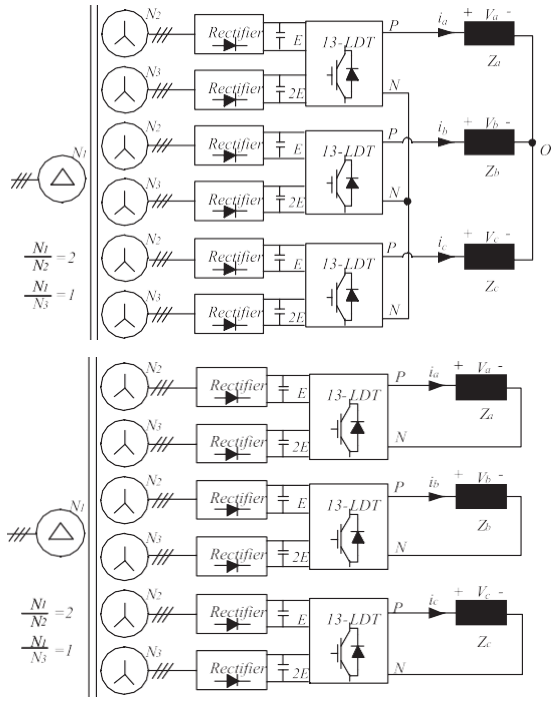

Fig. 3. 13-LDT three-phase configurations: up) wye, down) open-end winding.

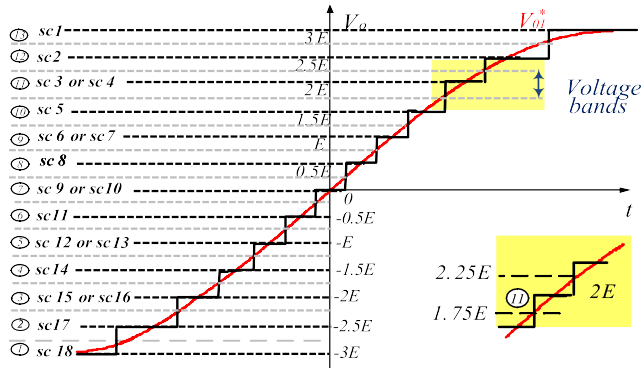

Fig. 4. 13-LDT NLM: voltage bands and switching table.

voltage, leading to lower switching power losses. Among the numerous modulation strategies, the selective harmonic elimination (SHE) and NLM have been implemented in the 13-LDT inverter.

SHE is a well-known technique which achieves the elimination of specific low-order harmonics from the output voltage waveform by suitably selecting the firing angles of power switches. These are determined by solving a system of trigonometric equations carried out from the Fourier expansion of the inverter output voltage waveform. The higher number of firing angles managed per period, the higher the number of harmonics eliminated, but also the higher the number of equations to be solved. On-line processing these equations is computationally intensive, thus, firing angles are offline precomputed and stored in a look-up table. A hybrid SHE-PWM technique has been also proposed in for a multilevel open-winding inverter structure.

In the NLM strategy the inverter switching pattern is selected to generate the output voltage as close as possible to the reference fundamental phase voltage V_{01}^*. Fig. 4 displays the voltage levels in case of the 13-LDT topology, where 12 voltage bands are defined, each one located around one of the 13 possible levels of the output phase voltage. The inverter switching configuration is then selected according to the switching pattern of Fig. 6, by detecting in which of the 13 bands falls the actual reference voltage V_{01}^*.

The ratio between the magnitude of the output voltage fundamental harmonic V_{o1} and the maximum output voltage ($3V$) has been determined by simulation as function of the modulation

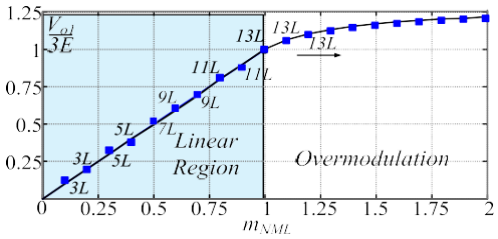

Fig. 5. 13-LDT NLM: $V_{01}/3E$ vs. modulation index m_{NML}.

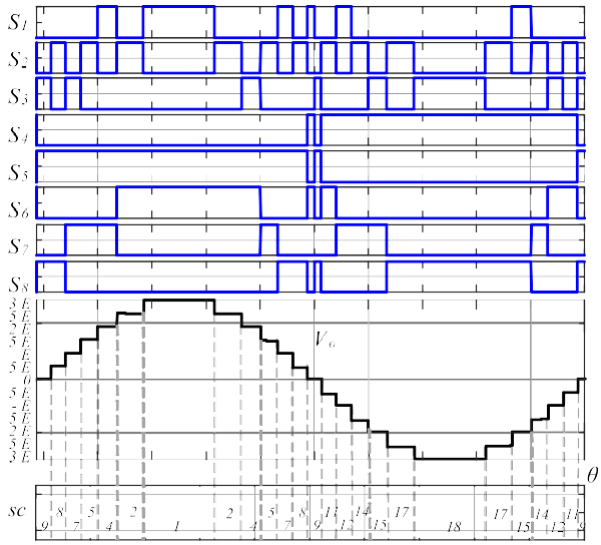

Fig. 6. 13-LDT NLM: Switching pattern and output voltage V_o.

index m_{NLM}, which is defined as the ratio between the magnitude of the reference output voltage V_{01}^* and the maximum output voltage. As shown in Fig. 5, a linear relationship exists for $m_{NLM} \leq 1$, while a nonlinear behavior occurs for higher values of the modulation index, due to overmodulation. The amount of voltage levels used by NLM is a function of the modulation index, as the amount of voltage levels used to synthesize the reference voltage increases with the increase of m_{NLM}. While three voltage levels are used for low m_{NLM}, this number progressively increases up to reaching thirteen levels for m_{NLM} close to 1. The switching pattern related to a fundamental period T_o of V_{01}^* at unitary m_{NLM} is shown in Fig. 6. The number of switching events occurring in T_o differs from device to device, leading to different switching frequencies, which vary with m_{NLM}, as shown in Fig 7. The THD is also affected by m_{NLM}, as shown in Fig. 8. However, the NLM features a lower THD_v compared to SHE for almost the entire linear modulation index interval.

III. Capacitor Voltages Self-Balance

Two pairs of capacitors, C_a, C_b, and C_c, C_d are present in a pole of the 13-LDT inverter. The voltage at the terminals of each pair of capacitors is determined by the two dc power sources. A key feature of this topology is the automatic balancing of the voltage between each pair of capacitors, leading to achieve

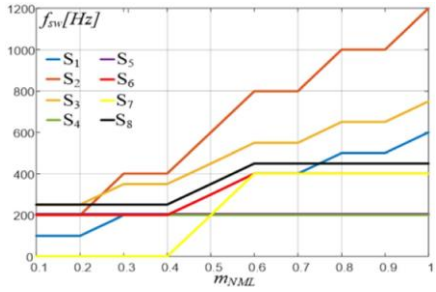

Fig. 7. Switching frequency of 13-LDT devices versus m_{NML} (f_o = 50 Hz).

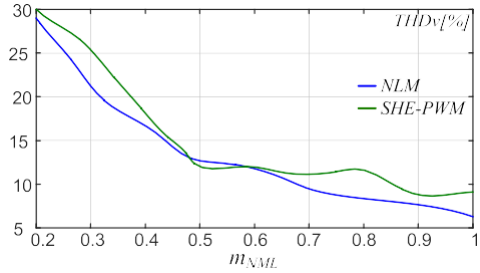

Fig. 8. Output voltage THDv versus m_{NML}.

TABLE II
Switching Combinations vs. Capacitor Currents

SC	V_o	i_{ca}	i_{cb}	i_{cc}	i_{cd}	$i_o > 0$		$i_o < 0$	
						Discharge	Charge	Discharge	Charge
1	3V	0	0	0	0	/	/	/	/
2	2.5V	i_o	$-i_o$	0	0	C_b	C_a	C_a	C_b
3	2V	0	0	0	0	/	/	/	/
4		0	0	i_o	$-i_o$	C_d	C_c	C_d	C_c
5	1.5V	i_o	i_o	$-i_o$	$-i_o$	C_bC_d	C_aC_c	C_aC_c	C_bC_d
6	V	0	0	0	0	/	/	/	/
7		0	0	i_o	$-i_o$	C_d	C_c	C_c	C_d
8	0.5V	i_o	$-i_o$	0	0	C_b	C_a	C_a	C_b
9	0	0	0	0	0	/	/	/	/
10									
11	-0.5V	$-i_o$	$-i_o$	0	0	C_b	C_a	C_a	C_b
12	-V	0	0	0	0	C_d	C_c	C_c	C_d
13		i_o	$-i_o$	0	0	/	/	/	/
14	-1.5V	$-i_o$	i_o	$-i_o$	i_o	C_bC_d	C_aC_c	C_aC_c	C_bC_d
15	-2V	0	0	0	0	/	/	/	/
16		0	0	i_o	$-i_o$	C_d	C_c	C_c	C_d
17	-2.5V	i_o	$-i_o$	0	0	/	/	/	/
18	-3V	0	0	0	0	C_a	C_b	C_b	C_a

null average capacitor currents in each fundamental period T_o, without using extra circuits or special modulation techniques. In fact, according to Table I and Fig. 2, the capacitors C_a, C_b, C_c, C_d are charged and discharged when the inverter takes specific switching configurations (*sc*), as shown in Table II. Due to the symmetry of the output voltage waveform in a fundamental period T_o, positive and negative voltage levels feature same magnitude at steady state, for the same amount of time, leading to null average capacitors currents. As an example, Fig. 9 shows the current i_{Ca} of the capacitor C_a for m_{NLM} = 1. i_{Ca} is mirrored in the second half of the fundamental period with respect to the first half period, leading to a null integral over T_0 (charge

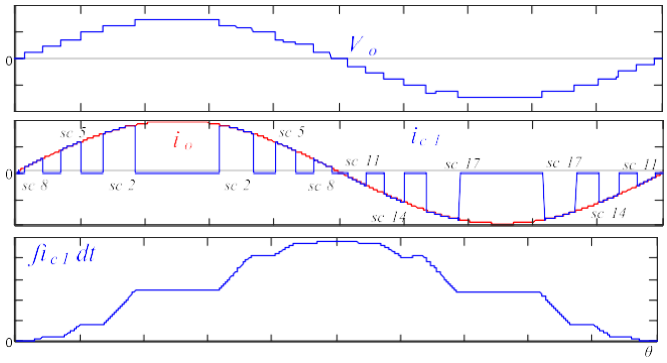

Fig. 9. Steady state: Output voltage V_o, i_{c1}, and integral of i_{c1} ($m_{NLM} = 1$).

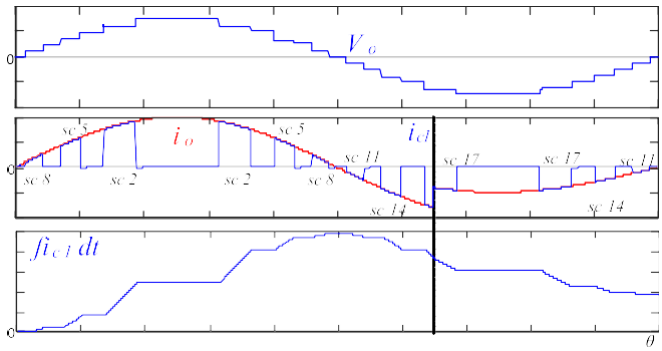

Fig.10.Load change: output voltage V_o, i_{ca}, and integral of i_{Ca} ($m_{NLM} = 1$).

balance). At steady state, the voltage v_{c1} of the capacitor C_a in T_0 is given by

(1)

$$v_{Ca} = v_{Ca(0)} + \frac{1}{C}\int_0^{2\pi} iC1 d\theta$$

As a consequence, the average voltage value of C_a is constant at steady state. However, changes in modulation index or load can cause small voltage unbalances because of different charging and discharging times during transients, as shown in Fig. 10. Small variations of capacitors voltages do not significantly impair the performance of the inverter, as a voltage balance is automatically accomplished when the inverter takes switching configurations in which C_a, C_b (sc8&sc11) or C_c, C_d (sc7 & sc12) are charged/discharged. For example, when the inverter output voltage falls inside the band 8, the switching configuration sc8 is selected, then, if $i_O > 0$, C_a is charged and C_b is discharged. As shown in Fig. 11 the lower/higher is v_{c1} than v_{cb} and the more/less C_a is charged and C_b is discharged, hence reducing the voltage unbalance. A simulation of the automatic correction of a voltage unbalance is shown in Fig. 12.

The ripple Δv_C superimposed to the dc capacitor voltages is depending on the value of capacitance C, modulation index

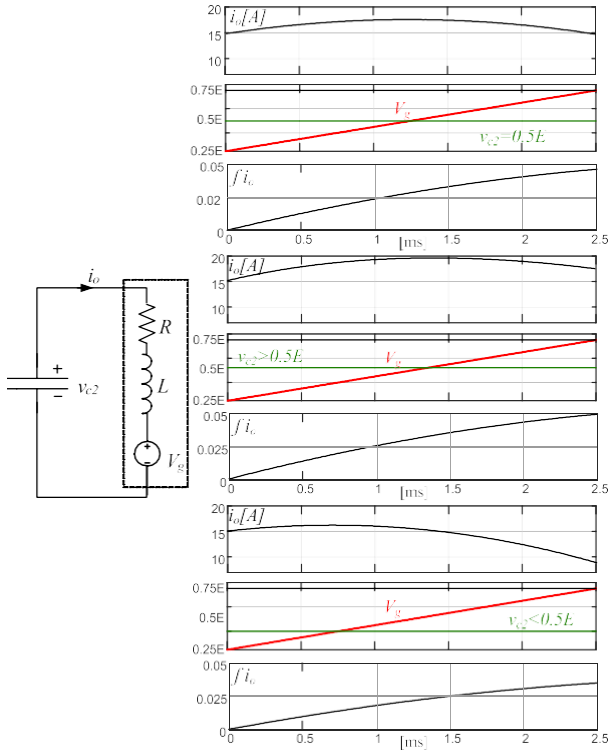

Fig. 11. (left) Equivalent circuit of a single inverter pole, for sc8. (right) i_0, v_g and $\int i_0$, for $v_{c2} = .5V$, $v_{c2} > .5V$ and $v_{c2} < .5V$.

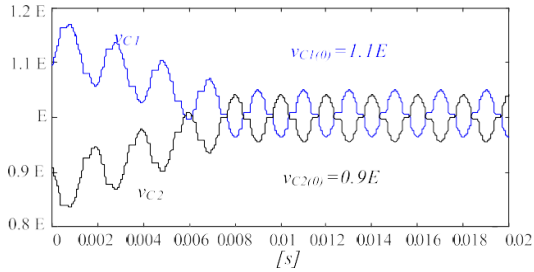

Fig. 12. Self-equalization at the terminals of capacitors C_a, C_b, starting from an unbalanced condition.

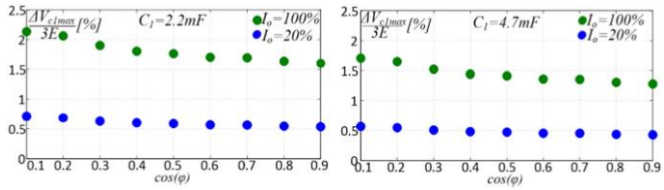

Fig. 13. Estimated voltage ripple on C_a versus power factor for $I_0 = 20\%$ and $I_0 = 100\%$. (a) $C = 2.2$ mF. (b) $C = 4.7$ mF.

m_{NLM}, load current I_o and phase shift ϕ. Fig. 13 shows the estimated voltage ripple carried out from simulations, performed considering the system specifications given in Table III. A light

TABLE III
SIMULATION PARAMETERS

Rated Power [kVA]	*E_n [V]*	*I_n [A]*	*C_n [mF]*	*f_n [Hz]*
42	*400 V*	*50*	*2.2*	*50*

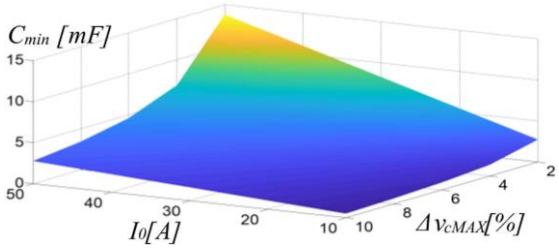

Fig. 14. C_{min} versus I_o and Δv_{CMAX}.

a larger variation occurs as the load current increases but still remains below the 2.5%. The minimum capacitance value C can be established by imposing a limit to the voltage ripple Δv_{CMAX}:

$$C_{min} = \frac{1}{\Delta v_{CMAX}} \max \int_0^{2\pi} i_C d\vartheta - \min \int_0^{2\pi} i_C d\vartheta \quad (2)$$

where i_c is the current flowing through each capacitor.

Fig. 14 deals with C_{min} versus I_o and Δv_{CMAX}. The higher the load current, the higher the capacitance required to limit the capacitor voltage ripple for a given load current I_o.

IV. 13-LDT Versus Other 13-Level Topologies

A comparison between the proposed 13-LDT and other 13-levels topologies can be played in terms of THDs, amount of power switches N_{sw}, gate drivers N_{gd}, capacitors N_{Cap}, power diodes N_{diod}, dc power supplies N_{dc} and total standing voltage (TSV). conventional NPC, T-Type, CHB, FC 13-level inverters presented have been considered in the following comparison.

A. Total Harmonic Distortions

Whenever all configurations are driven by NLM, same THD*v* of the output voltage is obtained for any load condition. Differently, the THD*v* value changes with the type of modulation technique. Table IV gives the THDs of voltages and currents evaluated simulating the topologies presented in with their respective modulation strategies and with the system specifications given in Table III.

The THDs have been calculated taking up to 49th-order of harmonics. The switching frequency is set at 5 kHz in case of PWM modulation, while 50 Hz is considered for NLM, fundamental switching modulations power balance modulation (PBM). All simulations have been performed at unitary modulation index with the same RL load (47 Ω, 2.5 mH). Although the values of THD*v* changes according to the modulation technique, a similar THD*i* is observed for all configurations. It worth noting that NLM is the easiest modulation technique among the ones considered in featuring lower computational effort, without the necessity of using look-up tables.

TABLE IV
THDs Comparison at Unitary Modulation Index

Configuration	Modulation	THD*i* (%)	THD*v* (%)
Foti et al. [26]	Hybrid	3.1	5.01
Samadaei et al. [27]	NLM	3.12	5.35
Taghvaie et al. [28]	PWM	3.25	6.9
Panda et al. [29]	SHE	3.37	6.5
Alishah et al. [30]	FSF	3.26	7.57
Mahato et al. [31]	PWM	3.25	8.9
Vasuki et al. [32]	NLM	3.12	5.35
Anand and Singh [33]	PWM	3.95	6.9
Roy et al. [34]	FSF	3.26	7.57
Samadaei et al. [35]	SHE	3.05	4.54
Peng et al. [36]	PBM	3.16	5.43
Iqbal et al. [37]	PWM	3.25	6.9
13-LDT	NLM	3.12	5.35

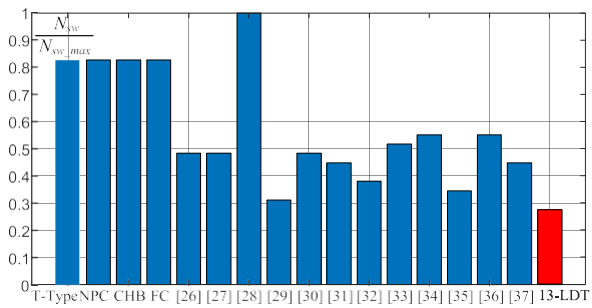

Fig. 15. Number of switches.

B. Cost Function Analysis

The cost function CF of (3) has been used to compare the proposed 13-LDT with the other 13-levels topologies investigated in. The cost function takes into account the amount of power switches N_{sw}, gate drivers N_{gd}, capacitors N_{Cap}, power diodes N_{diod}, dc power supplies N_{dc}, and TSV

$$CF = \frac{N_{sw} + N_{GD} + N_{Diod} + N_{cap} + \alpha TSV}{13} N_{DC} \quad (3)$$

where α presents the weightage of the TSV. The amount of each components category composing the considered configurations have been normalized with respect to the corresponding highest value. Hence, the lower is the result obtained by a topology in evaluating a specific parameter, the better is the estimated specific performance. As an example, among all the considered topologies, the 13-LDT topology requires 8 power switches per pole, while that proposed in requires the largest amount of power switches, namely 29 per pole; therefore, the score achieved by the proposed 13-LDT topology in terms of amount

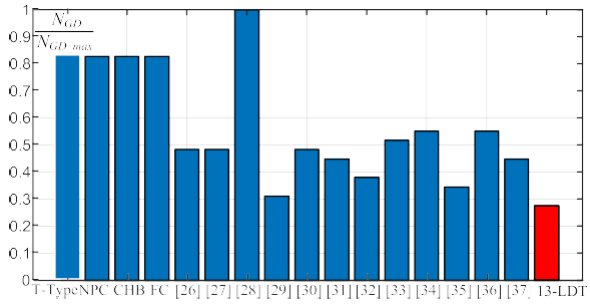

Fig. 16. Number of gate drivers.

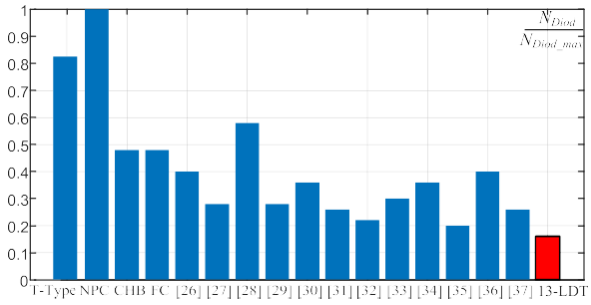

Fig. 17. Number of diodes.

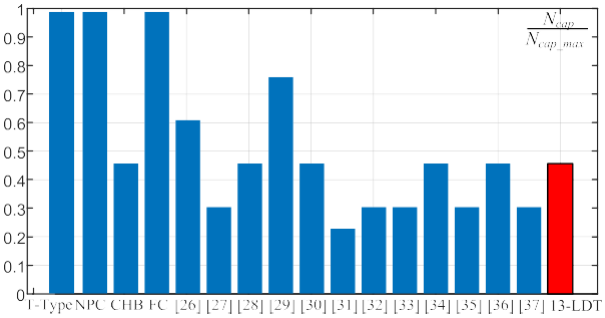

Fig. 18. Number of capacitors.

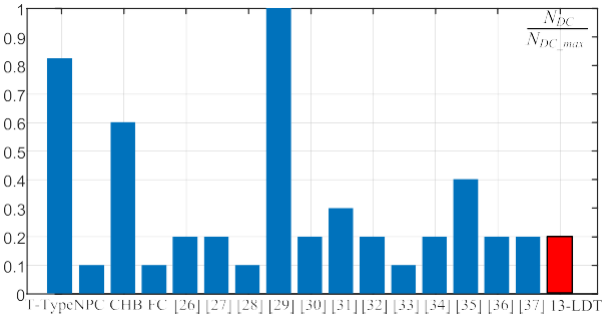

Fig. 19. Number of isolated DC sources.

of power switches is

$$n_{sw\_13-LDT} = \frac{N_{sw\_13-LDT}}{N_{sw\_[22]}} = \frac{8}{29} = 0.276. \quad (4)$$

Figs. 15–20 provide a comparison of the 13-LDT with the other 13-level topologies.

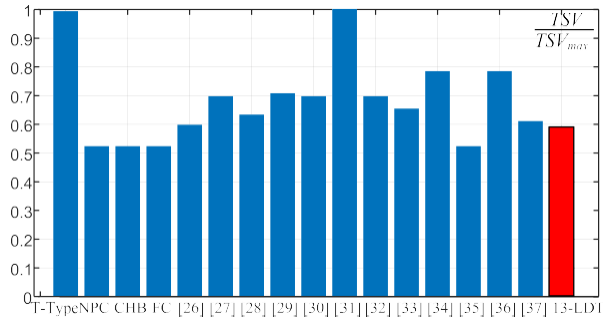

Fig. 20. TSV for the considered 13 level topologies.

TABLE V
PEAK VOLTAGES SUSTAINED BY 13-LDT DEVICES

Power Switches	Highest voltage Blocked by Switches	Conclusion
S_a	V	S_c ON
S_b	0.5V	S_a ON or S_c ON
S_c	V	S_a ON
S_d	3V	S_e ON
S_e	3V	S_d ON
S_f	2V	S_h ON
S_g	V	S_f ON or S_h ON
S_h	2V	S_f ON
Total	13.5V	

With regards to the TSV, it is a quality figure for multilevel converters taking into account the number of devices and voltage rating requirements. It is given by the sum of the highest voltages supported by all the switches, normalized to the highest level of the output voltage that can be generated. Table V gives the highest voltage sustained by the 8 switches composing the 13-LDT pole and the condition for which it occurs. The TSV of a pole of the 13-LDT topology then is

$$TSV_{13-LDT} = \frac{13.5\ V}{3\ V} = 4.5. \quad (5)$$

Fig. 20 displays the TSV values of the 13-level topologies. The results of this comparison are given in Table VI, highlighting the smallest value of CF achieved in the proposed inverter, for both $\alpha = 0.5$ and $\alpha = 1.5$. Table VI gives the maximum blocking voltage (MBV) and the voltage balancing capability. The proposed 13-LDT topology performs better than others in terms of number of switches, number of gate drivers, number of diodes, while is around average in terms of number of capacitors, number of isolated dc power supplies and TSV. As a general remark the 13-LDT topology is effective in reducing the complexity of the power circuit, with a largely reasonable penalization in terms of TSV and number of capacitors.

C. Cost Analysis

The results obtained in Table VI must be confirmed by a cost analysis also considering the power system of each configuration. Each isolated independent voltage source needs an ac transformer and an ac/dc rectifier. Thus, in case of more of one isolated voltage sources, more of one ac/dc converters and more windings transformer are needed. Many solutions can be

TABLE VI
COMPARISON OF DIFFERENT 13-L TOPOLOGIES

Topology	N_L	N_{sw}	N_{gd}	N_{cap}	N_{dc}	N_{diod}	TSV	MBV	Balancing	CF	
										α=0.5	α=1.5
13-L NPC	13	24	24	12	1	22	4	0.16	No-self	6.76	7.07
13-L CHB	13	24	24	0	6	0	4	0.16	No-self	23	24.9
13-L FC	13	24	24	12	1	0	4	0.16	No-self	4.76	5.07
13-L T-Type	13	24	24	12	1	0	7.66	1	No-self	4.91	5.5
Foti et al. [26]	13	14	14	6	2	10	4.57	0.25	No-self	6.7	7.5
Samadaei et al. [27]	13	14	14	2	2	0	5.33	2	Self	5.02	5.84
Taghvaie et al. [28]	13	29	29	5	1	6	4.84	1	Self	5.13	5.5
Panda et al. [29]	13	9	9	0	10	5	5.41	1	No-self	19.86	24.22
Alishah et al. [30]	13	14	14	4	2	4	5.33	1	Self	5.94	6.76
Mahato et al. [31]	13	13	13	0	3	0	7.66	1	/	7.8	9.57
Vasuki et al. [32]	13	11	11	0	4	0	5.33	1	Self	5.58	5.63
Anand and Singh [33]	13	15	15	3	1	0	5	0.5	Self	4.84	5.45
Roy et al. [34]	13	16	16	4	2	2	6	0.33	Self	6.3	7.23
Samadaei et al. [35]	13	10	10	0	4	0	3.33	0.83	/	6.66	7.69
Peng et al. [36]	13	16	16	4	2	4	5.33	0.5	Self	6.56	7.38
Iqbal et al. [37]	13	13	13	2	2	0	4.67	1.5	/	4.66	5.38
13-LDT	**13**	**8**	**8**	**4**	**2**	**8**	**4.5**	**1**	Self	**4.65**	**5.34**

considered about the type of the ac transformer. It is possible to use N_{DC} number of transformers or a multiwinding transformer with N_{DC} number of windings. However, in has been demonstrated that in case of more of one dc-link input, a multi-winding transformer is more efficient in terms of lower weight, losses and cost of using more of one two windings transformer, with the same rated power. Even in, the weight of the core and copper versus the number of secondary windings N_{coil} have been found and shown in Fig. 21. The cost of the transformer that take into account only the cost of core and windings, has been obtained by considering the average cost of copper (869 ₹/kg) and core (210 ₹/kg). The minimum cost is obtained for three windings. Table VII shows the total cost which includes the cost of power switches, power diodes, capacitors, gate drives, ac/dc rectifier and ac transformer. About the ac/dc, a three-phase uncontrolled diode rectifier equipped with 6 power diodes has been considered for each N_{DC} isolated voltage source. The results confirm that the proposed configuration is less expensive thanks to lower CF and lower cost of a three-winding transformer.

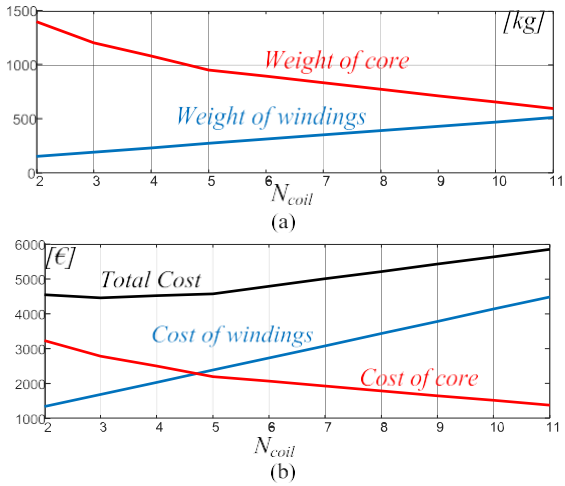

Fig. 21. Cost of the transformer. (a) Weight of transformer's core and winding versus number of secondary windings. (b) Cost of transformer's core and copper versus number of secondary windings.

V. EXPERIMENTAL ASSESSMENT

Performance of the 13-LDT inverter has been assessed by experimental tests with a 1.5 kVA scale prototype. The experimental setup is shown in Fig. 22. The power converter is equipped with ST Microelectronics IGBT STGB10H60DF 600 V/20 A switches. Modulation and control are accomplished through a dSpace Scalexio rapid prototyping board. A dead time equal to 2μs has been introduced to safely switch complementary devices. *RC* snubber circuits (R = 5.7 Ω, C = 2.2 μF) have been installed in parallel to the power switches of the converter prototype to reduce the voltage spikes.

TABLE VII
COST COMPARISON OF DIFFERENT 13-L TOPOLOGIES ENABLING TO PROVIDE 800 V MAXIMUM OUTPUT VOLTAGE

Components	Rating	Unit Price	Topologies																
			NPC	CHB	FC	NPP	[26]	[27]	[28]	[29]	[30]	[31]	[32]	[33]	[34]	[35]	[36]	[37]	13-LDT
IGBT IGW25T120FKSA1	1200 V, 50 A	5.46 €	/	/	/	2	/	2	/	4	/	4	2	/	/	4	/	2	2
IGBT IGP50NG0TXKSA 1	600 V, 50 A	4.73 €	/	/	/	/	/	12	/	/	14	9	9	15	6	6	16	11	2
IGBT FGD3040G2-F085	300 V, 41 A	1.01 €	24	24	24	22	14	/	29	5	/	/	/	/	10	/	/	/	4
Diode IDP30E120XKSA1	1200V, 50 A	3.08 €	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	20
Diode IDW50E60FKSA1	600 V, 50 A	3.22 €	/	/	/	/	6	12	6	/	16	/	12	6	14	24	16	/	/
Diode VS-60APH03-N3	300 V, 50 A	4.22 €	22	/	/	/	10	/	6	65	/	18	/	/	/	/	/	12	/
Capacitor	300 V,2.2 mF	42.80 €	12	/	12	12	/	2	/	/	4	/	2	3	/	/	4	2	/
Capacitor	400 V,2.2 mF	48.72 €	/	/	/	/	6	2	5	/	/	/	2	/	4	/	/	/	4
Gate drive HCPL-316J-000E	/	6.77 €	24	24	24	24	14	12	29	9	14	13	11	15	16	10	16	13	8
DC supplies NMH0515SC	/	10.64 €	24	24	24	24	14	12	29	9	14	13	11	15	16	10	16	13	8
Three-Phase Transformer 10kVA – Number of three-phase primary+secondary windings	2 Coils	4556 €	1	/	1	1	/	/	1	/	/	/	/	1	/	/	/	/	/
	3 Coils	4462 €	/	/	/	/	1	1	/	/	1	/	1	/	1	/	1	1	1
	4 Coils	4530 €	/	/	/	/	/	/	/	/	/	1	/	/	/	/	/	/	/
	5 Coils	4793 €	/	/	/	/	/	/	/	/	/	/	/	/	/	1	/	/	/
	7 Coils	5218 €	/	1	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
	11 Coils	5855 €	/	/	/	/	/	/	/	1	/	/	/	/	/	/	/	/	/
Tot. Cost €			5604	5659	5511	5520	5074	4960	5378	6312	4995	4897	4929	5035	5019	5094	5039	4888	**4882**

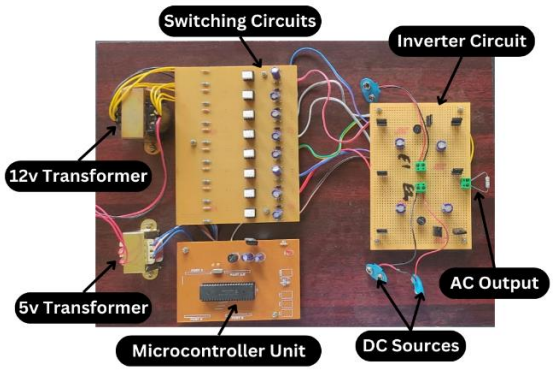

Fig. 22. Experimental system.

A variable *RL* load is exploited to set the output loads. Two isolated dc sources, $V = 48$ V and $2V = 96$ V supply the inverter. Thus, the maximum output voltage is $3V = 144$ V. Each power supply delivers power proportionally to its rated voltage. The capacitance of the four capacitors has been de- termined, according to the procedure reported in Section III, achieving a good compromise between cost and residual voltage ripple. Main parameters of the experimental system are given in Table VIII.

TABLE VIII
POWER SYSTEM SPECIFICATIONS

IGBT STGB10H60DF	$V_n = 600$ V, $i_n = 20$ A, $V_{gs} = +15$V
Capacitors	2.2 mF
Variable *RL* Load	R = 0÷47 Ω and L = 0÷0.51 H

Fig. 23 shows the inverter output voltage waveform and gate signals for the eight IGBT devices. The bidirectional device S_2 switches several times more than the other devices, reaching, according to Fig. 7(a) switching frequency equal to 1200 Hz, when the inverter generates an AC output voltage at 50 Hz, while devices S_d and S_e switch only two times per fundamental period T_0.

Experimental tests have been carried out using both NLM and SHE. Fig. 24 shows the output voltage and load current obtained by implementing the NLM at unitary modulation index, with $\cos(\phi) = 0.95$ and $Z = 11.4+j3.74$ Ω.

Harmonic spectra of the voltage and current are shown in Fig. 25. The THDs of the output voltage is 5.3%, according to Fig. 8, while the THD*i* of the current is 1.2%. Even though by using the SHE is possible to eliminate the 3th, 5th, 7th, 9th, and 11th harmonics, the THDs are higher and respectively equal to 9% and 2.1%, Fig. 26. This last test has been taken without *RC* snubbers to observe the small voltage spikes during dead time. Harmonic spectra in this last case are displayed in Fig. 27.

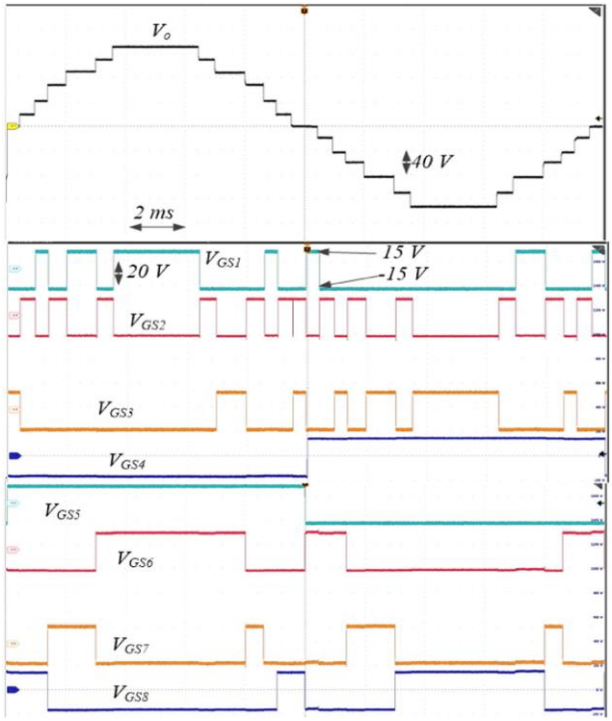

Fig. 23. NLM (f_o = 50 Hz): output voltage *Vo* and gate signals.

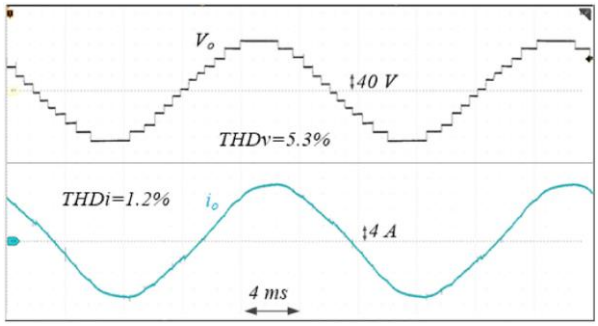

Fig. 24. NLM [cos(ϕ) = 0.95, m_{NLM} = 1, f_o = 50 Hz]: V_o and i_o.

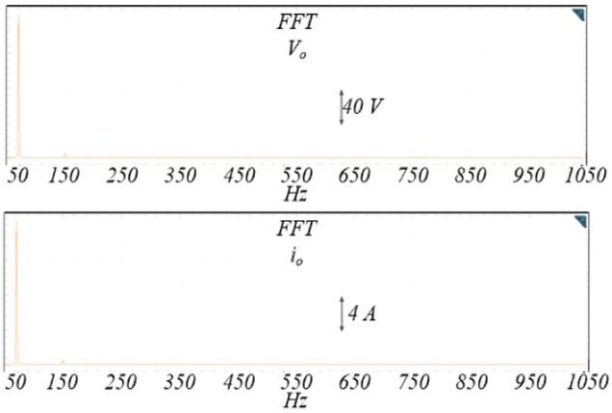

Fig. 25. NLM [cos(ϕ) = 0.95, m_{NLM} = 1, f_o = 50 Hz]: (up) V_o FFT, (down) i_o FFT.

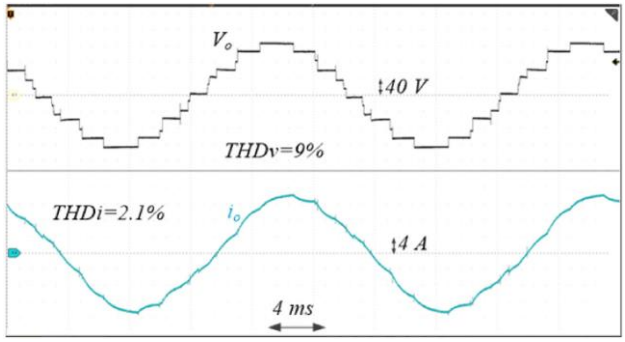

Fig. 26. SHE [cos(ϕ) = 0.95, m_{NLM} = 1, f_o = 50 Hz]: V_o and i_o.

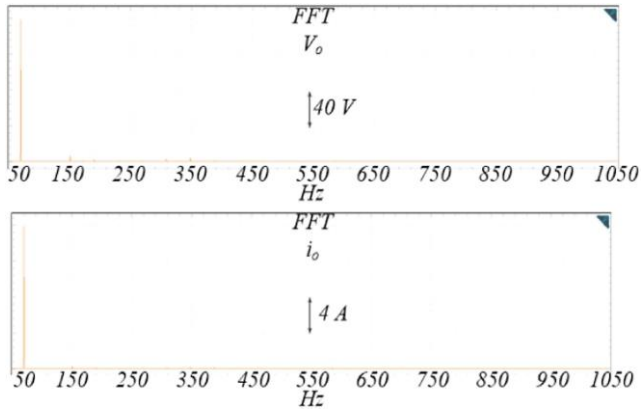

Fig. 27. SHE [cos(ϕ) = 0.95, m_{NLM} = 1, f_o = 50 Hz]: (up) V_o FFT, (down) i_o FFT.

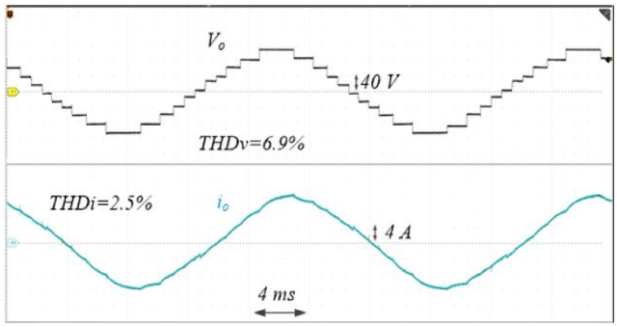

Fig. 28. NLM [cos(ϕ) = 0.95, m_{NLM} = 0.8, f_o = 50 Hz]: V_o and i_o.

All the other figures were taken with the snubbers working. Similar differences have been achieved also at m_{NLM} = 0.8, as shown in Figs. 28 –31. In these last tests the peak output voltage of the fundamental harmonic is equal to 144 V when m_{NLM} = 1 and 115 V when m_{NLM} = 0.8.

Dynamic performance of the proposed topology has been also assessed. Fig. 32 shows the output voltage and current when a load is changed from $Z = 11.4 + j3.74\ \Omega$ to $Z = 12.6 + j12.85\ \Omega$. Therefore, the load current drops from 12 A to 8 A while the power factor changes from 0.95 to 0.7. The same, a variation of power factor from 0.95 to 0.2 is instead shown in Fig. 33, by

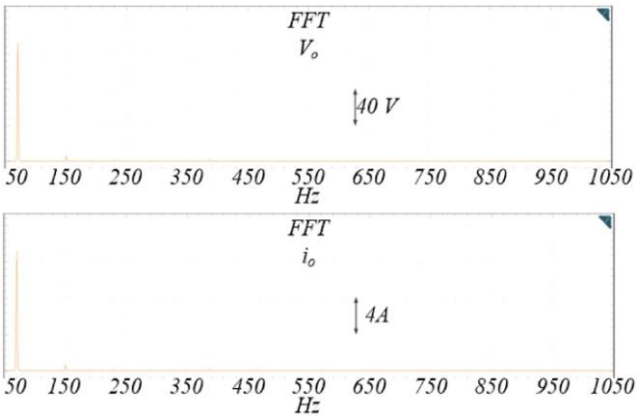

Fig. 29. NLM [$\cos(\phi) = 0.95$, $m_{NLM} = 0.8$, $f_o = 50$ Hz]: (up) V_o FFT, (down) i_o FFT.

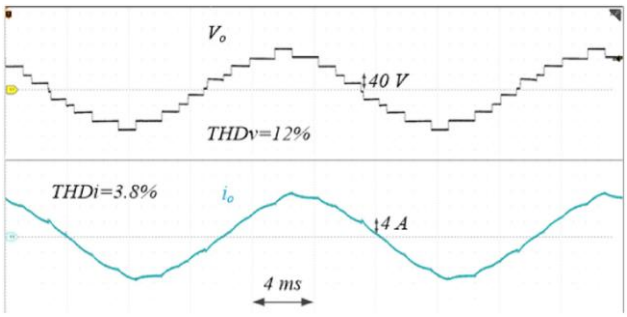

Fig. 30. SHE [$\cos(\phi) = 0.95$, $m_{NLM} = 0.8$, $f_o = 50$ Hz]: V_o and i_o.

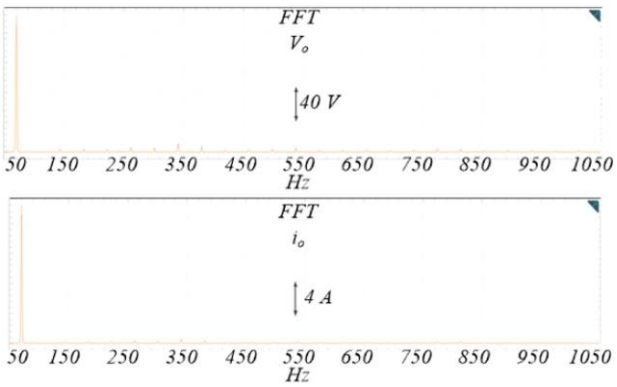

Fig. 31. SHE [$\cos(\phi) = 0.95$, $m_{NLM} = 0.8$, $f_o = 50$ Hz]: (up) V_o FFT, (down) i_o FFT.

confirming the good working at low power factor. The response to a variation of the modulation index from 1 to 0.8 with $Z = 11.4 + j3.74\ \Omega$ is shown in Fig. 34. The output voltage levels drop from 13 to 11, with a limited impact on the harmonic current content, which still remains close to sinusoidal. Figs. 35–38 deal with capacitor voltages. According to Table II, when the inverter is in the switching configurations 2, 5, 8, 11, 14, and 17, the voltages at the terminals of capacitors C_a and C_b vary, while they remain constant when the inverter is in the other switching

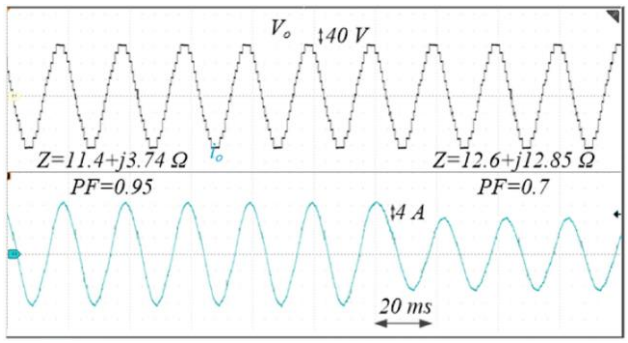

Fig. 32. NLM—Load variation ($m_{NLM} = 1$, 50 Hz), PF from 0.95 to 0.7: V_o and i_o.

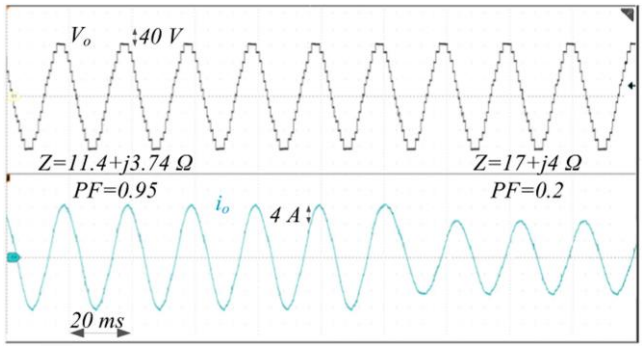

Fig. 33. NLM—Load variation ($m_{NLM} = 1$, 50 Hz) PF from 0.95 to 0.2: V_o and i_o.

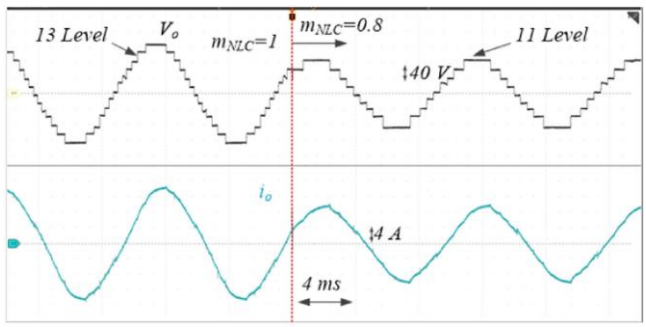

Fig. 34. NLM —Modulation index variation from 1 to 0.8 (50 Hz): V_o and i_o.

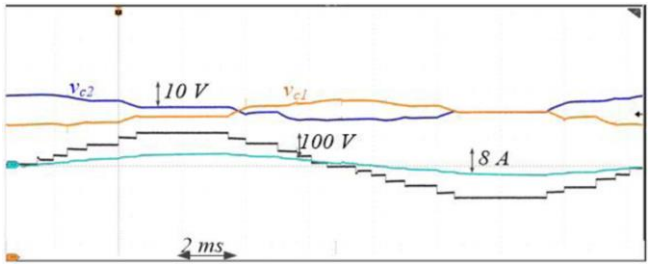

Fig. 35. Voltages on C_a and C_b ($m_{NLC} = 1$, $\cos(\phi) = 0.95$, 50 Hz).

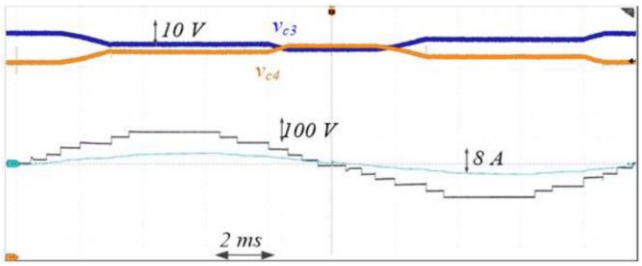

Fig. 36. Voltages on C_c and C_d ($m_{NLC} = 1$, $\cos(\phi) = 0.95$, 50 Hz).

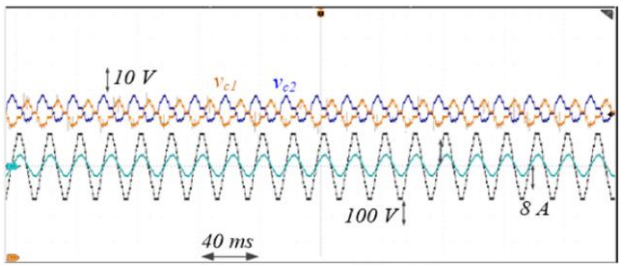

Fig. 37. Voltages measured at the terminals of C_a and C_b ($m_{NLC} = 1$, $\cos(\phi) = 0.95$, 50 Hz).

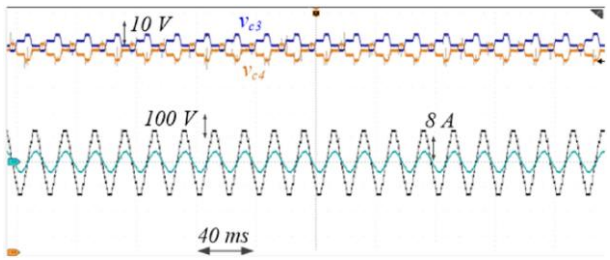

Fig. 38. Voltages measured at the terminals of C_c and C_d ($m_{NLC} = 1$, $\cos(\phi) = 0.95$, 50 Hz).

configurations. Similarly, the voltages at the terminals of C_c and C_d vary if the inverter switches are set in configuration 4, 5, 7, 13, 14, and 16, while they are constant when the inverter switches are set on the other switching configurations.

As shown in Figs. 37 and 38, the average voltage of the four capacitors is constant at steady state. The capacitors voltage ripple have been measured at different values of capacitance and power factor at rated current, as shown in Fig. 39. The power factor doesn't impact the voltage ripple as much as the capacitance value.

The efficiency E_f of the 13-LDT inverter can be evaluated as

$$E_f = \frac{P_L}{P_{in}} \tag{6}$$

where P_{in} is the power supplied by the two dc sources and P_L is the power fed to the load. Efficiency versus output power is diagrammed in Fig. 40. The max value of efficiency is achieved at full load (E_f = 99.3%), while it drops to 94.2% at light load.

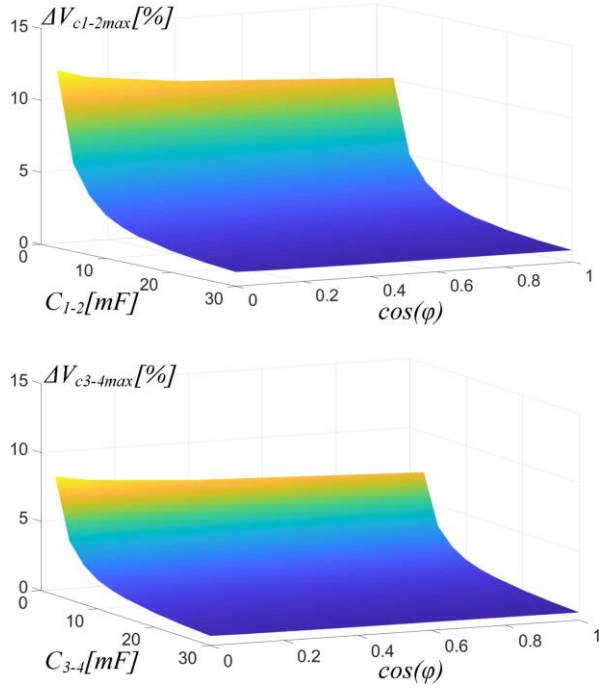

Fig. 39. Capacitor voltage ripple versus capacitance value and power factor, at rated current.

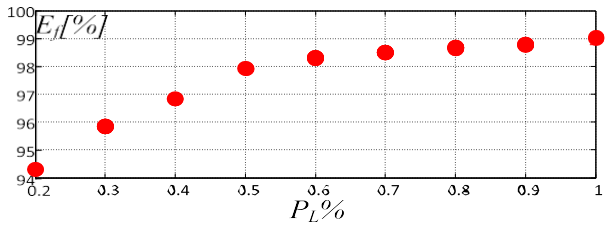

Fig. 40. NLM—inverter efficiency versus output power.

VI. Conclusion

A dual T-type-based 13-Level Inverter has been proposed which performs better than other conventional and previously developed reduced switch-count topologies in terms of number of switches, number of gate drivers and number of diodes. A key feature of the proposed topology is an easy self-balancing of the voltage between dc-bus capacitors, leading to achieve null average capacitor currents in a period T_o, without requiring the introduction of extra circuits, nor special modu- lation strategies. Exploiting an NLM technique, the proposed topology outperforms high efficiency and low total harmonic distortion in a wide operating range. Experimental validation confirmed the feasibility and effectiveness of the proposed power conversion unit.