CHAPTER 1

INTRODUCTION

The idea of this mini project is to create a circuit which determines which participant has responded the earliest. These types of circuits are useful in the buzzer rounds of quiz shows. In first response rounds of quiz contests, the question is thrown open to all the teams. The person who knows the answer hits his/her switch first and then answers the question. Sometimes two or more players hit the switch almost simultaneously and it is very difficult to detect which of them has pressed the switch first. This mini project helps eliminate that case and provides ease to the organizers.

CHAPTER 2

BLOCK DIAGRAM

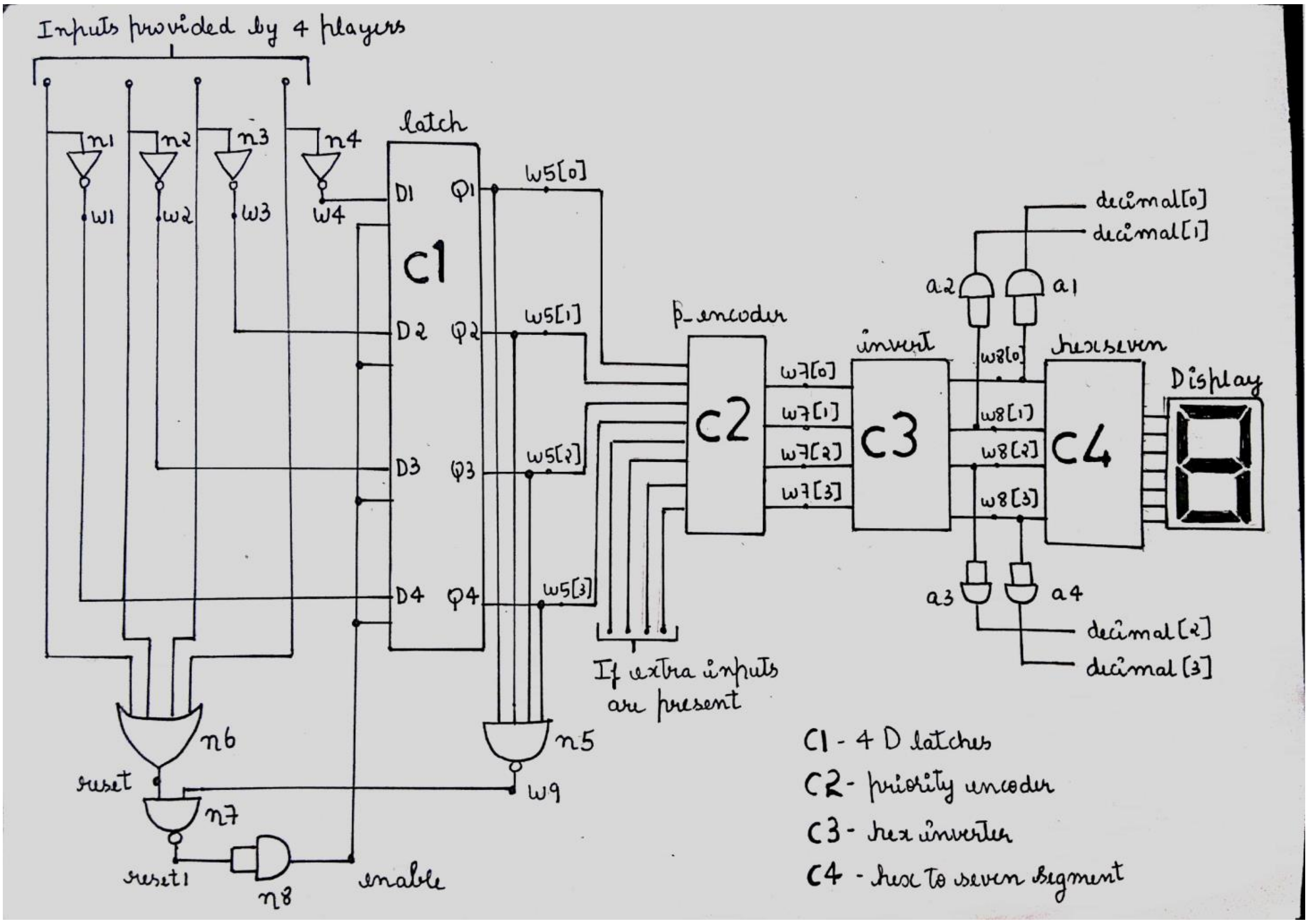

Figure 2.1: Block Diagram of the design

Figure 2.1 shows the block diagram of the design. When a contestant presses switch, the corresponding output of the inverter changes its logic state from 1 to 0 and further latch C1 passes the variable without any change. The combinational circuitry comprising dual 4-input OR gate locks out subsequent entries by producing the appropriate latch-disable signal. Priority encoder C2 encodes the active-low input condition into the corresponding binary coded decimal (BCD) number output. The outputs of C2 after inversion by inverter gates inside hex inverter C3 are coupled to BCD to- 7-segment decoder/display driver C4. The output of C4 drives common anode 7-segment LED display.

player	**display**	**decimal**	**control**
0000	1111110	0000	0111
0001	0110000	0001	0111
0000	1111110	0000	0111
0010	1101101	0010	0111
0000	1111110	0000	0111
0100	1111001	0011	0111
0000	1111110	0000	0111
1000	0110011	0100	0111
0000	1111110	0000	0111

Table 2.1 Simulation Table

CHAPTER 3

COMPONENT DESCRIPTION

3.1 Hardware Requirements

3.1.1. FPGA (Field-Programmable Gate Array):

A Field-Programmable Gate Array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing, hence 'field-programmable'. FPGAs contain an array of programmable logic blocks and a hierarchy of reconfigurable interconnects that allow the blocks to be 'wired together', like many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions or merely simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Specifications:

1. Family – Spartan6
2. Device – XC6SLX9
3. Package – TQG144
4. Speed – (-2)
5. Simulator – ISim (VHDL/VERILOG)

Figure 3.1.1: FPGA board

The FPGA board is shown in Figure 3.1.1.

3.1.2 USB (Universal Serial Bus) Programmer:

Figure 3.1.2: USB programmer

A programmer is a device used to configure the target device on the printed circuit board. It is an electronic device that can convert written software in high level language to machine level language to be interfaced with programmable devices. The USB Programmer is shown in Figure 3.1.2.

3.1.3 9V Adapter:

Figure 3.1.3: 9V Adapter

It is used to convert the 230V from the AC mains to 9V power supply for the FPGA board. 9V Adapter is shown in the above Figure 3.1.3.

3.1.4 Flat Ribbon Cable (FRC):

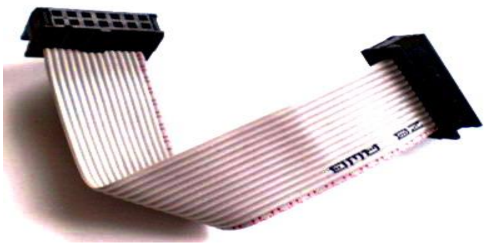

Figure 3.1.4: Flat Ribbon Cable

A ribbon cable (also known as multi-wire planar cable) is a cable with many conducting wires running parallel to each other on the same flat plane. As a result, the cable is wide and flat. Its name comes from its resemblance to a piece of ribbon. The FRC Cable is shown in Figure 3.1.4.

3.1.5 Seven Segment Display:

Figure 3.1.5: Seven Segment Display

A Seven-Segment Display (SSD) or seven-segment indicator is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot matrix displays. Seven- segment displays are widely used in digital clocks, electronic meters, basic calculators and other electronic devices that display numerical information. The 7-segment display, also written as “seven segment displays”, consists of seven Light Emitting Diode (LED) arranged in a rectangular fashion as shown in Figure 3.1.5. Each of the seven LEDs is called a segment because when illuminated the segment forms part of a numerical digit (both Decimal and Hex) to be displayed. An additional 8th LED is sometimes used within the same package thus allowing the indication of a decimal point, (DP) when two or more 7-segment displays are connected to display numbers greater than ten.

Each one of the seven LEDs in the display is given a positional segment with one of its connection pins being brought straight out of the rectangular plastic package. These individually LED pins are labelled from “a” to “g” representing each individual LED. The other LED pins are connected together and wired to form a common pin. So, by forward biasing the appropriate pins of the LED segments in a particular order, some segments will be lit and others will be dark allowing the desired character pattern of the number to be generated on the display. This then allows us to display each of the ten decimal digits 0 through to 9 on the same 7-segment display. The FPGA board is shown in Figure 3.1.5.

3.1.6 Push Button:

Figure 3.1.6: Push Button switch

A push button switch is a small, sealed mechanism that completes an electric circuit when the user presses on it. When it's on, a small metal spring inside makes contact with two wires, allowing electricity to flow. The Push Button is shown in Figure 3.1.6.

3.1.7 LED (Light Emitting Diode):

Figure 3.1.7: LED's

A Light-Emitting Diode (LED) is a semiconductor device that emits visible light when an electric current pass through it. The light is not particularly bright, but in most LED's, it is monochromatic, occurring at a single wavelength. The LED's are shown in Figure 3.1.7.

3.1.8 Jumper Wires:

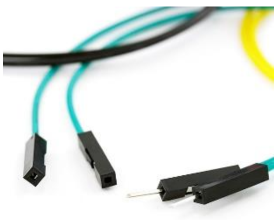

Figure 3.1.8: Jumper Wires

Jumper wires are simply the wires that have connector pins at each end, allowing them to be used to connect two points to each other without soldering. Jumper wires are typically used with breadboards and other prototyping tools in order to make it easy to change a circuit as needed. The Jumper Wires shown in Figure 3.1.8.

3.1.9 Printed Circuit Board (PCB):

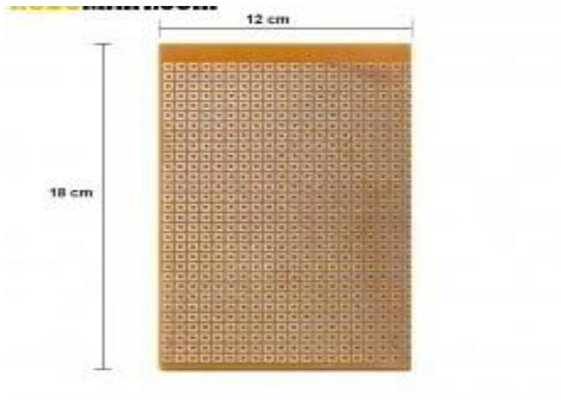

Figure 3.1.9: PCB

Stands for "Printed Circuit Board." A PCB is a thin board made of fiberglass, composite epoxy, or other laminate material. Conductive pathways are etched or "printed" onto board, connecting different components on the PCB, such as transistors, resistors, and integrated circuits. PCB is as shown in Figure 3.1.9.

3.1.10 10KΩ Resistors:

A resistor is a passive two-terminal electrical component that implements electrical resistance as a circuit element. In electronic circuits, resistors are used to reduce current flow, adjust signal levels, to divide voltages, bias active elements, and terminate transmission lines, among other uses. 10kΩ resistor is as shown in Figure 3.1.10.

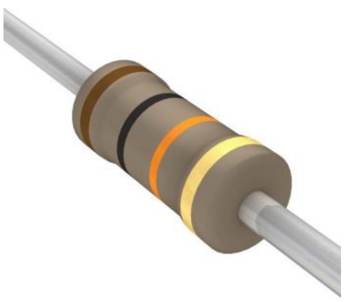

Figure 3.1.10: 10kΩ resistor

3.2 Software Requirements:

3.2.1 Xilinx ISE Design suite 14.7:

Xilinx ISE is a design environment for FPGA products from Xilinx and is tightly coupled to the architecture of such chips. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or ModelSim logic simulator is used for system level testing.

CHAPTER 4

WORKING PRINCIPLE

- Code of the project (consisting of both '.v' file and '.ucf' file) is written in Xilinx software and interfacing is done with FPGA.
- FPGA is powered directly by power supply and connections are made as follows:
  - FRC 1 is connected to push buttons.
  - FRC 10 is connected to seven-segment display.
  - FRC 2 is connected to LED display.
  - FPGA is connected to computer through USB (Universal serial bus) port.
- Firstly, the user will press the button using Push button switch.
- Input from the user is inverted and given to D latch(C1). The combinational circuitry comprising dual 4-input OR gate locks out subsequent entries by producing the appropriate latch-disable signal. Output of D latch is given to a NAND gate with output of OR gate. From NAND gate there is a delay to the enable inputs of the D latches. Then the output from C1 is passed on to priority encoder.
- Priority encoder C2 encodes the active-low input condition into the corresponding binary coded decimal (BCD) number output. The outputs of C2 after inversion by inverter gates inside hex inverter C3 are coupled to BCD to- 7-segment decoder/display driver C4. The output of C4 drives common anode 7-segment LED display.
- Similarly, the outputs of the hex inverter is delayed and given to 4 LEDs in binary values. Starting from the right, Most Significant Bit (MSB) precedes the Least Significant Bit (LSB).

CHAPTER 5

RESULTS

The ‘Fastest Finger First’ circuit takes input from the Push Button switch and gives the desired output after being processed by a combinational logic circuit. When a correct combination of switch is applied, the seven-segment display displays the number of the switch which had been pressed first. Accordingly, the LED’s will display the output in binary values through the port decimal.

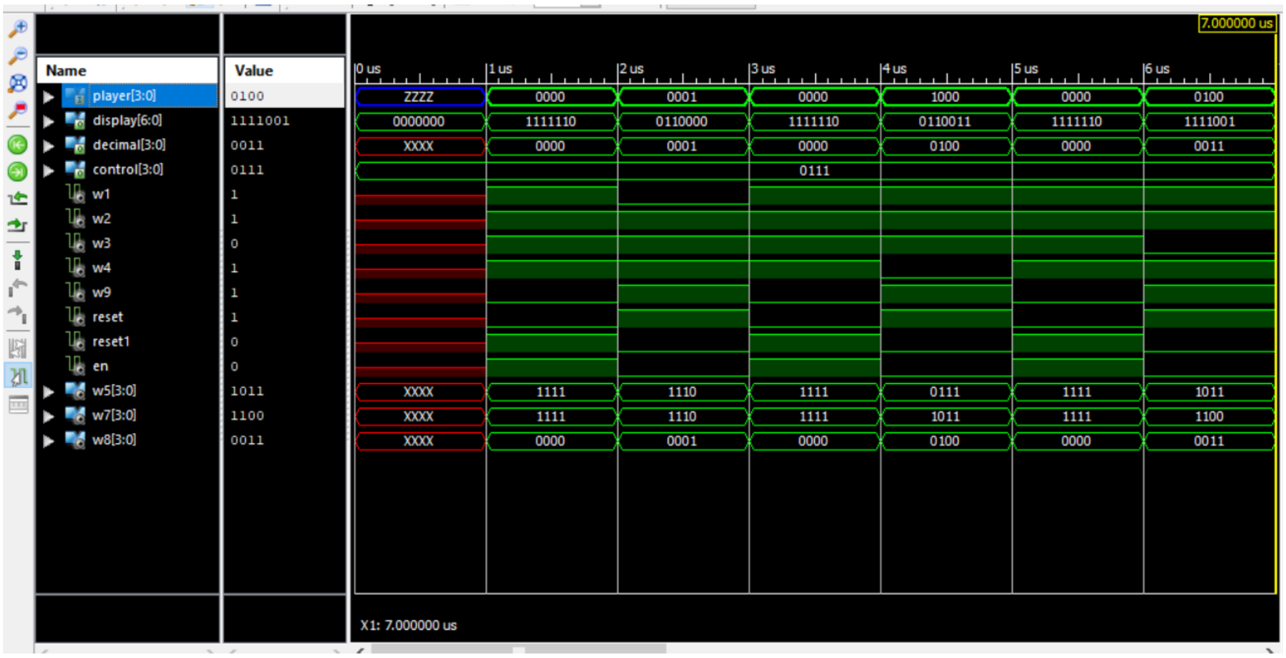

Figure 5.1.1: Project Simulation Output

Figure 5.1.1 shows the Simulation output of the project.

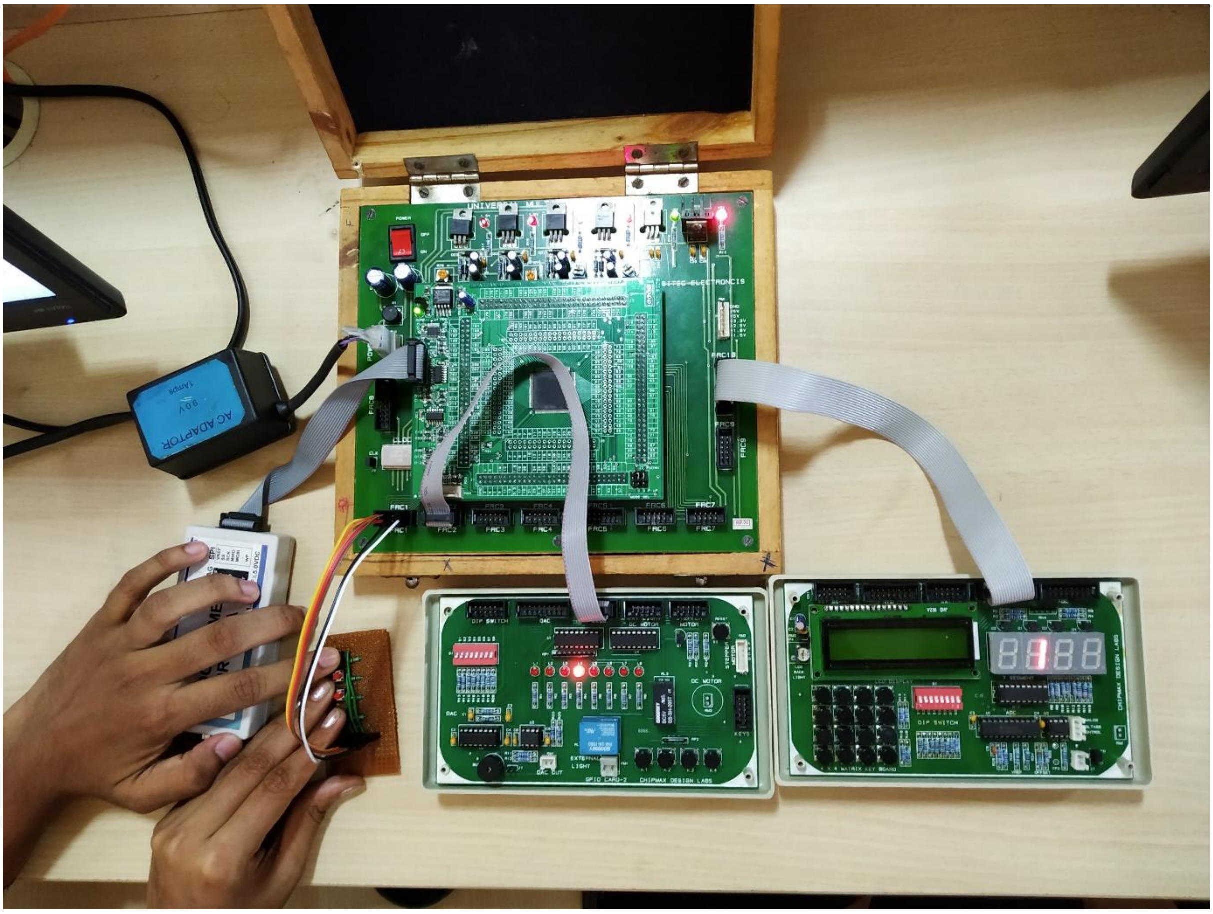

Figure 5.1.2: Project Output when more than one push button is active.

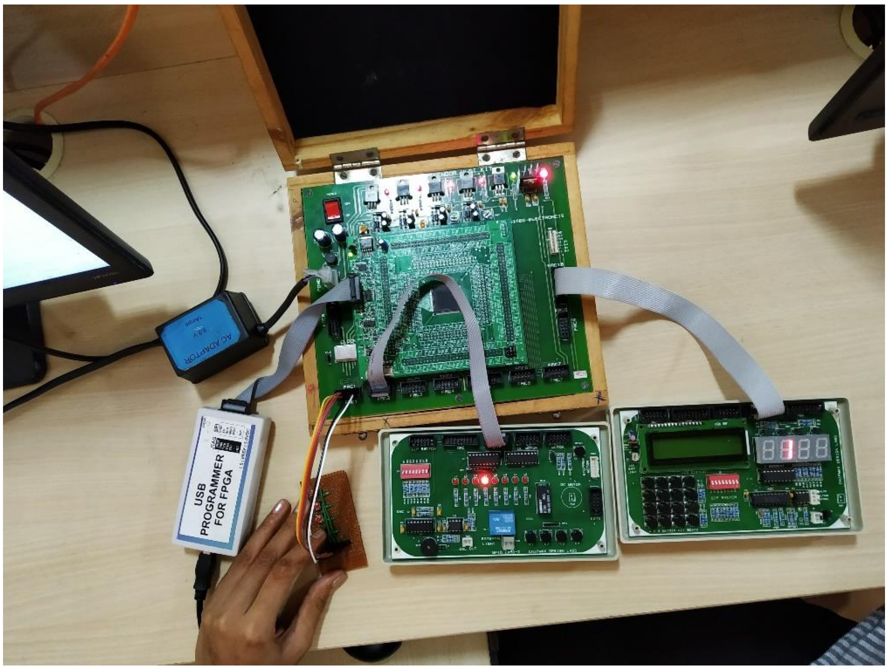

Figure 5.1.3: Project Output when a single push button is active

Figure 5.1.2 and Figure 5.1.3 shows the outputs of the project.

CHAPTER 6

CONCLUSION

The project successfully fulfills the aim of detecting the first response when there are multiple responses. It is simple in construction and easy to operate. It can be used in first response rounds of quiz contests; the question is thrown open to all the teams. The person who knows the answer hits his switch first and then answers the question. Sometimes two or more players hit the switch almost simultaneously and it is very difficult to detect which of them has pressed the switch first. This project is an electronic first response detector that is affordable by the colleges and even individuals. This project is useful for a 4-team quiz contest, although it can be modified for a greater number of teams.