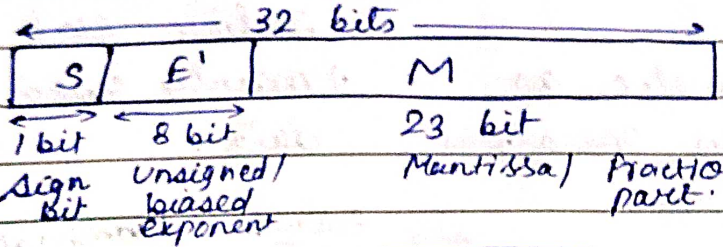
Computer Organisation

30/01/24

① IEEE → Institute of Electrical and Electronics Engineers.
The most common ways for representing the floating point number in computer are the format standardized as the IEEE-754 standards commonly called the IEEE floating point.

- It has 2 similar formats :-
  (i) Single precision format (32 bits)
  (ii) Double precision format (64 bits)

- **Single Precision Format**



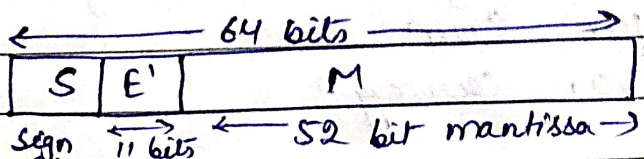
⇒ **Value Represented = $\pm 1.M \times 2^E$**

⇒ 0 → + } Sign
⇒ 1 → − } Bit

⇒ It is a 32 bit single precision format in which 8 bits is for exponent part and remaining 23 bits is for mantissa part. First 1 bit is sign bit i.e., 0 for + and 1 for −.

⇒ $E' = E + 127$
E' → unsigned integer.

- **Double Precision Format**



0 → +
1 → −

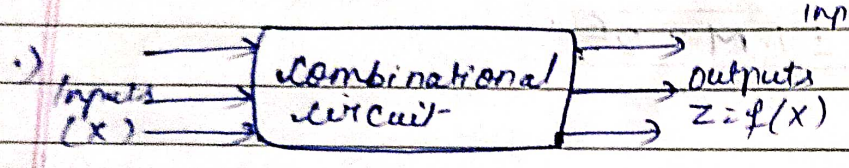
Value Represented :- $\pm 1.M \times 2^E$

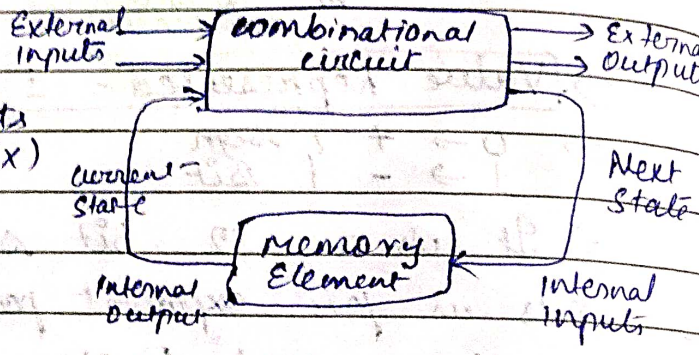
② Combinational circuit

- Defined as the time independent circuits which don't depends upon previous inputs to generate any output are termed as combinational cir.
- Speed is fast
- designed easy.
- don't have capability to store any state.
- used for arithmetic as well as boolean operations.

Sequential circuit

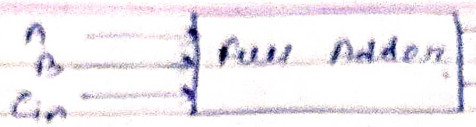
- dependent on clock cyc and depends on the as well as past input to generate any outp
- Speed is slow.
- designed tough
- have capability to store any state or to retain earlier state.
- mainly used for storing data.



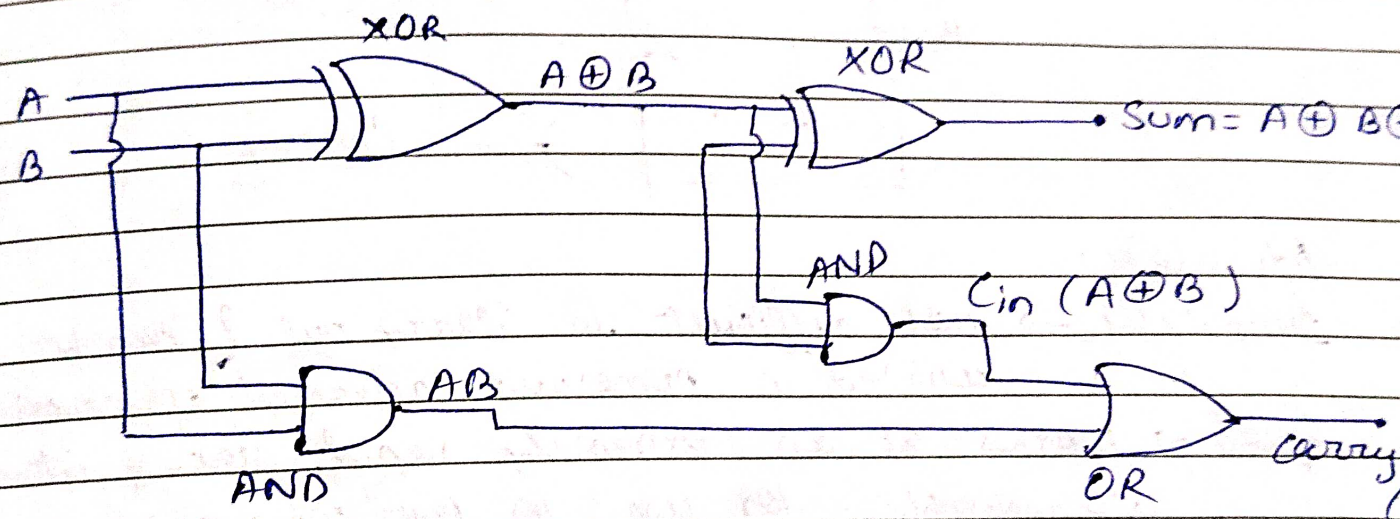


③ Full Adder

→ Combinational circuit.
→ 3 inputs (each of 1 bit) A, B and Cin
→ generates Sum (S) and carry (C) in the outputs.
→ designed using 2 AND gate, 1 OR gate and 2 XOR
→ XOR gate → output for Sum
OR gate → output for carry.

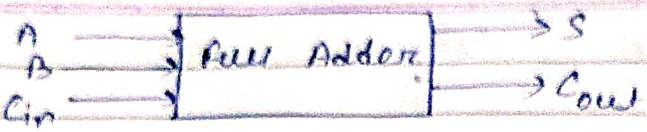


Input			Output	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

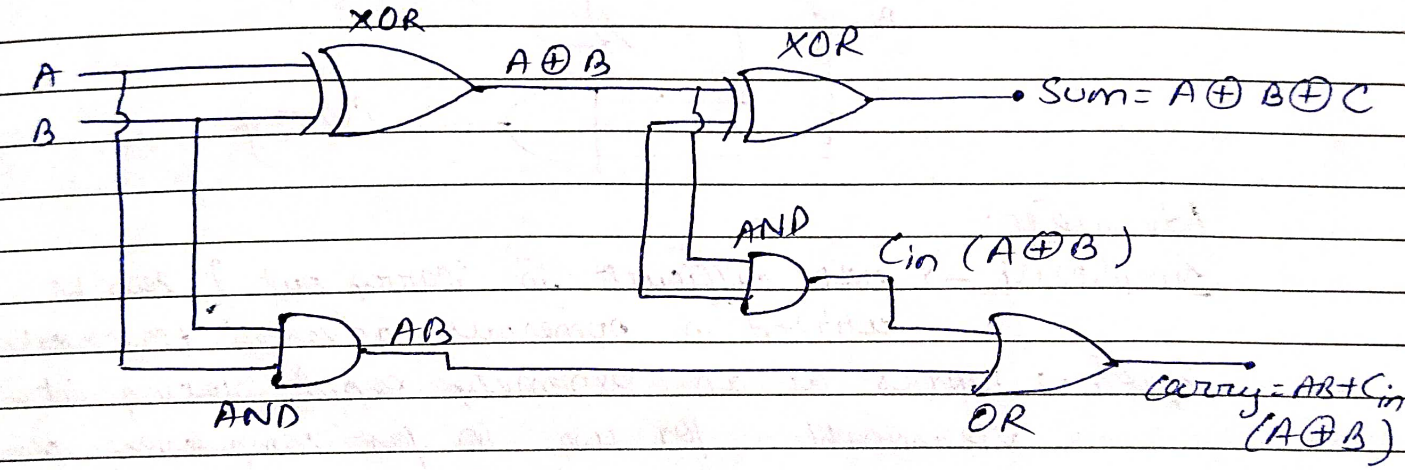


(4) Half Adder.

→ digital logic circuit that performs binary addⁿ of single-bit binary no.
→ 2 inputs, A and B
→ 2 Outputs, SUM and CARRY.
→ Implemented using basic gates such as XOR &
→ Simplest of all adder circuits.
→ Combinational arithmetic circuit that adds 2 bits & produces a sum bit (S) and carry bit (C) both



Input-			Output-	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



(4) Half Adder

→ digital logic circuit that performs binary addⁿ of 2 single-bit binary no.
→ 2 inputs, A and B
→ 2 outputs, SUM and CARRY.
→ Implemented using basic gates such as XOR & AND gate
→ Simplest of all adder circuits.
→ Combinational arithmetic circuit that adds 2 no. and produces a sum bit (S) and carry bit (C) both as outputs

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Karnaugh Expression:

For Sum:

A \ B	0	1
0	0	1
1	1	0

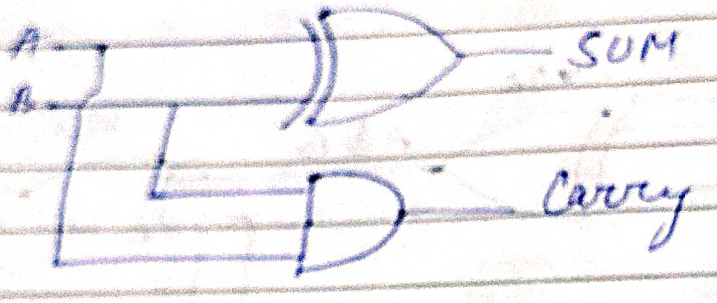
Sum = A XOR B

For carry:

A \ B	0	1
0	0	0
1	0	1

Carry = A AND B.

Implementation:



Advantages

Simplicity → not difficult to carry out & can be utilized in numerous advanced frameworks

Speed → works at an extremely rapid, making it reasonable for use in fast computerized circuits.

Disadvantages

Limited usefulness

Lack of convey info

Propagation deferral

Applications → Arithmetic circuits
→ Data handling
→ Multiplexers & demultiplexers
→ Encoder & decoder circuits.
→ Counters.

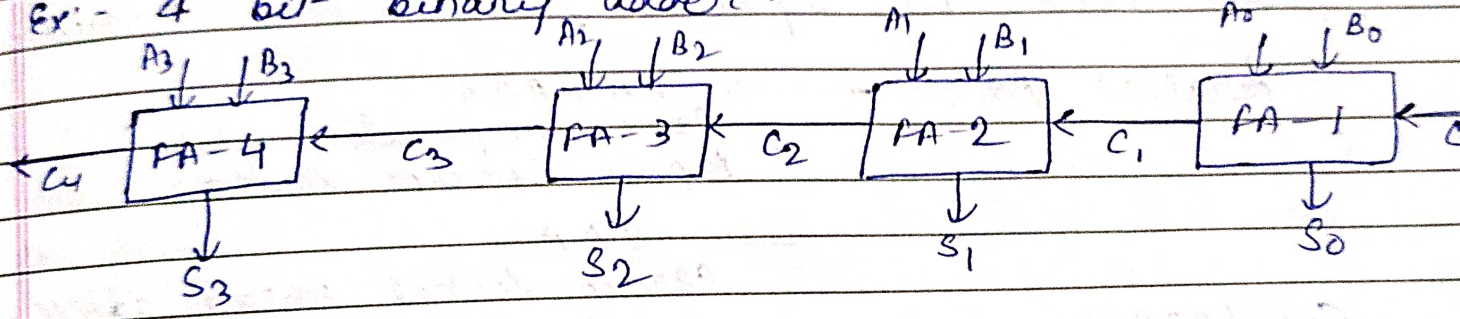
(5) Binary Adder

Serial adder

Parallel Adder
- CPA/RCA
- CLA

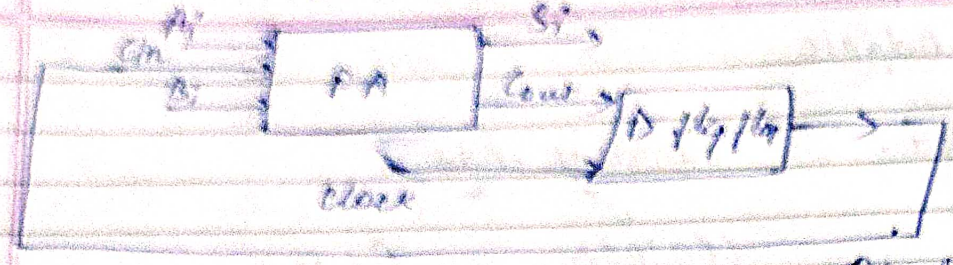
Binary adder:-
→ digital circuit which perform the add? of 2 binary no. of any length stored in 2 diff. registers.
→ micro operation add & sub are performed.
→ constructed with full adder circuit connected in ser
→ carry output of 1 full adder will be carry inpu of the next full adder.

Ex:- 4 bit binary adder.



Serial Adder:-
→ binary adder which perform add? of 2 binary no. serially bit by bit starting with LSB (Least Sign.
→ Add? of 1-bit pos? takes one block cycle.
" " n-bit " " n " "
→ At each cycle, carry produced by one-bit po should be stored in d-flipflop & it will be giv as input during the next cycle.
→ Sequential circuit.

Serial adder



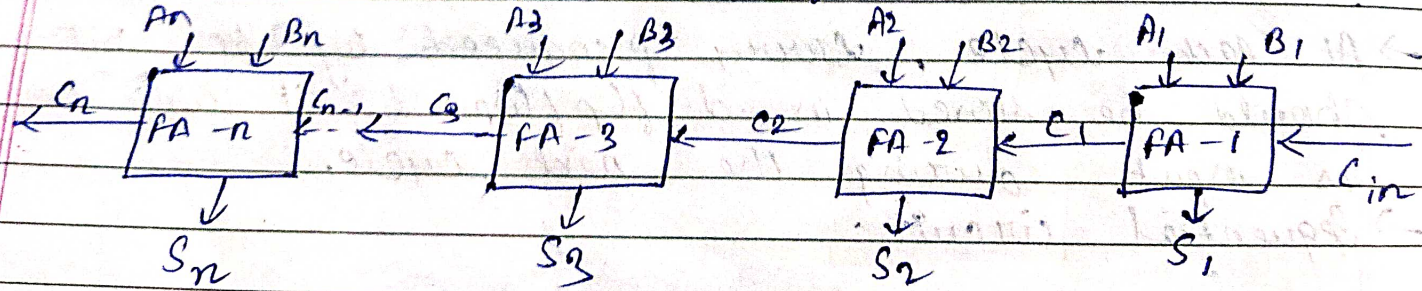
Advantage
→ very small bit it has only one full adder circuit
→ not expensive.

Disadvantage.
→ very slow
→ ∵ it takes n block cycle for add" of 2 bit n binary no.

Parallel Adder:-
→ a binary adder which adds all bit of 2 binary no. in one block cycle only.
→ has separate adder circuit for each bit.
→ for add" of 2 n-bit binary no. parallel adder need n separate full adder circuit.

Parallel Adder → CPA / RCA
Carry propagate adder
Ripple carry adder.
→ CLA
Carry looked Ahead adder.

CPA/RCA:-
→ for add" of n bit binary no., n full adder are req.
→ Each full adder carry output will be carry input for the next higher bit full adder.



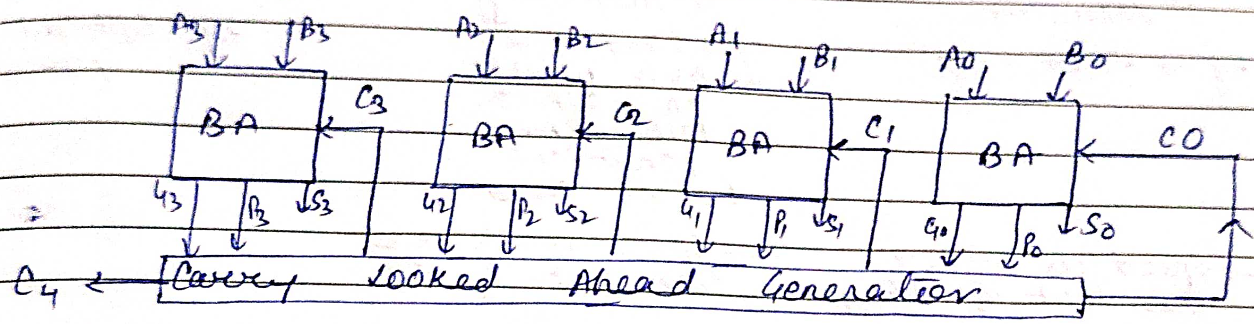
→ $\Delta \times n$
↓ time ↓ no. of delay.

Adv:
→ combination of circuit
→ faster than that of serial adder
- 1 clock cycle.

Disadv:
→ Expensive bcz n full adder are there
→ add^n time become large of no. of bit inc.

CLA :

→ high speed adder which adds 2 binary no. without waiting for the carry from the prev. stages.
→ In CLA, carry input of all stages are generated simultaneously.



→ max. delay of CLA is $6 \times \Delta$ (for G_i and P_i) generation delay = 1Δ, for C_i generation delay = 2Δ for S_i generator delay = 3Δ.

(6) Compilar | Interpreter

Compilar	Interpreter
→ is a system prog. that translate HLL into corres. eq. to LLL or MLL at a time.	→ a system that translate the HLL prog. into eq. LLL or MLL line by line.
→ takes less time	→ takes more time.
→ req. large space	→ req. small space.
→ aquracy is high	→ aquracy is low.
→ eg. C, C++, FORTRAN	→ eg. BASIC, PERL

⑦ Memory / Brain of a computer.

→ Storage device which stores data & program.

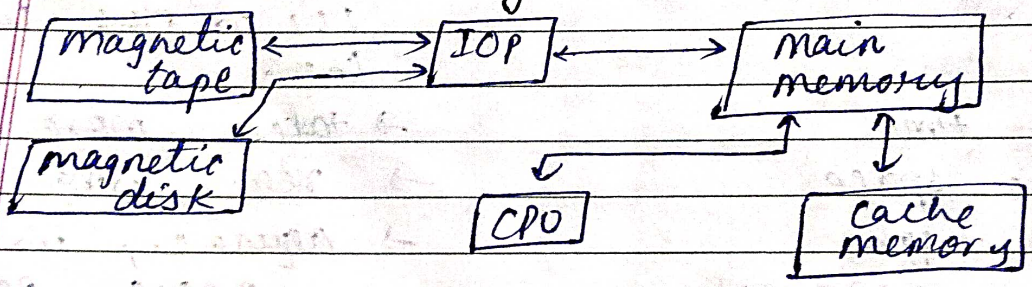
→ Data :- Value of attribute of an entity.
properties, features or characteristics
phy. existence, real life object or thing.

→ Features of memory :-
Speed, Capacity, Cost, Data Transfer rate / Bandwidth

→ Memory

1° memory	2° memory	3° memory
eg → RAM, ROM	eg → hard disk, DVD write, CD write, DVD RAM, pendrive, Punch card	eg: Optical disk, juke box
→ Speed is higher than that of 2°ary	→ Speed is slower than that of 1°	
→ Expensive	→ Cheap	
→ less capacity	→ high capacity	
→ connected directly to CPU.	→ not connected directly to CPU.	
→ used to store data i.e., likely to be inactive use.	→ used to store data that is not in active use.	

Memory Hierarchy



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Memory Pyramid