

## (1) Astable Multivibrator using 555 Timer

- 555 timer IC operated in astable mode.

The 3 int. resistances divide the volt.  $(R_1, R_2, R_3)$

into 3 parts. So,  $V_1 = 2V_{cc}/3$  ;

$V_2 = V_{cc}/3$  while the capacitor is changing.

and capacitor voltage is  $2V_{cc}/3$  and  $V_{cc}/3$ ,

the output of resistor of the

comparator undergoes a change in sign of their output, which is logic 0.

If the capacitor is charging & its voltage tends to rise

above  $2V_{cc}/3$ , comparator 1 output jumps to the saturation value,

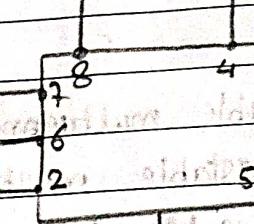
i.e., it is logic 1 at R input of flip-flop.

Similarly, if the capacitor is discharging & its voltage

tends to fall below  $V_{cc}/3$  & comparator 2 output

jumps to the saturation value for logic 1 at S input

of flip-flop.



## (2) Monostable Multivibrator using 555 Timer

-ve edge triggers the timer.

positive trigger

reset

output

input

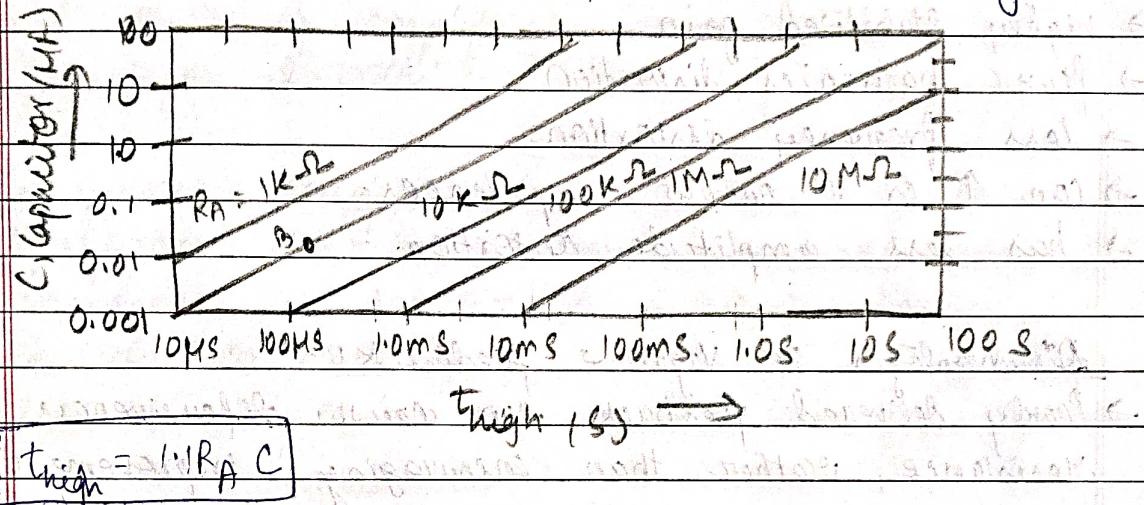
clock

reset

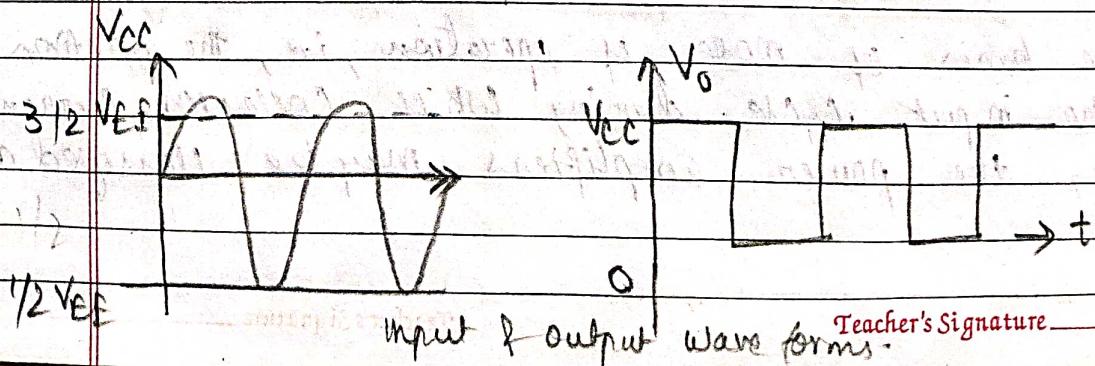
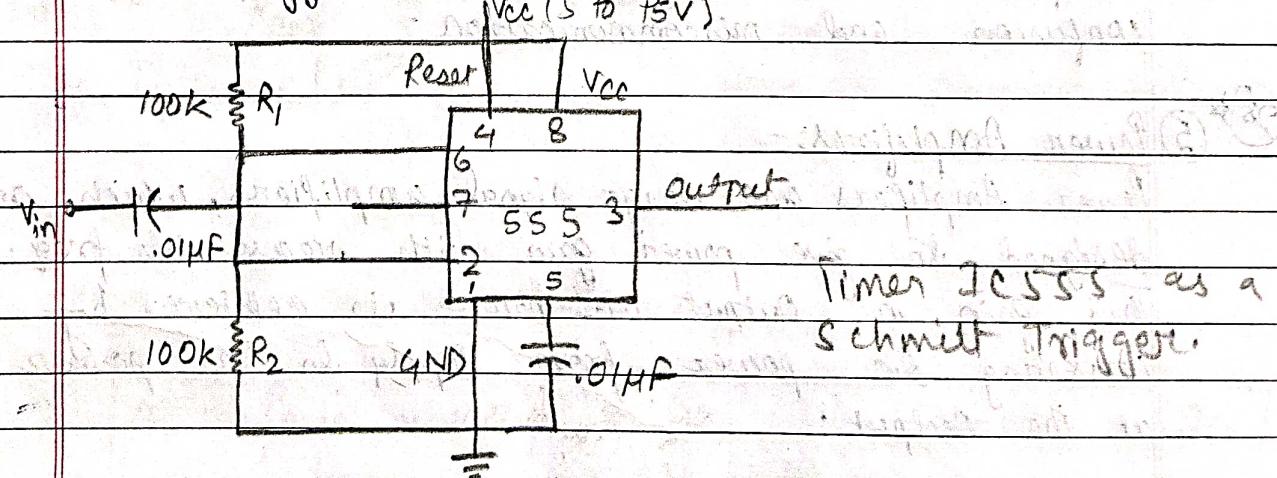
output

When a -ve going pulse is connected to trigger input (pin no. 2) the output goes high. The terminal 7 is shorted by capacitor C. When the voltage across the capacitor C comes  $\frac{2}{3} V_{cc}$ , the the upper comparator changes the output from high voltage value to low voltage value. The 3 internal resistances act as voltage dividers & it provides the bias voltages of  $(\frac{2}{3})V_{cc}$  to upper comparator &  $(\frac{1}{3})V_{cc}$  to lower comparator. ∵ these 2 voltages fix the necessary comparator threshold voltages, they also aids in determining the timing interval.

Graph of RC combinations for diff. time delay.



(3) Schmitt trigger circuit using 555 Timer.



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The input of 2 compilation threshold input (6) & trigger input (2) are connected together and externals biased at  $V_{CC}/2$ .  $\therefore$  a voltage divider formed by  $R_1$  and  $R_2$ . As upper comparator will trip at  $1/3 V_{CC}$  & lower comparator (2) at  $2/3 V_{CC}$ , the bias provided by resistances  $R_1$  &  $R_2$  is centered within these two thresholds.

The circuit can convert wave form of shape.

(27)

#### (4) Advantages of Negative feedback:-

- Reduces the size.
- highly stabilized gain
- fewer harmonics distortion
- less frequency distortion
- can ↑ or ↓ output impedance.
- has less amplitude distortion.

#### Disadvantages of Negative feedback:-

- Poorly delivered feedback can cause defensiveness and resistance, rather than encouraging improvement.
- Interpretation: feedback can be misinterpreted, causing confusion and miscommunication.

(28)

#### (5) Power Amplifiers:-

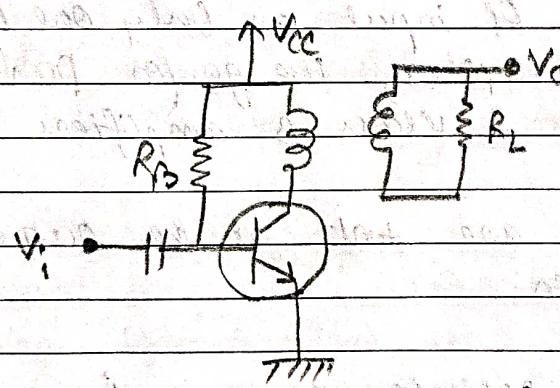
Power Amplifiers are large signal amplifiers, which are designed to give power gain with reasonable freq. This gain in output ac power is achieved by converting dc power from supply to ac power at the output.

On the basis of mode of operation, i.e., the portion of the input cycle during which collector current flows, the power amplifiers may be classified as

- (i) Class A power Amplifier  $\rightarrow$  When no collector current flows at all times during the full cycle of the signal, the power amplifier is known as class A -
- (ii) Class B power Amplifier  $\rightarrow$  When the collector current flows only during the two half cycle of the input signal
- (iii) Class C power Amplifier  $\rightarrow$  When no collector current flows for less than half cycle of the input signal
- (iv) Class AB power Amplifier  $\rightarrow$  if we combine the Class A and Class B amplifiers so as to utilize the advantages of both.

### (b) Transformer coupled Class A power Amplifiers.

Transformer coupling becomes necessary when the load impedance is smaller than the one needed in the collector for matching or, when the load is to be isolated & can't carry a dc collector current.

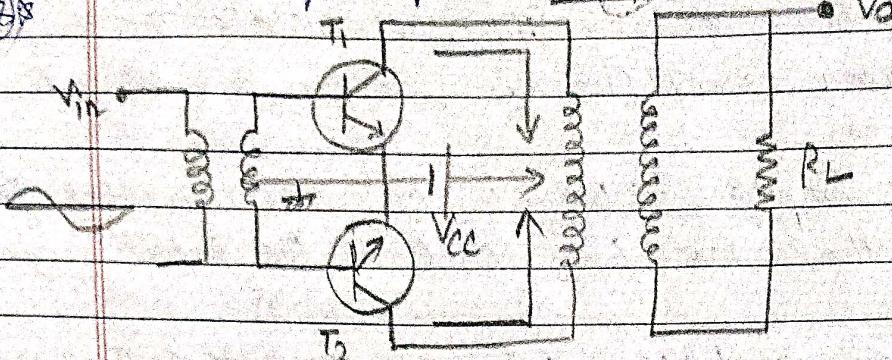


here, load is coupled with a  
Transformer

Maximum Conversion efficiency,

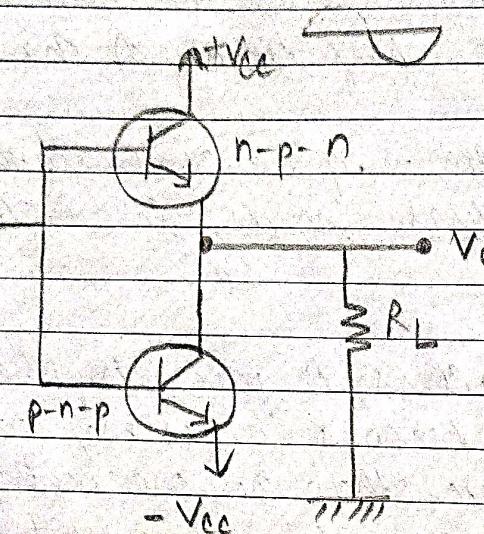
$$\eta = \frac{P_{o,ac}}{P_{i,dc}} \times 100\% = \frac{V_{cc}^2 / 2R_L}{V_{cc}^2 / R_L} \times 100\% = 50\%$$

## 7 Class B push-pull Amplifier



Push-Pull

Configuration



Complementary

Symmetry

push-pull

configuration

With only one class B amplifier, the output is not a faithful reproduction of input as only one half cycle is present. For both cycles, we go for push-pull arrangement - where 2 class B amplifiers are used for 2 half cycles.

No even harmonics are present at the output due to push-pull configuration.

When,  $T_1$  conducts, collector current  $i_c =$

$$i_{c1} = I_C + a_0 + a_1 \cos \omega t + a_2 \cos 2\omega t + a_3 \cos 3\omega t$$

When,  $T_2$  conducts, collector current  $i_c =$

$$i_{c2} = i_{c1} (\omega T + \pi) = I_C + a_0 - a_1 \cos \omega t + a_2 \cos^2 \omega t - a_3 \cos^3 \omega t$$

Total current,  $i_c = i_{c1} - i_{c2}$

as  $i_{c1}$  and  $i_{c2}$  flows in diff'nt directions.  
So, even order harmonics get ~~cancel~~ suppressed.

Efficiency:-

180° phase diff. exists so harmonic produced by each transistor cancel out thereby almost distortion free output is being obtained.

$$I_{C_1} = (I_{C_2} - I_C)$$

$$I_C = \frac{I_m}{\pi}$$

$$\text{So, } I_{dc} = \frac{I_m}{\pi}$$

So, total  $I_{dc}$  current for 2 transistors

$$I_{dc} = 2I_C = 2 \frac{I_m}{\pi}$$

$$P_{in(dc)} = V_{cc} \times I_{dc} = 2 \frac{I_m V_{cc}}{\pi}$$

AC power delivered to load,  $P_{(dc)} = \frac{V_m I_m}{2}$

Total collector dissipation.

$$P_{(dc)} = 2I_m \left( \frac{V_{cc}}{\pi} - \frac{V_m}{4} \right)$$

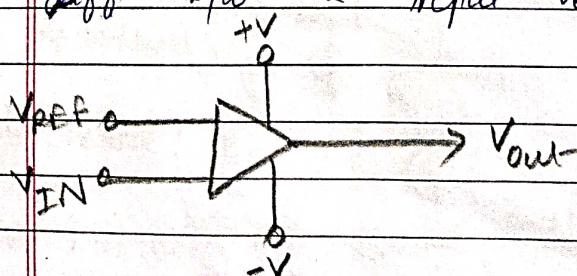
$$\therefore \eta(\text{overall}) = \frac{P_{(dc)}}{P_{in(dc)}} \times 100 = \frac{\left( \frac{V_m I_m}{2} \right)}{\left( \frac{2 I_m}{\pi} \right)} \times 100$$

Under ideal condition, max. Power in load =  $V_{cc}$

$$\text{Maxima} = \frac{\pi}{4} \times 100 = 78.5\%$$

⑧

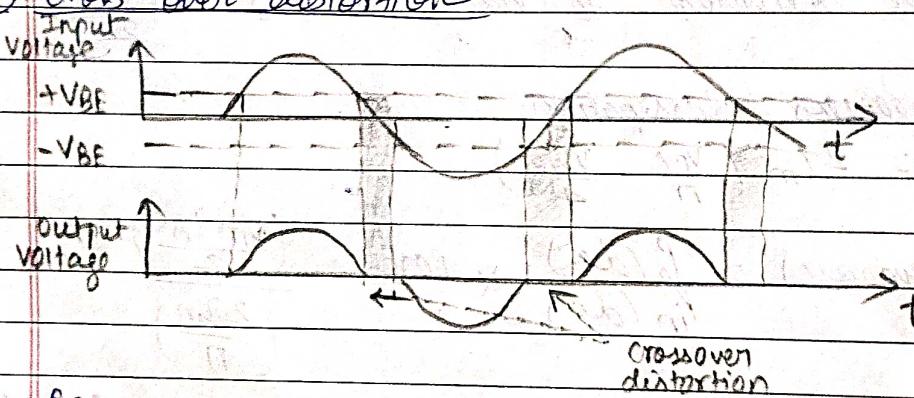
a) Voltage Comparator using Op-Amp.  
Voltage Comparator is an electronic circuit that compares 2 input voltages & lets you know which of the two is greater. It's easy to create a Voltage comparator from an op amp, bcz the polarity of the op-amp's output circuit depends on the polarity of the diff. b/w 2 input voltages.



In the voltage comparator circuit, 1<sup>st</sup> a reference voltage is applied to inverting input ( $V_+$ ); then the voltage to be compared with no reference voltage is applied to the non-inverting input. The output voltage depends on the value of input voltage relative to the reference voltage.

Input voltage	Output voltage
Less than Ref. voltage	-ve
Equal to Ref. volt.	0
Greater than Ref. volt.	+ve

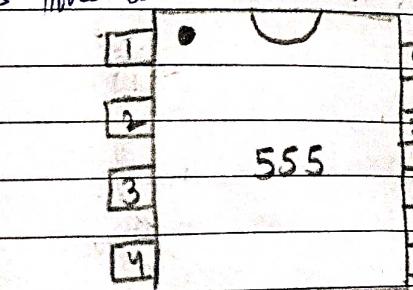
### (8) (b) Crossover distortion



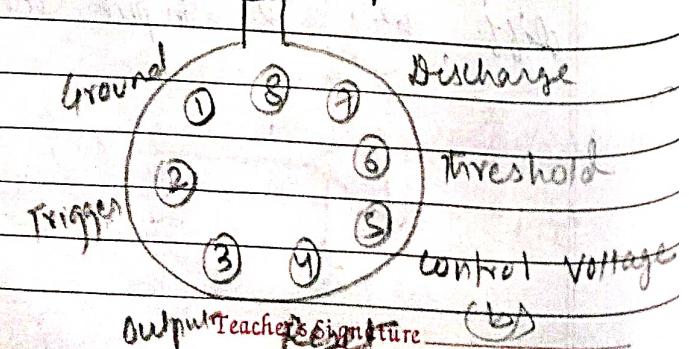
For Class B operation, the  $B$  junction voltage must be greater than cut-in voltage ( $V_{BE} \geq 0.65$  V) so that linear operation is guaranteed. Whenever there is a zero crossing at the input, we get output only after the input voltage reaches  $+V_{BE}$  (or  $-V_{BE}$  for the -ve half-cycle). This phenomenon results in a distortion which is known as crossover distortion.

### (8) (c) 555 Timer

555 Timer connection diag. (top view)



metal can package (top view)



(a)

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(b)

The IC 555 Timer is available in 2 package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP.

Imp. features of 555 Timer:-

- (1) Operating voltage  $\Rightarrow +5V$  to  $+18V$ .
- (2) Capacitor to source or sink current of  $200mA$ .
- (3) It has in both free-running (astable) & one shot (monostable) modes.
- (4) It has an adjustable duty cycle & timing is from microsec. through hours.
- (5) Operating temp. of SE 555  $\rightarrow -55^\circ$  to  $+125^\circ C$ .  
NE 555  $\rightarrow 0^\circ$  to  $+70^\circ C$ .
- (6) Very reliable, low cost & easy to use.

### Application of timer IC SE/NE 555

1. Monostable, astable multivibrator.

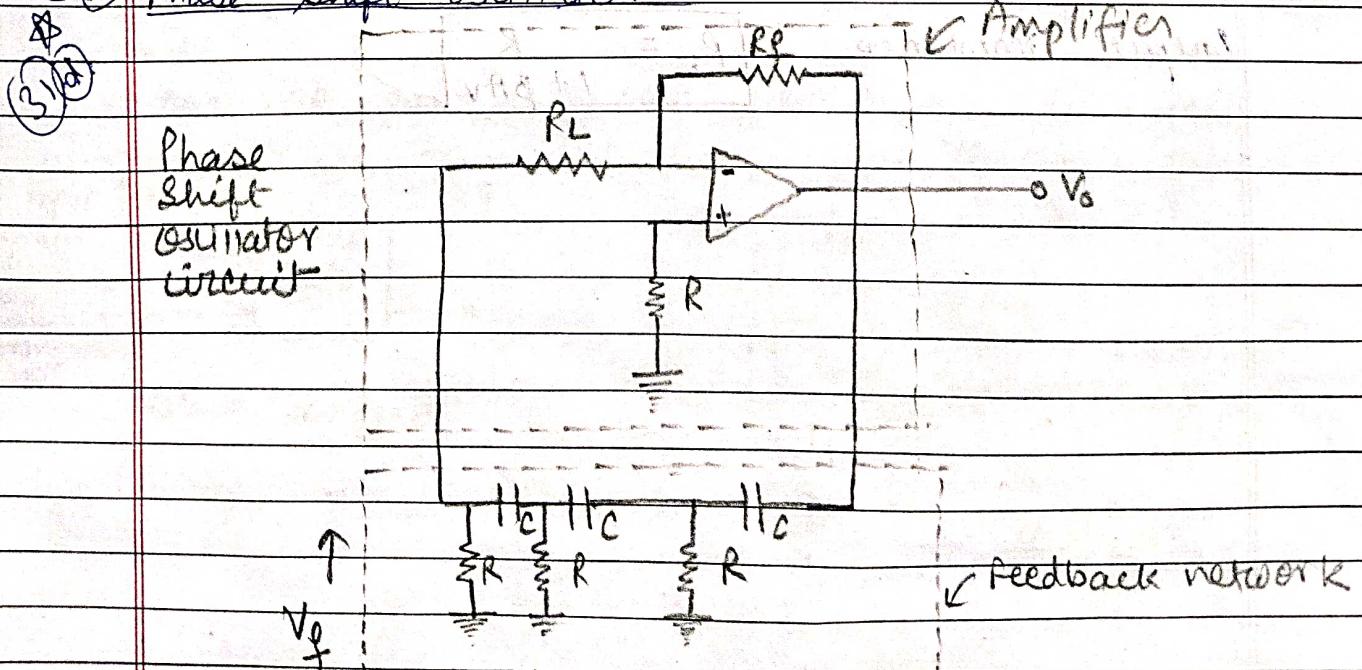
2. Digital logic probes.

3. DC to AC converters.

4. Pulse generation.

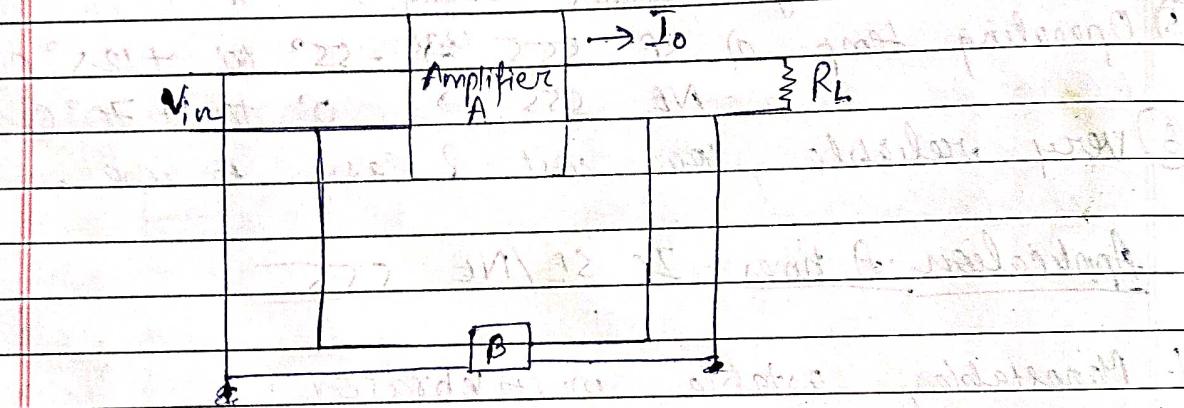
5. Waveform generator.

(6) Phase-shift oscillator  $\xrightarrow{\text{often used at audio frequencies}}$



Phase shift oscillator is a linear electronic circuit that produces a sine wave output. It consists of an inverting amplifier element such as a transistor or op amp with its output fed back to its input through a phase-shift network consisting of resistors & capacitors in a ladder network. The feedback network 'shifts' the phase of the amplifier output by  $180^\circ$  at the oscillation to give the feedback.

### (8e) Current shunt feedback



The above fig. is called current-shunt feedback. In this connection, a fraction of output current converted into a proportional voltage by the feedback network and this applied in coupled with input voltage.

Output resistance

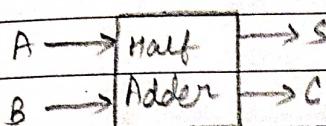
$$R_o = \frac{R}{1 + \beta A_v}$$

① Implement full adder circuit - using 2 half-adders.

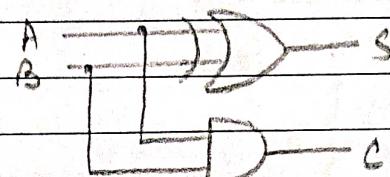
Write the truth table of half-subtractor.

→ Half Adder

- Combinational logic circuit designed to add 2 binary digits.
- Half Adder provides the output along with a carry.
- Designed by connecting an XOR gate & one AND gate.
- has 2 input terminals and 2 output terminals for S, C.



Block diagram



Circuit diagram.

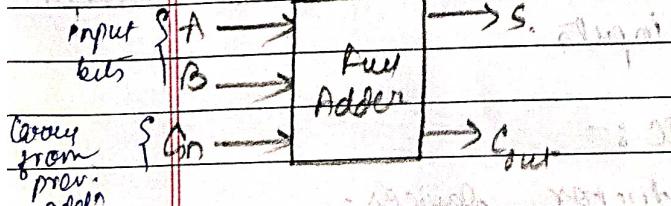
- Output of the XOR gate is Sum of 2 bits & output of AND gate is carry bit;
- Carry obtained in one add? will not be forwarded in next add.

$$\text{Output eq'st} \quad \text{Sum, } S = A \oplus B$$

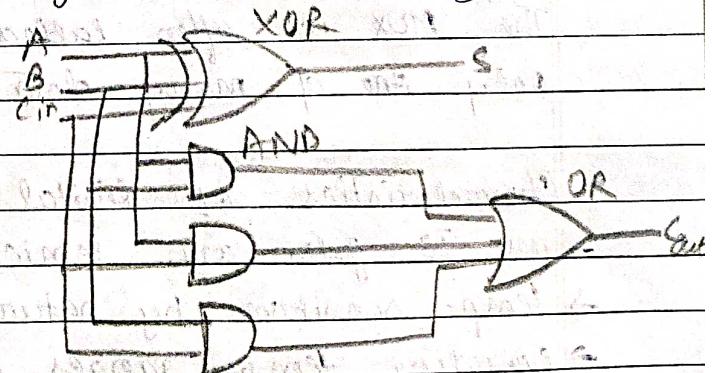
$$\text{Carry, } C = A \cdot B$$

→ Full Adder

- Combinational logic circuit, adds 2 binary digits & a carry bit, & produces a sum bit & carry bit as output.
- Full adder circuit adds 3 binary digits, where 2 are the inputs & one is the carry forwarded from previous add.
- One XOR gate, 3 AND gates & one OR gate.



Block diagram



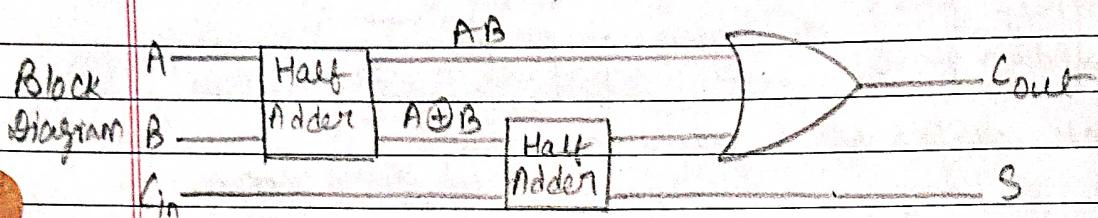
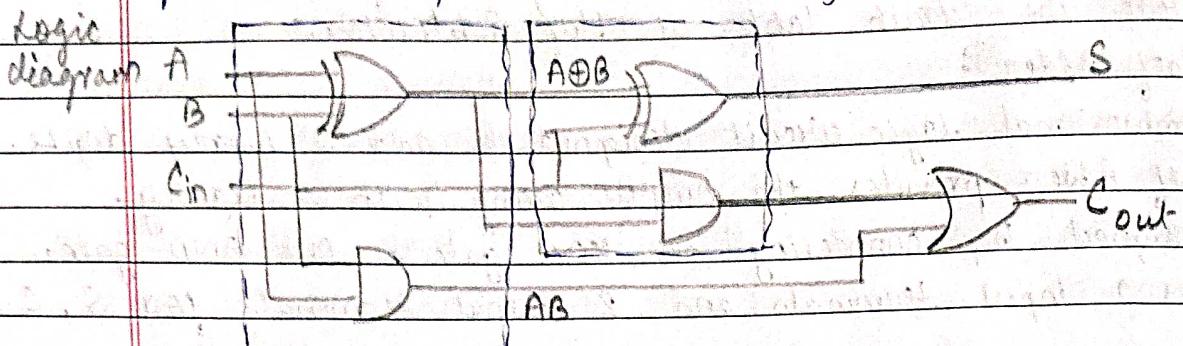
Circuit diagram

$$\text{Sum, } S = A \oplus B \oplus \text{Cin}$$

$$\text{Carry, } \text{Cout} = AB + AC_{\text{in}} + BC_{\text{in}}$$

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Implementation of Full Adder using 2 Half Adder:



We req. 2 XOR gates, 2 add AND gates & one OR gate for implementation of a full adder circuit using half adder.

\* Increased Propagation Delay  $\rightarrow$  Disadvantage

(2) What is Multiplexer? Why it is called data selector?

Write the imp. characteristics of digital IC:-

$\rightarrow$  A multiplexer (MUX) is a network device that allows one / more analog or digital input signals to travel together over the same communications transmission link.

The selection of a particular input data line for the output is decided on the basis of selection lines. The MUX is often called data Selector  $\therefore$  it selects only one of many data inputs.

Characteristics of digital IC :-

$\rightarrow$  all IC gates are semiconductor devices.

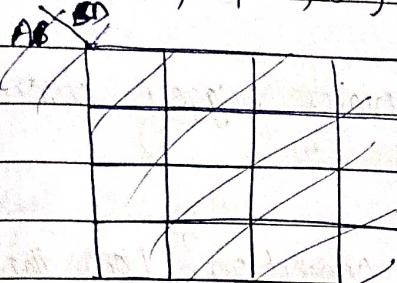
$\rightarrow$  temp. sensitive by nature.

$\rightarrow$  operating temp. ranges of an IC vary from  $0^\circ\text{C}$  to  $+70^\circ\text{C}$  for consumer & industrial applic.

temp. ranges from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  for military applications.

③ Implement the function  $F(A, B, C) = \sum m(1, 3, 5, 6)$  using decoder. Diff b/w Combinational circuit & Sequential circuit  
 $\rightarrow F(A, B, C) = \sum m(1, 3, 5, 6)$

K-map:-

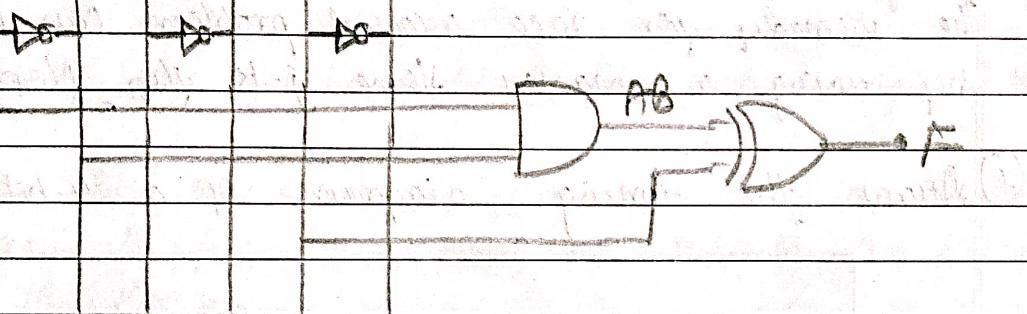


A	BC	$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	$B\bar{C}$
$\bar{A}=0$	0	1	1	1	3
$A=1$	4	1	5	7	1

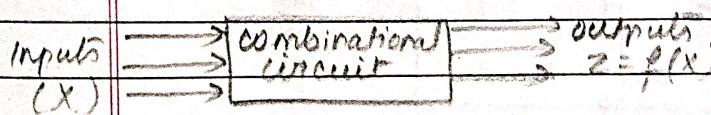
$$\begin{aligned}
 F &= \bar{A}C + \bar{B}C + A\bar{B}\bar{C} \\
 &= C(\bar{A} + \bar{B}) + A\bar{B}\bar{C} \\
 &= C(\bar{A}\bar{B}) + A\bar{B}\bar{C} \\
 &= AB\bar{C} + A\bar{B}\bar{C} \\
 &= AB \oplus C
 \end{aligned}$$

Implementation using Decoder:-

A    A    B     $\bar{B}$     C     $\bar{C}$

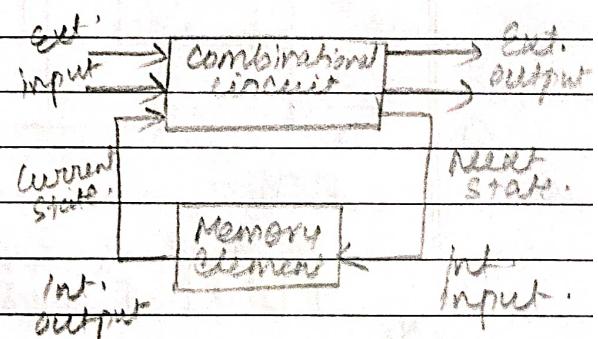


Combinational Circuit



- Output depends upon present state of inputs.

Sequential Circuit-



- Output depends not only on the ext. input but also on the history of inputs.

- Speed is fast.
- Time independent.
- don't have any memory element.
- easy to use & handle
- ex - Encoder, Decoder, MUX, DEMUX.

- Speed is slow.
- time dependent.
- have memory element.
- not easy to use & handle.

(4) Explain the operation of Monostable multivibrator using 555 Timer.

→ Check previous (2)

(5) Draw & explain Schmitt trigger circuit.

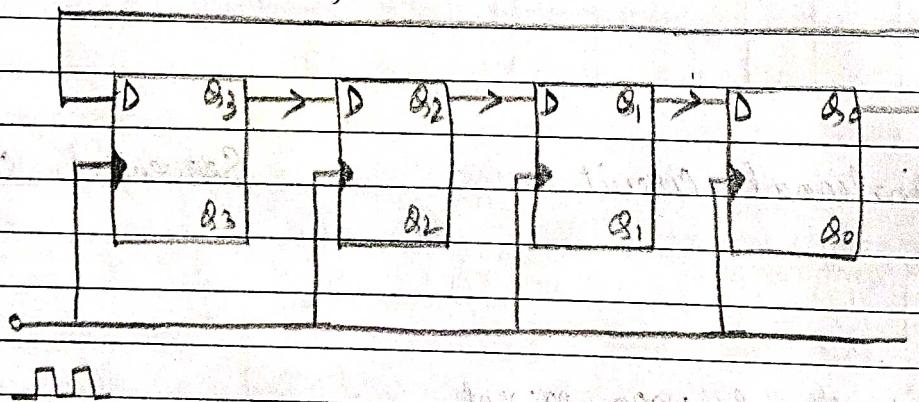
Check previous (3)

(6) What is race around condition? How this problem is solved by using master-slave flip-flop?

→ Race around condition occurs when both the inputs are high. And the output thus undergoes a transition state. For ex - consider the input values in a JK flip-flop; i.e.;  $J=K=1$ , the output  $Q=0$  in normal case will change to 1 and vice versa.

The remedy for race around problem can be eliminated by using a master-slave J-K flip flop.

(7) Draw the timing diagram of a 4-bit ring counter.



1 2 3 4 5 6 7 8

$Q_3$

$Q_2$

$Q_1$

$Q_0$

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AMBA

(8) Why Gray code is called reflected code?

In this case, a decimal no. is represent in <sup>binary</sup> form in such a way that each gray code no. differs from the preceding & succeeding no. by a single bit. Then it is called reflected code.

(9) A Wien bridge oscillator has a  $\omega$  of 1000 Hz and a capacitance of 100 pF. Find the resistance. If the amplifier gain is 10, obtain the ratio of the resistances in the other arms.

$$\rightarrow \omega = 10^3 \text{ Hz} ; C = (10^2 \times 10^{-12}) \text{ F} ; A = 10 ; R = ?$$

$$f = \frac{1}{2\pi CR} = \frac{0.159}{10^{-10} \times R} \Rightarrow 10^3 \times 10^{-10} \times R = 0.159$$

$$(0.159 \times 10^7) \Omega. \text{ Ans.}$$

(10) Implement the function of D flip-flop using J-K flip-flop.

$\rightarrow$  In order to create D flip-flop using J-K, inputs are given as D flip-flop inputs and outputs are taken from J-K flip-flop.

Conversion table:-

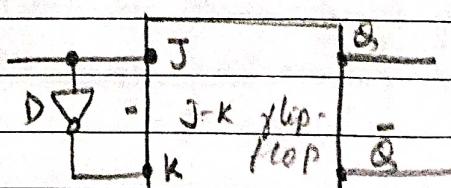
D	$Q_n$	$Q_{n-1}$	J	K
0	0	0	0	X
0	1	0	X	1
1	0	1	1	X
1	1	1	X	0

K Map sol. for J=0 & K=0

D	$Q_n$	$Q_{n-1}$
0	0	X
1	1	X

$$J=D \quad K=\bar{D}$$

Logic Diagram:-



D flip-flop using J-K flip flop.

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(1) Simplify the using K-map.

a)  $F(A, B, C, D) = \sum m(7, 9, 10, 11, 12, 13, 14, 15)$   
 b)  $F(A, B, C, D) = \Pi_m(0, 2, 3, 6, 7) + \Pi_d(8, 10, 11, 15)$

→  $F(A, B, C, D) = \sum m(7, 9, 10, 11, 12, 13, 14, 15)$  (II) POS  $\rightarrow 0 \rightarrow A$   
 $A \bar{B} \bar{C} \bar{D}$  00 01 110 10

00	0	,	3	2
01	4	,	1	5
11	8	7	11	10
10	1	12	13	14

(E) SOP  $\rightarrow 0 \rightarrow \bar{A}$   
 $A \bar{B} \bar{C} \bar{D}$  00 01 110 10

$$f = AB + AD + AC + \bar{B}CD$$

Q

b)  $F(A, B, C, D) = \Pi_m(0, 2, 3, 6, 7) + \Pi_d(8, 10, 11, 15)$

AB	CD	00	01	11	10
00	11	0	13	1	2
01	1	4	14	16	
11	X <sub>8</sub>	9	X <sub>5</sub>	X <sub>10</sub>	
10	X <sub>11</sub>	13	X <sub>15</sub>	14	

POS: -  $0 \rightarrow A$   
 $A \bar{B} \bar{C} \bar{D}$  00 01 110 10

$$(A+B+C+D) \cdot (A+\bar{C})$$

(2) Design 5:32 decoder using 2:4 and 3:8 decoders.

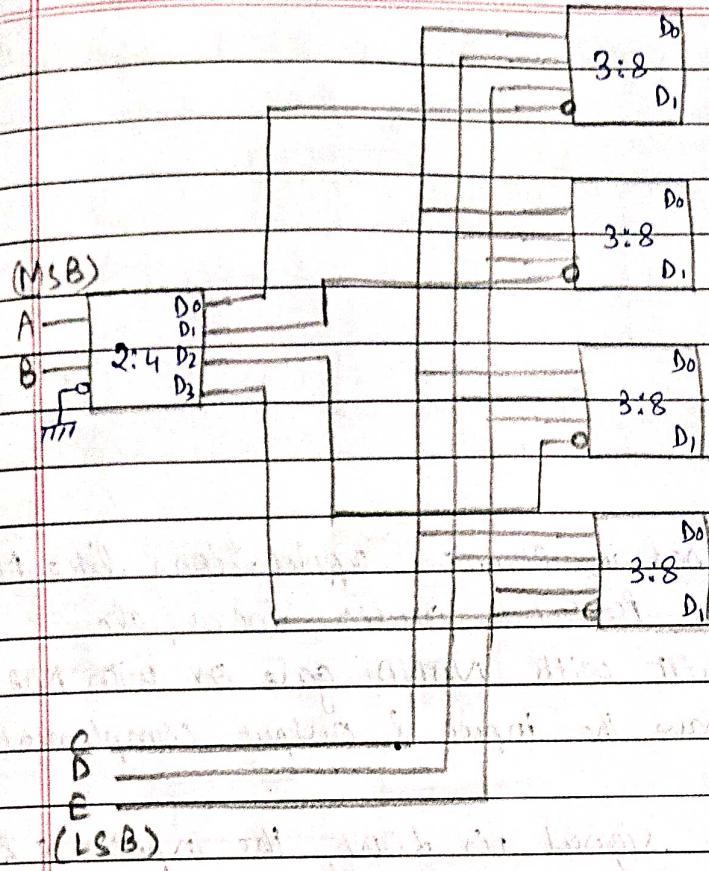
Let consider 5 input lines are ABCDE,

here, A is MSB & E is LSB.

1<sup>st</sup> we have to use 2:4 decoder whose inputs are A & B and output D<sub>0</sub>D<sub>1</sub>D<sub>2</sub>D<sub>3</sub> are enable inputs of 4 3x8 decoders respectively.

CDE are 3 input lines of 3x8 decoder, each of decoder produces 8 output lines.

are the 3 input lines of 3x8 decoder, each of decoder produces 8 output lines.



- Q) (13) Describe the working of S-R flip flop using truth table, logic diagram & excitation table.

S-R Flip Flop

Set Pin — S      Q      Output

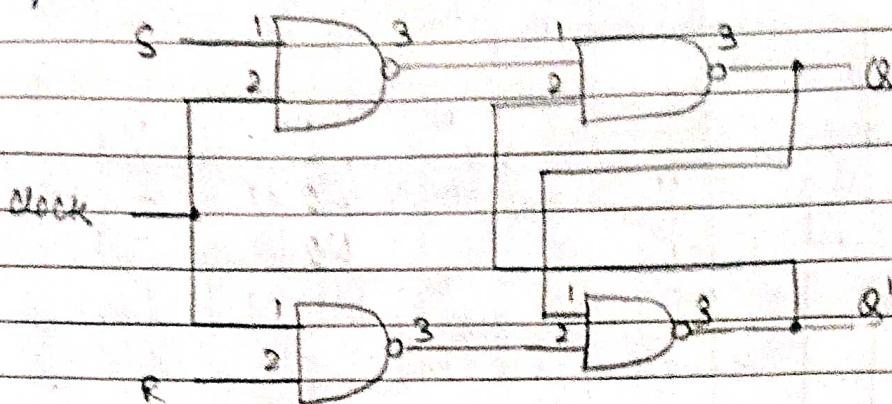
Reset Pin — R      Q'      Inverted Output

Clock

Truth Table

Clock State	Input		Output	
Clock	S	R	Q	Q'
Low	X	X	0	1
High	0	0	0	1
High	1	0	1	0
High	0	1	0	1
High	1	1	1	0

Diagram:



- SR Flip-flops were used in common applications like MP3 players, Home theaters, Portable audio docks, etc.
- SR latch can be built with NAND gate or with NOR gate.
- Either of them will have no input & output complemented to each other.
- Whenever the clock signal is low, the inputs S & R are never going to affect the output.  
The clock has to be high for the inputs to get active. Thus, SR flip-flop is a controlled Bi-Stable latch where the clock signal is the control signal.
- Again, this gets divided into two edge triggered SR flip flop & -ve edge triggered SR flip-flop.

(Q) What is triggering? How many types of triggering are there in sequential circuits?

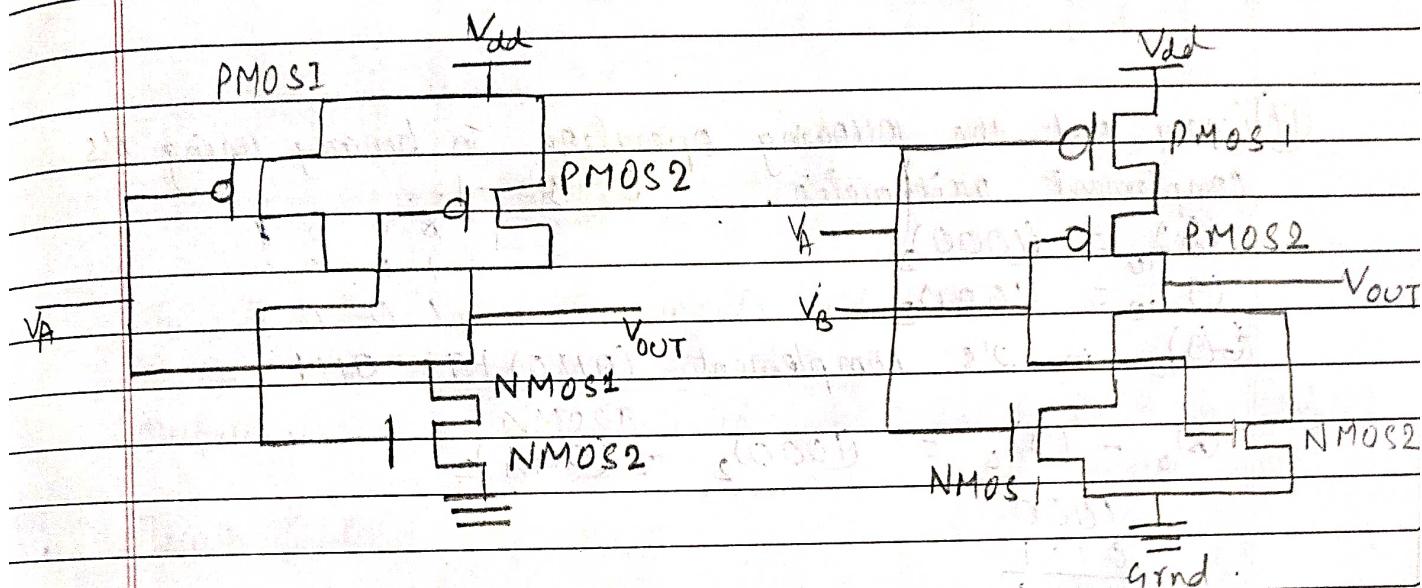
→ Triggering means excitation by some means. It is subdivided into 2 grp: namely (i) Edge triggering (ii) Level triggering.

Edge-triggering flip-flop → A flip-flop where state changes on the rising (+ve) or falling (-ve) edge of a clock pulse.

Level-triggering flip-flop → A flip-flop that is triggered (i.e., outputs respond to the inputs when level of the clock signal is appropriate.)

(15) Design NAND and NOR logic gates using CMOS technology.  
→ 2 input NAND gate → 2 input NOR gate.

$V_A$	$V_B$	$V_{OUT}$		$V_A$	$V_B$	$V_{OUT}$
LOW	LOW	HIGH		LOW	LOW	HIGH
LOW	HIGH	HIGH		LOW	HIGH	LOW
HIGH	LOW	HIGH		HIGH	LOW	LOW
HIGH	HIGH	LOW		HIGH	HIGH	LOW.



(16) Obtain the minimal POS expression of the following and implement the same using only NOR gates.

$$F(A, B, C, D) = \sum_m (1, 4, 7, 8, 9, 11) + \sum_d (0, 3, 5).$$

$\rightarrow$	POS :-	$0 \rightarrow A$	$AB \setminus 00$	$01$	$11$	$10$	$AB \setminus 00$	$01$	$11$	$10$	
		$1 \rightarrow A$	$00$	$X_0$	$(P_1)$	$X_2$	$2$	$00$	$X_0$	$(P_1)$	$X_2$
			$01$	$P_1$	$X_4$	$(P_5)$	$6$	$01$	$P_1$	$X_4$	$(P_5)$
			$11$	$11$	$8$	$11$	$11$	$10$	$11$	$n$	$12$
			$00$	$12$	$13$	$15$	$13$	$10$	$11$	$12$	$14$

$$F = (A+C) \cdot (A+\bar{D}) \cdot (\bar{A}+B+C) \cdot (\bar{A}+B+\bar{D})$$

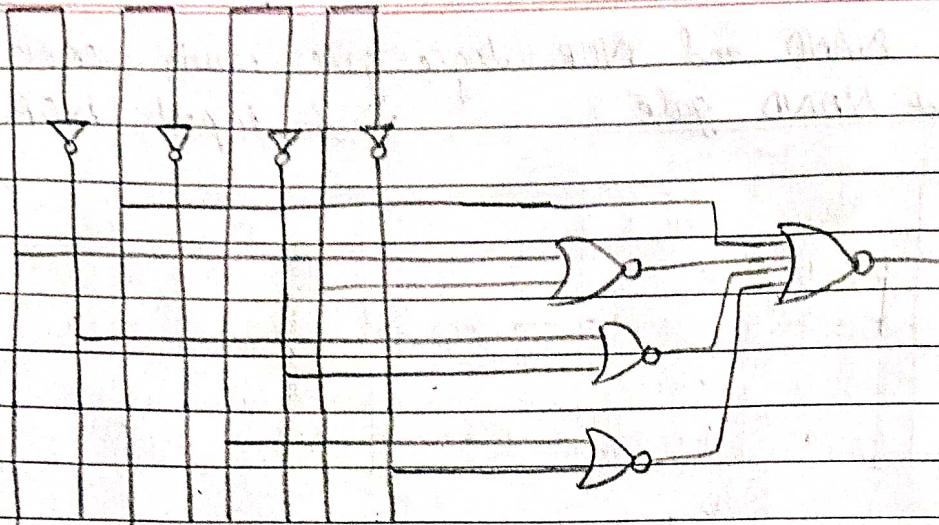
$$= \cancel{AA} + \cancel{AD} + \cancel{CA} + \cancel{CD}$$

$$B + AD + \bar{A}\bar{C} + \bar{C}\bar{D}$$

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A  $\bar{A}$  B  $\bar{B}$  C  $\bar{C}$  D  $\bar{D}$



- (17) Carry out the following operation in binary using 1's complement arithmetic.  $8 - 9 = -1$ .

$$(8)_{10} = (1000)_2$$

$$\begin{array}{r} 8 \ 4 \ 2 \ 0 \\ 1 \ 0 \ 0 \ 0 \end{array}$$

$$(9)_{10} = (1001)_2$$

$$\begin{array}{r} 8 \ 4 \ 2 \ 0 \\ 1 \ 0 \ 0 \ 1 \end{array}$$

$$(8-9)_{10} \text{ in 2's complement} = (0110) + 1 = 0111$$

$$(8)_{10} - (9)_{10} = (1000)_2 - (0111)_2$$

$$\begin{array}{r} 1000 \\ 0111 \\ \hline 0001 \end{array}$$

$[0-1=1^*$  (↑ → borrow)]

$$(0001)_2 = (-1)$$

- (18) Solve using K-map. Implement using NOR gates only.

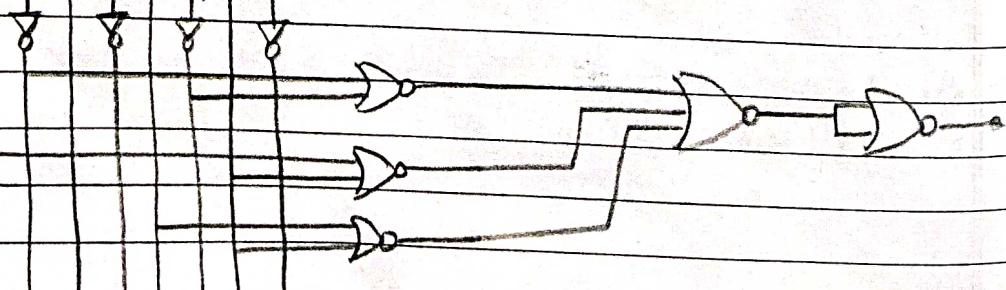
$$F(A, B, C, D) = \sum(0, 1, 4, 6, 7, 10, 11, 12, 13, 15) + d(2, 5, 9, 14)$$

SOP:  $- O \rightarrow \bar{A}$   $AB' \rightarrow 00$  or  $10 \rightarrow 00$

00	1	1	X	0
01	X	1	1	0
10	1	0	1	X

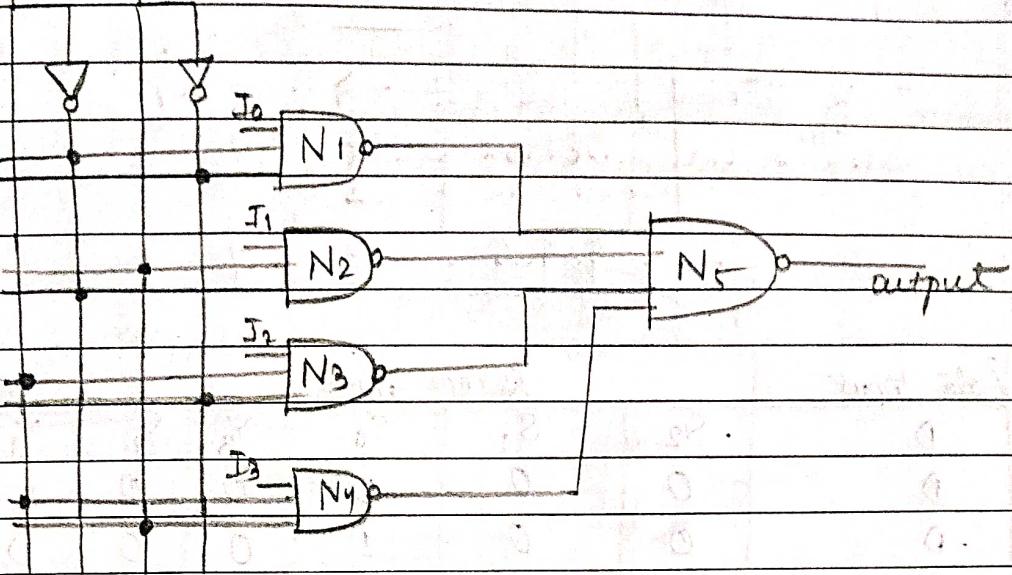
$$F = (\bar{A} \cdot \bar{C}) + (B) + (AD) + \bar{CD}$$

A  $\bar{A}$  B  $\bar{B}$  C  $\bar{C}$  D  $\bar{D}$



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(19) Explain the working principle of 4:1 MUX with a truth table.  
Realize it using NAND gates only.

 $A$  $\bar{A}$  $B$  $\bar{B}$ 

$I_0, I_1, I_2, I_3$  are inputs of MUX.

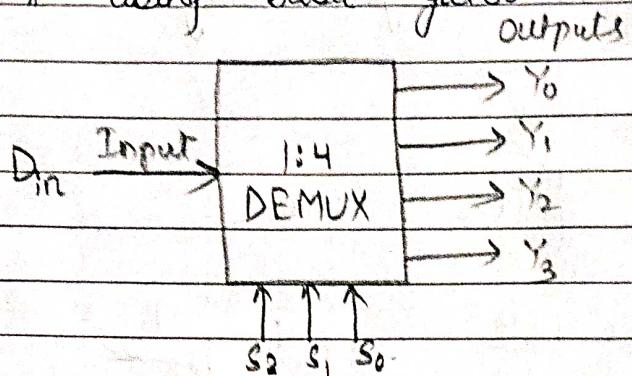
$A, B$  are control input.

Output is,  $I_0\bar{A}\bar{B} \cdot I_1\bar{A}B \cdot I_2A\bar{B} \cdot I_3AB = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2A\bar{B} + I_3AB$

Truth Table

Select input-		Enable input	Inputs				Outputs
$S_1$	$S_0$	$E$	$I_0$	$I_1$	$I_2$	$I_3$	$Y$
X	X	1	X	X	X	X	0
0	0	0	0	0	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

(20) Explain the working principle of 1:4 DEMUX with truth table.  
Realize it using basic gates.



Data Input	Select Inputs			Outputs			
D	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	Y <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>
D	0	0	0	0	0	0	D
D	0	0	1	0	0	D	0
D	0	1	0	0	0	D	0
D	0	1	1	D	0	0	0
D	1	0	0	0	0	0	0
D	1	0	1	0	0	0	0
D	1	1	0	0	0	D	0
D	1	1	1	0	0	0	0

Truth Table shows the equation:-

$$Y_0 = D \bar{S}_2 \bar{S}_1 \bar{S}_0$$

$$Y_1 = D \bar{S}_2 \bar{S}_1 S_0$$

$$Y_2 = D \bar{S}_2 S_1 \bar{S}_0$$

$$Y_3 = D S_2 \bar{S}_1 \bar{S}_0$$

(21) Implement your adder using 3x8 decoder with all active

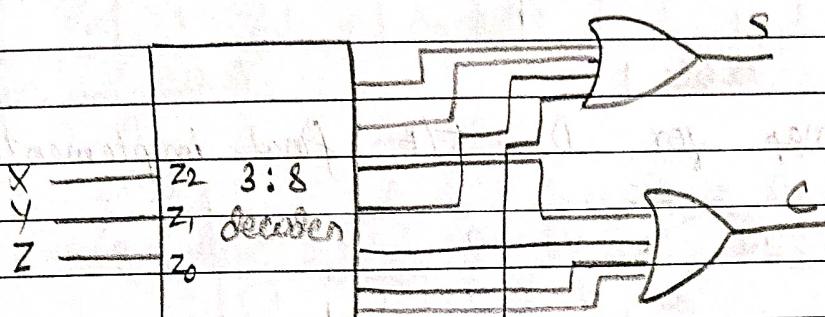
The fig. shows the block diagram of a 1-to-4 demultiplexer that consists of single input D, 3 select inputs S<sub>2</sub>, S<sub>1</sub> and S<sub>0</sub> and 4 outputs from Y<sub>0</sub> to Y<sub>3</sub>. It is also called as 1-to-4 demultiplexer due to 3 select input lines. It distributes one input line to one of 4 output lines depending on the combination of select inputs.

(22) Implement full-adder using 3x8 decoder with all active-low outputs & one additional logic gate if req.

$$S(x, y, z) = \sum m(1, 2, 4, 7) = \text{Sum}$$

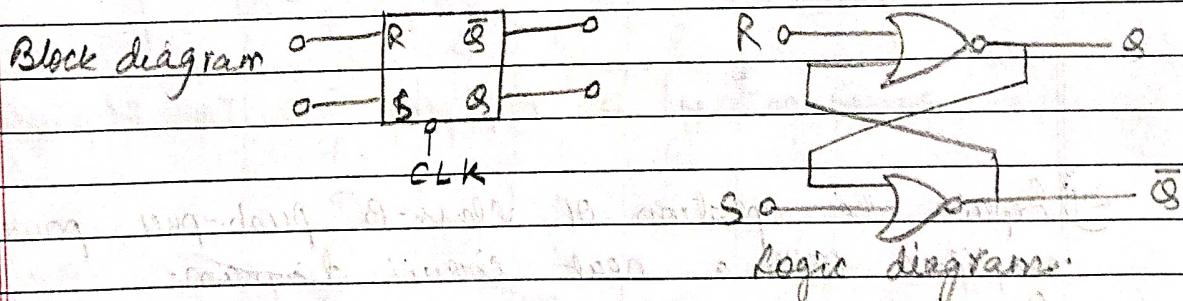
$$C(x, y, z) = \sum m(3, 5, 6, 7) = \text{Carry}$$

∴ there are 3 inputs and a total of 8 midterms we need a 3 to 8 decoder. The implementation is shown as:-



(23) a) Write truth table, circuit diagram and timing diagram of SR flip-flop using NOR gate.

→ RS flip-flop used as restoring information. It has 2 stable states, which can be achieved by giving proper inputs to R and S inputs. The flip-flop will assume one of its 2 stable states depending upon any asymmetry in the circuit.



Truth Table:

Inputs		Outputs	Mode	
S	R	Q	$\bar{Q}$	
0	0	0	1	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	-	-	Prohibited

b) Convert D Flip-flop into JK flip-flop.

The truth table of JK flip-flop & characteristic table for D flip flop is shown :-

J	K	$Q_{n+1}$	$Q_n \rightarrow Q_{n+1}$	D
0	0	$Q_n$	$0 \rightarrow 0$	0
0	1	0	$0 \rightarrow 1$	1
1	0	1	$1 \rightarrow 0$	0
1	1	$Q_n$	$1 \rightarrow 1$	1

Table 1

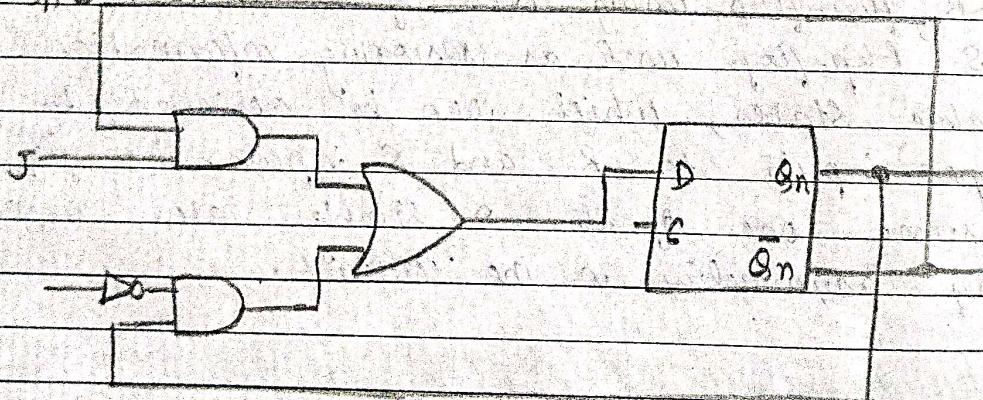
Table 2

The K-map for D F/F final implementation :-

J \ K $Q_n$		00 01 11 10			
		00	01	11	10
0	0	0	1	1	1
	1	0	0	1	0

$$D = KQ_n + \bar{J}K\bar{Q}_n$$

$$D = \bar{Q}_n J + Q_n K$$



Conversion of D flip-flop to JK flip-flop.

(24) Explain the operation of class-B push-pull power amplifier (with a neat circuit diagram).

Determine its collector circuit efficiency.

Explain why even harmonics are not present in push-pull amplifier.

→ 1<sup>st</sup> part → Check previous → (7)

2<sup>nd</sup> part → Check previous → (7)

3<sup>rd</sup> part → But the 2 transistors work in tandem to cancel out any even harmonics that may be there in the output signal.

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(25) Design & implement a comparator circuit, which can compare 2 3-bit binary numbers.

Let  $A = A_2 A_1 A_0$        $A, B$  are 2 inputs.

$B = B_2 B_1 B_0$

$$E_0 = \bar{B}_0 \bar{A}_1 + \bar{B}_0 A_0$$

$$E_1 = \bar{B}_1 \bar{A}_1 + B_1 A_1$$

$$E_2 = \bar{B}_2 \bar{A}_2 + B_2 A_2$$

where,

$$A = B, E = E_0, E_1, E_2$$

$$(A > B), F = A_2 \bar{B}_2 + E_2 A_1 \bar{B}_1 + E_2 E_1 \bar{A}_0 B_0$$

$$(A < B), G = \bar{A}_2 B_2 + E_2 \bar{A}_1 B_1 + E_2 E_1 \bar{A}_0 B_0$$

Simplify the Boolean function using Quine McCluskey method.

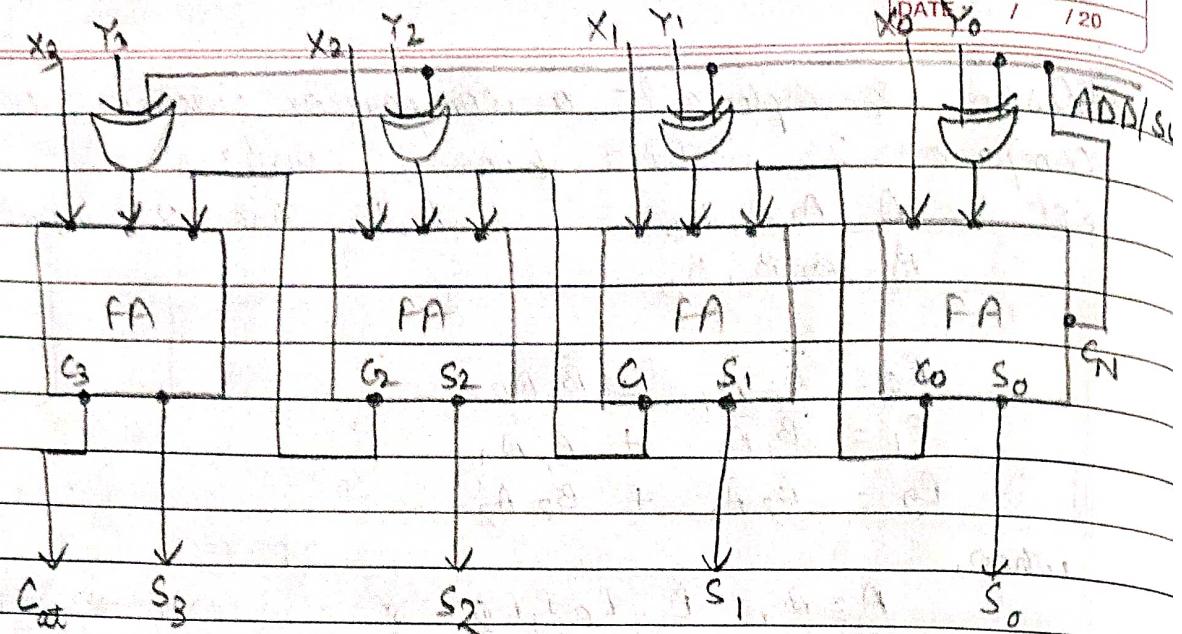
$$F = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$$

$$\rightarrow F = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$$

Primary representation of minterm.

Minterm	A	B	C	D
1	0	0	0	1
3	0	0	1	0
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0

Design a 3 bit binary parallel combined ADDER SUBTRACTOR circuit.



4-bit parallel adder / Subtractor.

It has 2 4-bit  $X_3 X_2 X_1 X_0$  and  $Y_3 Y_2 Y_1 Y_0$ .

The ADD / SUB control line connected with Add? / Subtract. The EX-OR gate are used Control Inverses. The circuit functions as a 4-bit adder resulting in Sum  $S_3 S_2 S_1 S_0$ .

(26) What is Barkhausen Criteria for a feedback amplifier to function as an oscillator? Give a neat circuit diagram of Wien bridge oscillator & explain how it works. Find an expression for the  $\omega$  of oscillation of the astable multivibrator.

→ For a the feedback system the overall gain can be written as

$$A_f = \frac{A}{1 - AB}$$

$A$  = gain of int. amplifier.

$B$  = feedback ratio.

$AB$  = loop gain

If  $AB = 1$ , from this eq?  $A_f \rightarrow \infty$ .

The amplifier then gives an output voltage without requiring any externally applied input voltage.

⇒ Amplifier becomes an oscillator.

This condition of unity loop gain, i.e.,  $AB = 1$  is called Barkhausen criterion.

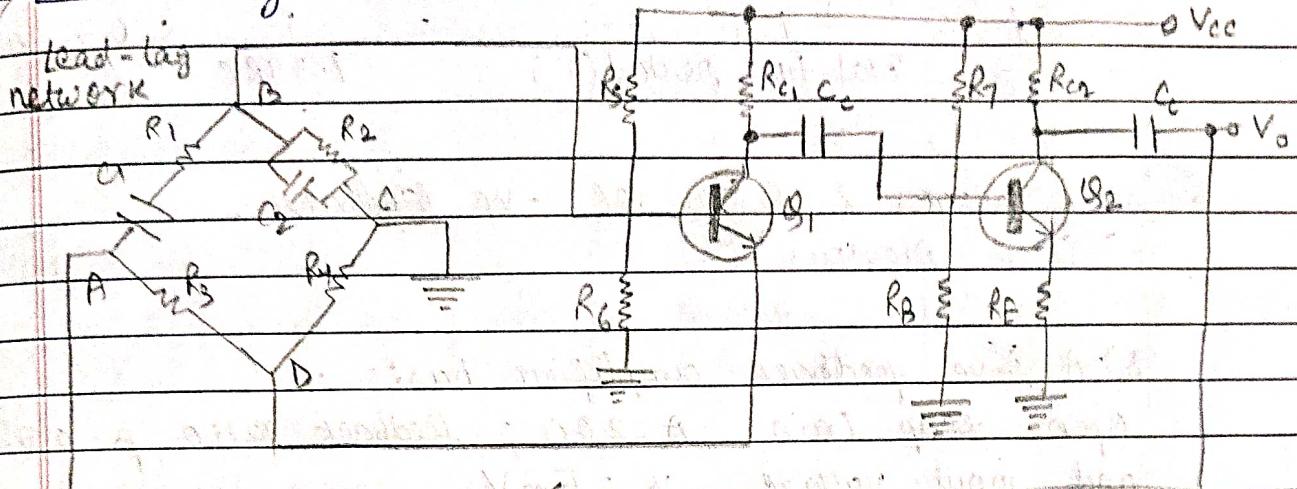
$|AB| = 1$ , phase angle of  $AB$  is multiple of  $360^\circ$ . Teacher's Signature

∴ the basic conditions for oscillation in a feedback amplifier are:-

(i) the feedback must be regenerative

(ii) loop gain must be unity

### → Wien-Bridge Oscillator



Feedback Signal

The circuit consists of a two-stage RC coupled amplifier which provides a phase shift of  $360^\circ$  or  $0^\circ$ .

A balanced bridge is used as the feedback network which has no need to provide any add'l phase shift.

The feedback network consists of a lead-lag network ( $R_1 - R_2 - C_1 - C_2$ ) and a voltage divider ( $R_3 - R_4$ ).

The lead lag network provides a +ve feedback to the input of the 1<sup>st</sup> stage and the voltage divider provides a -ve feedback to the emitter of  $\beta_1$ .

If the bridge is balanced,

$$\frac{R_3}{R_4} = \frac{(R_1 - jX_{C_1})}{(R_2 - jX_{C_2})} \cdot \frac{SR_2(-jX_{C_2})}{(R_2 - jX_{C_2})}$$

$X_{C_1}$  and  $X_{C_2}$  = reactance of capacitors.

$$\omega_0 \text{ of oscillation: } \omega_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

if  $R_1 = R_2 = R$ , then,

$$C_1 = C_2 = C$$

$$\omega_0 = \frac{1}{2\pi R C}$$

The ratio of  $R_3$  to  $R_4 > 2$  will provide a suff. gain for the circuit to oscillate at the desired frequency. This oscillator is used in commercial audio signal generators.

→ Frequency of astable multivibrator:

$$f = \frac{1}{1.39RC} = \frac{1}{RC} = 0.7 \text{ Hz.}$$

(27) (a) Advantages & disadv. of -ve feedback.

→ Check previous (4)

b) A -ve feedback amplifier has:-

Open loop gain  $A = 200$ ; feedback ratio  $\beta = 0.02$  and input voltage  $V_i = 5 \text{ mV}$ .

Compute :- (i) Gain with feedback (ii) feedback factor  
(iii) Output voltage (iv) feedback voltage.

$$\rightarrow (i) A_f = \frac{A}{1 + AB} = \frac{200}{1 + 200 \times 0.2} = \frac{200}{1 + 4} = 40$$

$$(iii) \text{Gain} = \frac{V_o}{V_m} = 200 = \frac{V_o}{5 \times 10^{-3}} \Rightarrow V_o = 10^3 \times 10^{-3} = 1 \text{ V}$$

$$(iii) \text{Feedback factor} = \beta_{AV} = 200 \times 0.02 = 4$$

(28) (a) Power amplifier. Types of classification, Operation of Class B push-pull amplifier.

(b) Cross-over distortion.

→ Check previous (3), (2), (8)(b).

(29) (a) Determine minterm and maxterm. What is canonical form?

→ A sum term contains all the K variables of the function in either complemented or not is called Max term & complement of max terms is called min term.

Each individual term in a standard (canonical) SOP form is called Minterm and each individual term in a standard (canonical) POS form is called max-

Representing the Boolean expression in terms of minterm allows us to introduce a very convenient shorthand notation.

No:	Variables			Minterms	Maxterms
	A	B	C	$m_i$ :	$M_i$ :
0	0	0	0	$\bar{A} \cdot \bar{B} \cdot \bar{C} = m_0$	$A + B + C = M_0$
1	0	0	1	$\bar{A} \cdot \bar{B} \cdot C = m_1$	$A + B + \bar{C} = M_1$
2	0	1	0	$\bar{A} \cdot B \cdot \bar{C} = m_2$	$A + \bar{B} + C = M_2$
3	0	1	1	$\bar{A} \cdot B \cdot C = m_3$	$A + \bar{B} + \bar{C} = M_3$
4	1	0	0	$A \cdot \bar{B} \cdot \bar{C} = m_4$	$\bar{A} + B + C = M_4$
5	1	0	1	$A \cdot \bar{B} \cdot C = m_5$	$\bar{A} + B + \bar{C} = M_5$
6	1	1	0	$A \cdot B \cdot \bar{C} = m_6$	$\bar{A} + \bar{B} + C = M_6$
7	1	1	1	$A \cdot B \cdot C = m_7$	$\bar{A} + \bar{B} + \bar{C} = M_7$

### Canonical form:-

In Boolean algebra, any Boolean function can be expressed in a canonical form using the dual concepts of minterms and maxterms.

Minterms are called products bcz they are the logical AND of a set of variables, and maxterms are called sum bcz they are the logical OR of a set of variables.

b) Minimize the following expressions using K-map.

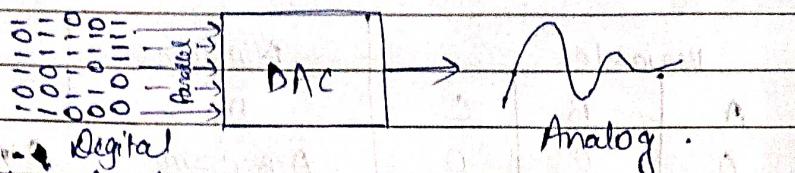
$$f(A, B, C, D) = \Sigma m(3, 4, 5, 6, 7, 12, 13, 14, 15)$$

$$\text{SOP: } 0 \rightarrow A \\ 1 \rightarrow A.$$

		AB	CD	00	01	11	10
		00		0	1	$\boxed{1}_3$	2
		01		$\boxed{1}_4$	$1_5$	$\boxed{1}_7$	$1_6$
		11		$\boxed{1}_{12}$	$1_{13}$	$1_{15}$	$1_{14}$
		10		8	9	11	10

Q6) a) Explain the operation of a D/A converter.

→ D/A converters convert digital signals into analog format.



Evenly spaced discontinuous values.  
Temporarily discrete, quantitatively, discrete.

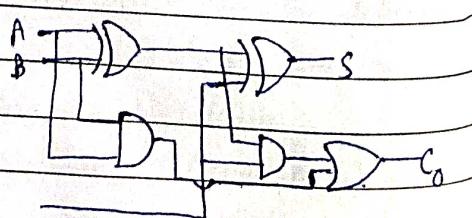
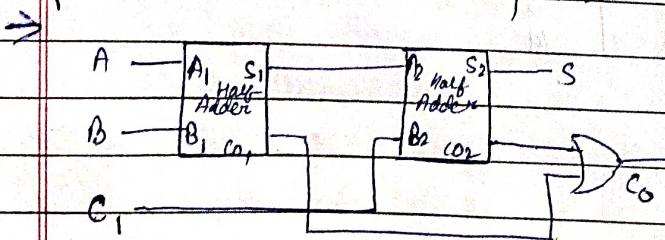
### Basic operations

- A D/A converter takes a precise no. and converts it into a physical quantity.
- D/A converters are often used to convert finite precision time series data to a continually varying physical signal.
- A D/A converter reconstructs original signals so that its bandwidth meets certain requirements.

b) Advantages of R-2R type D/A converter over other type of D/A converter?

- easier to build accurately as only 2 precious metal film resistors are required.
- No. of bits can be expanded by adding many sections of same R-2R values.
- Due to small resistance spread only 2: the R-2R ladder can be fabricated monolithically with high accuracy & stability.
- it uses only diff. resistor values.
- inherently fast & don't require expensive oversampling.

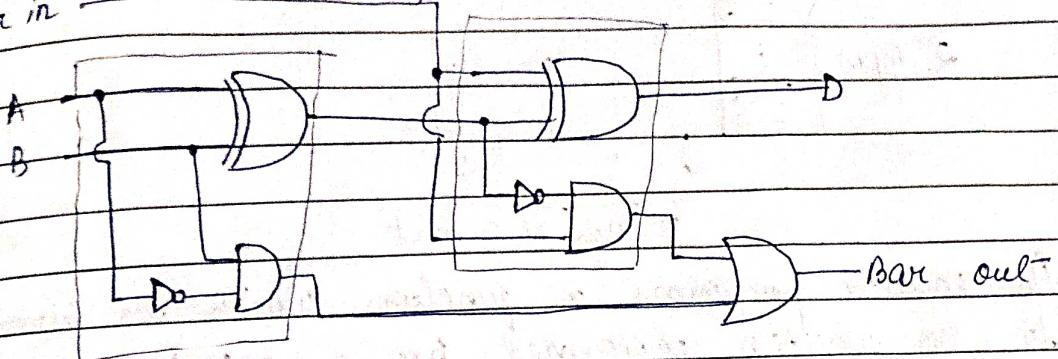
c) Draw circuit of a full adder. How you obtain a full subtractor using 2 half subtractor?



Block diagram of full adder circuit using half adder circuit.

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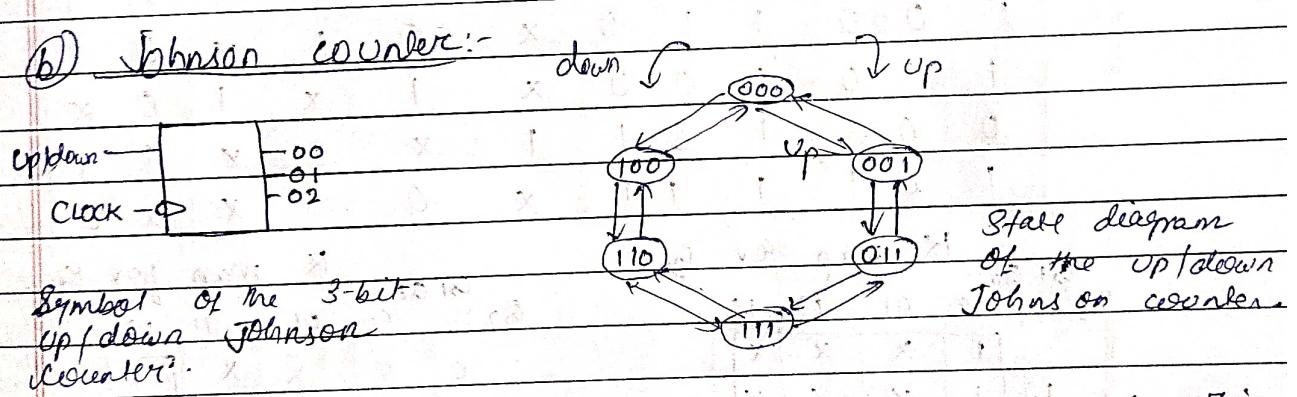
full subtractor using 2 half subtractor  
Bar in



- 3) Short notes on:- (a) Gray code (b) Johnson counter.  
(c) current shunt feedback. (d) Encoder (e) Phase shift oscillator.

→ (a) Gray code:- It is a non-weighted code. In this code a decimal no. is represented in binary form in such a way that each gray code no. differs from the preceding & succeeding no. by a single bit. This code is a reflected code.

### (b) Johnson counter:-



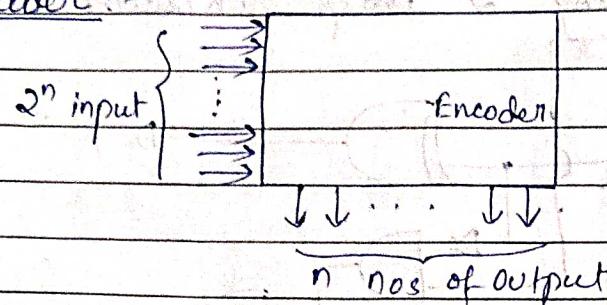
The counter has an asynchronous reset input which brings the outputs to 0 as soon as the RESET signal is asserted. The counter counts at the negedge of the clock.

When the UP input is high, the counter counts in one direction & when UP is low, it counts in the other direction.

- (d) Phase Shift oscillator:- Check previous

(8)(d)

## (C) Encoder



An encoder performs a function which is inverse to the function performed by a decoder.

An encoder has  $2^n$  nos of input and  $n$  nos of output line. The output line generates the binary code for  $2^n$  input variables.

## (32) Design a MOD 4 synchronous counter using J-K flip-flops and implement it.

$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$
1	1	1	1	0	0	X	0	X	1	X	1
1	0	0	1	1	0	X	0	1	X	0	X
1	1	0	0	0	0	X	1	X	1	0	X
0	0	0	1	0	1	1	X	0	X	1	X
1	0	1	1	1	1	X	0	1	X	X	0

K-map for  $J_2$ 

$Q_2$	00	01	11	10
0	1	X	X	X
1	1	X	X	X

K map for  $K_2$ 

$Q_2$	00	01	11	10
0	X	X	X	X
1	0	0	0	0

$$J_2 = 1$$

$Q_2$	00	01	11	10
0	0	X	X	X
1	1	1	X	X

$$K_2 = Q_1, Q_0$$

$$J_1 = Q_2$$

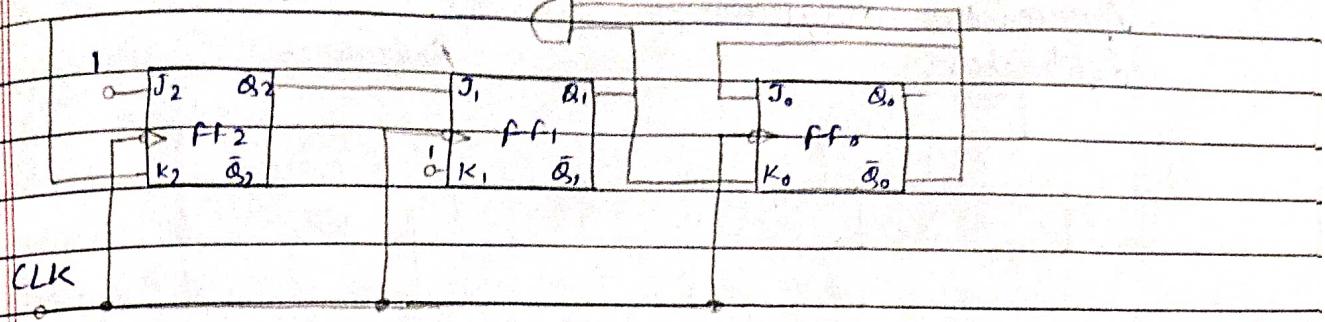
$Q_2$	00	01	11	10
0	1	X	X	1
1	0	X	X	0

$$K_1 = 1$$

$Q_2$	00	01	11	10
0	X	X	X	X
1	X	0	1	X

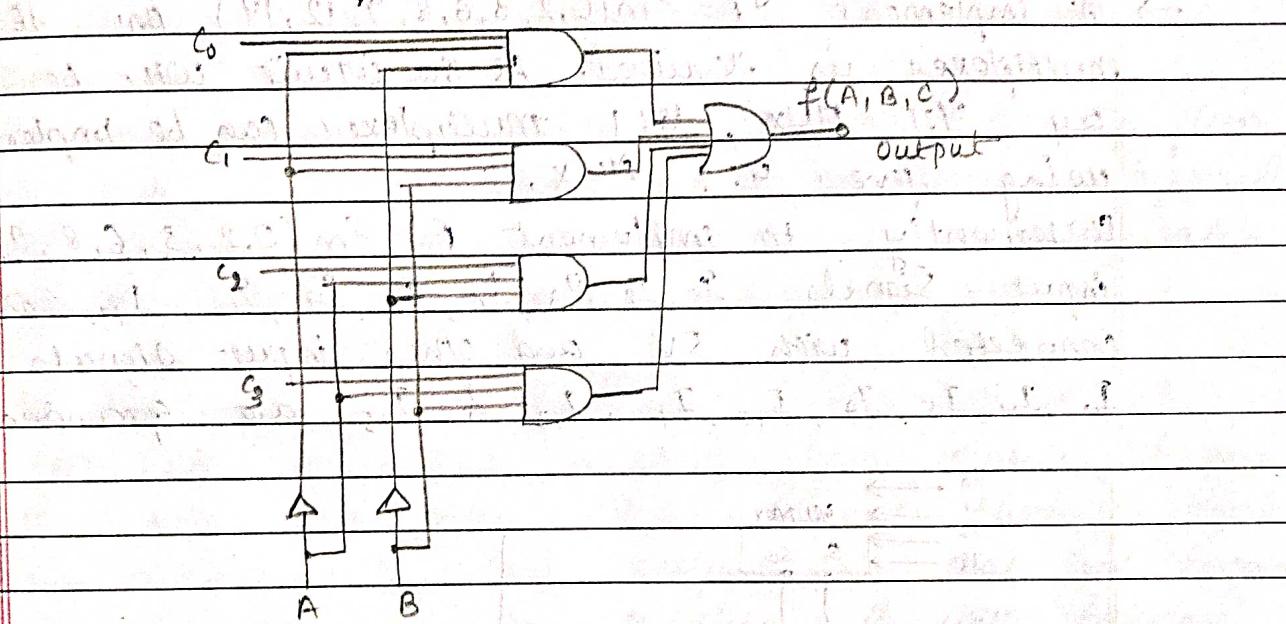
$J_0 = Q_2$

$K_0 = Q_1$



Logic diagram of the synchronous counter, which cycles through the 7-4-6-0-5-2 using J-K flip-flops.

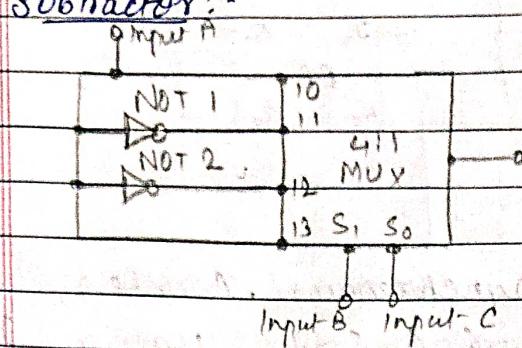
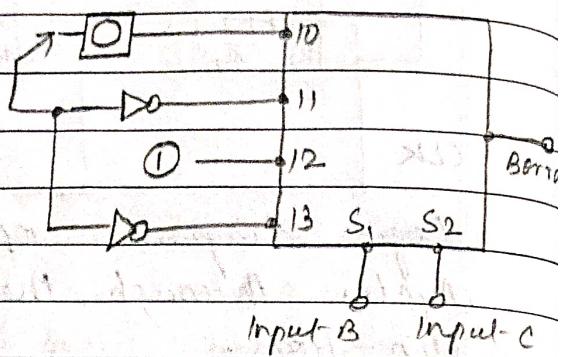
Implement a full subtractor using demultiplexer.  
The Mux diagram is shown below:



There are 2 outputs i.e., Sub and Borrow. So two MUX are to be selected.

Truth Table:-

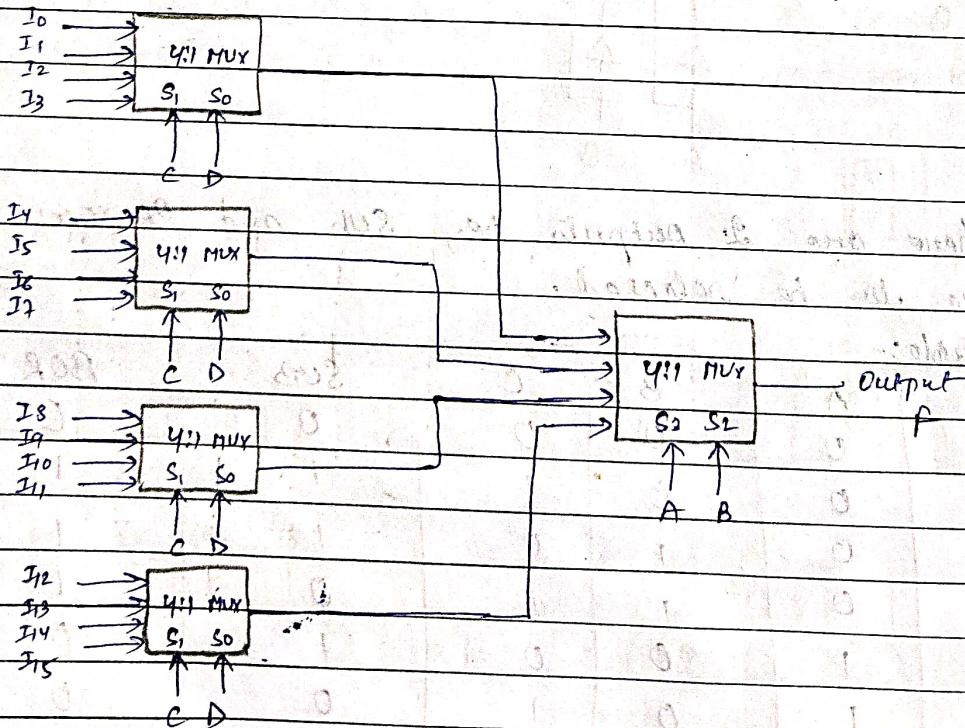
	A	B	C	SUB	BOR
	0	0	0	0	0
	0	0	1	1	1
	0	1	0	1	1
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
	1	1	1	1	1

Connection diagramSubtractor:-Borrow :-

(33) Implement  $F = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$  using 4:1 MUX only.

→ To implement  $F = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$ , one 16:1 multiplexer is required. As the circuit will be designed by 4:1 MUX, 16:1 multiplexer can be implemented using five 4:1 MUX.

consequently to implement  $F = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$   
input Signals  $I_0, I_2, I_3, I_6, I_8, I_9, I_{12}, I_{14}$  are  
connected with 5V and other input signals  
 $I_1, I_4, I_5, I_7, I_{10}, I_{11}, I_{13}$  &  $I_{15}$  are grounded.



(3) What are the main differences b/w a latch and a flip-flop? Explain the working of S-R flip flop.

1<sup>st</sup> part:-

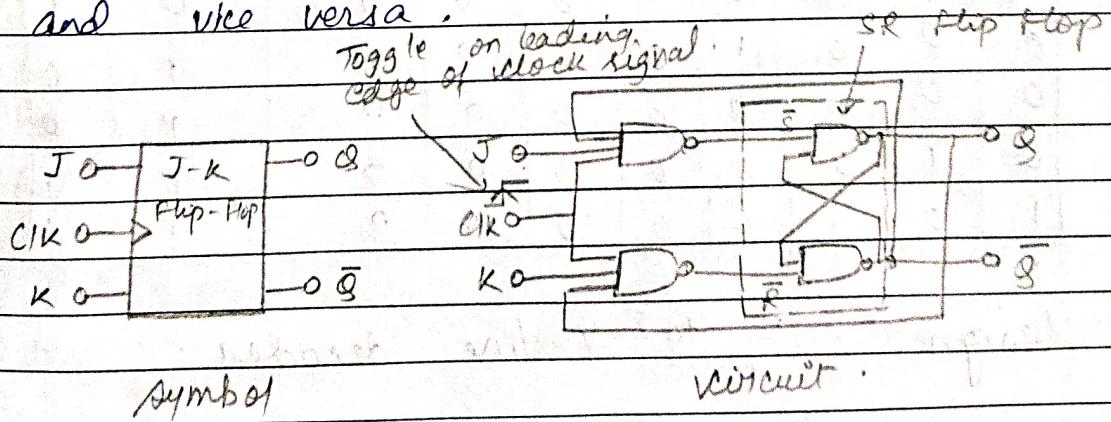
Both flip-flop and latch are bi-stable and are used to store binary data but in flip-flop state change only occurs on a clock edge or pulse whereas in latch, state change occurs without being clocked. So it can be concluded that - flip flops are clocked but latches are not.

2<sup>nd</sup> part:- Clock previous. (B)

Disadvantage of S-R flip flop? How can it be overcome? Explain.

⇒ The one major disadvantage of the S-R flip flop is that in no condition when the clock is triggered the inputs become high which is an undesirable condition bcz it causes invalid input.

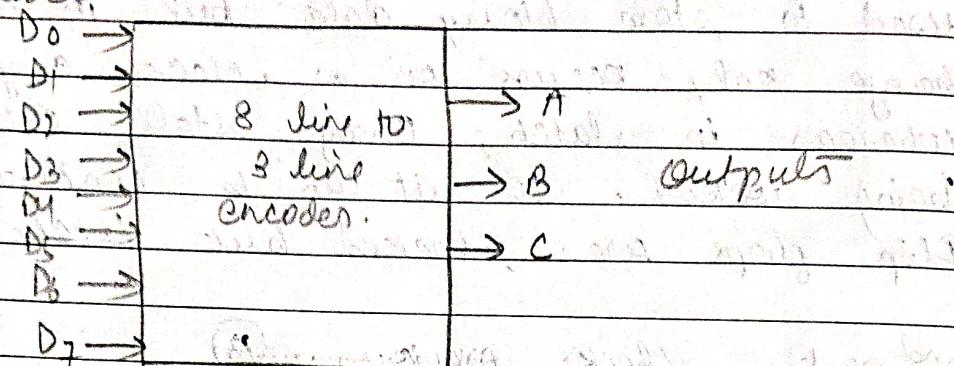
It is avoided by feedback to convert it into JK FF in which making both inputs J and K will give more diff. output that is toggled. This toggles it's last output so that if output was earlier 0 by toggling it will become 1 and vice versa.



(35) Design a binary to BCD converter.

(35) Design an 8 to 3 line encoder.

8:3 Encoder.



Outputs of encoder can be expressed in Boolean expressions as:

$$A = D_4 + D_5 + D_6 + D_7$$

$$B = D_2 + D_3 + D_6 + D_7$$

$$C = D_1 + D_3 + D_5 + D_7$$

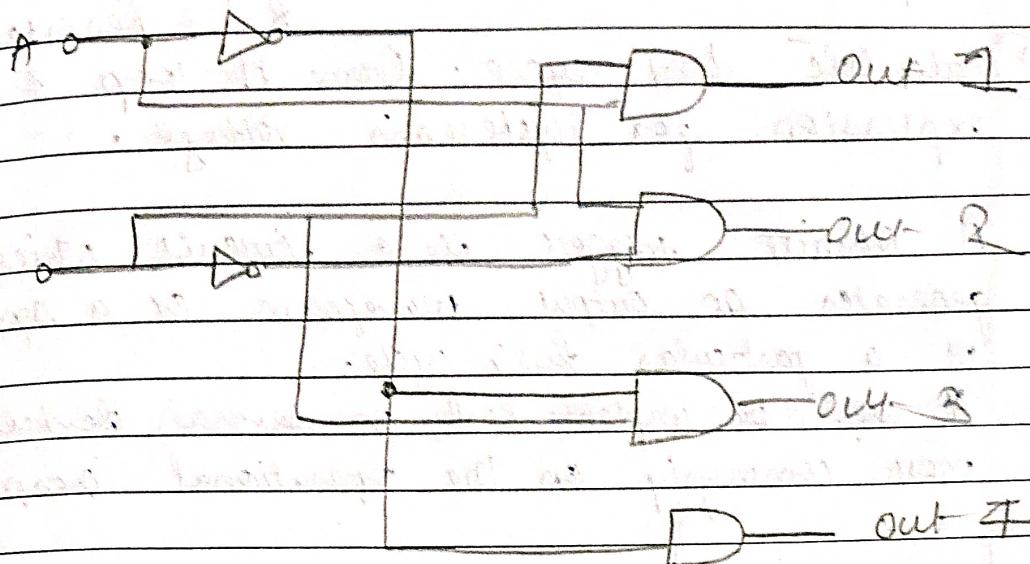
Truth Table for 8 lines to 3 line decoder.

Inputs							Outputs		
D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	A	B	C
0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	0
0	0	0	0	1	0	0	0	0	1
0	0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0	0
0	1	0	0	0	0	0	1	0	1
1	0	0	0	0	0	0	1	1	0

Design 2 to 4 line decoder.

A	B	Out 1	Out 2	Out 3	Out 4
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	Teacher's Signature	0

$$\text{out } 1 = AB, \quad \text{out } 2 = \bar{AB}, \\ \text{out } 3 = \bar{A}\bar{B}, \quad \text{out } 4 = \bar{A}\bar{B}$$



Realization of 4 output decoder using gates.

Implement  $Y_0(A, B, C) = \sum m(0, 1, 2, 4)$  using 3-to 8 line decoder.

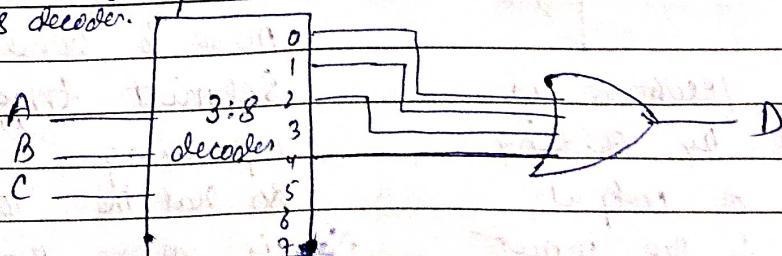
Inputs

Outputs

A	B	C	$Z_1$	$Z_2$
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D(A, B, C) = \sum m(0, 1, 2, 4)$$

∴ there are 3 inputs & total of 8 minterms, we need a 3 to 8 decoder.



525 times

- (36) Calculate the width of the generated pulse.

Monostable Multivibrator pulse width.

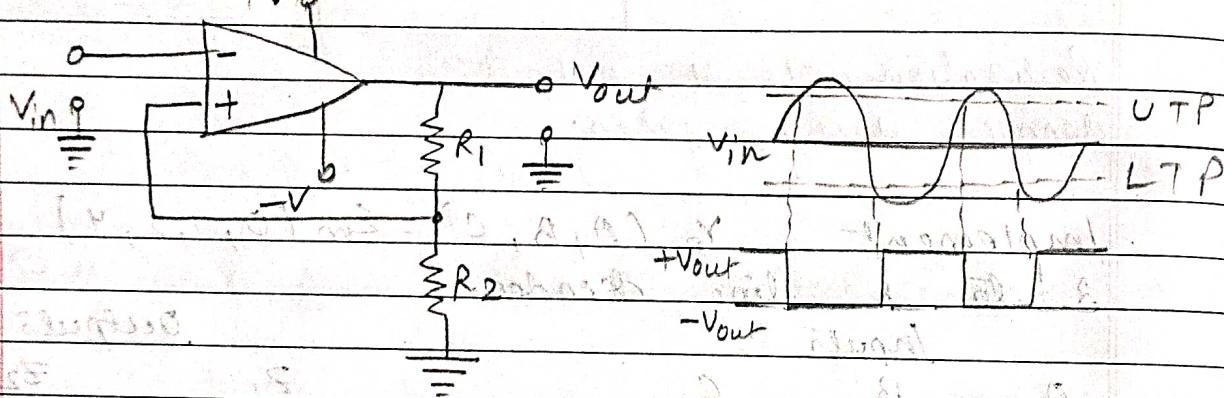
$$T_p = 1.1 * R_1 * C_1 \text{ where } C_1 = \text{capacitance}$$

$R_1 = \text{Resistance.}$

- (37) Calculate duty cycle. Draw H loop & find the expression for hysteresis voltage.

A Schmitt trigger is a circuit which generates an output waveform of a Sq. wave of a particular duty cycle.

It can be implemented on several devices, however most commonly on the operational amplifier.

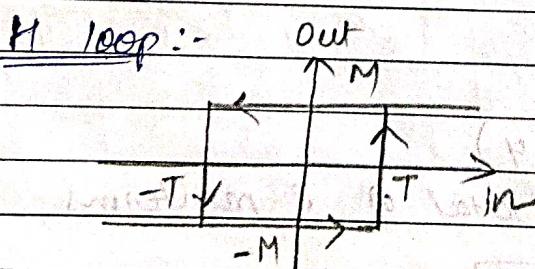


When we give a +ve feedback to the opamp, it no more behaves as a linear IC.

If the input voltage diff. ( $V_p - V_n$ )  $> 0$ , then it gives a +V sat output &

if input voltage diff. is lesser  $< 0$ , it gives -Vsat output.

H loop:-

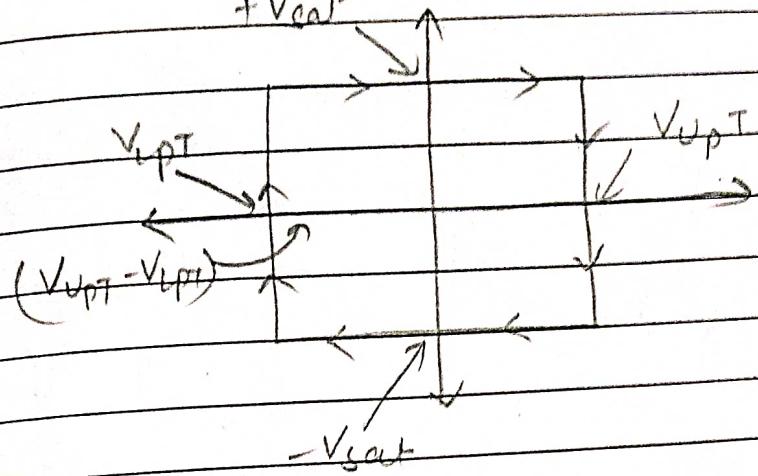


The +ve feedback is introduced by adding a part of output voltage to the input voltage.

Circuits with hysteresis are based on fundamental +ve feedback idea:

Any active circuit can be made to behave as a Schmitt trigger by applying a +ve feedback so that the loop gain is more than 1.

Expression for Hysteresis voltage :-



$$\Delta V_T = (V_{UPT} - V_{LPT}) \text{ volt} = \text{Hysteresis voltage.}$$