

Two-Stage Op-Amp Overview

1. What is a Two-Stage Op-Amp?

A two-stage operational amplifier has:

- Stage 1: Differential amplifier with active load.
- Stage 2: Common-source gain stage.
- Compensation capacitor (Miller compensation) for stability.

2. Why Two Stages?

- High DC gain.
- Easy to stabilize with Miller capacitor.
- Good for moderate-to-high bandwidth and precision analog circuits.

3. Basic Equations:

Let g_{m1} , r_{o1} = transconductance and output resistance of stage 1.

Let g_{m2} , r_{o2} = transconductance and output resistance of stage 2.

DC Gain:

$$A = (g_{m1} * r_{o1}) * (g_{m2} * r_{o2})$$

Gain Bandwidth (GBW):

$$GBW \approx g_{m1} / (2\pi * C_c)$$

Dominant Pole:

$$p_1 \approx 1 / (r_{o1} * (C_{in} + C_c(1 + A_2)))$$

Non-Dominant Pole:

$$p_2 \approx 1 / (r_{o2} * (C_L + C_c))$$

Phase Margin (approx):

$$PM \approx 180^\circ - \arctan(GBW/p_2)$$

4. Design Steps:

1. Set specifications (gain, GBW, PM, power, load).
2. Choose tail current for differential pair.
3. Set g_{m1} from GBW requirement.
4. Choose compensation capacitor C_c .
5. Size transistors to meet gain.
6. Verify poles and adjust C_c for $PM \sim 60^\circ$.
7. Check slew rate $SR \approx I/C_c$.

5. Stability Techniques:

- Miller capacitor.
- Series resistor (nulling resistor).
- Feed-forward zero.
- Output buffer for heavy loads.

6. Layout Notes:

- Common-centroid for input differential pair.
- Symmetric current mirrors.
- Guard rings.
- Minimize parasitic capacitances at high-impedance nodes.