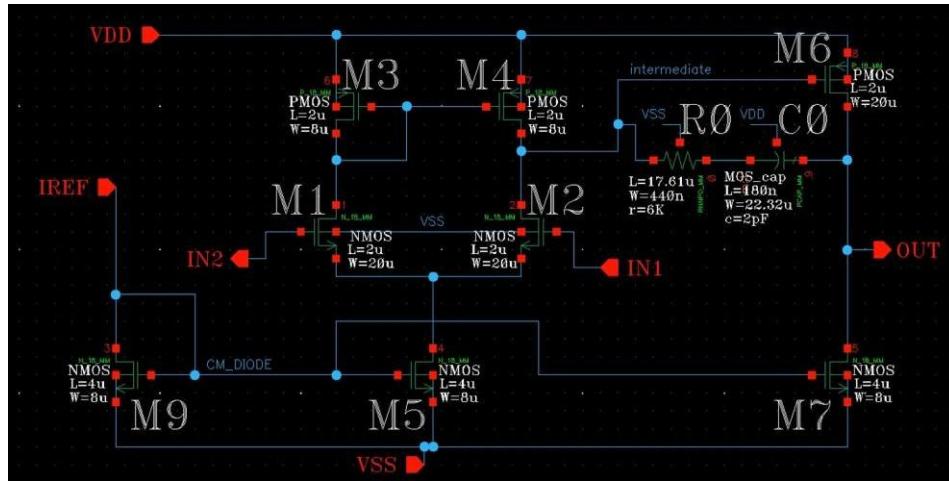


Two-stage Operational Amplifier

This report presents the complete design and layout of a Two-Stage CMOS Operational Amplifier. It includes schematic explanation, differential pair layout, current mirror design, routing strategy, and verification results. Additional focus is placed on performance optimization, layout symmetry, and matching techniques used (**Common centroid & Interdigititation**) to improve accuracy and noise immunity.

Schematic of two stage Op-amp

The schematic illustrates the transistor-level design of the amplifier, showing both gain stages, bias circuitry, and compensation network. Proper biasing ensures a stable operating point and high open-loop gain.

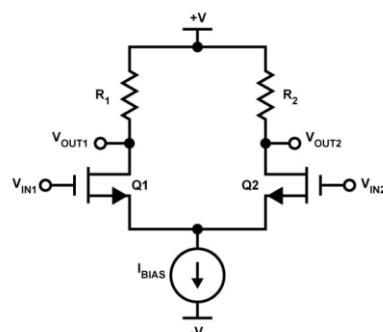


Schematic of Two-stage Op-amp

This Op-amp consists of

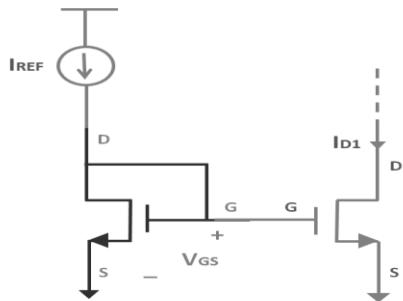
Differential Pair

- The differential input pair forms the first stage, ensuring high input impedance and excellent common-mode rejection.
- Common Centroid layout and dummy devices are employed to minimize mismatch and offset.
- The layout also maintains equal parasitic capacitances at each input for balanced operation.



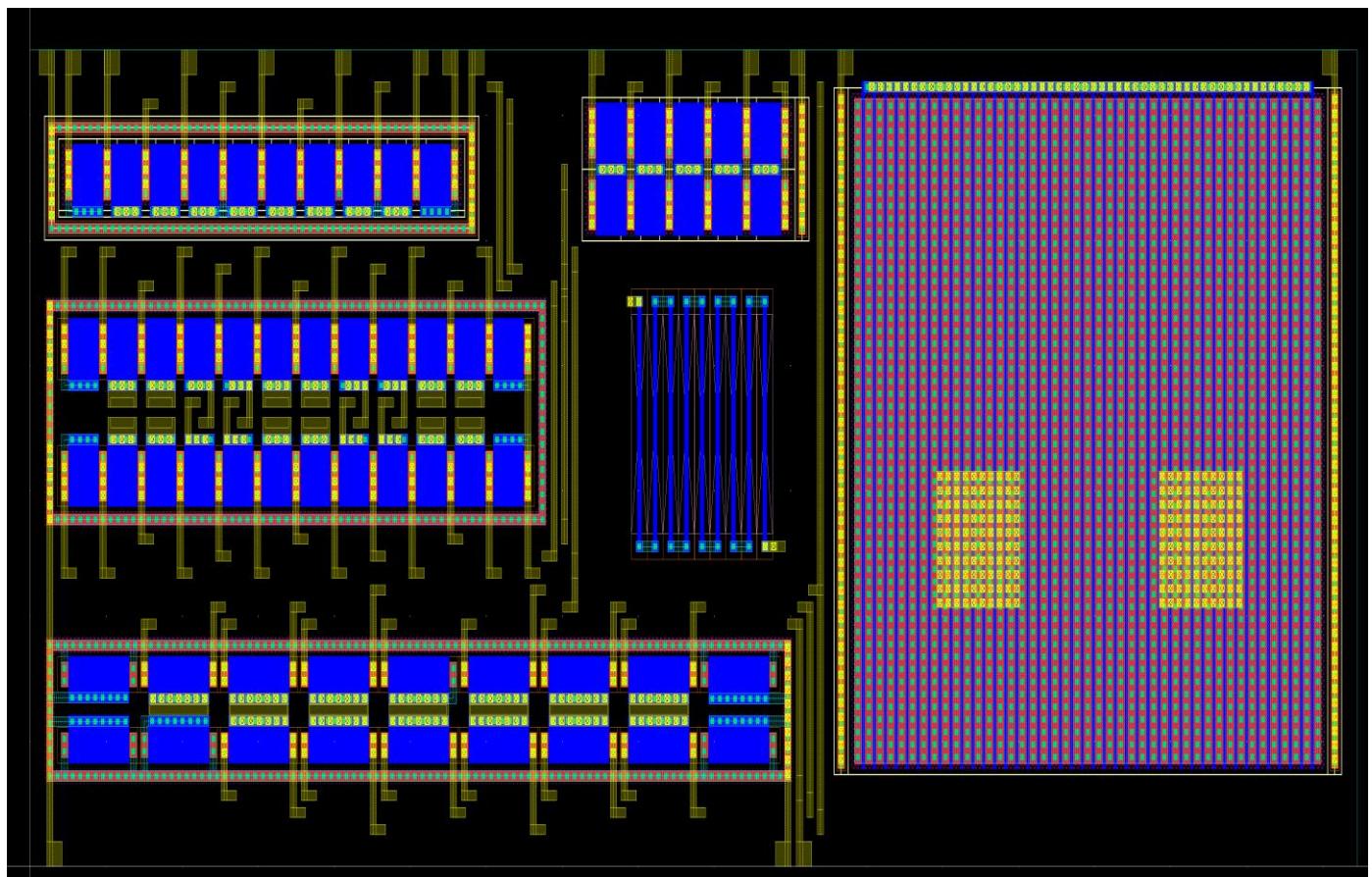
Current Mirror Layout

- Current mirrors are used for biasing and current replication across stages.
- Interdigititation and device symmetry ensure accurate current copying and temperature stability.
- Metal routing is balanced to avoid parasitic resistance mismatches that could degrade performance.



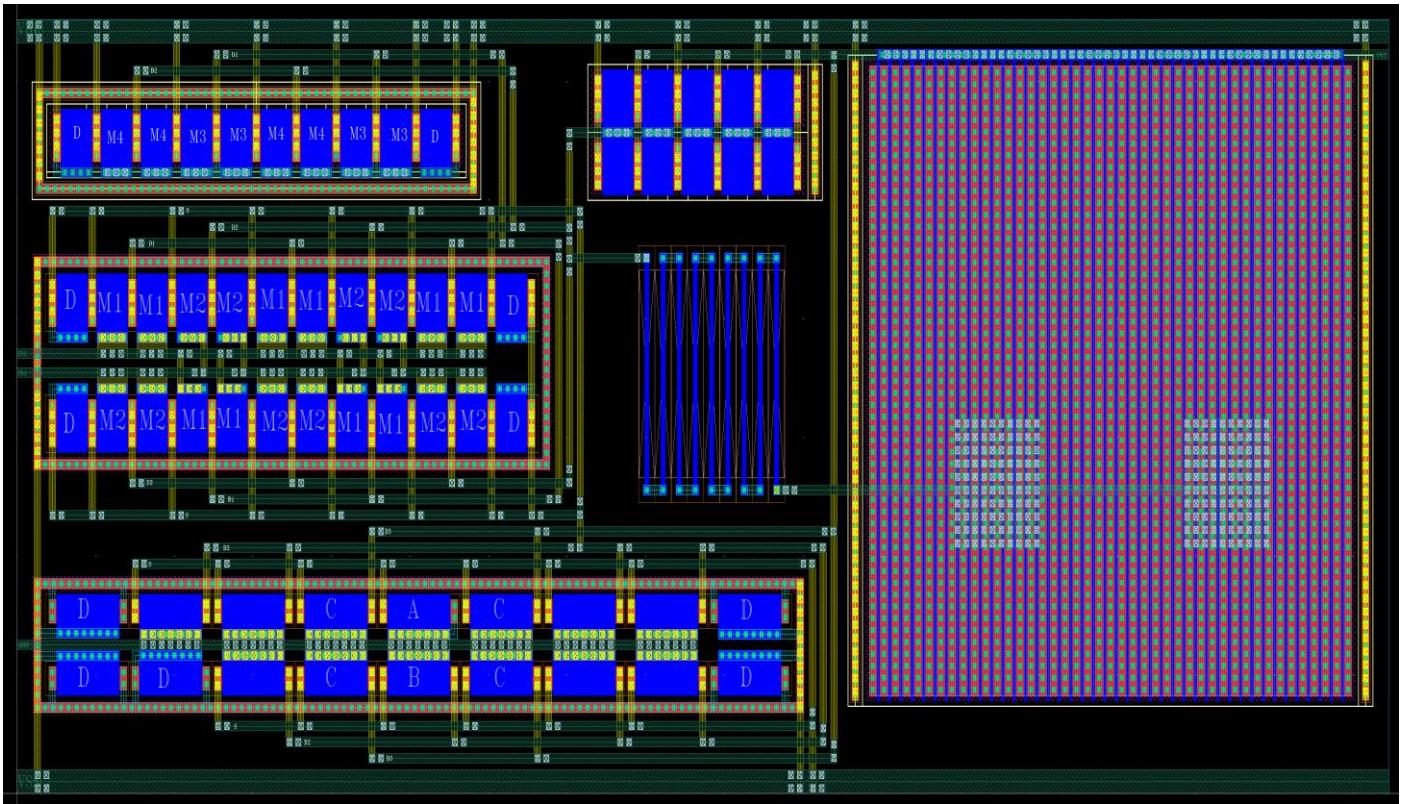
Routing for M1, M2

The interconnections between M1 and M2 are designed with equal-length paths to maintain matching. Routing uses higher metal layers where needed to minimize parasitic resistance. Care is taken to avoid crosstalk and ensure symmetry between the mirrored devices.



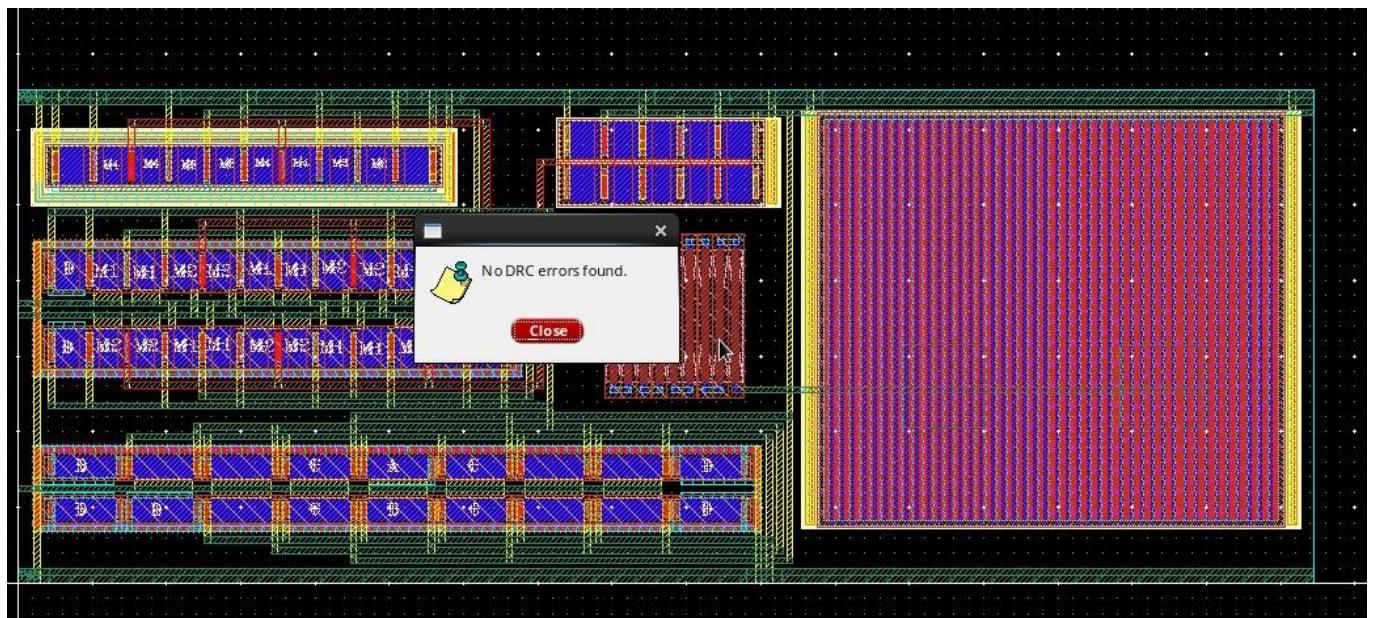
Routing for M2, M3

This stage handles the transition from input to intermediate nodes. Matched metal widths and equal spacing are used to ensure balanced delay and reduce the effect of parasitic capacitance. Proper shielding techniques are applied where necessary to reduce noise coupling.



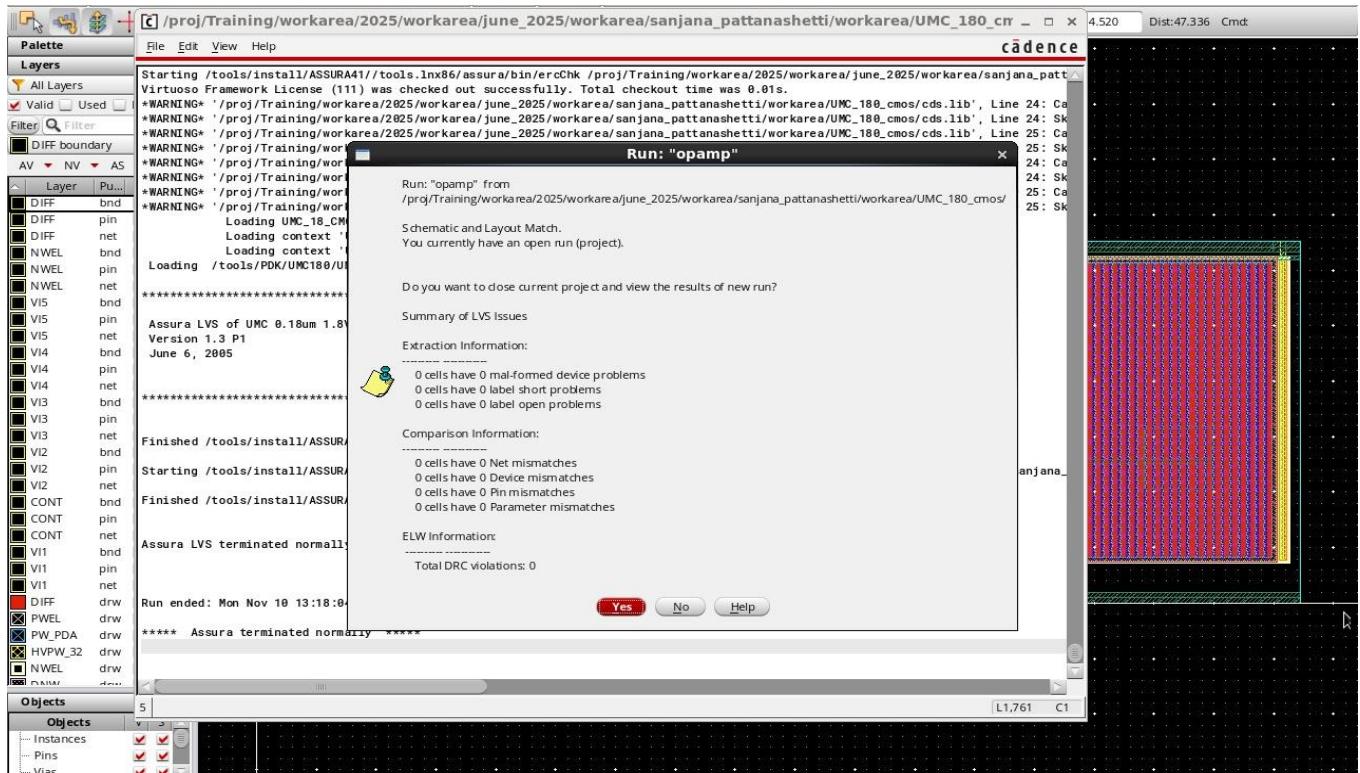
DRC Verification

Routing integrates the differential and current mirror sections with attention to device symmetry and signal balance. Metal connections are optimized for minimum IR drop and consistent current flow. The differential structure minimizes offset voltage and enhances linearity.



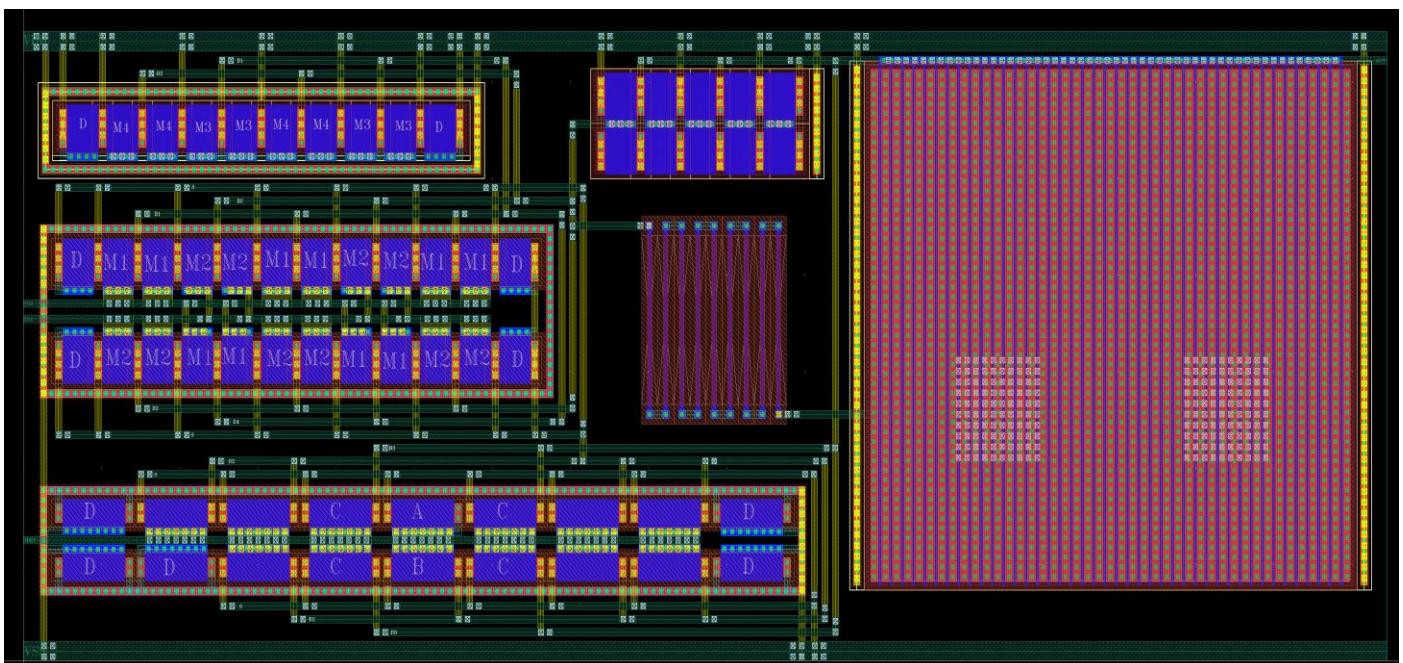
LVS Verification

Layout Versus Schematic (LVS) verification ensures that the physical layout matches the schematic connectivity exactly. Any discrepancies are resolved through netlist comparison and device annotation correction. A clean LVS result confirms that the design is logically and physically consistent.



Final Op-Amp Layout

The final layout showcases symmetry, matching, and efficient routing. All transistors are placed for minimum mismatch and optimal performance. The use of guard rings and dummy transistors improves noise immunity and stability.



Conclusion

The Two-Stage CMOS Operational Amplifier design effectively combines a differential input stage and current mirror biasing to achieve high gain, low offset, and stable operation. Matching techniques such as Common Centroid and Interdigitation were employed to minimize mismatch and ensure layout symmetry. Proper routing and shielding enhanced signal integrity and reduced parasitic effects.

Both DRC and LVS verifications confirmed that the design adheres to fabrication rules and accurately represents the schematic connections. The use of guard rings and dummy devices improved noise immunity and layout robustness.

Overall, the enhanced design demonstrates high precision, reliability, and strong analog performance, making it well-suited for applications in amplifiers, filters, and mixed-signal circuits.