Mini - Project

Block name : BIT1

Presented by:
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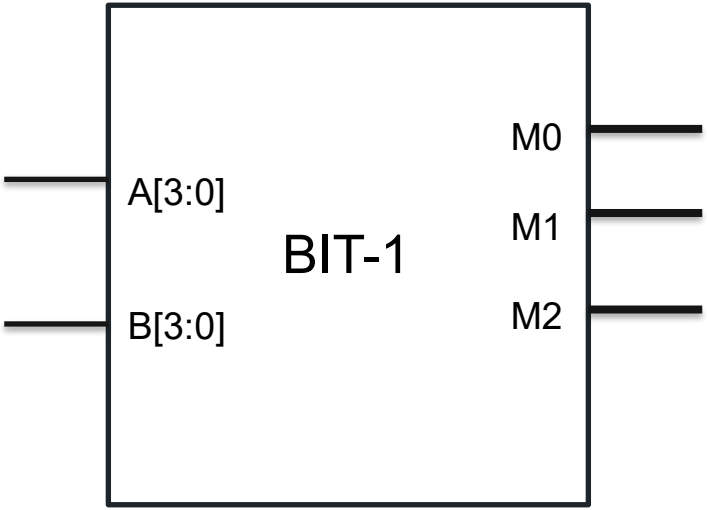
Introduction

- A Bit-1 block in an ALU is a combinational logic circuit that counts the total number of 1’s present in the binary input.
- It outputs this count as a binary number.

Block Diagram



Sub-blocks in this BIT-1

1. Ones3bit
2. Adder
3. Xor
4. And

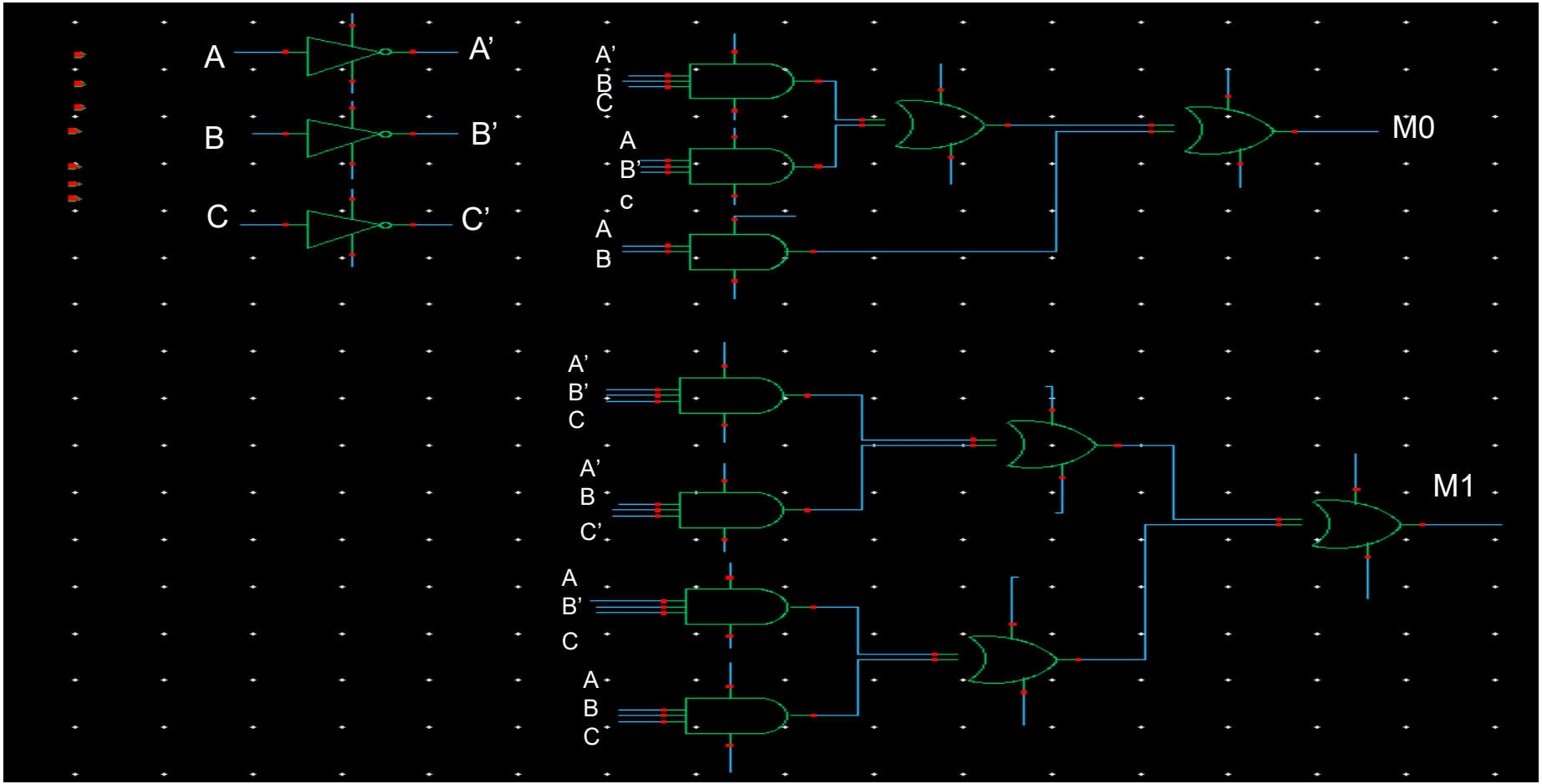
1. **Ones-3bit:** A 3-bit 1's block takes a 3-bit input (A2 A1 A0) and outputs the number of 1's present in it.

2. **Adder:** An Adder is a digital circuit used in computers and ALUs to perform binary addition.
   It takes binary numbers as input.
   Produces their sum and a carry as output.

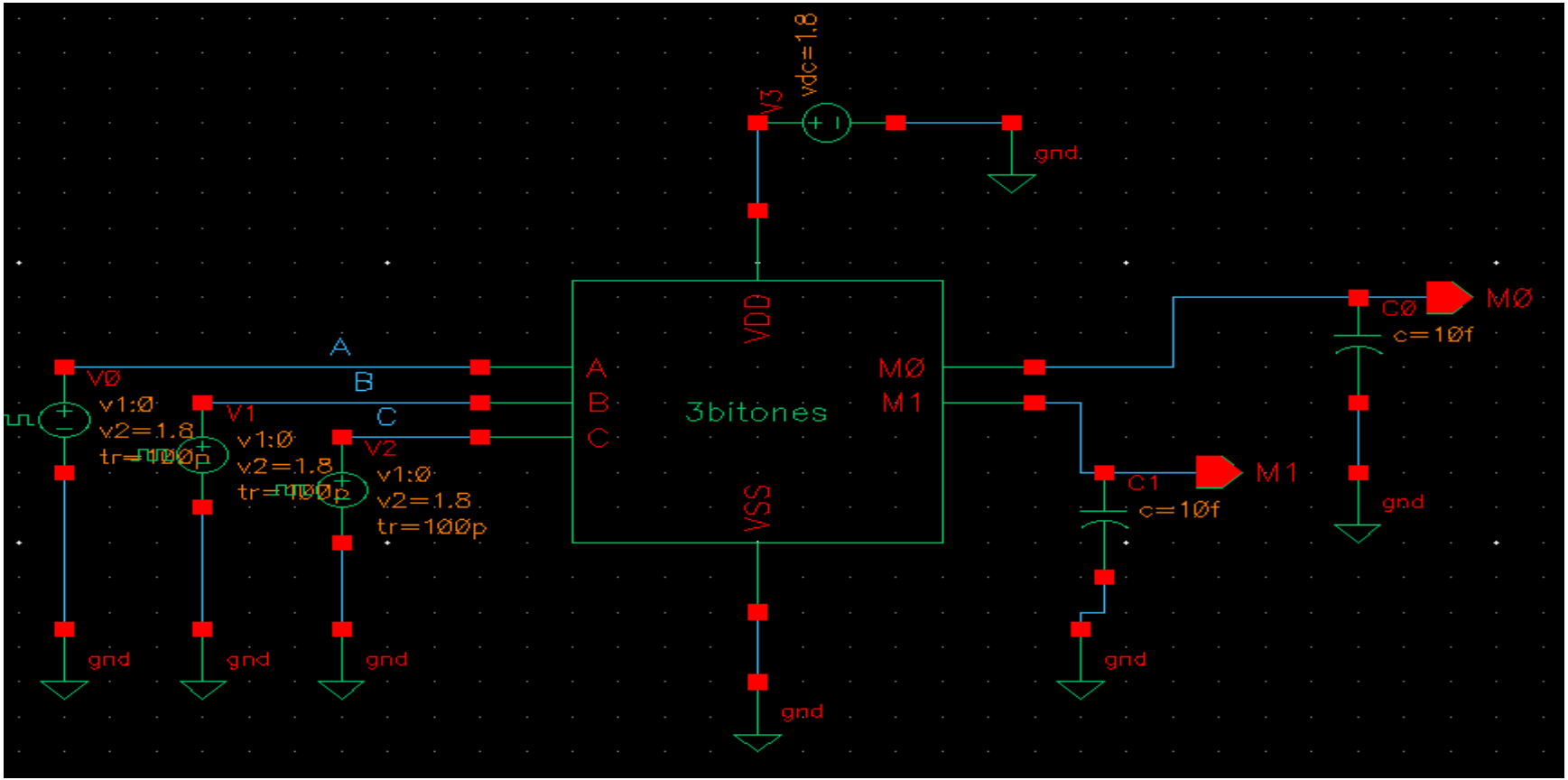
3. **Exor:** The XOR (Exclusive OR) gate is a digital logic gate that gives
   Output = 1 if the inputs are different
   Output = 0 if the inputs are the same.

4. **And:** An AND gate is a digital logic gate that gives
   Output = 1 only if all inputs are 1
   Output = 0 if any input is 0.

Ones-3bit Schematic



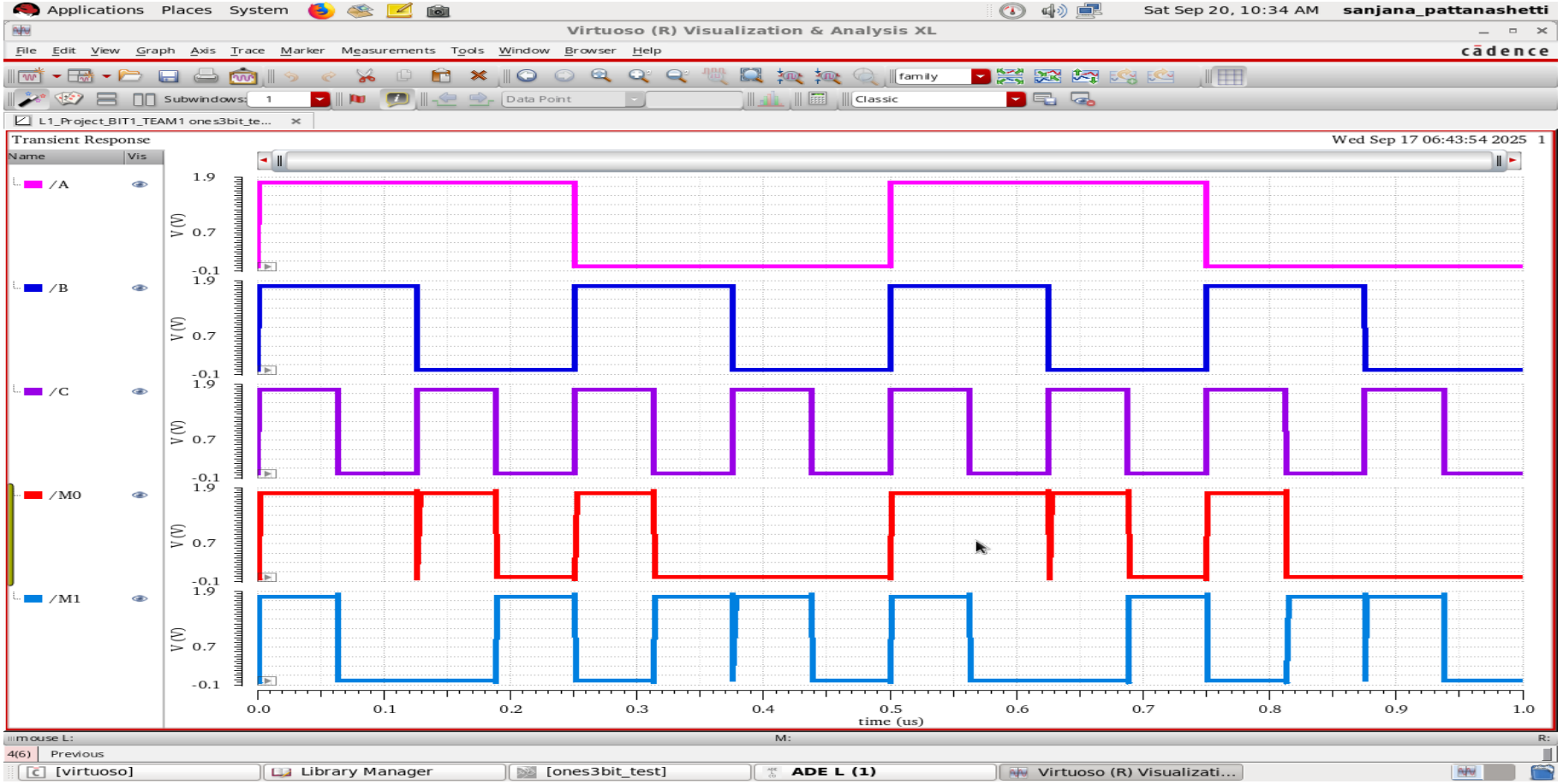
Ones-3bit testbench



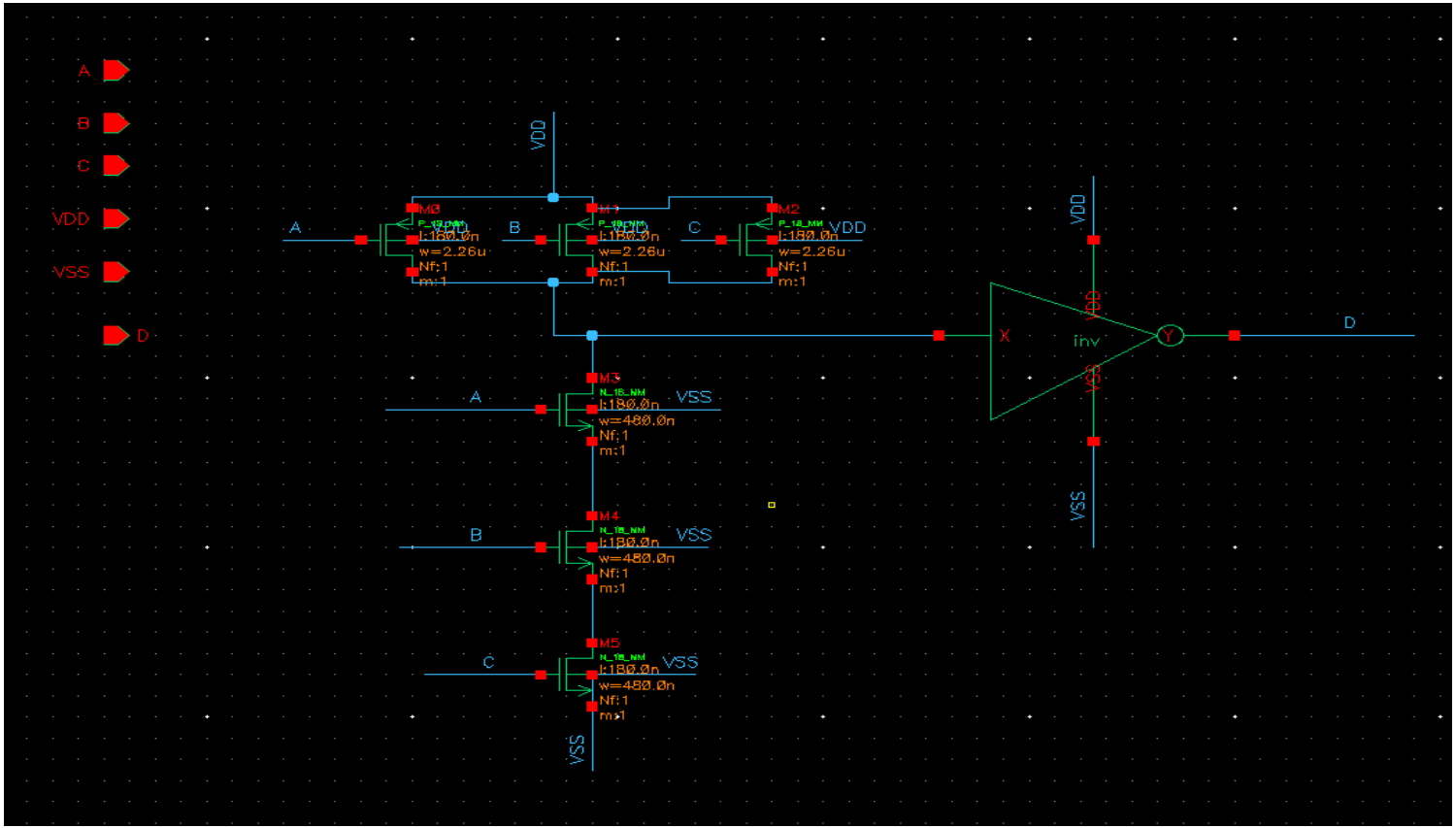
Ones-3bit Truth table

Ones3bit				
Truth Table				
A	B	C	M0	M1
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

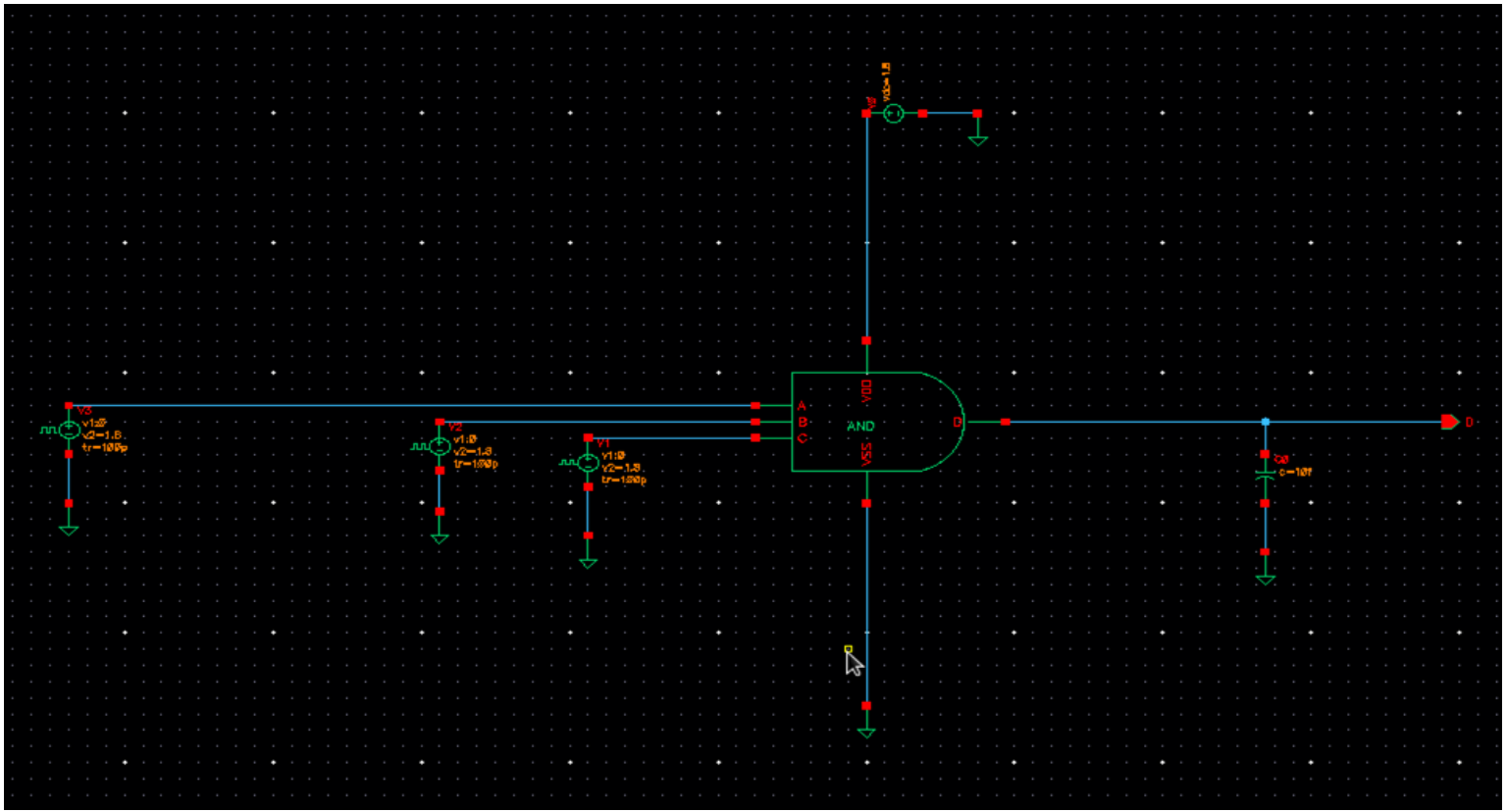
Ones-3bit - waveforms



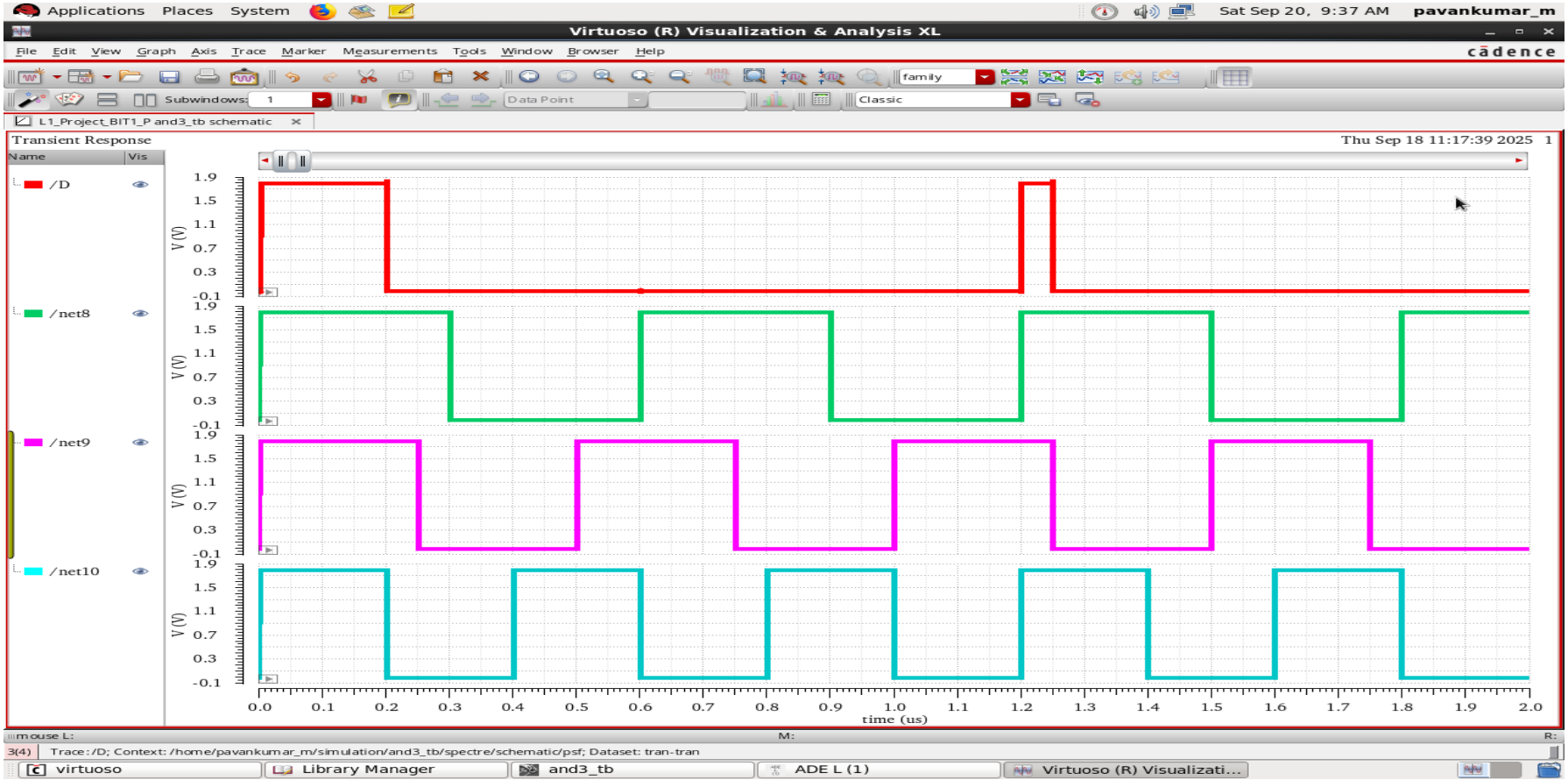
AND3 gate Schematic



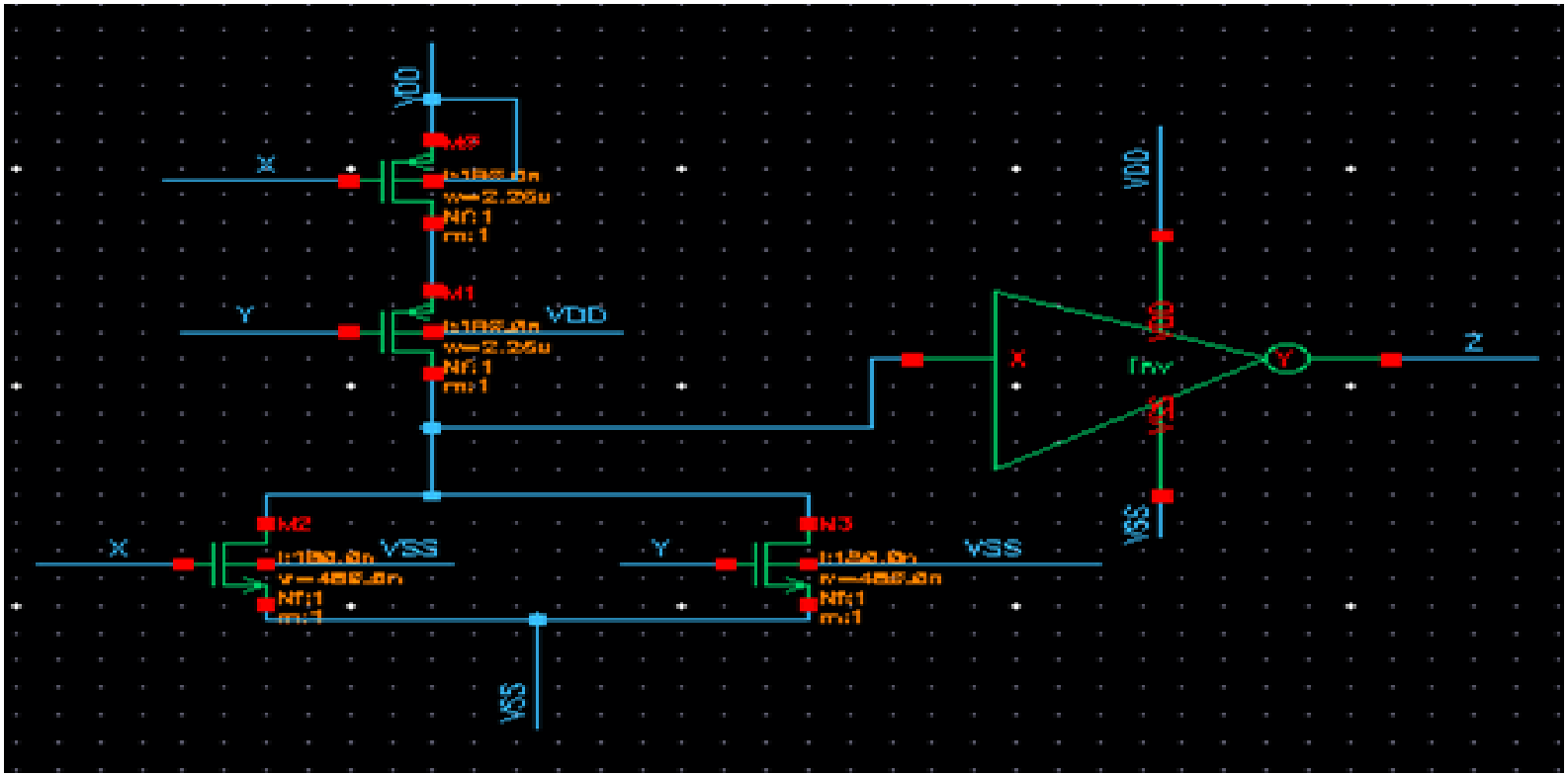
And3 Gate - testbench



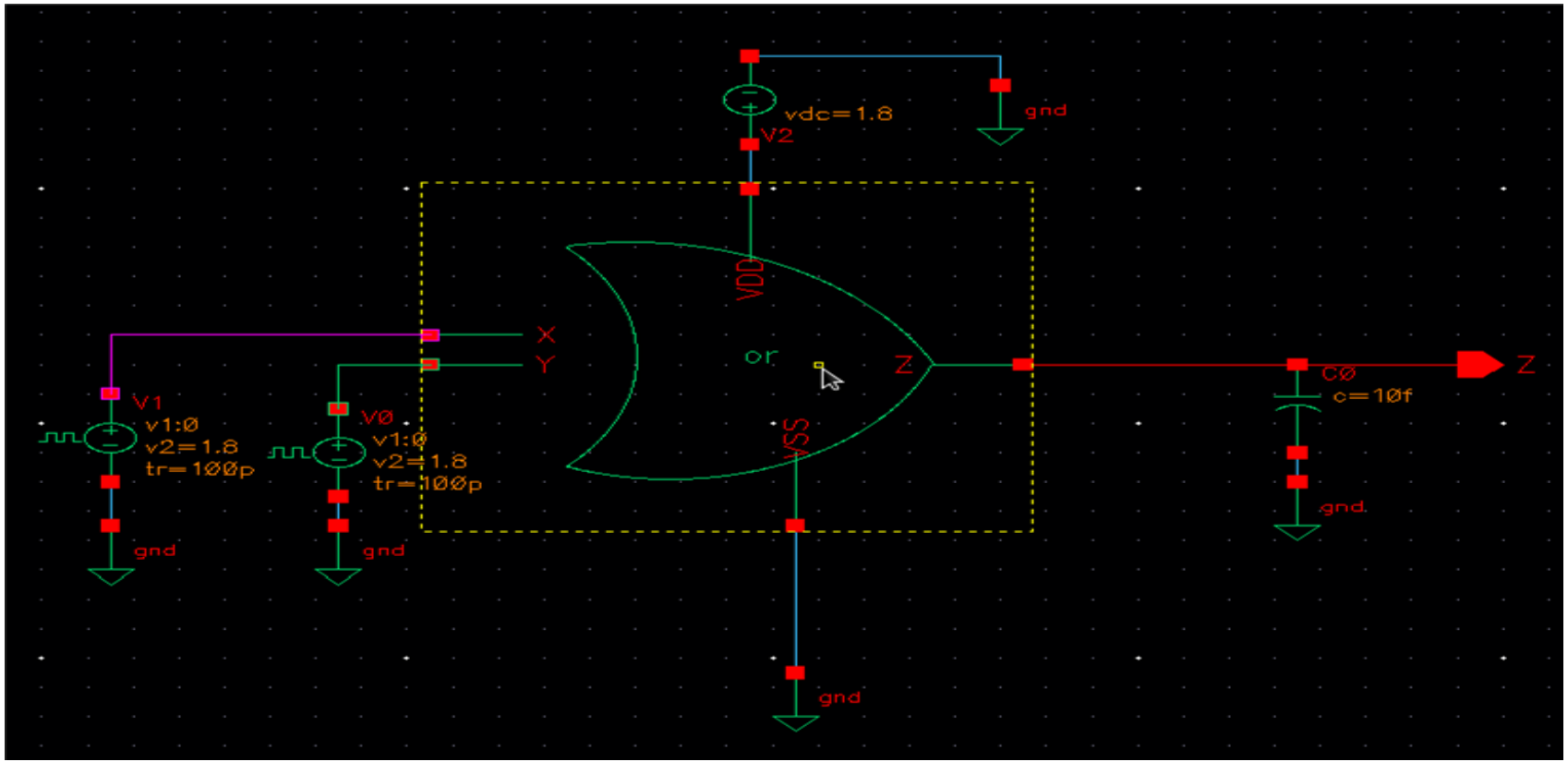
AND3 Gate - Simulation Result



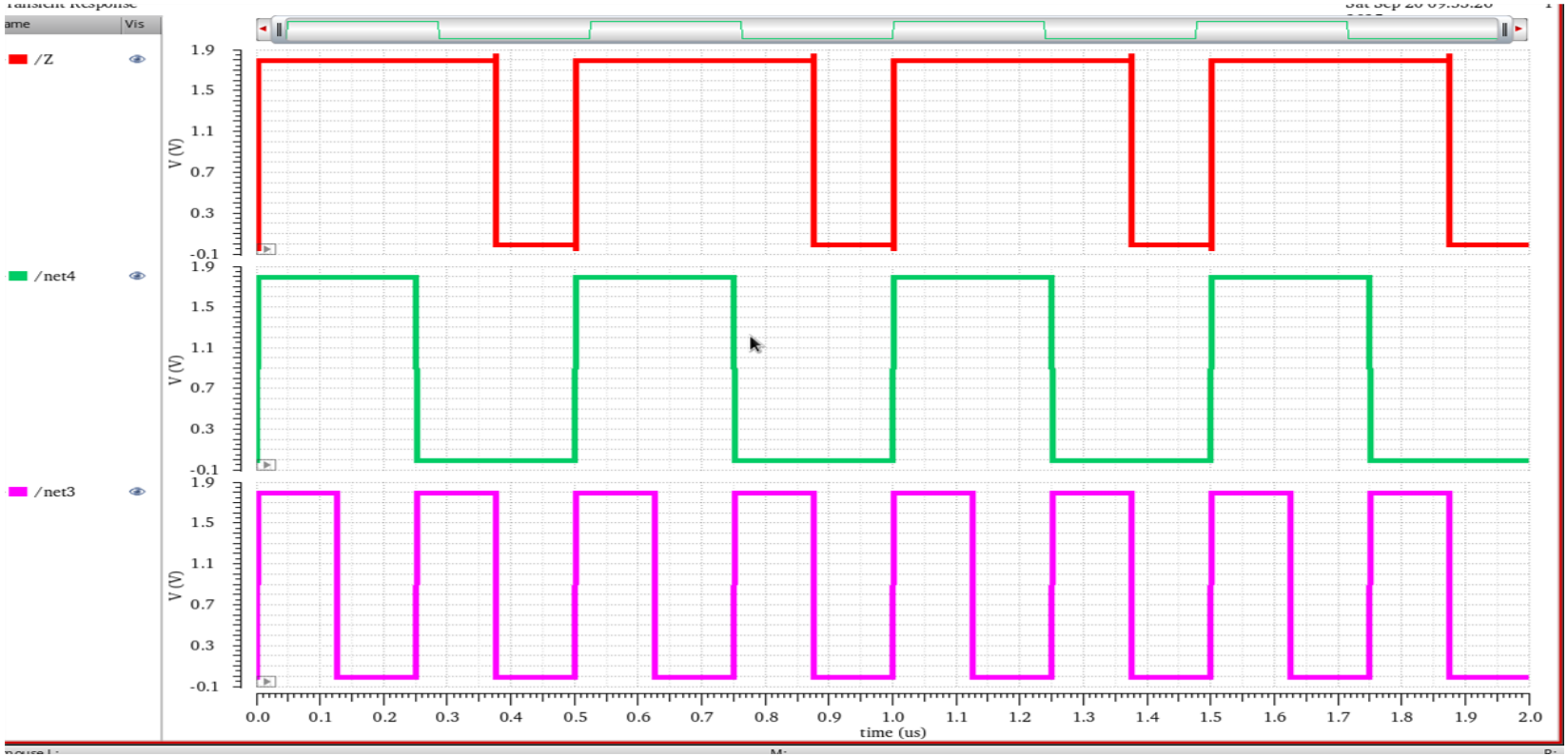
OR Gate Schematic



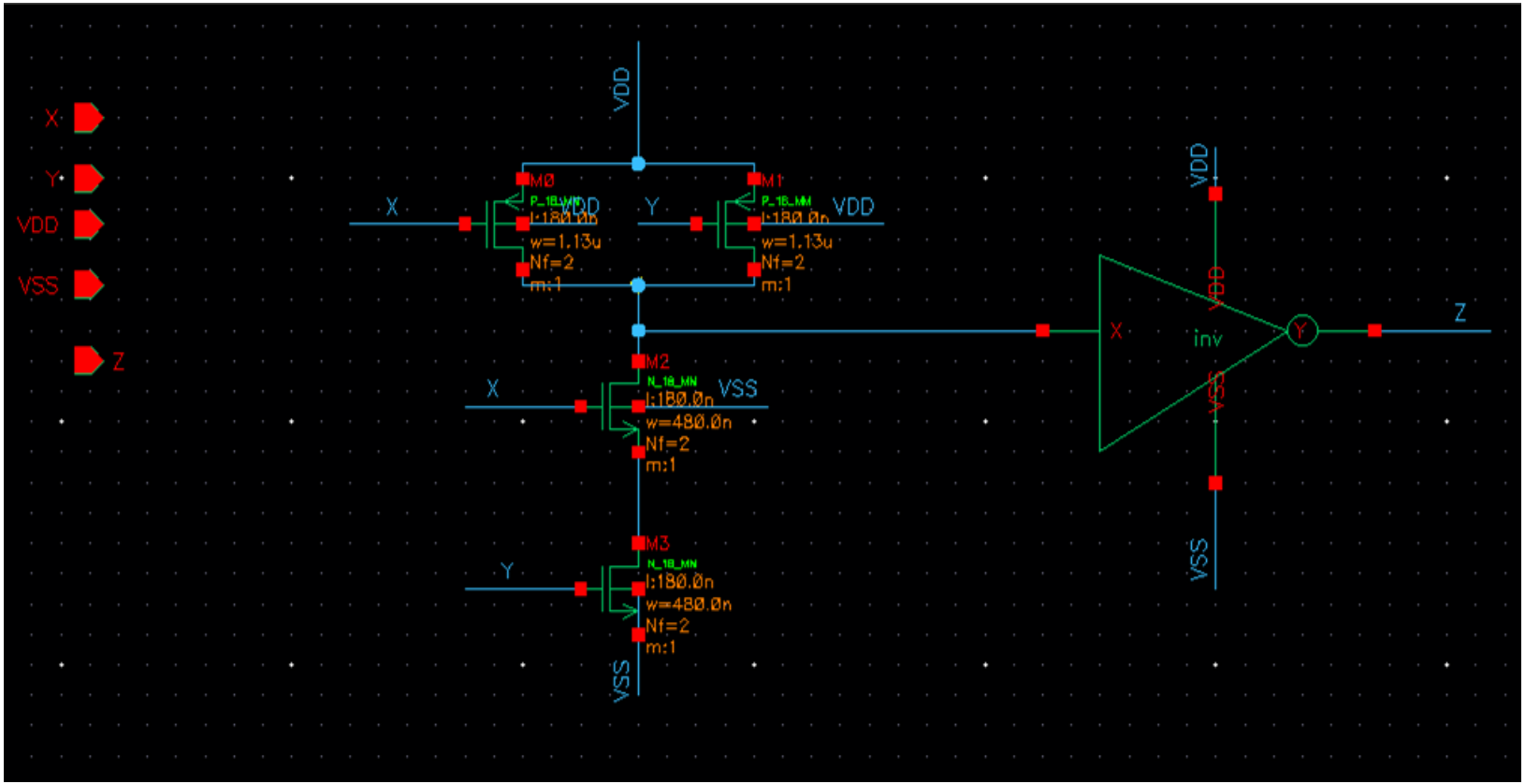
OR Gate - testbench



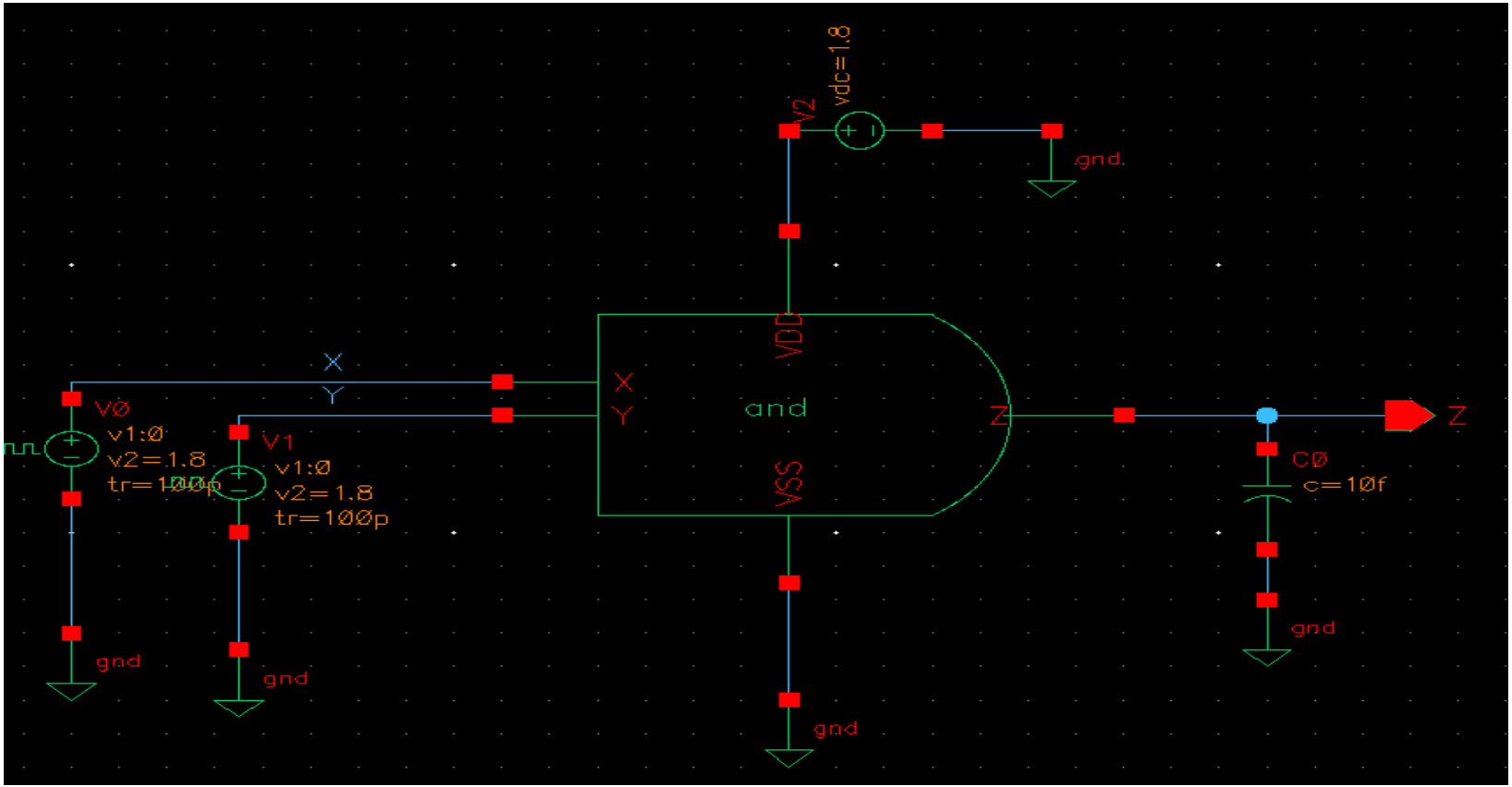
OR Gate waveforms



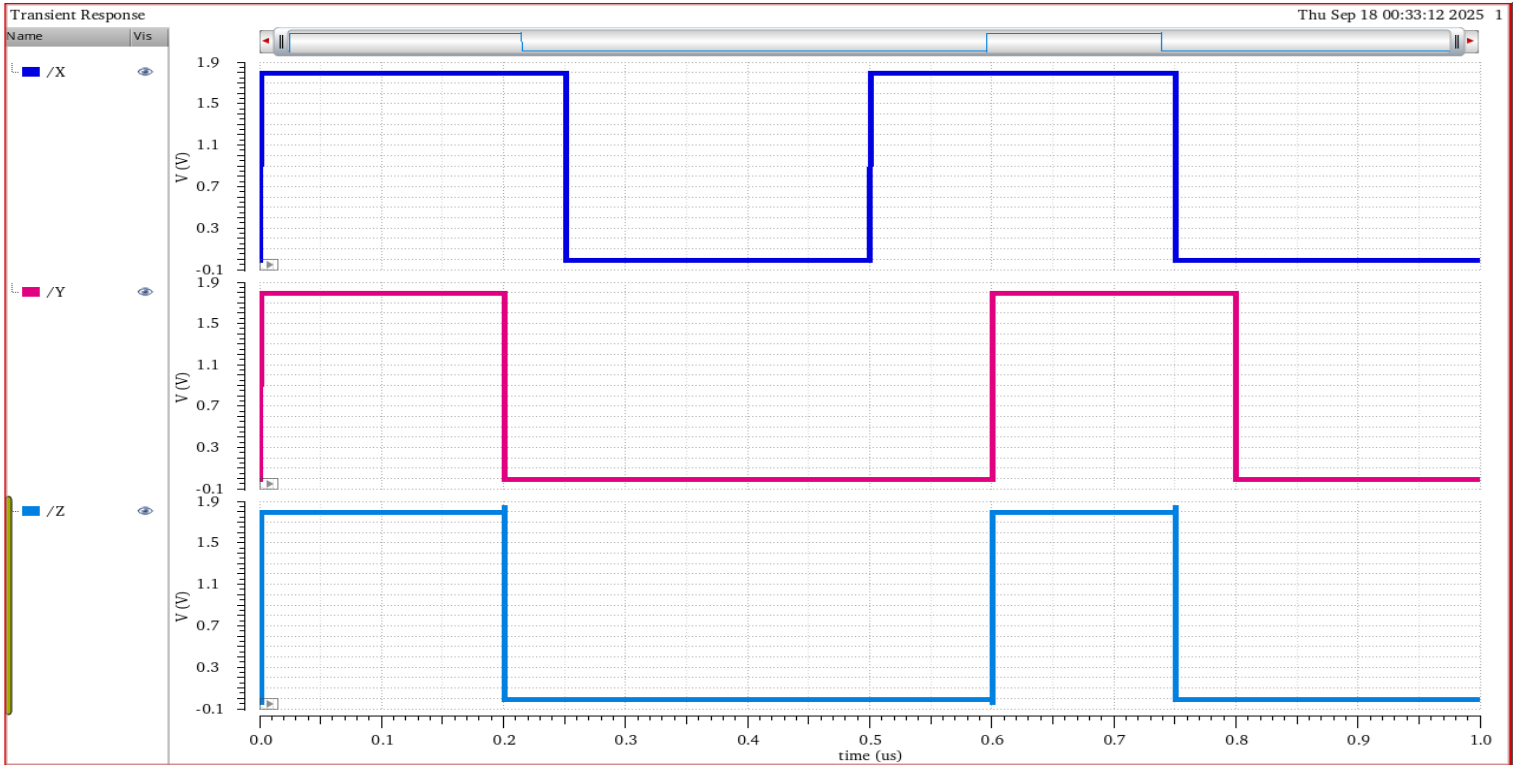
AND GATE - Schematic



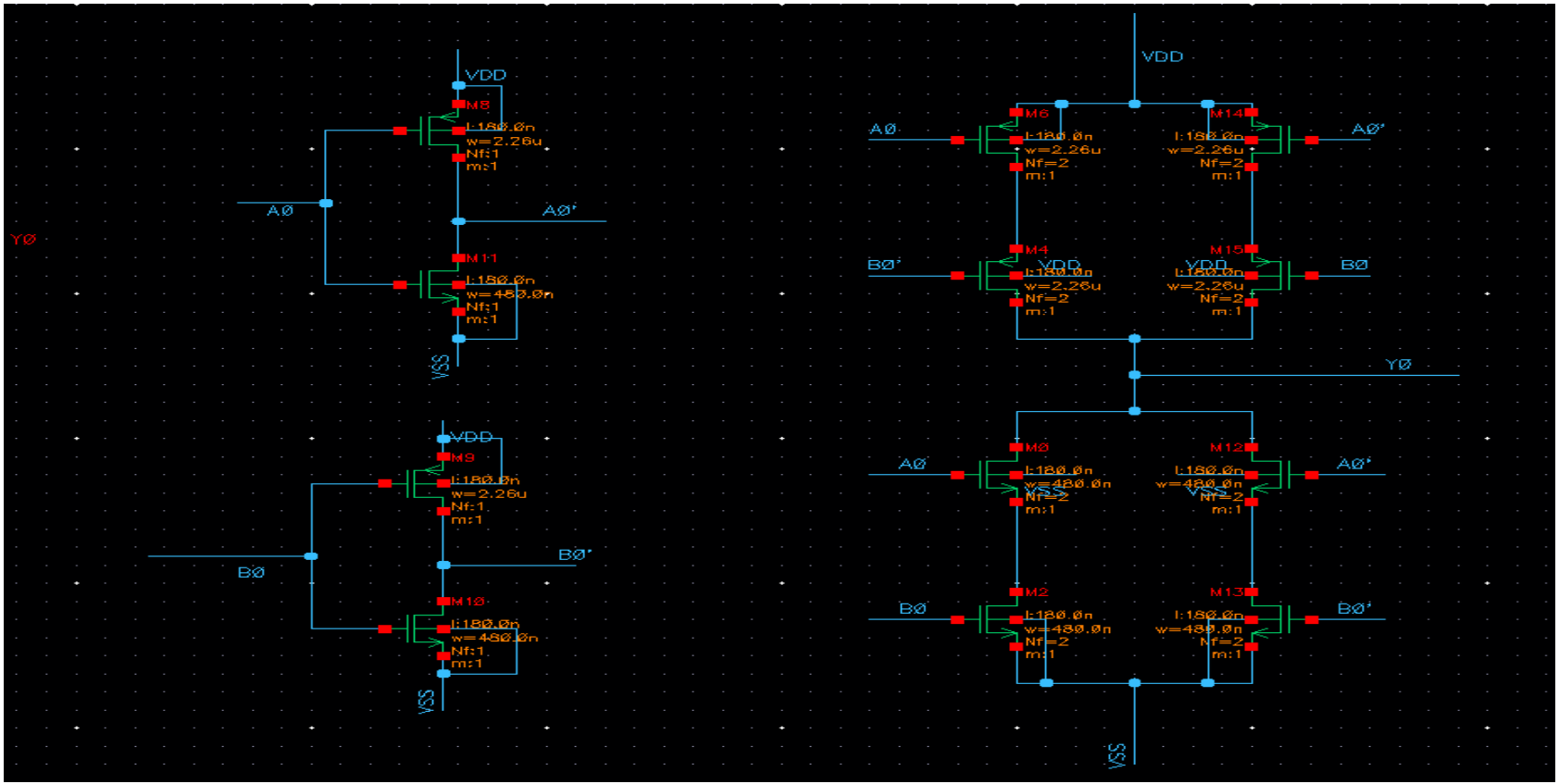
AND Gate -testbench



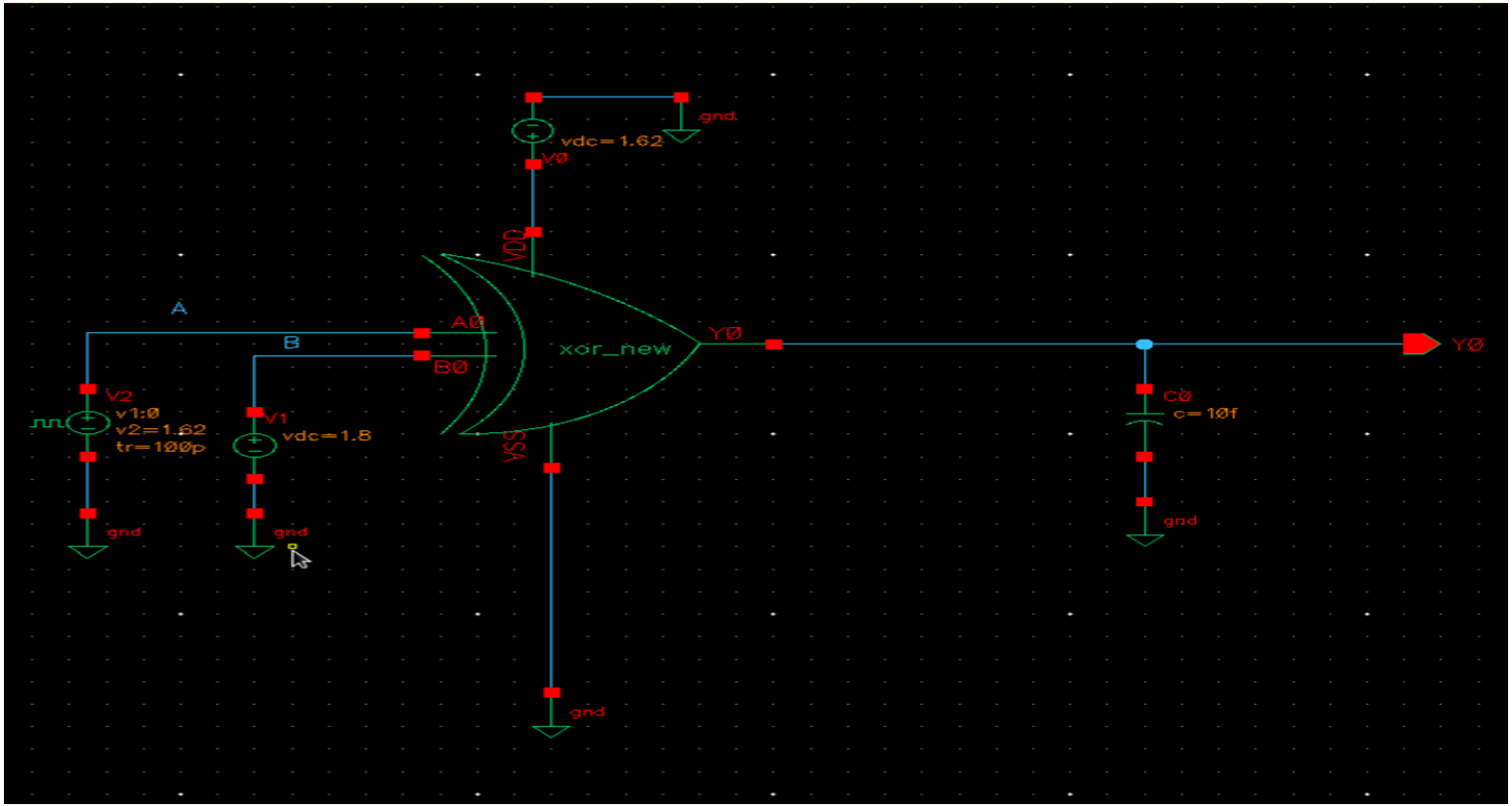
And gate waveform



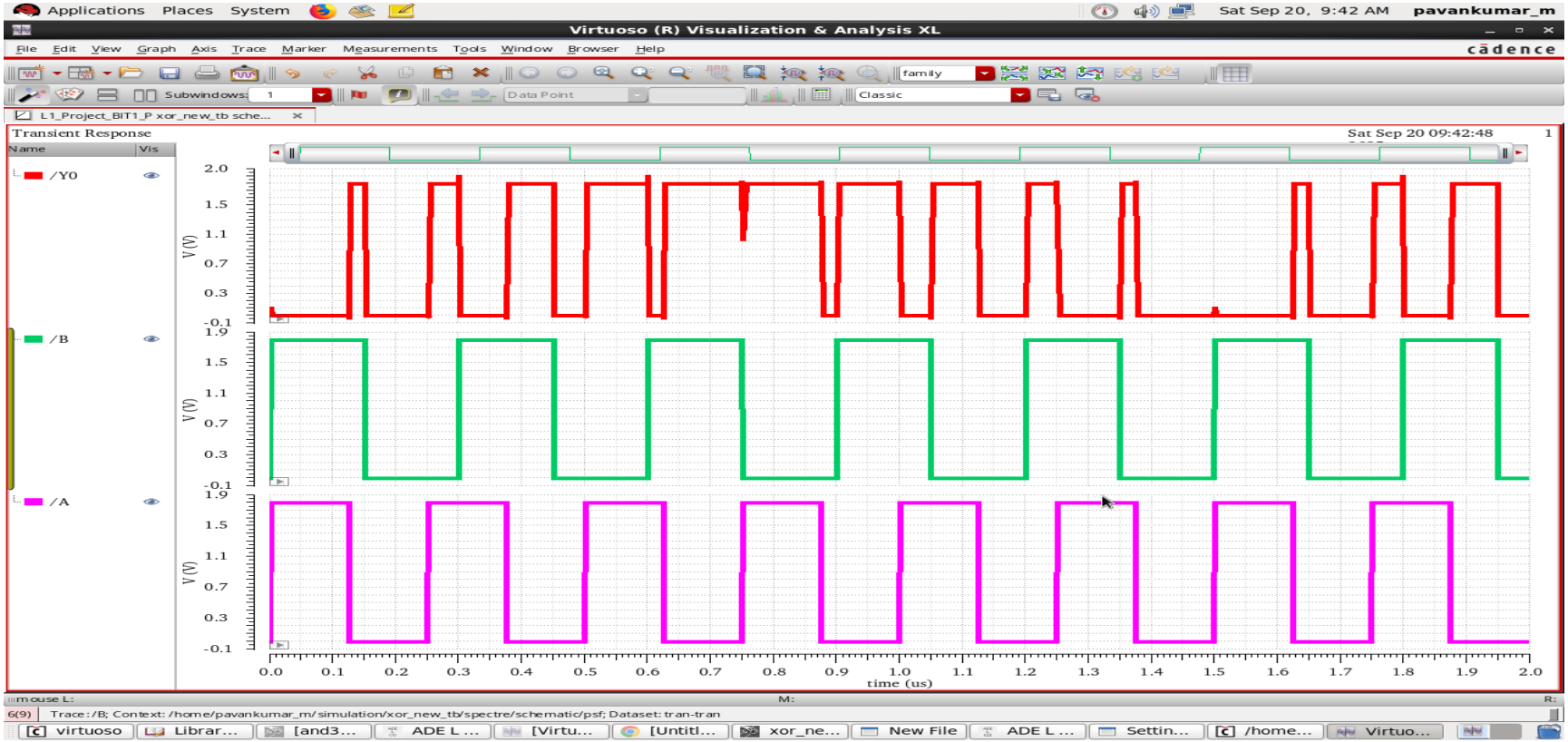
EXOR Schematic



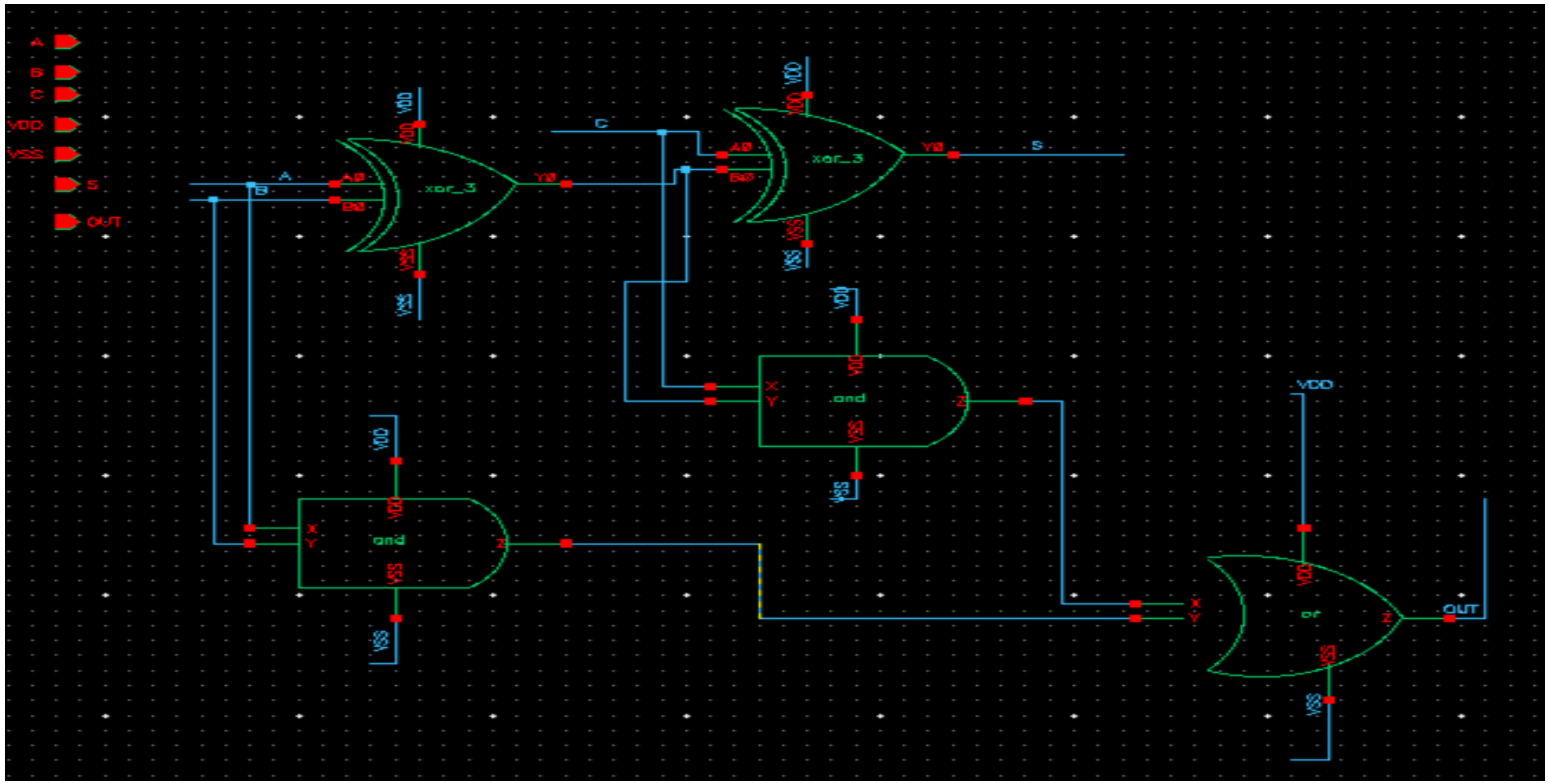
Exor - testbench



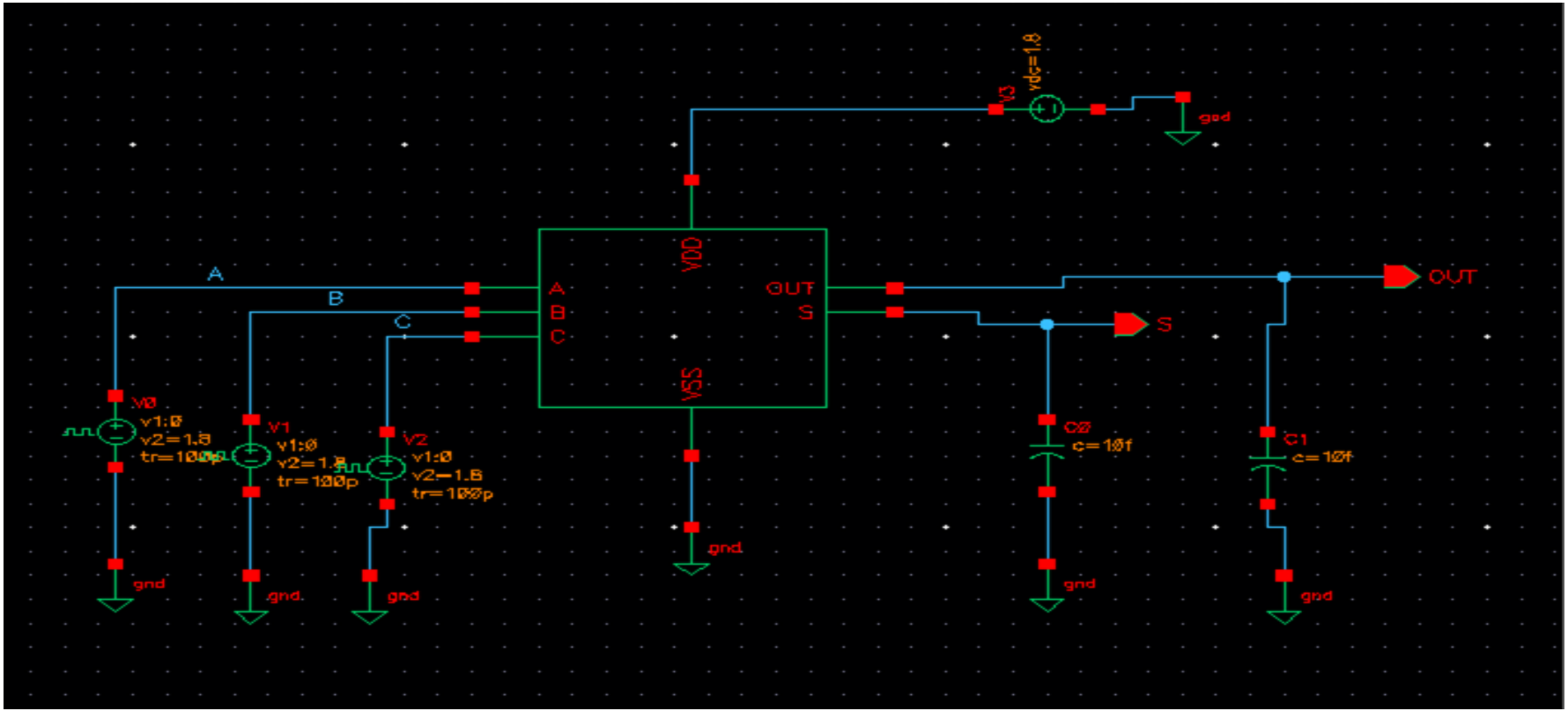
EXOR_New Simulation Result



FULL_Adder Schematic



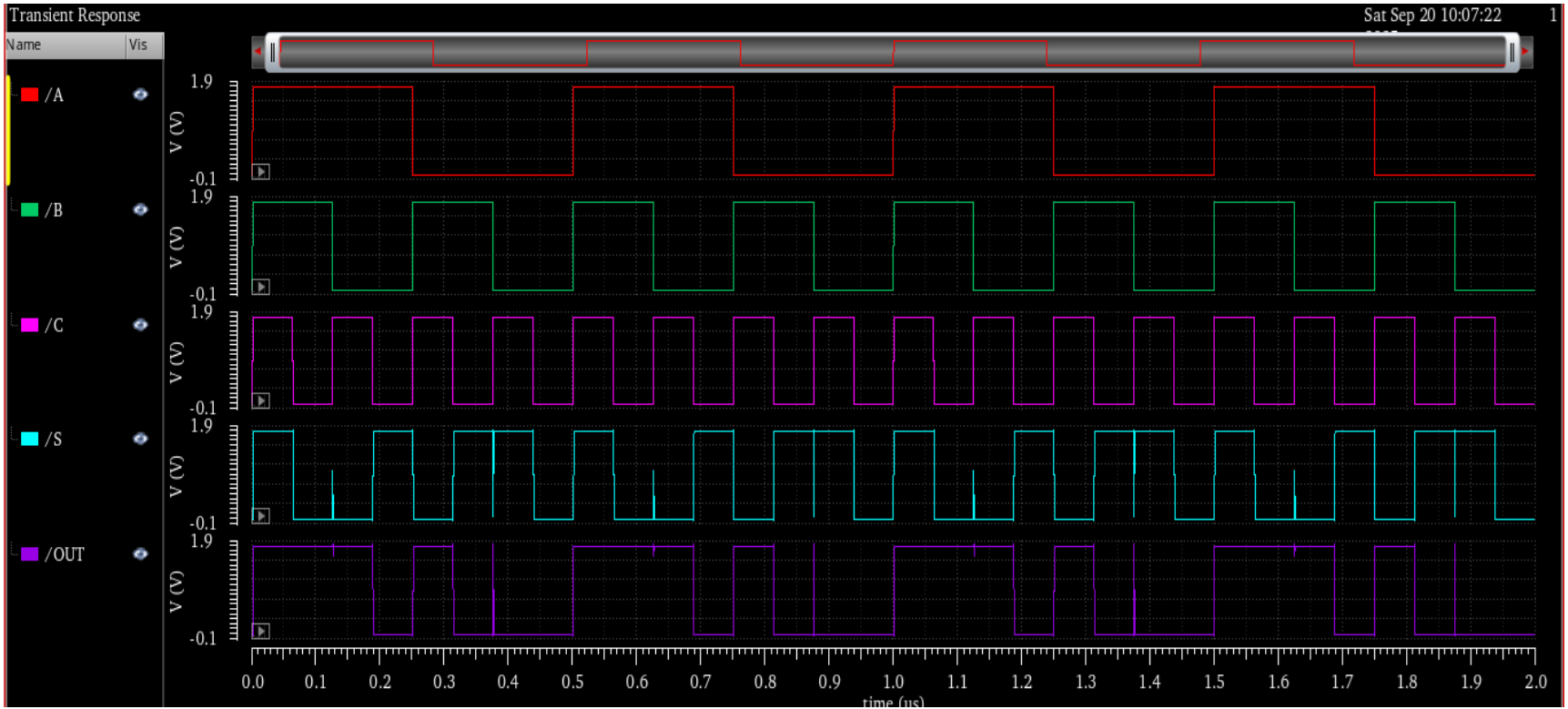
Full Adder - testbench



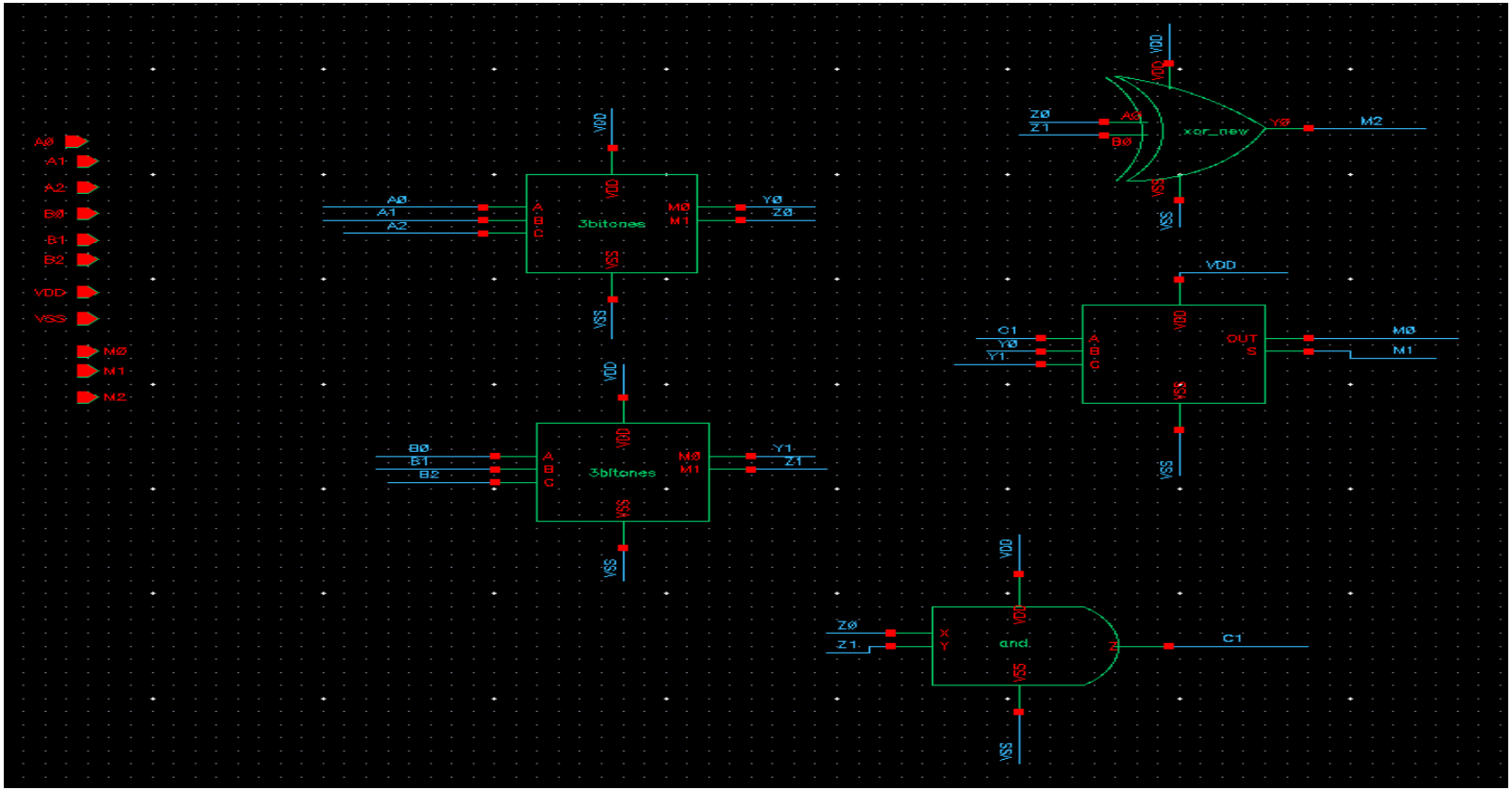
FULL ADDER truth table

Adder				
Truth Table				
A	B	C	S	OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

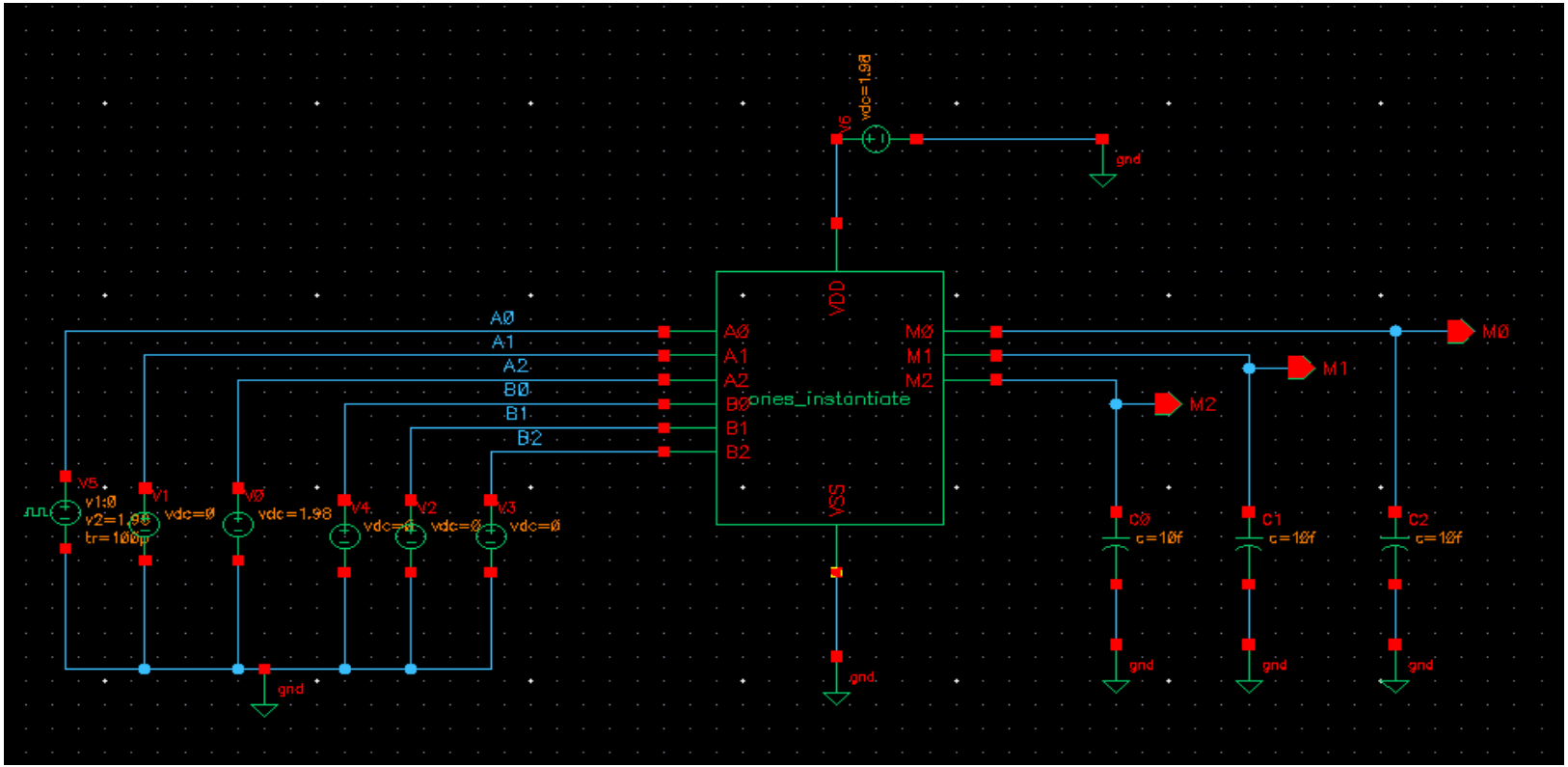
FULL ADDER Waveforms



Bit -1 Schematic



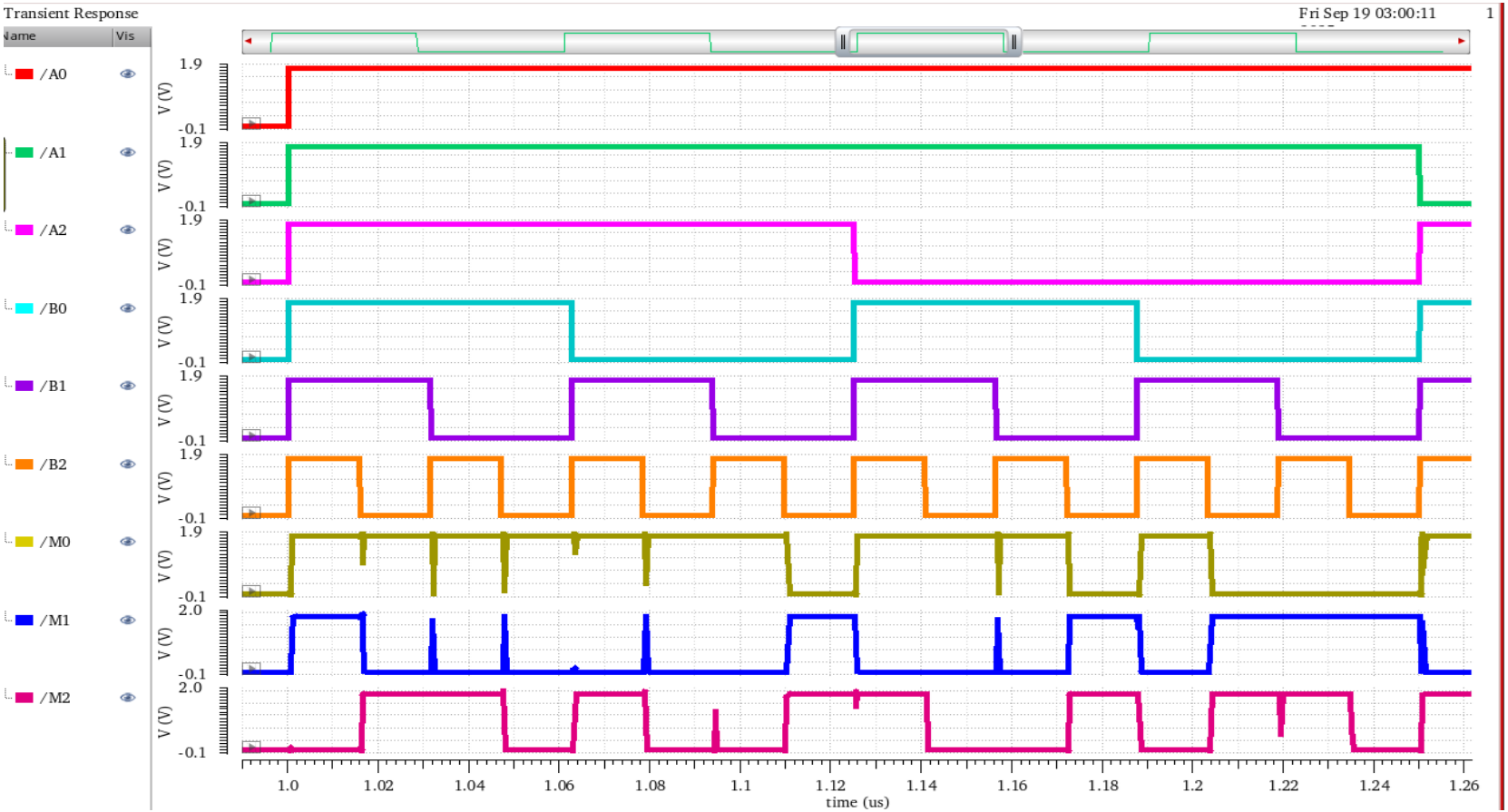
Bit1 - schematic_tb



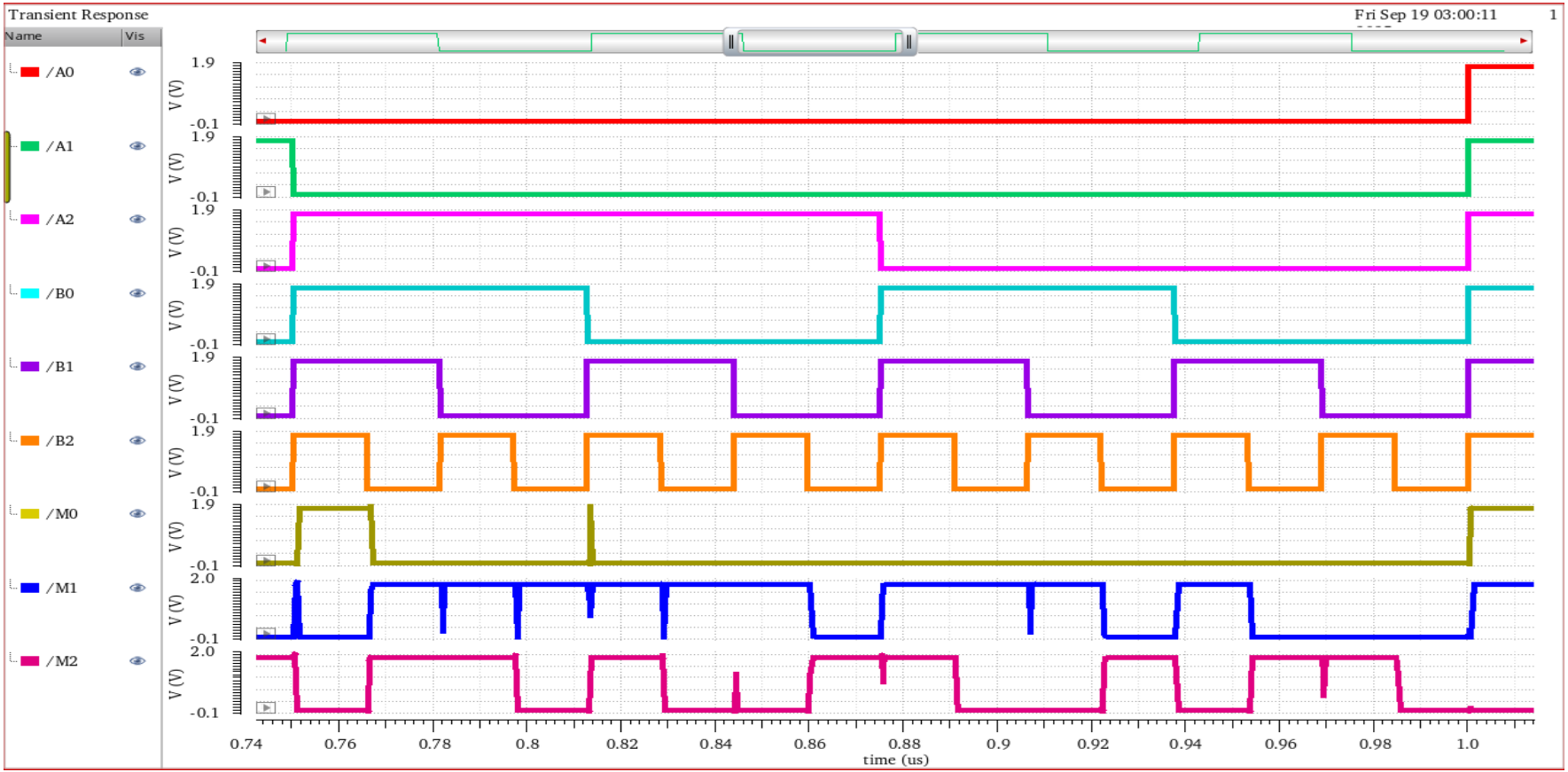
Bit1 - truth-table

BIT 1								
Truth Table								
A0	A1	A2	B0	B1	B2	M0	M1	M2
0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1
0	0	0	0	1	0	0	0	1
0	0	0	0	1	1	0	1	0
0	0	0	1	0	0	0	0	1
0	0	0	1	0	1	0	1	0
. .	. .	. .	. .	. .	. .	. .	. .	. .
1	1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1	0

Bit1 waveforms



Bit1 waveforms



Worst delay A0 → M0

Process	FF	TT	SS
Rise delay	618.87ps	849.22ps	1.138fs
Fall delay	696.24ps	927.601ps	1.198fs
Current	1.52uA	1.336uA	1.219uA

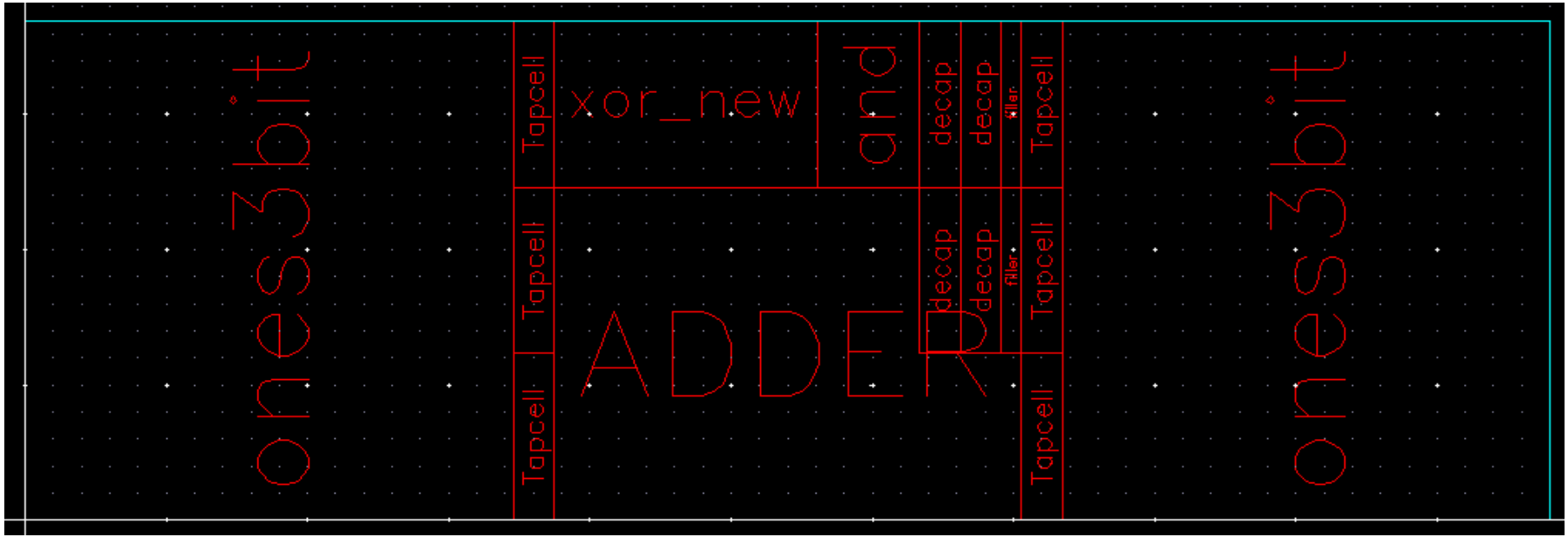
Number of Transistor used - 228

APPLICATIONS

- Error detection(In hamming code)
- Voting machine
- Image/data processing
- Networking

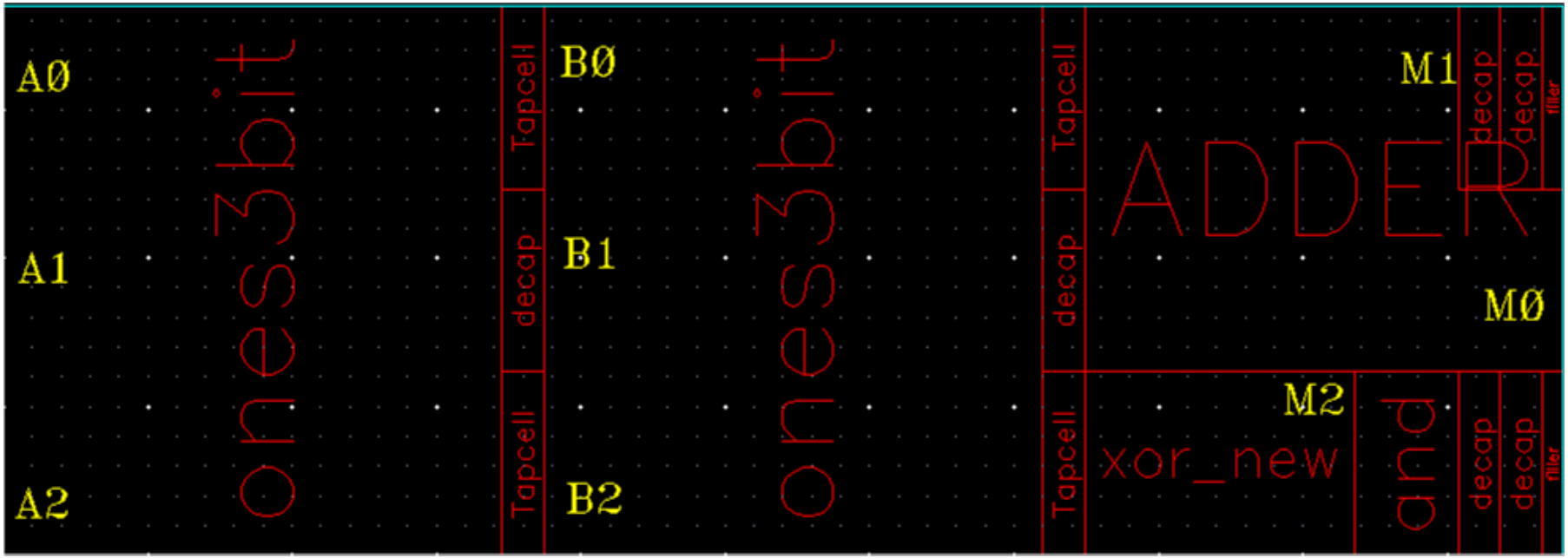
Floorplan - 1

Area - 997 um^2

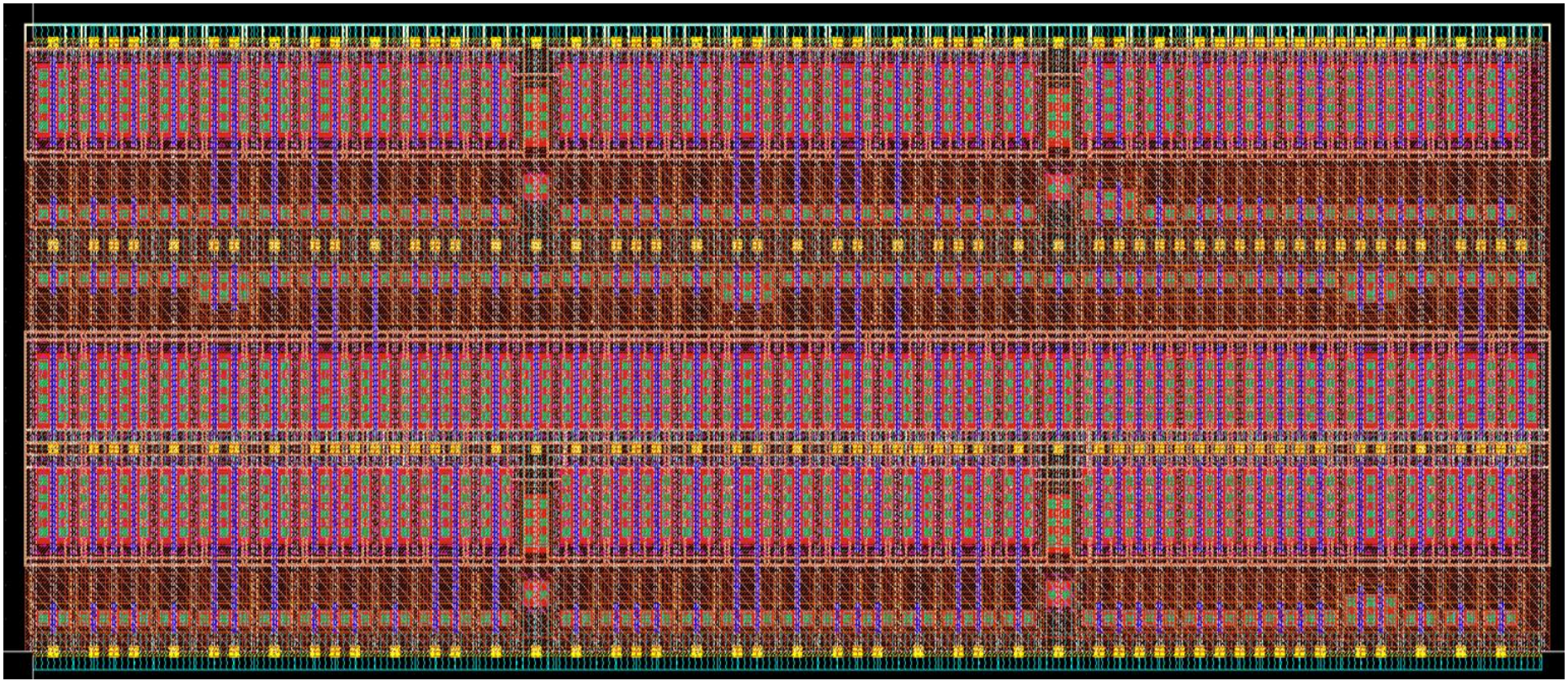


Floorplan - 2

Area - 997um^2

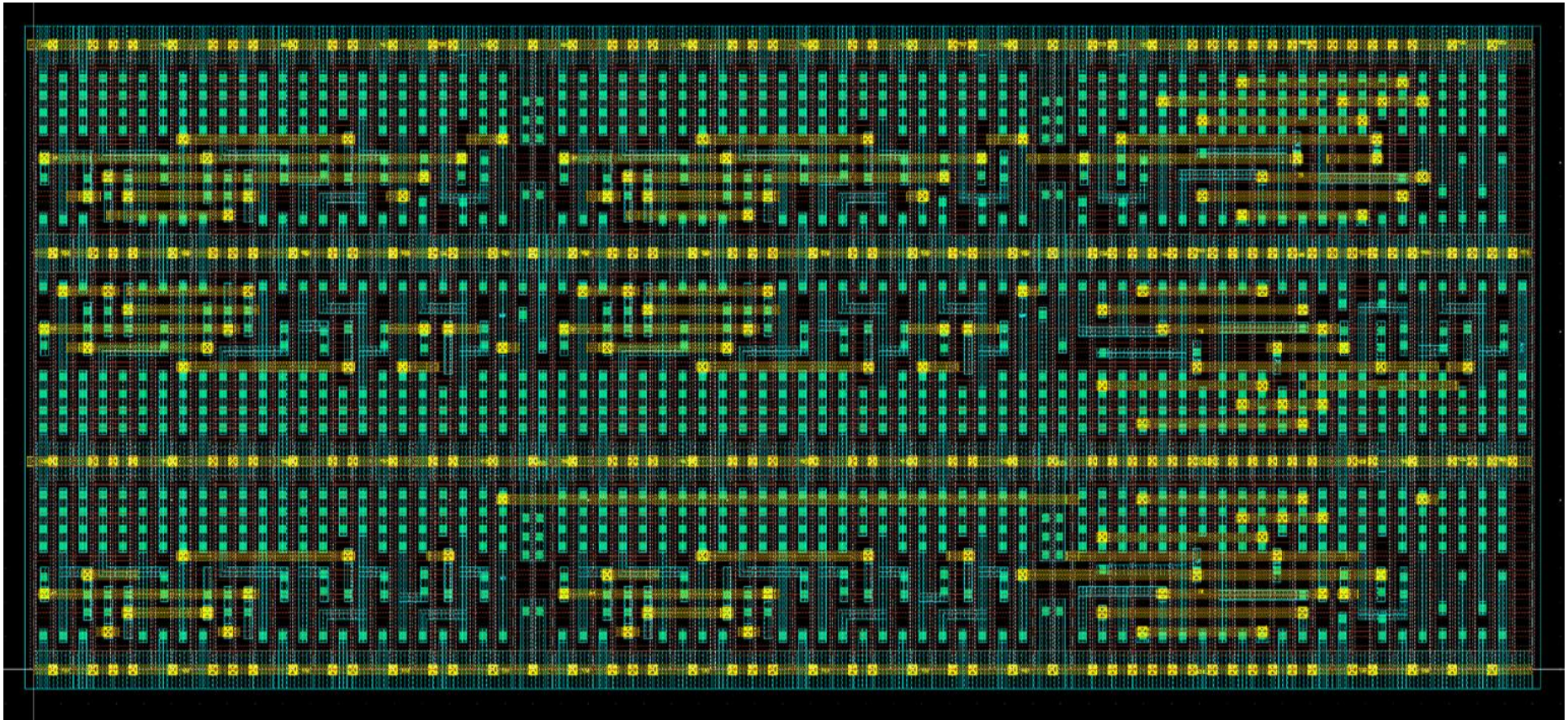


Main block Placement

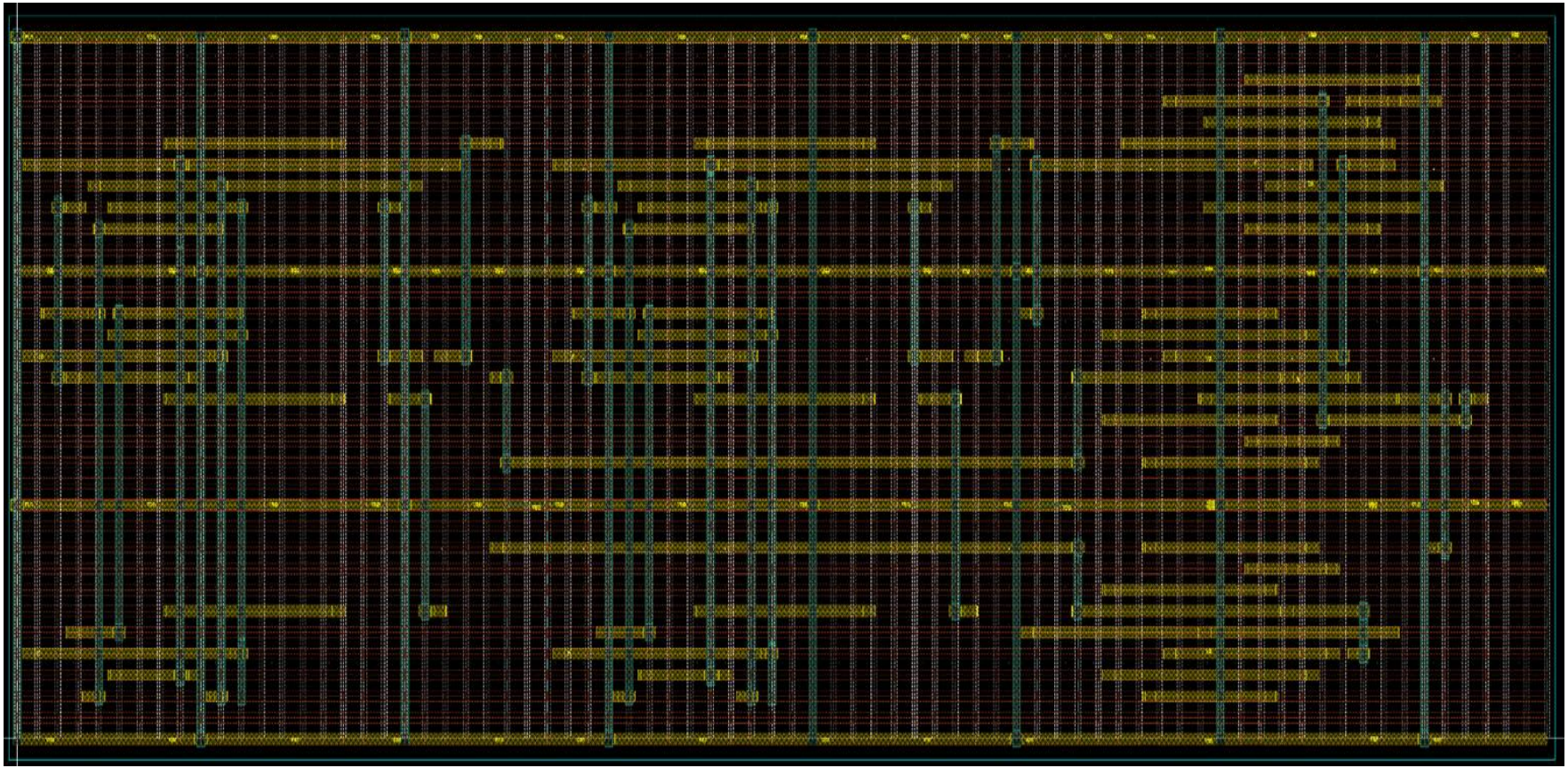


Routing top level

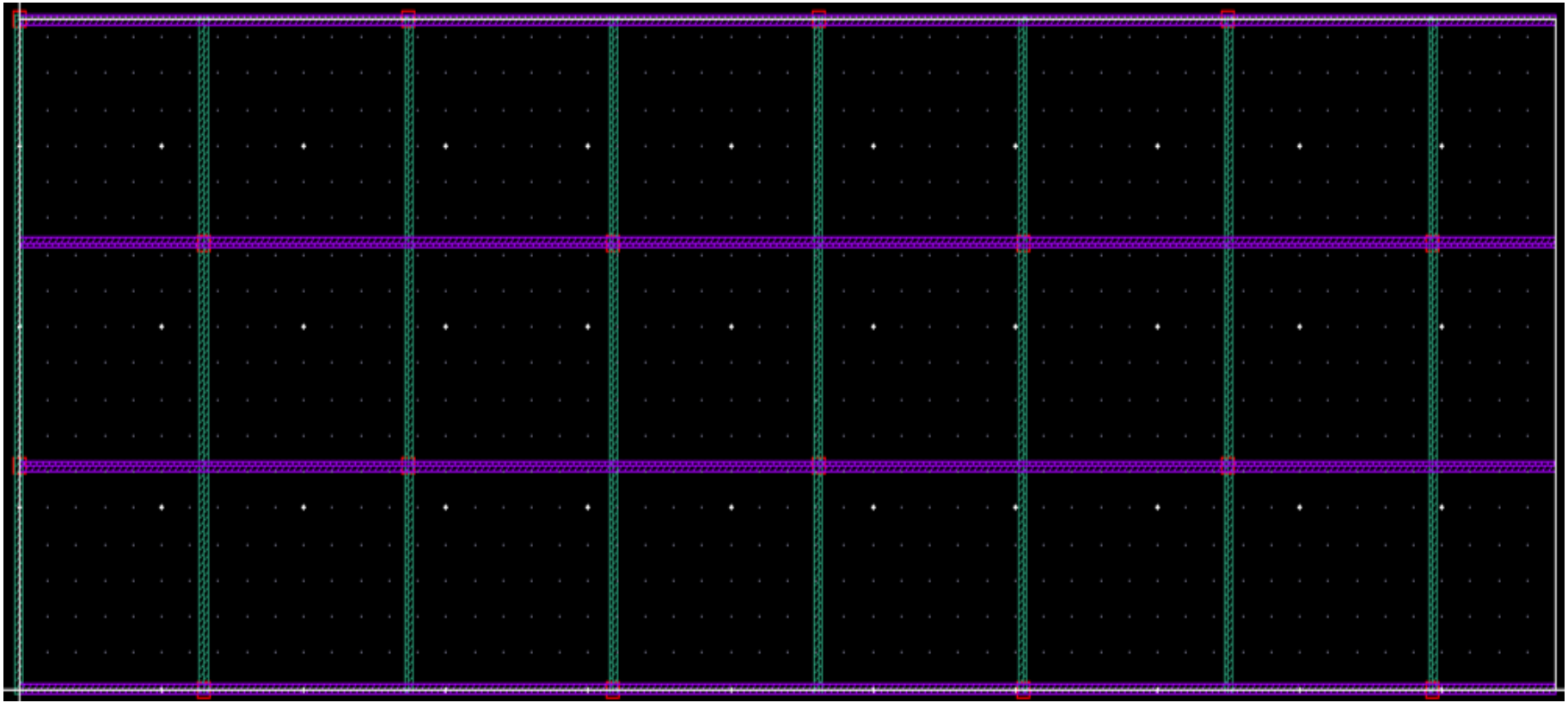
M1-M2 routing



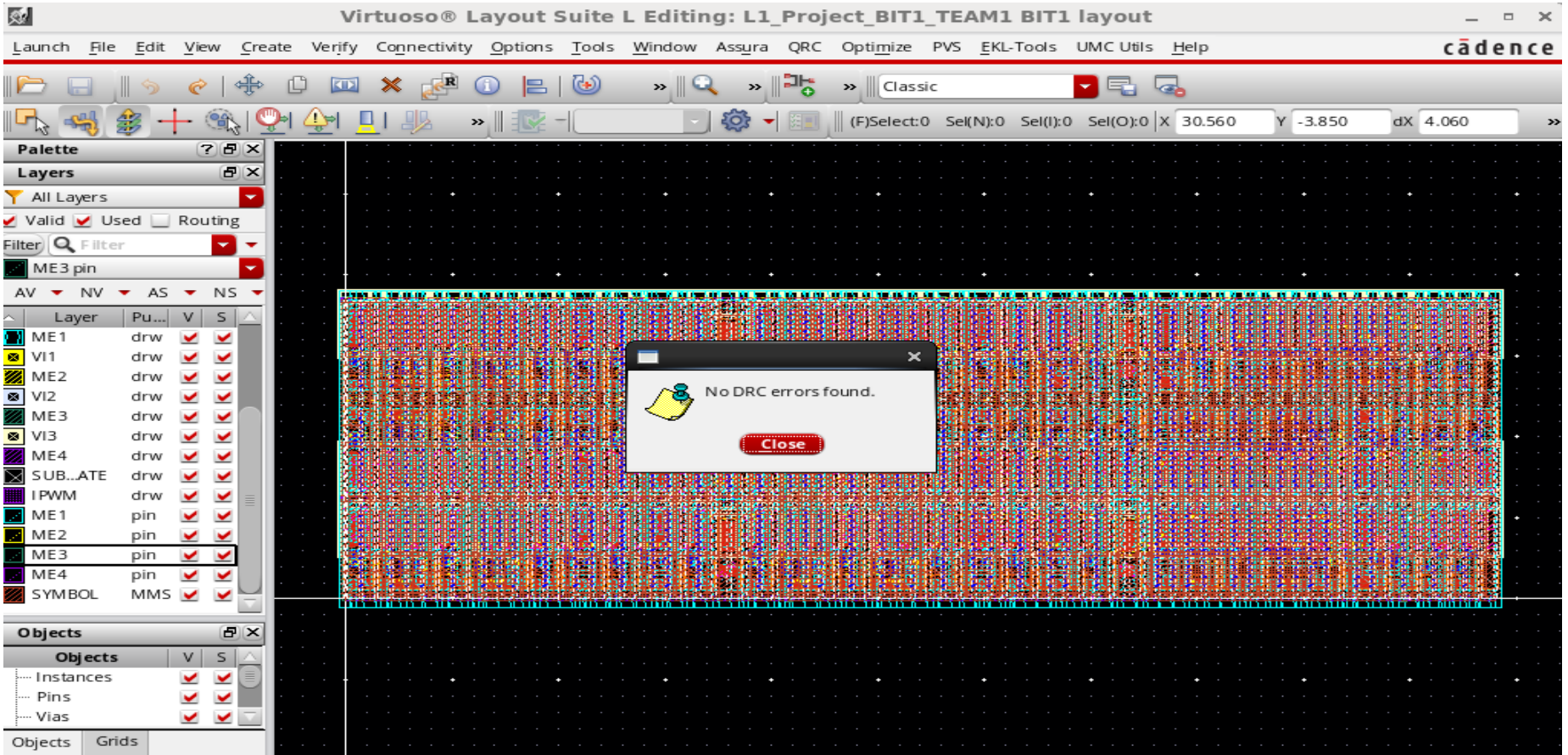
M2-M3 routing



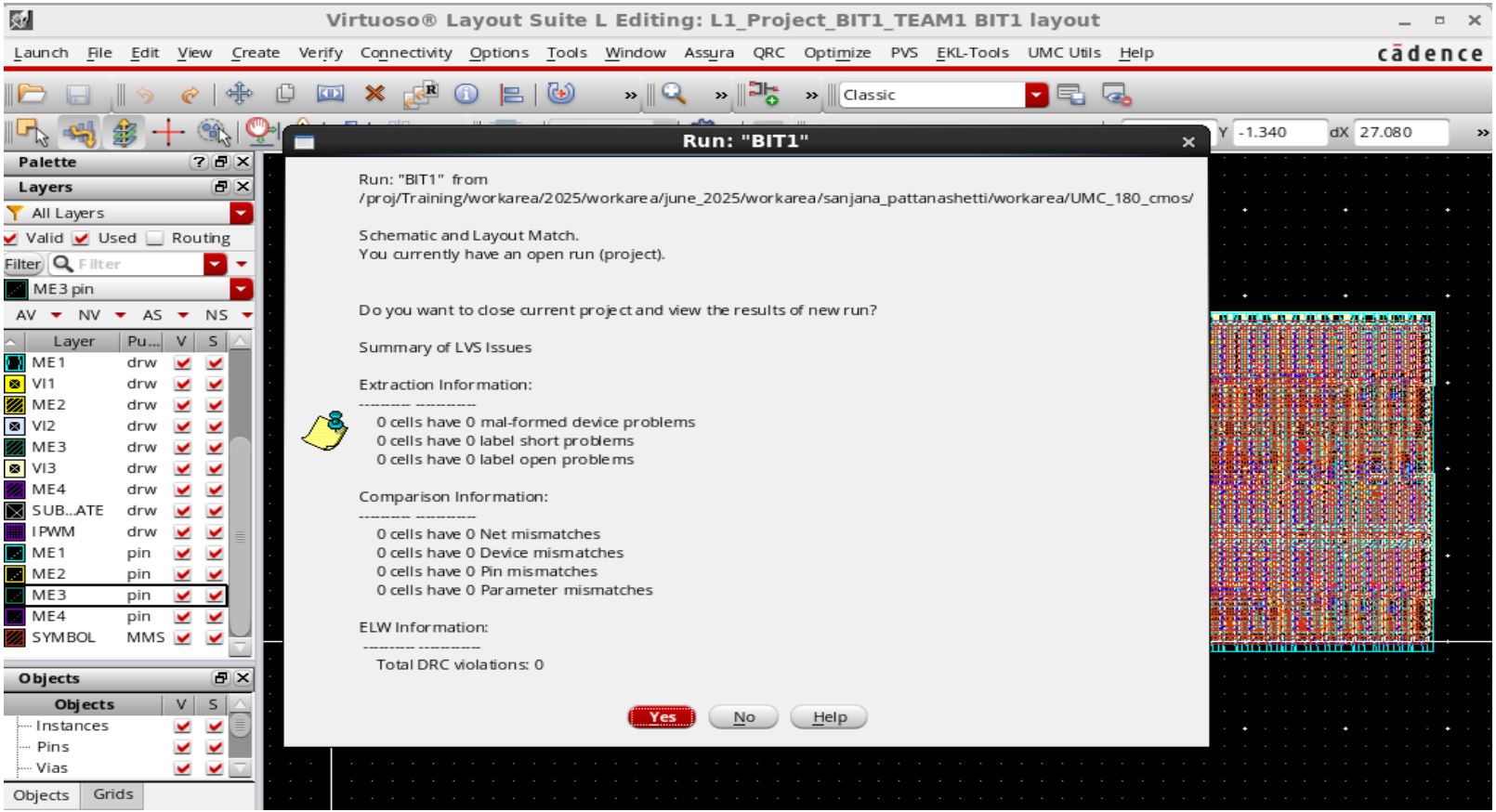
Power mesh



DRC - Check of Main Block



LVS Check Main Block



Overall Outcomes by the Team

1. Learned how to do floorplan.
2. Routing of sub-blocks
3. Top-level Routing
4. How to Plan Power Mesh
5. How to clean DRC and LVS in top-level.

Difficulties

1. Routing of Exor in 13 CPP
2. Decap
3. Routing of Ones-3bit

Work division between team members

1. Sanjana - Simulation of standard cells , 3-bit ones , main block , delay calculation , floorplan of main-block 1 , inv and full adder , ones3bit placement of inv , and3 , ones3bit , bit 1 .

2. Pavan - Simulation of standard cells , Simulation of OR EXOR, main block, current calculation, floorplan of OR , EXOR , ones3bit , de-cap layout , or layout ,Top level Routing Placement of De-cap ,OR , EXOR.

3. Jaine - Simulation of standard cells, simulation of Adder , PVT Analysis , floorplan of AND , AND 3, main block tried placements of AND , ADDER , Power Mesh, Routing of FULL ADDER.