EENG 5560 HW 2 Report

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Design

Block diagrams.

Overall design

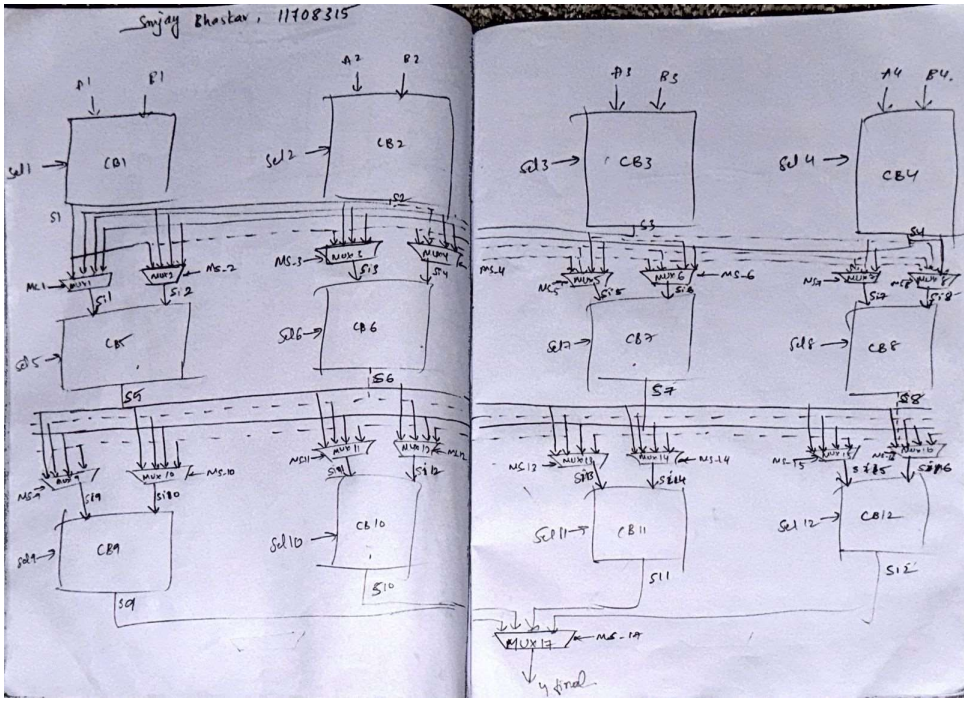


Figure 1- top module: Overall Design Block Diagram

- Overall Component: ASSIGNMENT_2[4X3]
- Overall ports for case_1:
  - Inputs:
    - A1: 6 bits
    - B1: 6 bits
    - A2: 6 bits
    - B2: 6 bits
    - A3: 6 bits
    - B3: 6 bits
    - A4: 6 bits
    - B4: 6 bits
  - Outputs:
    - YFINAL: 6 bits
- Subcomponents:

  1.COMPUTATIONAL BLOCK (CB1, CB2, CB3, CB4, CB5,CB7,CB10)—Rotate Right, Subtraction, NAND, XOR, OR, ADD and Greater Than.

2.MULTIPLEXER (Mux1, Mux2, Mux5, Mux6, Mux11, Mux12, Mux17)-4:1

- Necessary intermediate signals:
  - S1, S2, S3, S4, S5, S7, S10.
  - Sel_1, Sel_2, Sel_3, Sel_4, Sel_5, Sel_7, Sel_10—Each Computational Block
  - Ms_1, Ms_2, Ms_5, Ms_6, Ms_11, Ms_12, Ms_17—Each Mux

Parameters: d_w – data width (for inputs and outputs)

Input ports and intermediate signals:

Port name	Bit width	Purpose
A1, B1,A2,B2,A3,B3,A4,B4	d_w = 6	Data inputs
Sel_1, Sel_2, Sel_3, Sel_4, Sel_5, Sel_6, Sel_7, Sel_8, Sel_9, Sel_10, Sel_11, Sel_12.	w = 5	Selection line, selects data input to send to output for Computational Units
Ms_1, Ms_2, Ms_3, Ms_4, Ms_5, Ms_6, Ms_7, Ms_8, Ms_9, Ms_10, Ms_11, Ms_12, Ms_13, Ms_14, Ms_15, Ms_16, Ms_17.	w = 2	Selection line, selects data input to send to output for Mux's
S1, S2,S3,S4,S5,S6,S7,S8,S9,S10, S11,S12	w = 6	Signal lines i.e., Output from CU's
Si1, Si2, Si3, Si4, Si5, Si6, Si7, Si8, Si9, Si10, Si11, Si12, Si13, Si14, Si15, Si16	w = 6	Signal lines i.e., Output from MUX's

Output ports:

Port name	Bit width	Purpose
YFINAL	d_w = 6	Data output

- Overall ports for case_2:
  - Inputs:
    - A1: 6 bits
    - B1: 6 bits
    - A2: 6 bits
    - B2: 6 bits
    - A3: 6 bits
    - B3: 6 bits
    - A4: 6 bits
    - B4: 6 bits
  - Outputs:
    - YFINAL: 6 bits
- Subcomponents:

  1.COMPUTATIONAL BLOCK (CB1, CB2, CB3, CB4, CB6, CB8, CB11)—AND, LSL, LSR, MULT, ROL, NE, OR.

  2.MULTIPLEXER (Mux3, Mux4, Mux7, Mux8, Mux13, Mux14, Mux17)-4:1

- Necessary intermediate signals:
  - S1, S2, S3, S4, S6, S8, S11.
  - Sel_1, Sel_2, Sel_3, Sel_4, Sel_6, Sel_8, Sel_11—Each Computational Block
  - Ms_3, Ms_4, Ms_7, Ms_8, Ms_13, Ms_14, Ms_17—Each Mux

Subcomponents

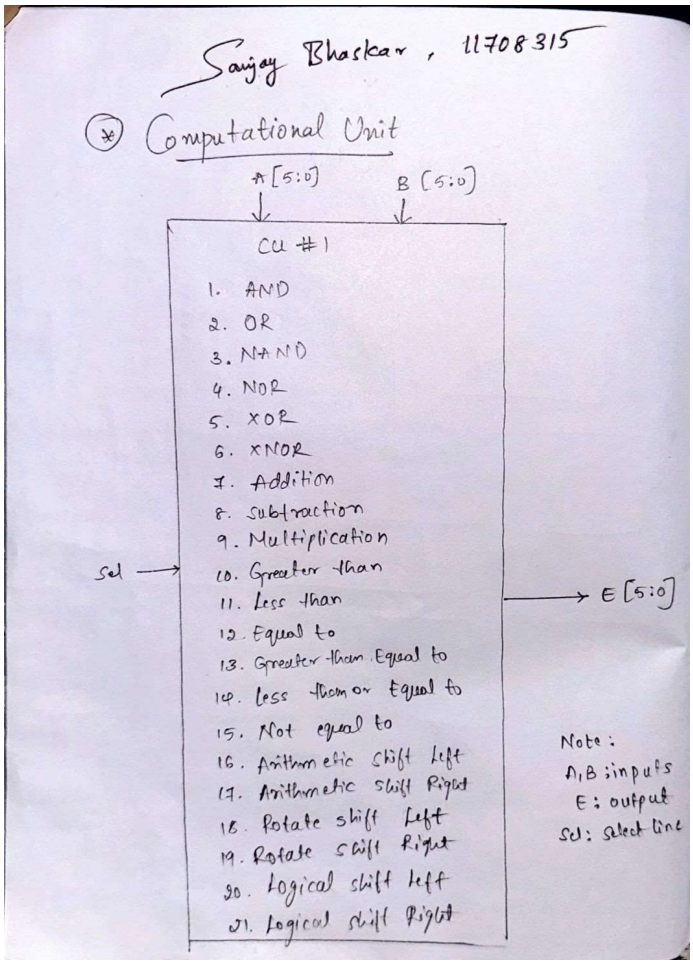


Figure 2- Subcomponent: Computational Unit Block Diagram

Subcomponent: Computational Unit Block Diagram

Input ports:

Port name	Bit width	Purpose
A,B	d_w = 6	Data inputs
Sel	5	Select line, selects which of the 2 data inputs to send to data output

Output ports:

Port name	Bit width	Purpose
E	d_w = 6	Data output

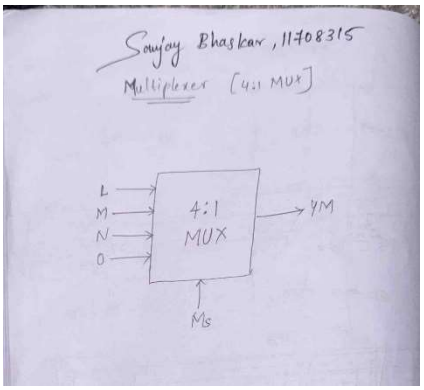


Figure 3- Subcomponent: 4:1 MUX Block Diagram

Subcomponent: 4x1 mux

Input ports:

Port name	Bit width	Purpose
L,M,N,O	d_w = 6	Data inputs
Ms	2	Select line, Selects one of the following operations out of 4.

Output ports:

Port name	Bit width	Purpose
YM	d_w = 6	Data output

Design Explanation

Functionality

Behavioral design functionality explanation: To form a Top-level Design there are few steps to follow First we need to write a code for Computational Unit and write the test bench for CU and verify all 21 operations are working properly, Verify the output waveform with the Expected calculations. Then write a code for MUX which is required to connect CUs in consecutive levels because we need to connect the CUs in matrix format. So, write the test bench for Mux and verify with the expected output.

In this case Mux expected output Truth Table is b

Select input	Resulting output
00	L
01	M
10	N
11	O

In this case 4:1 Mux is used which has 2 bits select line. Combination of the 2 bits select line is responsible for choosing the appropriate inputs.

If combination is resulting in “00” then resulting output will be 1st input i.e., L.

If combination is resulting in “01” then resulting output will be 2nd input i.e., M.

If combination is resulting in “10” then resulting output will be 3rd input i.e., N.

If combination is resulting in “11” then resulting output will be 4th input i.e., O.

Now, Computational Units outputs can be connected to Mux and Output of Mux can be connected to Computational Units.

After this write a code to connect Computations units and design an Overall Design i.e., 4X3 computational Unit.

All the computational units that were designed is arranged in a matrix(3X4) format and are named accordingly (1,1), (1,2), (1,3), (1,4), (2,1), (2,2), (2,3), (2,4), (3,1), (3,2), (3,3), (3,4).

In Case 1: The very first row CUs in the matrix is connected to two of the CUs in the second row respectively (2,1) and (2,3) via MUX [4:1]. Since the direct connection of CUs are not very efficient, Connection of required CUs are done with the help of MUX.

There is a total of 17 MUX used for building an overall design. Precisely in the above case a total of 7 Muxes are used to connect CUs per the given case: 1. Mux 1, 2, 5, 6 are used for connecting Cu’s in row 1 and row 2 whereas Mux 11 and 12 are used for connecting row 2 and 3 respectively. The final output is taken from CU (3,2) which is in turn connected to Mux 17.

Results

Generated Schematics

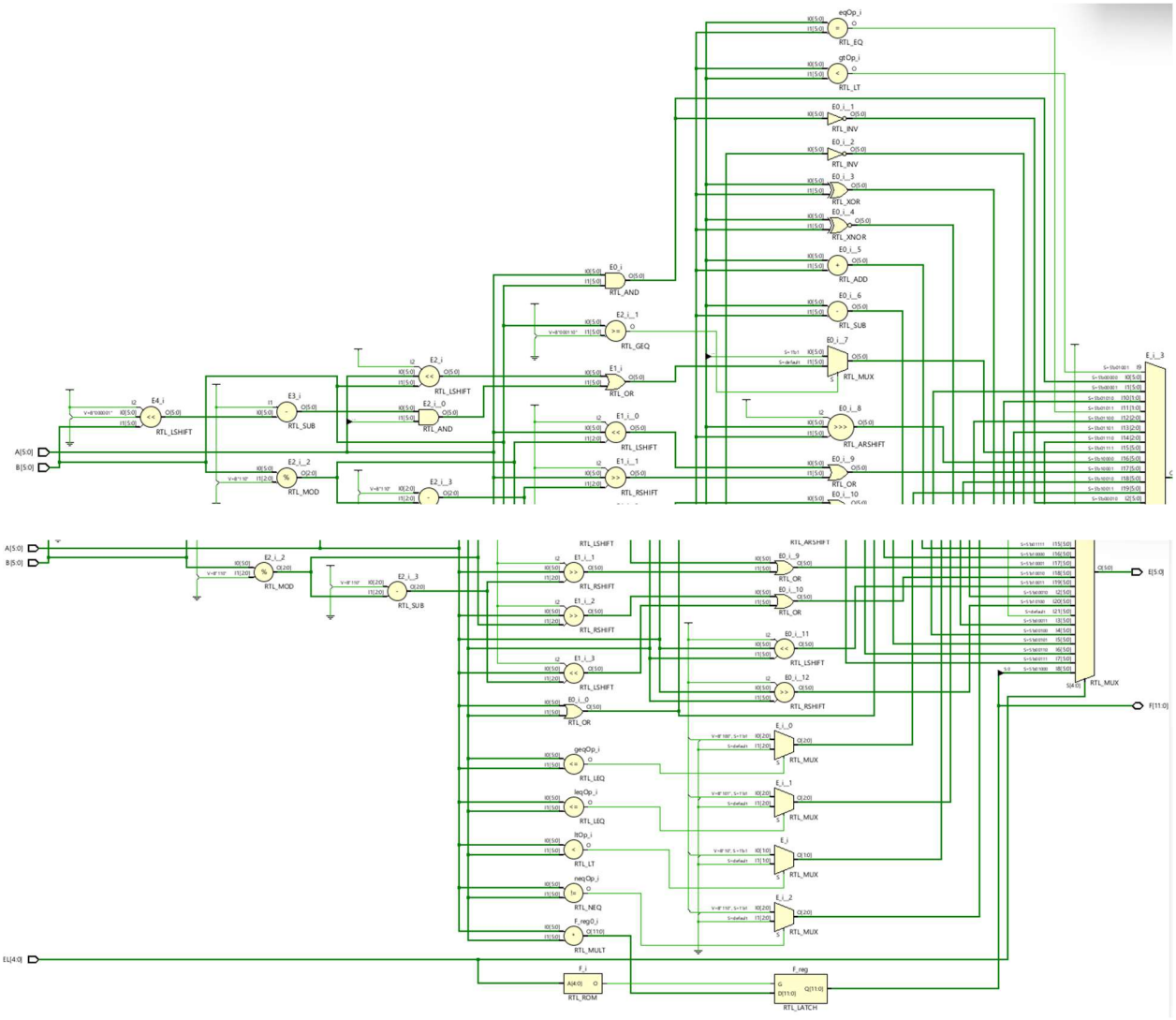


Figure 4 – Computational Unit RTL Schematic.

This is the RTL Schematic of Computational Unit.

All 21 operations are listed in this RTL Schematic and Due to picture is big I have added 2 pictures such as first part and second part.

All the 21 operations is listed in this RTL Schematic respectively, Whereas,

RTL Mux is the component the system is using to combine all 21 inputs and give only one output.

As there are 21 operations, we need at least 5 bit select line in binary.

1) If we select “00000” from the select line, then the output will be AND operation.
2) If we select “00001” from the select line, then the output will be OR operation.
3) If we select “00010” from the select line, then the output will be NAND operation.
4) If we select “00011” from the select line, then the output will be NOR operation.
5) If we select “00100” from the select line, then the output will be XOR operation.
6) If we select “00101” from the select line, then the output will be XNOR operation.
7) If we select “00110” from the select line, then the output will be ADD operation.
8) If we select “00111” from the select line, then the output will be SUB operation.
9) If we select “01000” from the select line, then the output will be MUL operation.
10) If we select “01001” from the select line, then the output will be GT operation.
11) If we select “01010” from the select line, then the output will be LT operation.
12) If we select “01011” from the select line, then the output will be EQ operation.
13) If we select “01100” from the select line, then the output will be GTE operation.
14) If we select “01101” from the select line, then the output will be LTE operation.
15) If we select “01110” from the select line, then the output will be NEQ operation.
16) If we select “01111” from the select line, then the output will be Arithmetic Shift Left operation.
17) If we select “10000” from the select line, then the output will be Arithmetic Shift Right operation.
18) If we select “10001” from the select line, then the output will be Rotate Shift Left operation.
19) If we select “10010” from the select line, then the output will be Rotate Shift Right operation.
20) If we select “10011” from the select line, then the output will be Logical Shift Left operation.
21) If we select “10100” from the select line, then the output will be Logical Shift Right operation.

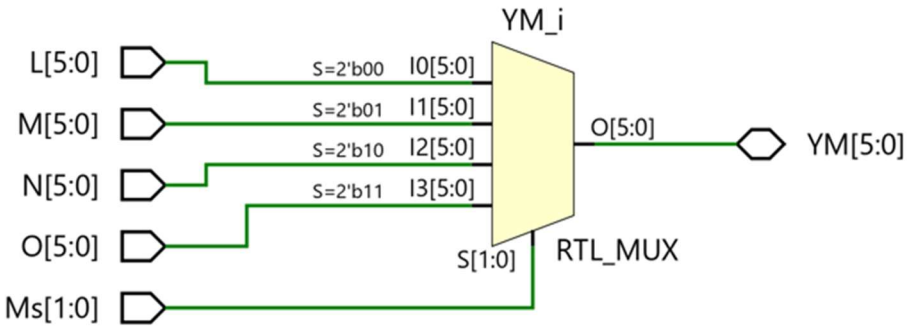


Figure 5 - 4x1 mux RTL schematic.

This is the RTL Schematic of Mux.

As per the above circuit diagram we can see RTL schematic diagram is same and naming is also same so that it will be easy to analyze and understanding the module.

L,M,N,O is the inputs taken in handwritten ckt diagram and it’s same in the RTL schematic too. Ms is the Mux Select line, and YM is the output.

1) L[5:0] is mapped with L
2) M[5:0] is mapped with M
3) N[5:0] is mapped with N
4) O[5:0] is mapped with O

5) Ms[1:0] is mapped with Ms
6) O[5:0] is mapped with O

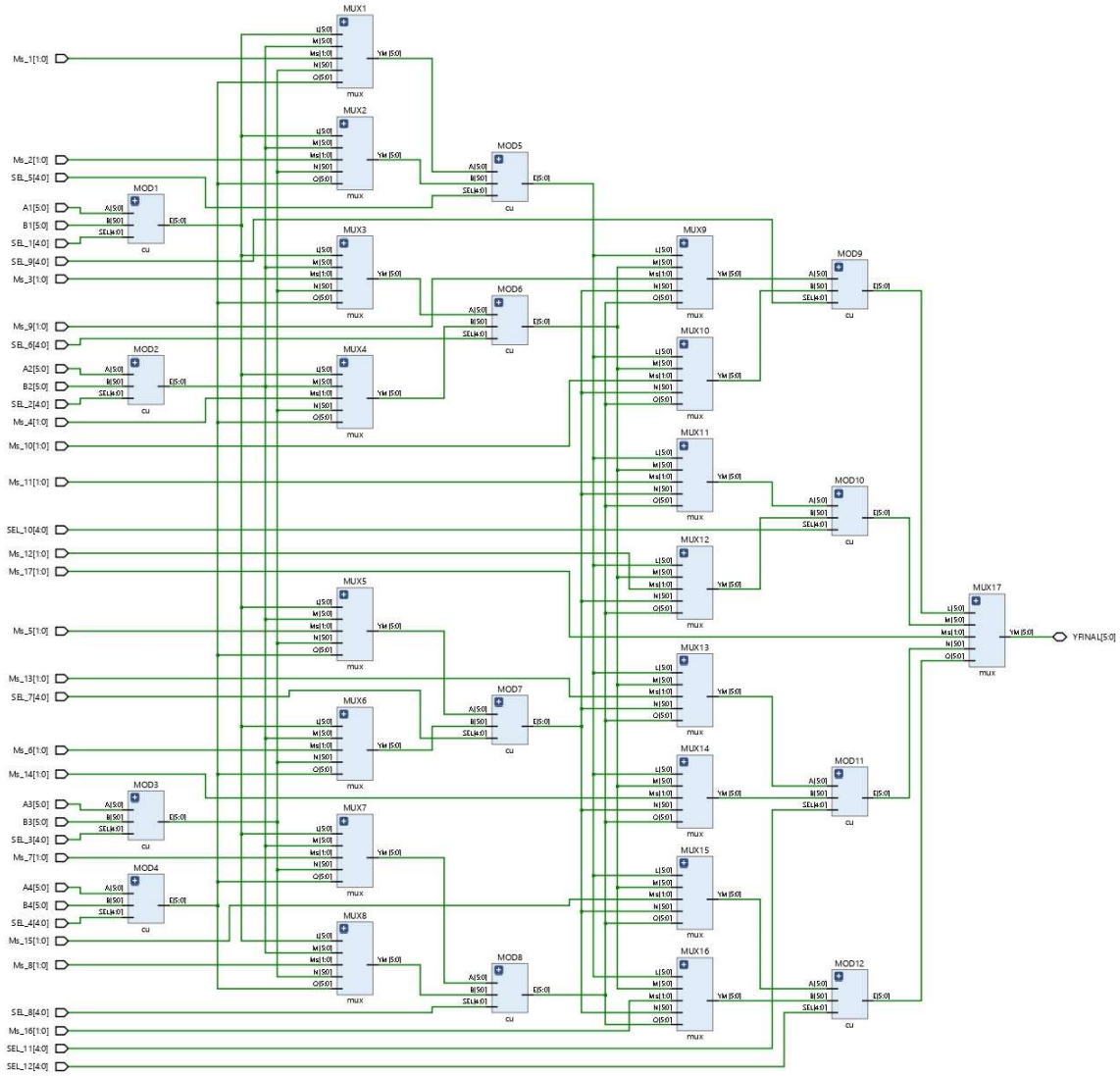


Figure 6 – Overall Design RTL schematic.

In the generated schematic, there are 4:1 muxes receiving the 6 bit data from Computational Units from row 1 to row 2 and row 2 to row 3, overall data inputs and using the select lines of Cus and select line of muxes we can connect any of the Cu in 1st row to the any of the Cu in the 2nd row and so on. The outputs of the 4x1 muxes are fed as inputs to the 2nd row CUs. The output of the 2nd row CUs is connected to again muxes as input and output of the mux is connected to Cu in the third row. This is effective connections where user can modify the path any time with any of the operation. This Behavior of output matches that of our design.

Waveforms

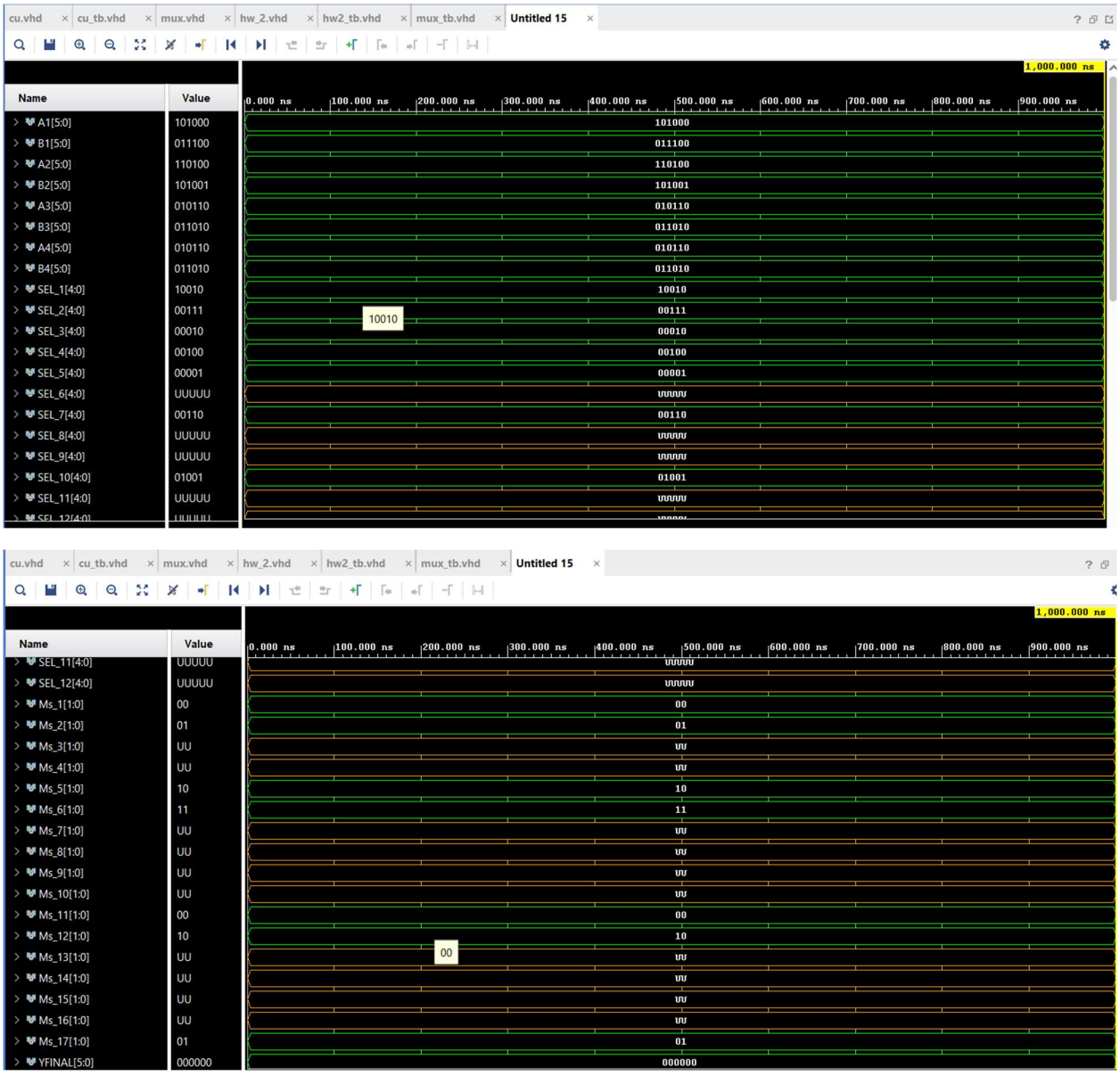


Figure 7 – Overall Waveforms for Case 1

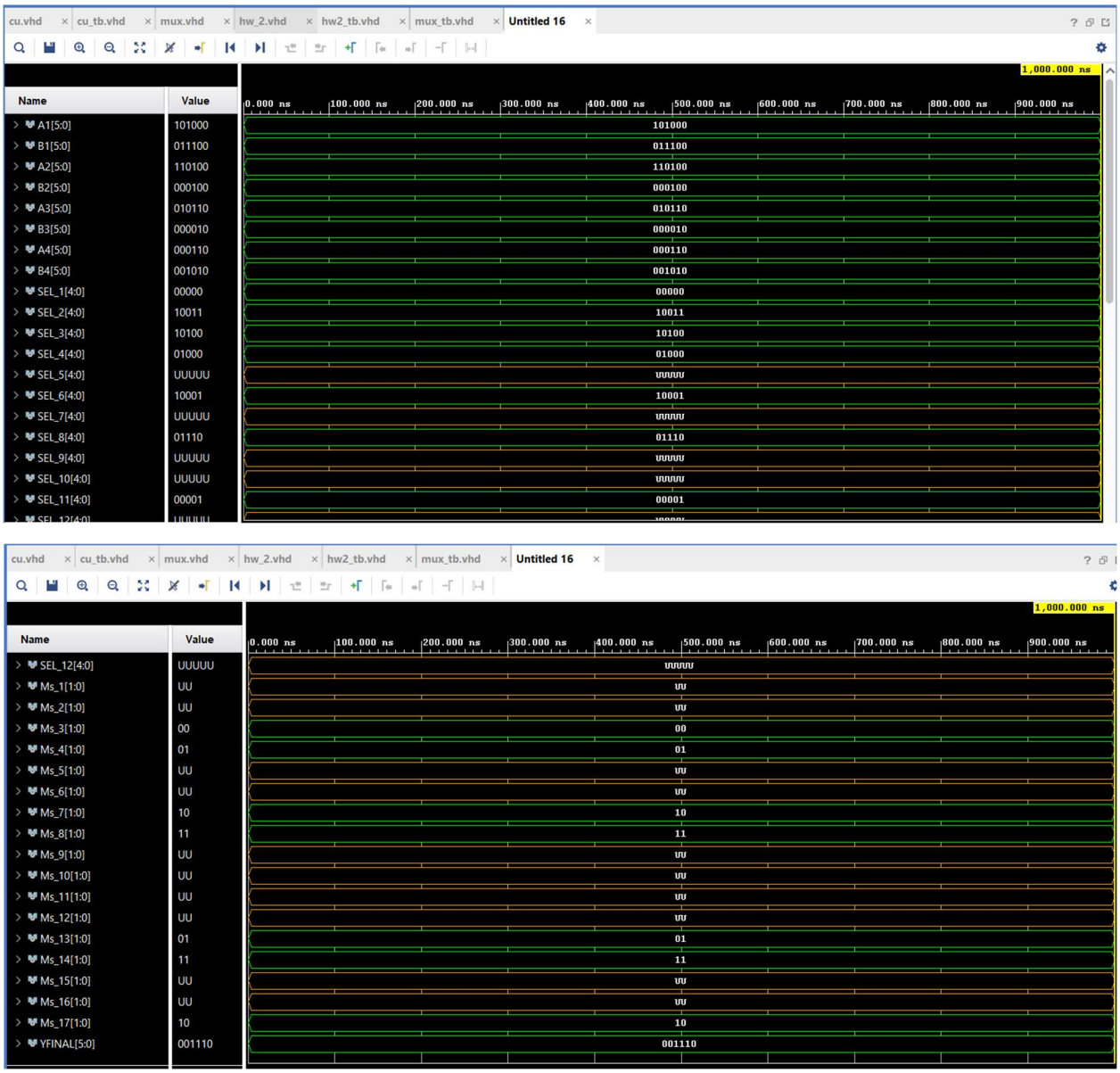


Figure 8 – Overall Waveforms for Case 2

Combinational Unit Waveforms.

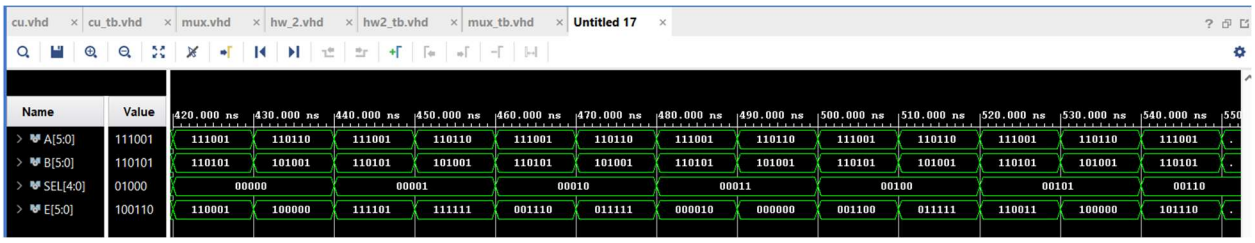


Figure 9 – Combinational Unit Waveform part 1

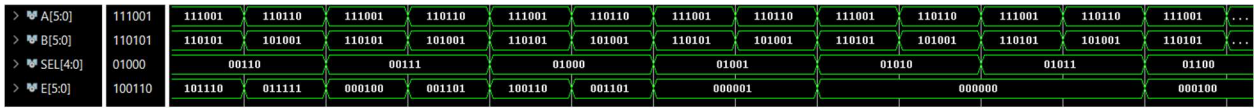


Figure 10 – Combinational Unit Waveform part 2

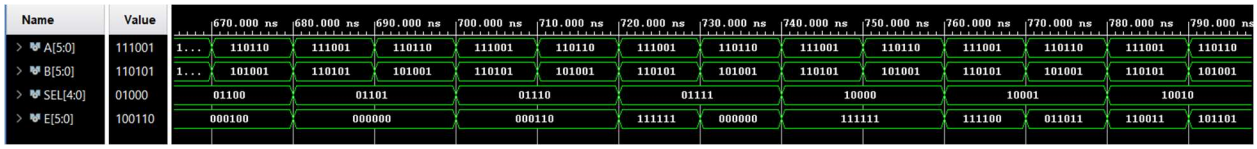


Figure 11 – Combinational Unit Waveform part 3

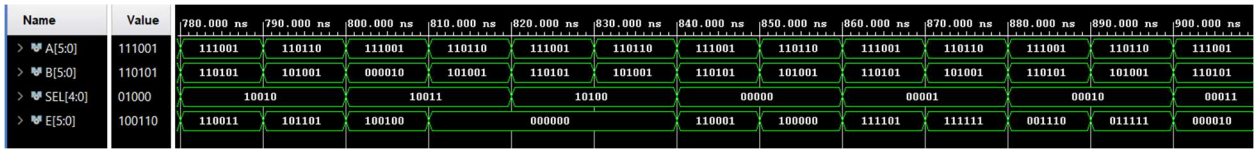


Figure 12 – Combinational Unit Waveform part 4

4:1 Mux Waveform.

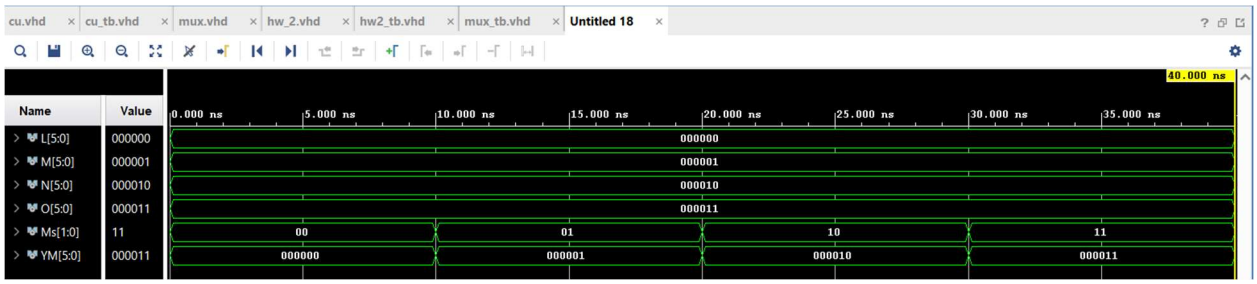


Figure 13 – 4:1 Mux Waveform

Table/Calculations

Overall Design

Test Case 1 (0ns to 10ns):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A1	B1	101000	011100	ROR	000001	000001	Yes
CU2	A2	B2	110100	101001	SUB	011111	011111	Yes
CU3	A3	B3	010110	011010	NAND	101101	101101	Yes
CU4	A4	B4	010110	011010	XOR	001100	001100	Yes
CU5	Si1	Si2	000001	011111	OR	011111	011111	Yes
CU7	Si5	Si6	101101	001100	ADD	111001	111001	Yes
CU10	Si11	Si12	011111	111001	GT	000000	000000	Yes

Test Case 2 (10ns to 20ns):

CU#	SourceA	SourceB	A	B	Oper	Calculated Op	Simulated Op	Match
CU1	A1	B1	101000	011100	AND	001000	001000	Yes
CU2	A2	B2	110100	000100	LSL	000000	000000	Yes
CU3	A3	B3	010110	000010	LSR	000101	000101	Yes
CU4	A4	B4	000110	001010	MULT	000110	000110	Yes
CU5	Si3	Si4	001000	000000	ROL	001000	001000	Yes
CU7	Si7	Si8	000101	000110	NE	000110	000110	Yes
CU10	Si13	Si14	001000	000110	OR	001110	001110	Yes

Explanation:

As can be seen by the table, the waveform output values for both test cases match the calculated values. This means the design works properly.

Case 1 manual calculations and waveform values matches exactly the same.

Subcomponent test cases

Test Case 0ns to 10ns:

Sl no.	A	B	Oper	Calculated Op	Simulated Op	Match
1	**111001**	**110101**	AND (00000)	110001	110001	Yes
2	**111001**	**110101**	OR (00001)	111101	111101	Yes
3	**111001**	**110101**	NAND(00010)	001110	001110	Yes
4	**111001**	**110101**	NOR(00011)	000010	000010	Yes
5	**111001**	**110101**	XOR(00100)	001100	001100	Yes
6	**111001**	**110101**	XNOR(00101)	110011	110011	Yes
7	**111001**	**110101**	ADD(00110)	101110	101110	Yes
8	**111001**	**110101**	SUB(00111)	000100	000100	Yes
9	**111001**	**110101**	MUL(01000)	100110	100110	Yes
10	**111001**	**110101**	GT(01001)	000001	000001	Yes
11	**111001**	**110101**	LT(01010)	000000	000000	Yes
12	**111001**	**110101**	EQ(01011)	000000	000000	Yes
13	**111001**	**110101**	GTE(01100)	000100	000100	Yes
14	**111001**	**110101**	LTE(01101)	000000	000000	Yes
15	**111001**	**110101**	NEQ(01110)	000110	000110	Yes
16	**111001**	**110101**	SLA(01111)	111111	111111	Yes
17	**111001**	**110101**	SRA(10000)	111111	111111	Yes
18	**111001**	**110101**	ROL(10001)	111100	111100	Yes
19	**111001**	**110101**	ROR(10010)	110011	110011	Yes
20	**111001**	**110101**	SLL(10011)	100100	100100	Yes
21	**111001**	**110101**	SRL(10101)	000000	000000	Yes

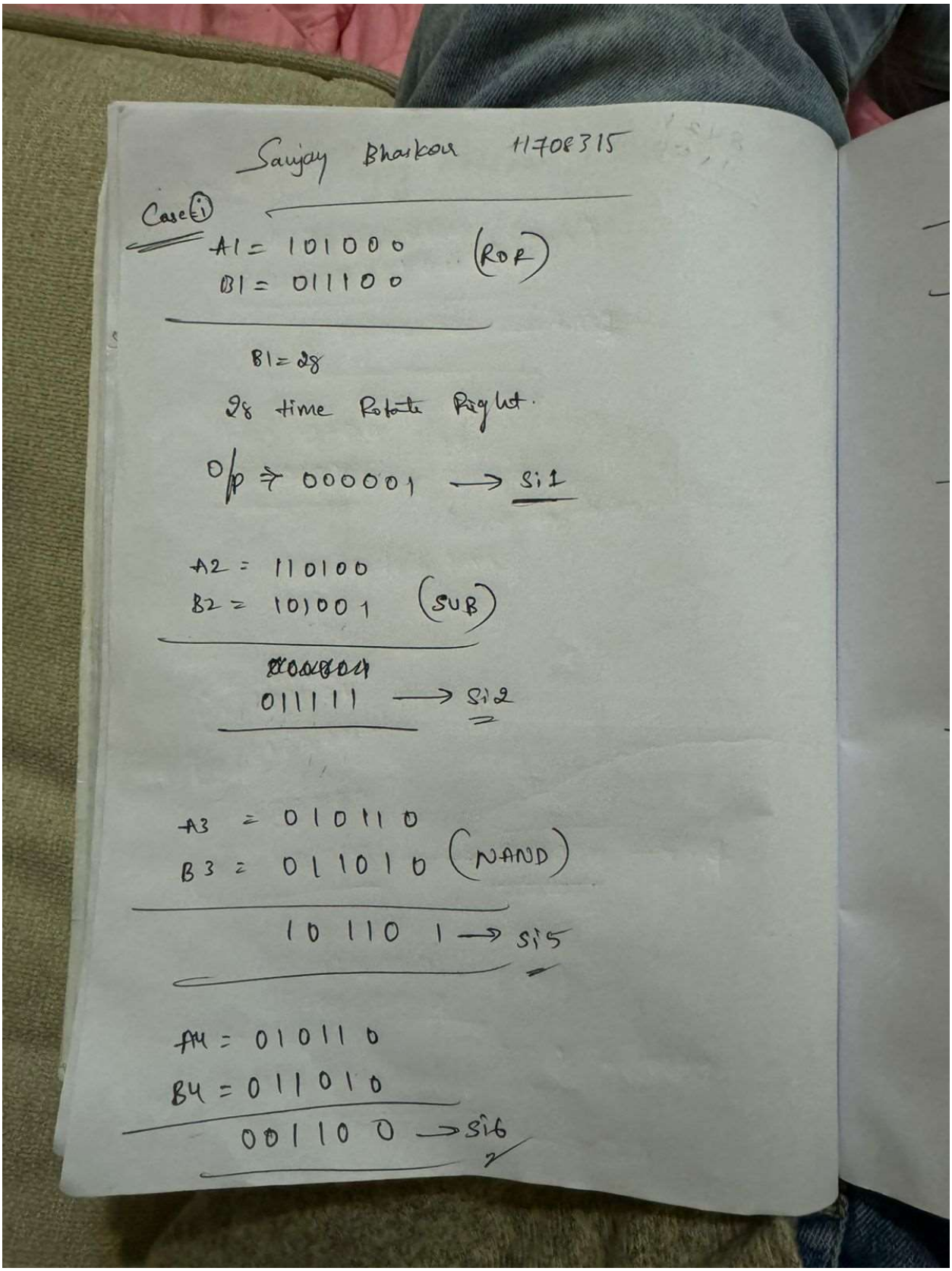
Test Case 2 (*5ns to 10ns*):

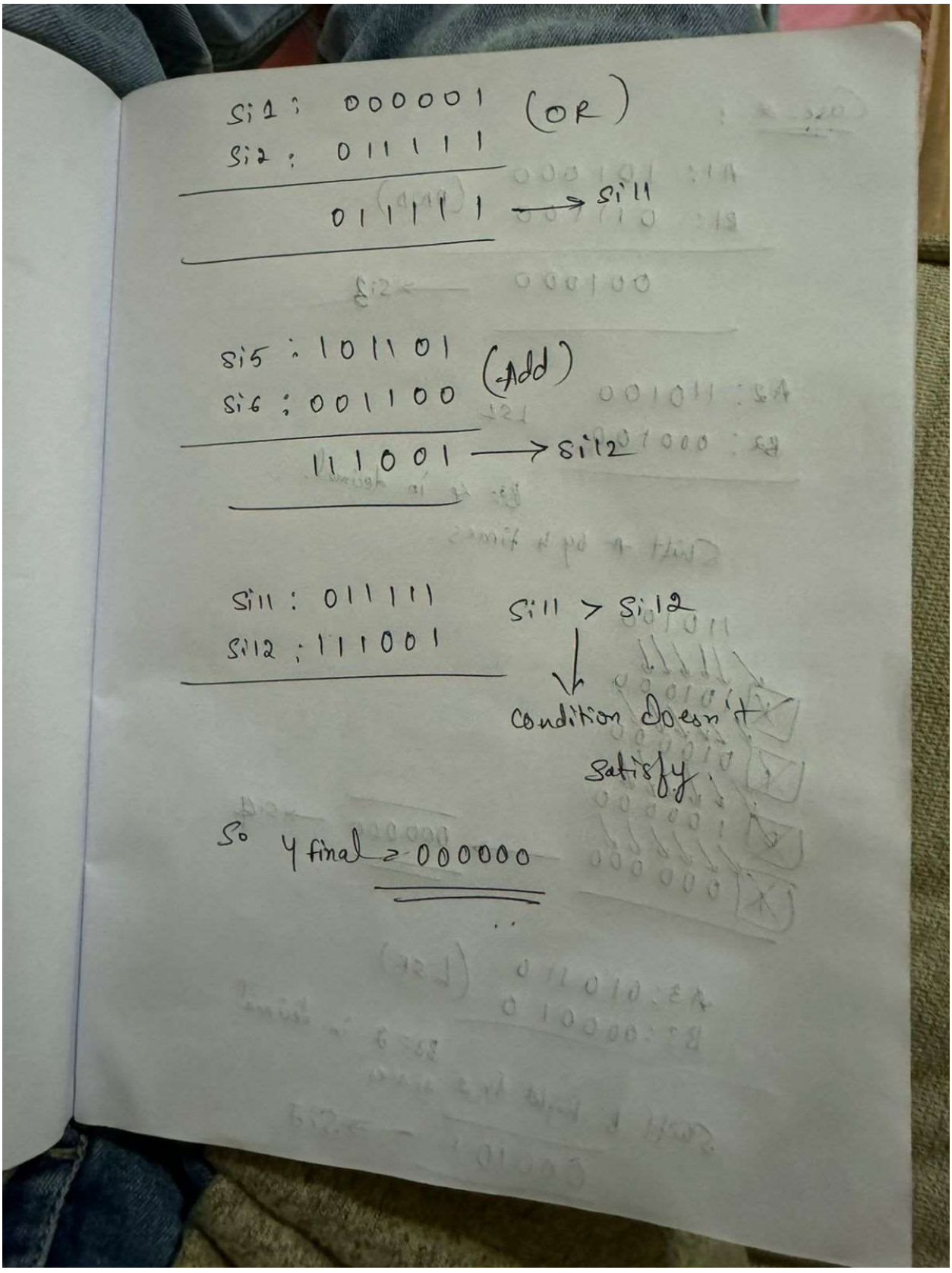
Sl no.	A	B	Oper	Calculated Op	Simulated Op	Match
1	110110	**101001**	AND (00000)	100000	100000	Yes
2	110110	**101001**	OR (00001)	111111	111111	Yes
3	110110	**101001**	NAND(00010)	011111	011111	Yes
4	110110	**101001**	NOR(00011)	000000	000000	Yes
5	110110	**101001**	XOR(00100)	011111	011111	Yes
6	110110	**101001**	XNOR(00101)	100000	100000	Yes
7	110110	**101001**	ADD(00110)	011111	011111	Yes
8	110110	**101001**	SUB(00111)	001101	001101	Yes
9	110110	**101001**	MUL(01000)	001101	001101	Yes
10	110110	**101001**	GT(01001)	000001	000001	Yes
11	110110	**101001**	LT(01010)	000000	000000	Yes
12	110110	**101001**	EQ(01011)	000000	000000	Yes
13	110110	**101001**	GTE(01100)	000100	000100	Yes
14	110110	**101001**	LTE(01101)	000000	000000	Yes
15	110110	**101001**	NEQ(01110)	000110	000110	Yes
16	110110	**101001**	SLA(01111)	000000	000000	Yes
17	110110	**101001**	SRA(10000)	111111	111111	Yes
18	110110	**101001**	ROL(10001)	011011	011011	Yes
19	110110	**101001**	ROR(10010)	101101	101101	Yes
20	110110	**101001**	SLL(10011)	000000	000000	Yes
21	110110	**101001**	SRL(10101)	000000	000000	Yes

References

Referred Files from Canvas.

Manual Calculations.





Si1 : 000001 (OR)
Si2 : 011111

011111 → Si11

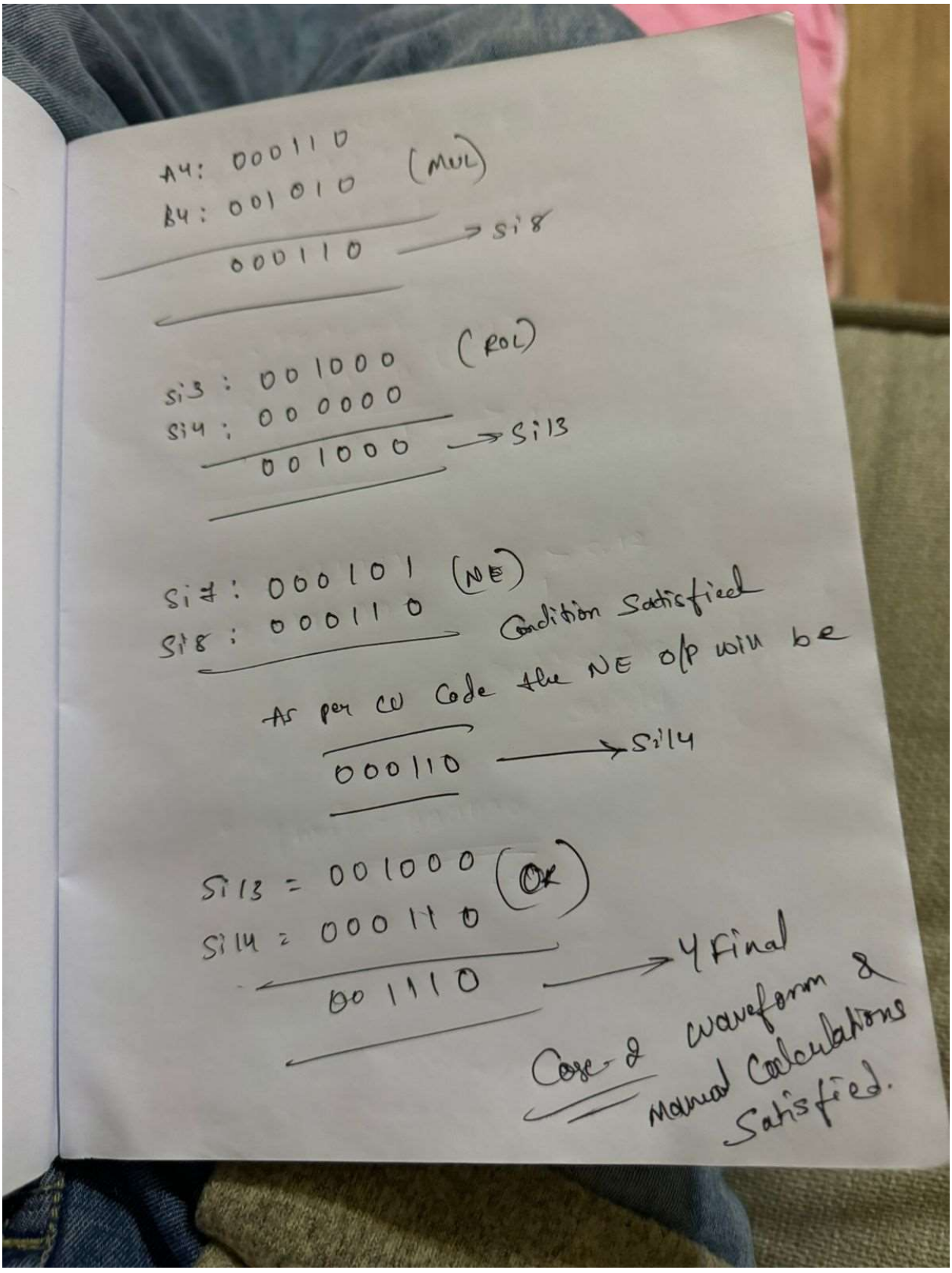
Si5 : 101101 (Add)
Si6 : 001100

111001 → Si12

Si11 : 011111
Si12 : 111001

Si11 > Si12
↓
condition doesn't satisfy.

So Y final = 000000


A4: 000110
B4: 001010 (MUL)
000110 → si8
si3: 001000 (ROL)
si4: 000000
001000 → si3
si7: 000101 (NE)
si8: 000110
Condition Satisfied
As per CW Code the NE o/p will be
000110 → si14
si13 = 001000 (OR)
si14 = 000110
001110 → 4 Final
Core & waveform & Manual Calculations Satisfied.

Case-2 :

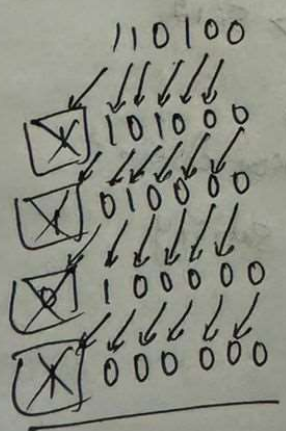
A1: 101000 (AND)
B1: 011100

001000 → Si3

A2: 110100 LSL
B2: 000100

B2 = 4 in decimal.

Shift A by 4 times



000000 → Si4

A3: 010110 (LSR)
B3: 000010

Shift B Right by 2 times

B3 = 2 in decimal

000101 → Si7