HW2_Main code.

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/07/2024 08:31:25 PM
-- Design Name:
-- Module Name: hw_2 - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;


-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity hw_2 is
port (A1,B1,A2,B2,A3,B3,A4,B4:IN std_logic_vector(5 downto 0);
   SEL_1,SEL_2,SEL_3,SEL_4,SEL_5,SEL_6,SEL_7,SEL_8,SEL_9,SEL_10,SEL_11,SEL_12:IN
std_logic_vector(4 downto 0);

Ms_1,Ms_2,Ms_3,Ms_4,Ms_5,Ms_6,Ms_7,Ms_8,Ms_9,Ms_10,Ms_11,Ms_12,Ms_13,Ms_14,Ms_15,Ms_
16,Ms_17 :IN std_logic_vector(1 downto 0);
   YFINAL:INOUT std_logic_vector(5 downto 0)
   );
end hw_2;

architecture Behavioral of hw_2 is
signal S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12 :std_logic_vector(5 downto 0);
signal Si1,Si2,Si3,Si4,Si5,Si6,Si7,Si8,Si9,Si10,Si11,Si12,Si13,Si14,Si15,Si16 : std_logic_vector(5 downto 0);
begin

MOD1:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>A1,B=>B1,SEL=>SEL_1,E=>S1);
MOD2:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>A2,B=>B2,SEL=>SEL_2,E=>S2);
MOD3:ENTITY WORK.cu(BEHAVIORAL)
```

```
PORT MAP(A=>A3,B=>B3,SEL=>SEL_3,E=>S3);
MOD4:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>A4,B=>B4,SEL=>SEL_4,E=>S4);

MUX1:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_1,YM=>Si1);
MUX2:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_2,YM=>Si2);
MUX3:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_3,YM=>Si3);
MUX4:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_4,YM=>Si4);
MUX5:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_5,YM=>Si5);
MUX6:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_6,YM=>Si6);
MUX7:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_7,YM=>Si7);
MUX8:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S1,M=>S2,N=>S3,O=>S4,Ms=>Ms_8,YM=>Si8);

MOD5:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si1,B=>Si2,SEL=>SEL_5,E=>S5);
MOD6:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si3,B=>Si4,SEL=>SEL_6,E=>S6);
MOD7:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si5,B=>Si6,SEL=>SEL_7,E=>S7);
MOD8:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si7,B=>Si8,SEL=>SEL_8,E=>S8);
```

```
MUX9:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_9,YM=>Si9);
MUX10:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_10,YM=>Si10);
MUX11:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_11,YM=>Si11);
MUX12:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_12,YM=>Si12);
MUX13:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_13,YM=>Si13);
MUX14:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_14,YM=>Si14);
MUX15:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_15,YM=>Si15);
MUX16:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S5,M=>S6,N=>S7,O=>S8,Ms=>Ms_16,YM=>Si16);

MOD9:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si9,B=>Si10,SEL=>SEL_9,E=>S9);
MOD10:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si11,B=>Si12,SEL=>SEL_10,E=>S10);
MOD11:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si13,B=>Si14,SEL=>SEL_11,E=>S11);
MOD12:ENTITY WORK.cu(BEHAVIORAL)
PORT MAP(A=>Si15,B=>Si16,SEL=>SEL_12,E=>S12);

MUX17:ENTITY WORK.mux(BEHAVIORAL)
PORT MAP(L=>S9,M=>S10,N=>S11,O=>S12,Ms=>Ms_17,YM=>YFINAL);
```

end Behavioral;

HW_2_Testbench

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/08/2024 12:40:19 PM
-- Design Name:
-- Module Name: hw2_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
```

```
use ieee.numeric_std.all;

use STD.ENV.FINISH;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC_STD.ALL;


-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;


entity hw2_tb is

--  Port ( );

end hw2_tb;


architecture Behavioral of hw2_tb is

signal A1,B1,A2,B2,A3,B3,A4,B4 :std_logic_vector(5 downto 0);

signal SEL_1,SEL_2,SEL_3,SEL_4,SEL_5,SEL_6,SEL_7,SEL_8,SEL_9,SEL_10,SEL_11,SEL_12:
std_logic_vector(4 downto 0);

signal
Ms_1,Ms_2,Ms_3,Ms_4,Ms_5,Ms_6,Ms_7,Ms_8,Ms_9,Ms_10,Ms_11,Ms_12,Ms_13,Ms_14,Ms_15,Ms_
16,Ms_17 : std_logic_vector(1 downto 0);

signal YFINAL: std_logic_vector(5 downto 0);



begin

instance : entity work.hw_2 (Behavioral)

port
```

```
map(A1=>A1,B1=>B1,A2=>A2,B2=>B2,A3=>A3,B3=>B3,A4=>A4,B4=>B4,SEL_1=>SEL_1,SEL_2=>SEL_2,SEL
_3=>SEL_3,SEL_4=>SEL_4,SEL_5=>SEL_5,SEL_6=>SEL_6,SEL_7=>SEL_7,SEL_8=>SEL_8,SEL_9=>SEL_9,SEL_
10=>SEL_10,SEL_11=>SEL_11,SEL_12=>SEL_12,Ms_1=>Ms_1,Ms_2=>Ms_2,Ms_3=>Ms_3,Ms_4=>Ms_4,
Ms_5=>Ms_5,Ms_6=>Ms_6,Ms_7=>Ms_7,Ms_8=>Ms_8,Ms_9=>Ms_9,Ms_10=>Ms_10,Ms_11=>Ms_11,
Ms_12=>Ms_12,Ms_13=>Ms_13,Ms_14=>Ms_14,Ms_15=>Ms_15,Ms_16=>Ms_16,Ms_17=>Ms_17,YFIN
AL=>YFINAL);

process

begin

---- case 1

--A1<="101000"; B1<="011100"; A2<="110100"; B2<="101001"; A3<="010110"; B3<="011010";
A4<="010110"; B4<="011010";

--SEL_1<="10010"; SEL_2<="00111"; SEL_3<="00010"; SEL_4<="00100";

--Ms_1<="00"; Ms_2<="01"; Ms_5<="10"; Ms_6<="11";

--SEL_5<="00001"; SEL_7<="00110";

--Ms_11<="00";Ms_12<="10";

--SEL_10<="01001";

--Ms_17<="01"; wait for 100ns;


 --case 2

A1<="101000"; B1<="011100"; A2<="110100"; B2<="000100"; A3<="010110"; B3<="000010";
A4<="000110"; B4<="001010";

SEL_1<="00000"; SEL_2<="10011"; SEL_3<="10100"; SEL_4<="01000";

Ms_3<="00"; Ms_4<="01"; Ms_7<="10"; Ms_8<="11";

SEL_6<="10001"; SEL_8<="01110";

Ms_13<="01";Ms_14<="11";

SEL_11<="00001";

Ms_17<="10"; wait for 100ns;

wait;

end process;


end Behavioral;
```

CU_Code

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/05/2024 01:25:00 PM
-- Design Name:
-- Module Name: cu - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;
--USE IEEE.std_logic_unsigned.ALL;
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if using
```

```
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity cu is
--generic (
    --constant R: natural := 1  -- number of shited or rotated bits
 --  );

 port (
 A: in std_logic_vector(5 downto 0);
 B : in std_logic_vector(5 downto 0);
 SEL : in std_logic_vector(4 downto 0);
 E : out std_logic_vector(5 downto 0);
 F : inout std_logic_vector(11 downto 0)
 );
end cu;

architecture Behavioral of cu is

begin
cu_proc : process(A,B,SEL)
begin
case SEL is
 When "00000"=> E <= A and B;
```

```
When "00001"=> E <= A or B;
When "00010"=> E <= A nand B;
When "00011"=> E <= A nor B;
When "00100"=> E <= A xor B;
When "00101"=> E <= A xnor B;
When "00110"=> E <= std_logic_vector(unsigned (A) + unsigned (B));
When "00111"=> E <= std_logic_vector(unsigned (A) - unsigned (B));
When "01000"=> F <= std_logic_vector(unsigned (A) * unsigned (B));
E <= F(5 Downto 0);
WHEN "01001" =>
IF (A>B) THEN
E <= "000001";
else
E <= "000000";
end if ;
WHEN "01010" =>
IF (A<B) THEN
E <= "000010";
else
E <= "000000";
end if ;
WHEN "01011" =>
IF (A=B) THEN
E <= "000011";
else
E <= "000000";
end if ;
WHEN "01100" =>
IF (A>=B) THEN
```

```
E <= "000100";
else
E <= "000000";
end if ;
WHEN "01101" =>
IF (A<=B) THEN
E <= "000101";
else
E <= "000000";
end if ;
--15
WHEN "01110" =>
IF (A/=B) THEN
E <= "000110";
else
E <= "000000";
end if ;
--16 arithemetic dhift left
WHEN "01111" => E <= to_stdlogicvector(to_bitvector(A) sla to_integer(unsigned(B)));

--17 arithematic shift right
WHEN "10000" => E <= to_stdlogicvector(to_bitvector(A) sra to_integer(unsigned(B)));

--18
WHEN "10001" => E <= to_stdlogicvector(to_bitvector(A) rol to_integer(unsigned(B)));
--WHEN "10001" => E <= std_logic_vector(unsigned(A) rol R);
--19
WHEN "10010" => E <= to_stdlogicvector(to_bitvector(A) ror to_integer(unsigned(B)));
-- WHEN "10010" => E <= std_logic_vector(unsigned(A) ror R);
```

```
 --WHEN "01111" => E <= std_logic_vector(unsigned(A) sll R);
--if std_logic_vector(unsigned(A) sll B);
 --E <= std_logic_vector(unsigned (A) * unsigned (B));
 --20

 WHEN "10011" => E <= to_stdlogicvector(to_bitvector(A) sll to_integer(unsigned(B)));
 --WHEN "10011" => E <= std_logic_vector(unsigned(A) sll R);
 --21
 WHEN "10100" => E <= to_stdlogicvector(to_bitvector(A) srl to_integer(unsigned(B)));
 --WHEN "10100" => E <= std_logic_vector(unsigned(A) srl R);
 when others =>
 E <="111111";
 end case;
 end process;
end Behavioral;
```

CU_Testbench

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/05/2024 10:53:33 PM
-- Design Name:
-- Module Name: cu_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
```

```
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;
use STD.ENV.FINISH;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity cu_tb is
--  Port ( );
end cu_tb;

architecture Behavioral of cu_tb is
signal A,B :std_logic_vector(5 downto 0);
```

```
signal SEL:std_logic_vector(4 downto 0);
signal E:std_logic_vector(5 downto 0);
begin
instance : entity work.cu (Behavioral)
port
map(A=>A,B=>B,E=>E,SEL=>SEL
);
stimulus:process
begin
A<="111001";B<="110101"; SEL<="00000"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00000"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00001"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00001"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00010"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00010"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00011"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00011"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00100"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00100"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00101"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00101"; wait for 10ns;

A<="111001";B<="110101"; SEL<="00110"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00110"; wait for 10ns;
```

```
A<="111001";B<="110101"; SEL<="00111"; wait for 10ns;
A<="110110";B<="101001"; SEL<="00111"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01000"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01000"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01001"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01001"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01010"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01010"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01011"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01011"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01100"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01100"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01101"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01101"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01110"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01110"; wait for 10ns;

A<="111001";B<="110101"; SEL<="01111"; wait for 10ns;
A<="110110";B<="101001"; SEL<="01111"; wait for 10ns;

A<="111001";B<="110101"; SEL<="10000"; wait for 10ns;
```

```
A<="110110";B<="101001"; SEL<="10000"; wait for 10ns;

A<="111001";B<="110101"; SEL<="10001"; wait for 10ns;
A<="110110";B<="101001"; SEL<="10001"; wait for 10ns;

A<="111001";B<="110101"; SEL<="10010"; wait for 10ns;
A<="110110";B<="101001"; SEL<="10010"; wait for 10ns;

A<="111001";B<="000010"; SEL<="10011"; wait for 10ns;
A<="110110";B<="101001"; SEL<="10011"; wait for 10ns;

A<="111001";B<="110101"; SEL<="10100"; wait for 10ns;
A<="110110";B<="101001"; SEL<="10100"; wait for 10ns;

end process;
end Behavioral;
```

Mux Code.

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/07/2024 09:43:54 PM
-- Design Name:
-- Module Name: mux - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
use ieee.numeric_std.all;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
```

```
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mux is
 Port (
L,M,N,O:IN std_logic_vector(5 DOWNTO 0 );
 Ms:in std_logic_vector(1 downto 0);
 YM:inout std_logic_vector(5 downto 0)
 );
end mux;

architecture Behavioral of mux is

begin
process(L,M,N,O,Ms,YM)
BEGIN
CASE Ms IS
   WHEN "00"=> YM <= L;
   WHEN "01"=> YM <= M;
   WHEN "10"=> YM <= N;
   WHEN "11"=> YM <= O;

   WHEN OTHERS => YM <=(OTHERS=>'Z');
 END CASE;
 END PROCESS;
```

```
end Behavioral;
```

Mux Testbench.

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date: 02/08/2024 12:40:51 PM
-- Design Name:
-- Module Name: mux_tb - Behavioral
-- Project Name:
-- Target Devices:
-- Tool Versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------


library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_SIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;
use STD.ENV.FINISH;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mux_tb is
--  Port ( );
end mux_tb;

architecture Behavioral of mux_tb is
signal L,M,N,O: std_logic_vector(5 DOWNTO 0 );
signal Ms: std_logic_vector(1 downto 0);
signal YM: std_logic_vector(5 downto 0);

begin
instance : entity work.mux (Behavioral)
port
map(L=>L,M=>M,N=>N,O=>O,Ms=>Ms,YM=>YM
);
stimulus:process
```

```
begin
L<="000000"; M<="000001";N<="000010"; O<="000011"; Ms<="00"; wait for 10ns;
L<="000000"; M<="000001";N<="000010"; O<="000011"; Ms<="01"; wait for 10ns;
L<="000000"; M<="000001";N<="000010"; O<="000011"; Ms<="10"; wait for 10ns;
L<="000000"; M<="000001";N<="000010"; O<="000011"; Ms<="11"; wait for 10ns;
finish;
end process stimulus;
end Behavioral;
```