**CDAC Feb 2015**

**LAB 1**

Q3. D latch

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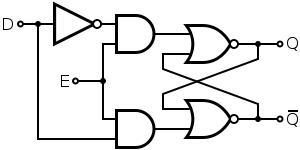
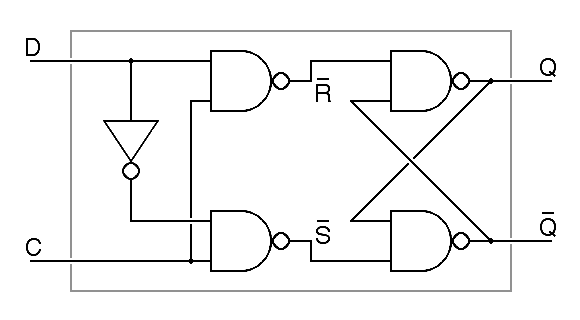
PRN: 150240133004

**D latch**

# Design Approach:

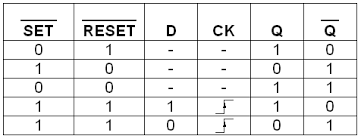
# This D-latch is obtained from SR by connecting both the inputs. This is also known as Toggle latch as output is toggled if T=1. The truth table is show in table 1.

# Circuit Diagram:

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**Fig 1:- Circuit Diagram of D latch**

**Truth Table:**

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**Source Code:**

module dl (nq,q,en,ip);

output nq,q;

input ip,en;

wire t1,t2;

nand n0 (t1,en,ip);

nand n1 (t2,en,~ip);

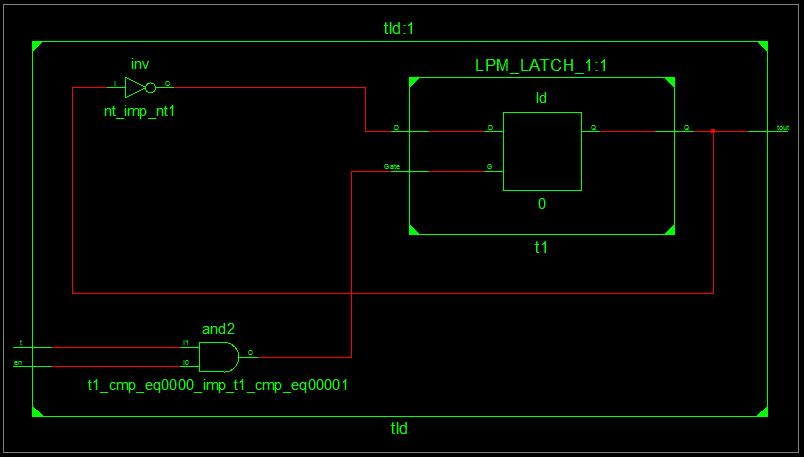
nand n2 (q,t1,nq);

nand n3 (nq,t2,q);

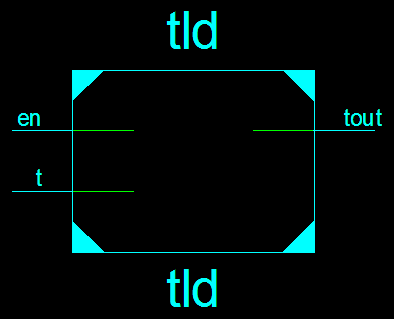
endmodule

**Synthesis:**

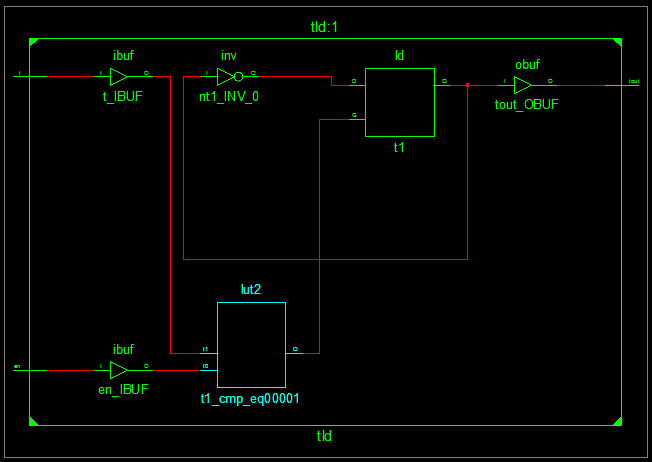
1. RTL Schematic



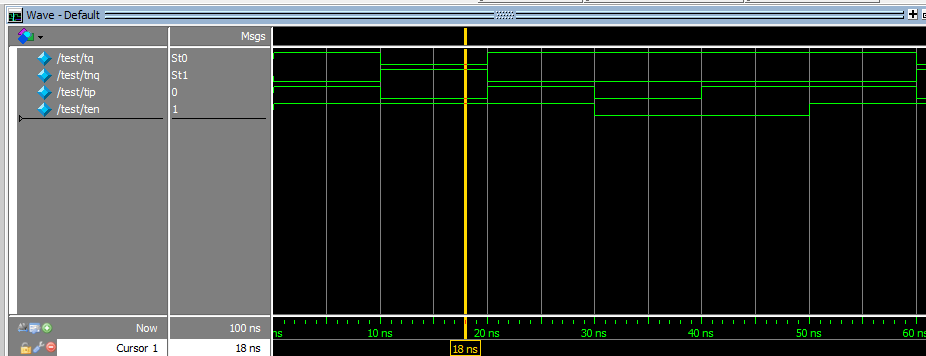
1. Block Diagram

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1. Tech Schematic



1. Simulation Waveform Result

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**Error:**

None.

**Verified by:**

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