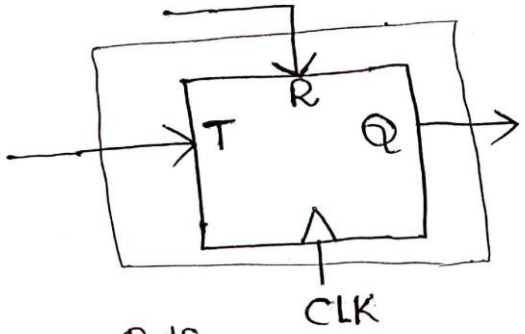
CS210 - Digital Systems Design

Lab 7

Negative Edge-triggered T Flip-Flop with an Asynchronous Reset

- Interface Diagram

INTERFACE Diagram of T-Flip Flop



Ports

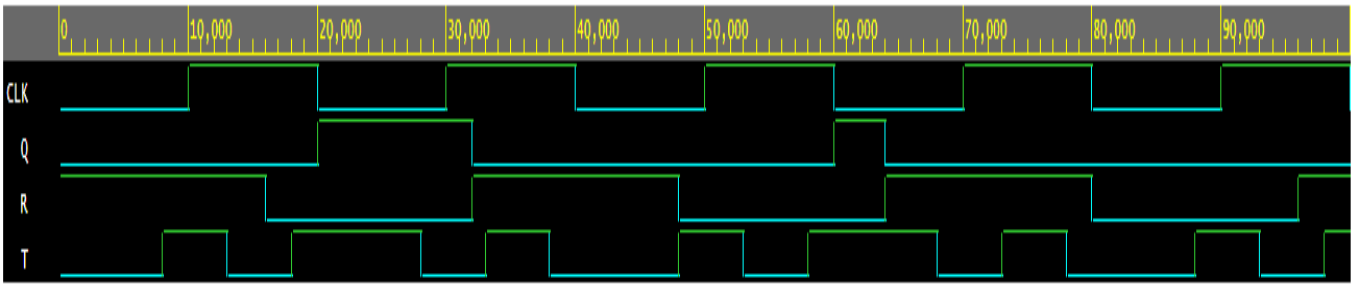
T: Input Data
R: Reset
Q: Output
CLK: clock Input

Functionality

* If R = 1; Irrespective of 'T' value, value of 'Q' = '0'

* If R = 0;
  - and T = 0 ⇒ Q(t+1) = Q(t)
  - and T = 1 ⇒ Q(t+1) = Q'(t)

- Simulation Waveform



- Architecture of TFF

1904119_lab7_Q1.vhdl

```vhdl
-- Importing the required Library and Packages.
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;


-- Creating an entity for Toggle Flip Flop.
entity TFF is
    port(CLK: in std_logic;
        T: in std_logic ;
        R: in std_logic ;
        Q: out std_logic );
end TFF;


-- Defining a Behavioural architecture of Toggle Flip Flop.
architecture Behav of TFF is
begin
    proc: process (CLK,R) is
    begin
    if R= '1' then                          -- Giving Higher Priority to Reset leads to Asynchronous Reset.
        Q <= '0';
    else
        if CLK'event and CLK = '0'  then    -- It is Negative Edge Triggered since we kept CLK = '0'
            if T = '1' then
                Q <= not Q;
            end if;
        end if;
    end if;
    end process proc;
end Behav;
```

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------The End------