- MIPS rate= $f/CPI*10^6$
  $= 40/ 1.55*10^6$
  $=40*10^6/1.55*10^6$
  $= \mathbf{25.8}$

- Given f=40 MHz ➔ $\tau = 1/40$
  $T = Ic * CPI * \tau$
  $= 100000*1.55*1/40$
  $= 100000*1.55*0.025$
  $= 3875$
  $= \mathbf{3.875\ ms}$

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Q2:

3 enhancement with the following speed up are proposed for a new architecture

- $Speedup_1 = 30$
- $Speedup_2 = 20$
- $Speedup_3 = 15$

If enhancement 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speed up of 10 ?

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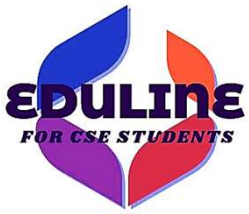
Important Problematic Questions for University Exam



MODULE 1

Q1:

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45.000	1
Data transfer	32.000	2
Floating point	15.000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

Clock speed of the Processor = 40 MHz

Instruction Type	Instruction Count	Cycles per Instruction	cycles
Integer arithmetic	45,000	1	45000
Data transfer	32,000	2	64000
Floating point	15,000	2	30000
Control transfer	8000	2	16000

- Total no: of cycles required to execute complete program
  - ➔ 45000+64000+30000+16000
  - ➔ 155000 cycles

C=155000 cycles

- Effective CPI= C/Ic
  - ➔ 155000/100000

CPI = 1.55

Total cost = $C_1S_1+C_2S_2+C_3S_3$

= $1.25 \times 512 + 0.2 \times 32 \times 10^3 + 39.8 \times 0.0002 \times 10^6$

= 640+6400+7960

= **$15000**

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MODULE 4

Q1:

Consider the execution of a program of **15,000 instructions** by a **linear pipeline** processor with a **clock rate of 25 Mhz**. Assume that the instruction pipeline has **five stages** and that **one instruction is issued per clock cycle**. The penalties due to branch instructions and out-of sequence executions are ignored.

- Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay.
- what are the efficiency and throughput of this pipelined processor?

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Ans:

Information we get are :

- $n = 15,000$ instructions or tasks.
- $f = 25\ MHz$.
- $k = 5$ stages.
- $1-$issued processor.

The Speedup (S_k), Efficiency, (E_k), and Throughput (H_k) factors are :

$$S_k = \frac{T_1}{T_k} = \frac{nk\tau}{k\tau + (n-1)\tau} = \frac{nk}{k+(n-1)} = \frac{(15,000)(5)}{5+(15,000-1)} = \frac{75,000}{15,004} = 4,999$$

$$H_k = \frac{nf}{k+(n-1)} = \frac{(15,000)(25)}{5+(15,000-1)} = \frac{375,000}{15,004} = 24,99\ MIPS$$

$$E_k = \frac{S_k}{k} = \frac{4,999}{5} = 0,999$$

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Q2:

Suppose the time delay of 4 stage are τ_1 = 60ns, τ_2 = 50ns, τ_3 = 90ns, τ_4 = 80ns and the interface latch has a delay of **d**= 10ns. Find the clock period and frequency of this pipeline?

$\tau = \tau_{max} + d = 90 * 10^{-9} + 10 * 10^{-9} = 100 * 10^{-9}$

This means that the clock frequency of the pipeline can be set to

$f = \frac{1}{\tau} = \frac{1}{100 * 10^{-9}} = 10$ MHz

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Q3:

Determine the frequency of the pipeline if the stage delays are τ1 = 3ns, τ2 = τ3=5ns and τ4 =8 ns and the latch delay is 1 ns.

$\tau_{max=}$ 8ns

d = 1ns

$\tau = \tau_{max} + d = 8 * 10^{-9} + 1 * 10^{-9} = 9 * 10^{-9}$

$f = \frac{1}{\tau} = = \frac{1}{9 * 10^{-9}} = 111.11$ MHz

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