

Clock speed of the Processor = 40 MHz

Instruction Type	Instruction Count	Cycles per Instruction	cycles
Integer arithmetic	45,000	1	45000
Data transfer	32,000	2	64000
Floating point	15,000	2	30000
Control transfer	8000	2	16000

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- Total no: of cycles required to execute complete program

$$\rightarrow 45000 + 64000 + 30000 + 16000$$

$$\rightarrow 155000 \text{ cycles}$$

$$C = 155000 \text{ cycles}$$

- Effective CPI = C/I_c

$$\rightarrow 155000 / 100000$$

$$CPI = 1.55$$

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- MIPS rate = $f / \text{CPI} \times 10^6$
 $= 40 / 1.55 \times 10^6$
 $= 40 \times 10^6 / 1.55 \times 10^6$
 $= \mathbf{25.8}$

- Given $f = 40 \text{ MHz} \rightarrow \tau = 1/40$
 $T = I_c \times \text{CPI} \times \tau$
 $= 100000 \times 1.55 \times 1/40$
 $= 100000 \times 1.55 \times 0.025$
 $= 3875$
 $= \mathbf{3.875 \text{ ms}}$

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Q2:

3 enhancement with the following speed up are proposed for a new architecture

- $\text{Speedup}_1 = 30$
- $\text{Speedup}_2 = 20$
- $\text{Speedup}_3 = 15$

If enhancement 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speed up of 10 ?

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Q2:

Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=25 \text{ ns}$	$s_1=512 \text{ Kbytes}$	$c_1=\$1.25$
Main Memory	$t_2=903 \text{ ns}$	$s_2=32 \text{ Mbytes}$	$c_2=\$0.2$
Disk array	$t_3=4 \text{ ms}$	$s_3=39.8 \text{ Gbytes}$	$c_3=\$0.0002$

Hit ratio of cache memory is $h_1=0.98$ and a hit ratio of main memory is $h_2=0.9$.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost.

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Effective access time

$$\begin{aligned}
 T_{eff} &= h_1 t_1 + (1-h_1) h_2 t_2 + (1-h_1)(1-h_2) h_3 t_3 \\
 &= 0.98 * 25 \times 10^{-9} + 0.02 * .9 * 903 \times 10^{-9} + 0.02 * .1 * 1 * 4 \times 10^{-3} \\
 &= 24.5 \times 10^{-9} + 16.254 \times 10^{-9} + .008 \times 10^{-3} \\
 &= 40.754 \times 10^{-9} + .008 \times 10^{-3} \\
 &= 40.754 \times 10^{-9} + 8000 \times 10^{-9} \\
 &= 8040.754 \times 10^{-9} \\
 &= \mathbf{8.04 \mu sec.}
 \end{aligned}$$

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Q3:

Determine the frequency of the pipeline if the stage delays are $\tau_1 = 3\text{ns}$, $\tau_2 = \tau_3 = 5\text{ns}$ and $\tau_4 = 8\text{ns}$ and the latch delay is 1ns .

$$\tau_{\max} = 8\text{ns}$$

$$d = 1\text{ns}$$

$$\tau = \tau_{\max} + d = 8 \times 10^{-9} + 1 \times 10^{-9} = 9 \times 10^{-9}$$

$$f = \frac{1}{\tau} = \frac{1}{9 \times 10^{-9}} = 111.11\text{ MHz}$$