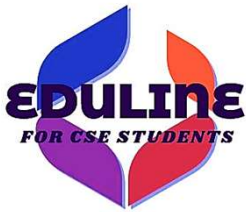


Important Problematic Questions for University Exam



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MODULE 1

Q1:

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45.000	1
Data transfer	32.000	2
Floating point	15.000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

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Clock speed of the Processor = 40 MHz

Instruction Type	Instruction Count	Cycles per Instruction	cycles
Integer arithmetic	45,000	1	45000
Data transfer	32,000	2	64000
Floating point	15,000	2	30000
Control transfer	8000	2	16000

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- Total no: of cycles required to execute complete program

$$\rightarrow 45000 + 64000 + 30000 + 16000$$

$$\rightarrow 155000 \text{ cycles}$$

$$C = 155000 \text{ cycles}$$

- Effective CPI = C/I_c

$$\rightarrow 155000 / 100000$$

$$CPI = 1.55$$

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- MIPS rate = $f / \text{CPI} \times 10^6$
 $= 40 / 1.55 \times 10^6$
 $= 40 \times 10^6 / 1.55 \times 10^6$
 $= \mathbf{25.8}$

- Given $f = 40 \text{ MHz} \rightarrow \tau = 1/40$
 $T = I_c \times \text{CPI} \times \tau$
 $= 100000 \times 1.55 \times 1/40$
 $= 100000 \times 1.55 \times 0.025$
 $= 3875$
 $= \mathbf{3.875 \text{ ms}}$

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Q2:

3 enhancement with the following speed up are proposed for a new architecture

- $\text{Speedup}_1 = 30$
- $\text{Speedup}_2 = 20$
- $\text{Speedup}_3 = 15$

If enhancement 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speed up of 10 ?

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Ans:

$$\begin{aligned}
 \text{Speedup}_{\text{overall}} &= \left[\frac{1}{(1 - \text{Fraction}_{\text{enhanced}}) + \frac{\text{Fraction}_{\text{enhanced}}}{\text{Speedup}_{\text{enhanced}}}} \right] \\
 &= \left\{ (1 - (FE_1 + FE_2 + FE_3)) + \left[\frac{FE_1}{SE_1} + \frac{FE_2}{SE_2} + \frac{FE_3}{SE_3} \right] \right\}^{-1} \\
 10 &= \left\{ (1 - (0.25 + 0.25 + FE_3)) + \left[\frac{0.25}{30} + \frac{0.25}{20} + \frac{FE_3}{15} \right] \right\}^{-1} \\
 10 &= \left\{ (0.5 - FE_3) + \left[\frac{0.5 + 0.75 + FE_3}{60} \right] \right\}^{-1} \\
 10 &= \frac{60}{30 - 60FE_3 + 1.25 + 4FE_3} \\
 -56FE_3 &= 6 - 31.25 \\
 FE_3 &= -25.25 / -56 = \underline{\underline{0.45}}
 \end{aligned}$$

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MODULE 2

Q: Consider the design of a 3 level memory hierarchy with following features

Memory level	Access time	Capacity	Cost/kbyte
Cache	t1= 25 ns	s1= 512 Kbytes	c1= \$1.25
Main memory	t2= unknown	s2= 32 Mbytes	c2= \$.2
Disk array	t3= 4 ms	s3= unknown	c3= \$0.0002

- Aim is to achieve effective memory access time $T_{\text{eff}}=850 \text{ ns}$

Cache hit ratio $h_1=0.98$

Main memory Hit ratio $h_2=0.99$

Disk array hit ratio $h_3=1$

Total cost is upper bounded by \$15000

Calculate the unknown specifications based on the given conditions ?

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$$\begin{aligned}
 \bullet C_{\text{total}} &= c_1 s_1 + c_2 s_2 + c_3 s_3 \leq 15000 \\
 15000 &= 1.25 \times 512 + .2 \times 32000 + .0002 * s_3 \\
 15000 &= 640 + 6400 + .0002 * s_3 \\
 .0002 * s_3 &= 15000 - 640 - 6400 \\
 &= 7960 / .0002 \\
 &= 39800000 \times 10^{-6} \\
 s_3 &= 39.8
 \end{aligned}$$

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$$\begin{aligned}
 T_{\text{eff}} &= h_1 t_1 + (1 - h_1) h_2 t_2 + (1 - h_1)(1 - h_2) h_3 t_3 \\
 T_{\text{eff}} &= h_1 t_1 + (1 - h_1) h_2 t_2 + (1 - h_1)(1 - h_2) h_3 t_3 \leq 850 \text{ ns} \\
 850 \times 10^{-9} &= .98 \times 25 \times 10^{-9} + .02 * .99 * t_2 + .02 * .01 * 1 * 4 * 10^{-3} \\
 850 \times 10^{-9} &= 24.5 \times 10^{-9} + .0198 t_2 + .0008 \times 10^{-3} \\
 .0198 t_2 &= 850 \times 10^{-9} - 24.5 \times 10^{-9} - .0008 \times 10^{-3} \\
 &= 825.5 \times 10^{-9} - .0008 \times 10^{-3} \\
 &= 825.5 \times 10^{-9} - 800 \times 10^{-9} \\
 &= 25.5 \times 10^{-9} \\
 &= 25.5 \times 10^{-9} / .0198 \\
 t_2 &= 1287 \times 10^{-9}
 \end{aligned}$$

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Q2:

Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	$t_1=25 \text{ ns}$	$s_1=512 \text{ Kbytes}$	$c_1=\$1.25$
Main Memory	$t_2=903 \text{ ns}$	$s_2=32 \text{ Mbytes}$	$c_2=\$0.2$
Disk array	$t_3=4 \text{ ms}$	$s_3=39.8 \text{ Gbytes}$	$c_3=\$0.0002$

Hit ratio of cache memory is $h_1=0.98$ and a hit ratio of main memory is $h_2=0.9$.

- (i) Calculate the effective access time.
- (ii) Calculate the total memory cost.

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Effective access time

$$\begin{aligned}
 T_{eff} &= h_1 t_1 + (1-h_1) h_2 t_2 + (1-h_1)(1-h_2) h_3 t_3 \\
 &= 0.98 * 25 \times 10^{-9} + 0.02 * .9 * 903 \times 10^{-9} + 0.02 * .1 * 1 * 4 \times 10^{-3} \\
 &= 24.5 \times 10^{-9} + 16.254 \times 10^{-9} + .008 \times 10^{-3} \\
 &= 40.754 \times 10^{-9} + .008 \times 10^{-3} \\
 &= 40.754 \times 10^{-9} + 8000 \times 10^{-9} \\
 &= 8040.754 \times 10^{-9} \\
 &= \mathbf{8.04 \mu sec.}
 \end{aligned}$$

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$$\begin{aligned}\text{Total cost} &= C_1S_1 + C_2S_2 + C_3S_3 \\ &= 1.25 \times 512 + 0.2 \times 32 \times 10^3 + 39.8 \times 0.0002 \times 10^6 \\ &= 640 + 6400 + 7960 \\ &= \text{\$15000}\end{aligned}$$

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MODULE 4

Q1:

Consider the execution of a program of **15,000 instructions** by a **linear pipeline** processor with a **clock rate of 25 Mhz**. Assume that the instruction pipeline has **five stages** and that **one instruction is issued per clock cycle**. The penalties due to branch instructions and out-of sequence executions are ignored.

- Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay.
- what are the efficiency and throughput of this pipelined processor?

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Ans:

Information we get are :

- ☞ $n = 15,000$ instructions or tasks.
- ☞ $f = 25 \text{ MHz}$.
- ☞ $k = 5$ stages.
- ☞ 1-issued processor.

The Speedup (S_k), Efficiency, (E_k), and Throughput (H_k) factors are :

$$\begin{aligned}
 S_k &= \frac{T_1}{T_k} = \frac{nk\tau}{k\tau + (n-1)\tau} & H_k &= \frac{nf}{k + (n-1)} & E_k &= \frac{S_k}{k} \\
 &= \frac{nk}{k + (n-1)} & &= \frac{(15,000)(25)}{5 + (15,000-1)} & &= \frac{4,999}{5} \\
 &= \frac{(15,000)(5)}{5 + (15,000-1)} & &= \frac{375,000}{15,004} & &= 0,999 \\
 &= \frac{75,000}{15,004} & &= 24,99 \text{ MIPS} & & \\
 &= 4,999 & & & &
 \end{aligned}$$

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Q2:

Suppose the time delay of 4 stage are $\tau_1 = 60\text{ns}$, $\tau_2 = 50\text{ns}$, $\tau_3 = 90\text{ns}$, $\tau_4 = 80\text{ns}$ and the interface latch has a delay of $d = 10\text{ns}$. Find the clock period and frequency of this pipeline?

$$\tau = \tau_{\max} + d = 90 \times 10^{-9} + 10 \times 10^{-9} = 100 \times 10^{-9}$$

This means that the clock frequency of the pipeline can be set to

$$f = \frac{1}{\tau} = \frac{1}{100 \times 10^{-9}} = 10 \text{ MHz}$$

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Q3:

Determine the frequency of the pipeline if the stage delays are $\tau_1 = 3\text{ns}$, $\tau_2 = \tau_3 = 5\text{ns}$ and $\tau_4 = 8\text{ns}$ and the latch delay is 1ns .

$$\tau_{\max} = 8\text{ns}$$

$$d = 1\text{ns}$$

$$\tau = \tau_{\max} + d = 8 \times 10^{-9} + 1 \times 10^{-9} = 9 \times 10^{-9}$$

$$f = \frac{1}{\tau} = \frac{1}{9 \times 10^{-9}} = 111.11\text{ MHz}$$