Clock speed of the Processor = 40 MHz

| Instruction Type | Instruction Count | Cycles per Instruction | cycles |
|---|---|---|---|
| Integer arithmetic | 45,000 | 1 | 45000 |
| Data transfer | 32,000 | 2 | 64000 |
| Floating point | 15,000 | 2 | 30000 |
| Control transfer | 8000 | 2 | 16000 |

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• Total no: of cycles required to execute complete program

➔ 45000+64000+30000+16000

➔ 155000 cycles

**C=155000 cycles**

• Effective CPI= C/Ic

➔ 155000/100000

**CPI = 1.55**

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# Important Problematic Questions for University Exam

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## MODULE 1

**Q1:**

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

| Instruction Type | Instruction Count | Cycles per Instruction |
|---|---|---|
| Integer arithmetic | 45.000 | 1 |
| Data transfer | 32.000 | 2 |
| Floating point | 15.000 | 2 |
| Control transfer | 8000 | 2 |

Determine the effective CPI, MIPS rate, and execution time for this program.

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**Ans:**

$$\text{Speed up}_{\text{overall}} = \left[ \cfrac{1}{\left(1 - \text{Fraction}_{\text{enhanced}}\right) + \cfrac{\text{Fraction}_{\text{enhanced}}}{\text{Speed up}_{\text{enhanced}}}} \right]$$

$$= \left\{ \left(1 - (FE_1 + FE_2 + FE_3)\right) + \left[ \frac{FE_1}{SE_1} + \frac{FE_2}{SE_2} + \frac{FE_3}{SE_3} \right] \right\}^{-1}$$

$$10 = \left\{ \left(1 - (0.25 + 0.25 + FE_3)\right) + \left[ \frac{0.25}{30} + \frac{0.25}{20} + \frac{FE_3}{15} \right] \right\}^{-1}$$

$$10 = \left\{ (0.5 - FE_3) + \left[ \frac{0.5 + 0.75 + 4 FE_3}{60} \right] \right\}^{-1}$$

$$10 = \frac{60}{30 - 60 FE_3 + 1.25 + 4 FE_3}$$

$$-56 FE_3 = 6 - 31.25$$

$$FE_3 = -25.25 / -56 = \underline{0.45}$$

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# MODULE 2

**Q:** Consider the design of a 3 level memory hierarchy with following features

| Memory level | Access time | Capacity | Cost/kbyte |
|---|---|---|---|
| Cache | t1= 25 ns | s1= 512 Kbytes | c1= $1.25 |
| Main memory | t2= **unknown** | s2= 32 Mbytes | c2= $.2 |
| Disk array | t3= 4 ms | s3= **unknown** | c3= $0.0002 |

• Aim is to achieve effective memory access time Teff=850 ns

　　Cache hit ratio $h_1$ =0.98

　　Main memory Hit ratio $h_2$ =0.99

　　Disk array hit ratio $h_3$ =1

　　Total cost is upper bounded by$15000

Calculate the unknown specifications based on the given conditions ?

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**Q3:**

Determine the frequency of the pipeline if the stage delays are τ1 = 3ns, τ2 = τ3=5ns and τ4 =8 ns and the latch delay is 1 ns.

$\tau_{max}$= 8ns

d = 1ns

τ= $\tau_{max}$ + d = 8* $10^{-9}$+1*$10^{-9}$ = 9* $10^{-9}$

f = $\frac{1}{\tau}$ = = $\frac{1}{9*10^{-9}}$ = 111.11 MHz

- $C_{total} = c_1 s_1 + c_2 s_2 + c_3 s_3 <= 15000$

    $15000 = 1.25*512 + .2*32000 + .0002*s3$

    $15000 = 640 + 6400 + .0002*s3$

    $.0002*s3 = 15000 - 640 - 6400$

    $= 7960/.0002$

    $= 39800000 \times 10^{-6}$

    s3 = **39.8**

$T_{eff} = h_1 t_1 + (1 - h_1) h_2 t_2 + (1 - h_1)(1 - h_2) h_3 t_3$

$T_{eff} = h1 \, t_1 + (1 - h_1) h_2 t_2 + (1 - h_1)(1 - h_2) h_3 t_3 <= 850 \text{ ns}$

    $850 \times 10^{-9} = .98*25 \times 10^{-9} + .02*.99*t_2 + .02*.01*1*4 \times 10^{-3}$

    $850 \times 10^{-9} = 24.5 \times 10^{-9} + .0198 t2 + .0008 \times 10^{-3}$

    $.0198 t2 = 850 \times 10^{-9} - 24.5 \times 10^{-9} - .0008 \times 10^{-3}$

    $= 825.5 \times 10^{-9} - .0008 \times 10^{-3}$

    $= 825.5 \times 10^{-9} - 800 \times 10^{-9}$

    $= 25.5 \times 10^{-9}$

    $= 25.5 \times 10^{-9}/.0198$

    $t_2$ = **1287 x $10^{-9}$**

**Total cost** = $c_1s_1 + c_2s_2 + c_3s_3$

$$= 1.25 \times 512 + 0.2 \times 32 \times 10^3 + 39.8 \times 0.0002 \times 10^6$$

$$= 640 + 6400 + 7960$$

$$= \ \$15000$$

# MODULE 4

**Q1:**

Consider the execution of a program of **15,000 instructions** by a **linear pipeline** processor with a **clock rate of 25 Mhz**. Assume that the instruction pipeline has **five stages** and that **one instruction is issued per clock cycle**. The penalties due to branch instructions and out-of sequence executions are ignored.

• Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay.

• what are the efficiency and throughput of this pipelined processor?

**Q2:**

Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

| Memory level | Access time | Capacity | Cost/Kbyte |
|---|---|---|---|
| Cache | t1=25 ns | s1=512 Kbytes | c1=$1.25 |
| Main Memory | t2=903 ns | s2=32 Mbytes | c2=$0.2 |
| Disk array | t3=4 ms | s3 =39.8 Gbytes | c3=$0.0002 |

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

(i) Calculate the effective access time.

(ii) Calculate the total memory cost.

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**Effective access time**

$T_{eff}$=h1t1+(1-h1)h2t2+(1-h1)(1-h2)h3t3

=0.98*25x10$^{-9}$+.02*.9*903x10$^{-9}$+.02*.1*1*4x10$^{-3}$

=24.5x10$^{-9}$+16.254x10$^{-9}$+.008x10$^{-3}$

=40.754 x10$^{-9}$ + .008x10$^{-3}$

=40.754x10$^{-9}$ +8000x10$^{-9}$

= 8040.754x10$^{-9}$

= **8.04 μsec.**

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