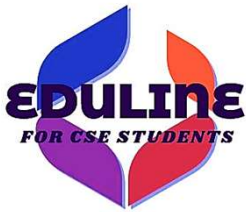# Important Problematic Questions for University Exam

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MODULE 1

Q1:

A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45.000	1
Data transfer	32.000	2
Floating point	15.000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program.

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- C_{total} = $c_1\,s_1$ + $c_2\,s_2$ + $c_3\,s_3$ <=15000

  15000 = 1.25*512 + .2*32000 + .0002*s3

  15000 = 640 + 6400 + .0002*s3

  .0002*s3 = 15000 - 640 - 6400

  = 7960/.0002

  = 39800000x 10^{-6}

  s3 = 39.8

T_{eff} = $h_1 t_1$ + (1- h_1) $h_2 t_2$ + (1- h_1)(1- h_2) $h_3\,t_3$

T_{eff} = h1 t_1 + (1- h_1) $h_2 t_2$ + (1- h_1)(1- h_2) $h_3\,t_3$ <=850 ns

850x10^{-9} = .98*25x10^{-9} + .02*.99* t_2 + .02*.01*1*4*10^{-3}

850x10^{-9} = 24.5x10^{-9} + .0198t2 + .0008x10^{-3}

.0198t2 = 850x10^{-9} - 24.5x10^{-9} - .0008x10^{-3}

= 825.5x10^{-9} - .0008x10^{-3}

= 825.5x10^{-9} - 800x10^{-9}

= 25.5x10^{-9}

= 25.5x10^{-9}/.0198

t_2 = **1287 x 10^{-9}**

Clock speed of the Processor = 40 MHz

Instruction Type	Instruction Count	Cycles per Instruction	cycles
Integer arithmetic	45,000	1	45000
Data transfer	32,000	2	64000
Floating point	15,000	2	30000
Control transfer	8000	2	16000

- Total no: of cycles required to execute complete program
  - ➜ 45000+64000+30000+16000
  - ➜ 155000 cycles

  C=155000 cycles

- Effective CPI= C/Ic
  - ➜ 155000/100000

  CPI = 1.55

Q2:

Consider the design of a three level memory hierarchy with the following specifications for memory characteristics:

Memory level	Access time	Capacity	Cost/Kbyte
Cache	t1=25 ns	s1=512 Kbytes	c1=$1.25
Main Memory	t2=903 ns	s2=32 Mbytes	c2=$0.2
Disk array	t3=4 ms	s3 =39.8 Gbytes	c3=$0.0002

Hit ratio of cache memory is h1=0.98 and a hit ratio of main memory is h2=0.9.

(i) Calculate the effective access time.

(ii) Calculate the total memory cost.

Effective access time

T_{eff}=h1t1+(1-h1)h2t2+(1-h1)(1-h2)h3t3

=0.98*25x10^{-9}+.02*.9*903x10^{-9}+.02*.1*1*4x10^{-3}

=24.5x10^{-9}+16.254x10^{-9}+.008x10^{-3}

=40.754 x10^{-9} + .008x10^{-3}

=40.754x10^{-9} +8000x10^{-9}

= 8040.754x10^{-9}

= **8.04 µsec.**

Total cost = $c_1s_1 + c_2s_2 + c_3s_3$

$\qquad\qquad = 1.25 \times 512 + 0.2 \times 32 \times 10^3 + 39.8 \times 0.0002 \times 10^6$

$\qquad\qquad = 640 + 6400 + 7960$

$\qquad\qquad =$ **$15000**

MODULE 4

Q1:

Consider the execution of a program of **15,000 instructions** by a **linear pipeline** processor with a **clock rate of 25 Mhz**. Assume that the instruction pipeline has **five stages** and that **one instruction is issued per clock cycle**. The penalties due to branch instructions and out-of sequence executions are ignored.

- Calculate the speedup factor using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow-through delay.

- what are the efficiency and throughput of this pipelined processor?

Ans:

Information we get are :

- ☞ $n = 15,000$ instructions or tasks.
- ☞ $f = 25\ MHz$.
- ☞ $k = 5$ stages.
- ☞ $1-$issued processor.

The Speedup (S_k), Efficiency, (E_k), and Throughput (H_k) factors are :

$$S_k = \frac{T_1}{T_k} = \frac{nk\tau}{k\tau + (n-1)\tau}$$
$$= \frac{nk}{k + (n-1)}$$
$$= \frac{(15,000)(5)}{5 + (15,000-1)}$$
$$= \frac{75,000}{15,004}$$
$$= 4,999$$

$$H_k = \frac{nf}{k + (n-1)}$$
$$= \frac{(15,000)(25)}{5 + (15,000-1)}$$
$$= \frac{375,000}{15,004}$$
$$= 24,99\ MIPS$$

$$E_k = \frac{S_k}{k}$$
$$= \frac{4,999}{5}$$
$$= 0,999$$

Q2:

Suppose the time delay of 4 stage are τ_1 = 60ns, τ_2 = 50ns, τ_3 = 90ns, τ_4 = 80ns and the interface latch has a delay of **d**= 10ns. Find the clock period and frequency of this pipeline?

$$\tau = \tau_{max} + d = 90 * 10^{-9} + 10 * 10^{-9} = 100 * 10^{-9}$$

This means that the clock frequency of the pipeline can be set to

$$f = \frac{1}{\tau} = \frac{1}{100 * 10^{-9}} = 10\ MHz$$

Q3:

Determine the frequency of the pipeline if the stage delays are τ1 = 3ns, τ2 = τ3=5ns and τ4 =8 ns and the latch delay is 1 ns.

$\tau_{max}=$ 8ns

d = 1ns

$\tau = \tau_{max} + d = 8*10^{-9}+1*10^{-9} = 9*10^{-9}$

$f = \dfrac{1}{\tau} = = \dfrac{1}{9*10^{-9}} = 111.11$ MHz

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