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Design and Implementation of Verilog Traffic Light Switching System for T-Intersection on FPGA

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***Abstract*— Traffic light switching in junction is crucial for managing traffic and ensuring road safety. They heavily rely on digital electronics and Verilog which is a hardware description language used for designing circuits and systems, including T-Intersection traffic control system. This paper presents an overview of Verilog implementation for the traffic control system and designing the system using finite state machine. The Verilog code is synthesized and simulated using a design compiler and hardware description language simulator. This implementation demonstrates power and efficiency in designing traffic control system, allowing for easy simulation and optimization for performance and reliability. In conclusion, Verilog language plays a major role for developing intelligent transportation systems, as highlighted in this paper.**

***Keywords*— FSM, Verilog HDL, T-Intersection, Combinational Logic Circuit,PCB, Microprocessor.**

I. INTRODUCTION

Traffic management is crucial for urban safety and congestion reduction. By controlling the movement of both vehicles and pedestrians, traffic control systems are essential to achieving this objective. System design, installation, programming, and maintenance are all steps in the process, and they all take equipment selection and traffic pattern analysis into account. Such well-designed systems help make transportation networks safer and more effective, which is advantageous to communities. In many places around the world, however, traffic congestion continues to be a major problem that results in delays, annoyance, and financial hardships. Due to delays in supplies and trade, businesses have decreased production, missed opportunities, and increased expenditures. Congestion control is crucial for enhancing urban life and boosting the local economy [1],[4],[7].

Traffic lights employ three colors: Red, instructing vehicles to stop, Green for movement, and Yellow as a preparation signal. This precise control minimizes idle time and congestion. Traffic light controllers (TLC) utilize micro-controllers, FPGAs, or ASICs for implementation. FPGAs offer advantages such as speed, numerous I/O ports, and high performance, vital in TLC design. ASICs, though powerful, tend to be costlier. The choice depends on system requirements and budget constraints [3].

In this paper, we present the design and implementation of a Verilog Traffic Light Switching system for a T-Intersection on FPGA, offering an innovative and efficient solution for managing traffic flow at such intersections.

II. OBJECTIVES

- The primary objective of a traffic light controller is to regulate the movement of vehicles at intersection or along a roadway.
- The design can be optimized for delay and less power consumption.
- The area and complexity of the traffic light controller system can be reduced by implementing it on the FPGA Kit.

III. METHODOLOGY

The provided Fig. 1. illustrates the movement of vehicles in all directions using specified RYG LED lights.

The primary objective of this project is to design and implement a Traffic Light Switching System for a T-intersection using Verilog and then load it onto an FPGA Kit to test its functionality.

Here are the key aspects of the project:

- M1: This signifies the direction of vehicle movement exclusively on the main road.
- MT: This indicates the direction of vehicles moving from the main road towards the side road.
- M2: This represents the direction of vehicles simultaneously moving on both the main road and side road.
- S: This signifies the direction of vehicles moving from the side road towards the main road.

The time delays for transitioning from one state to another are as follows:

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- TMG: This denotes the transition from the main road to Green light, allowing vehicles to move on the main road.
- TY: This represents the transition to Yellow, signaling vehicles to slow down in preparation for the next state.
- TTG: This signifies the transition for both the main road and side road to Green, enabling vehicles to move from the main road to the side road.
- TSG: This indicates the transition from the side road to Green, facilitating the movement of vehicles from the side road to the main road.

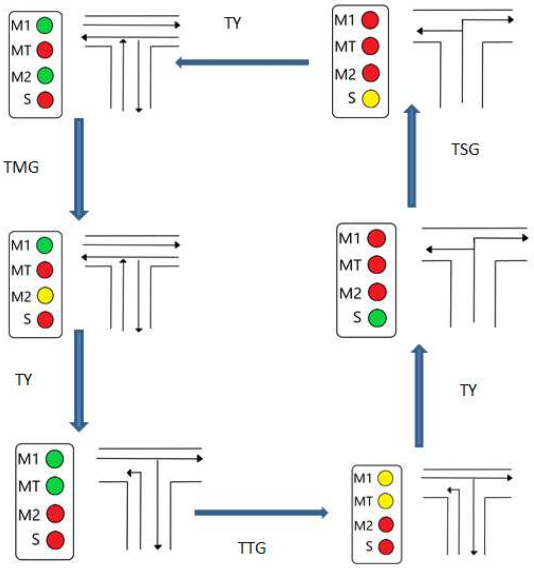


Fig. 1. Switching of LED lights at T-Intersection junction.

IV. Implementation

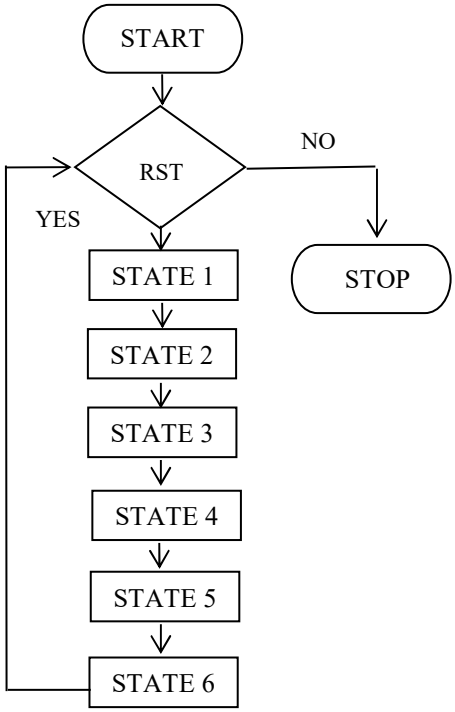


Fig. 2. Flow chart of the Design.

The flow diagram depicted above illustrates the operation of a Traffic Controller for a T-Intersection. Employing a finite state machine, the control flow, as depicted in Fig. 2. governs the system.

If the reset signal is set to one, the system terminates. Conversely, if the reset signal is zero, the system initializes in the first state, provided the delay for this state is satisfied. It subsequently transitions to the next state, or remains in the current state if the delay conditions are not met. This sequence continues, with transitions occurring between states in a cyclic manner.

To implement the Traffic Light Controller for a T-Intersection, Verilog code is utilized, and the system is realized on an FPGA kit using Xilinx ISE 14.7. The introduction of delays between each state facilitates the switching of traffic lights, enabling smooth vehicular movement without congestion and delays.

The time delays associated with each state are as follows:

- TMG: 30 seconds
- TY: 4 seconds
- TTG: 30 seconds
- TSG: 20 seconds

It's important to note that these delays can be adjusted to suit different areas and traffic conditions.

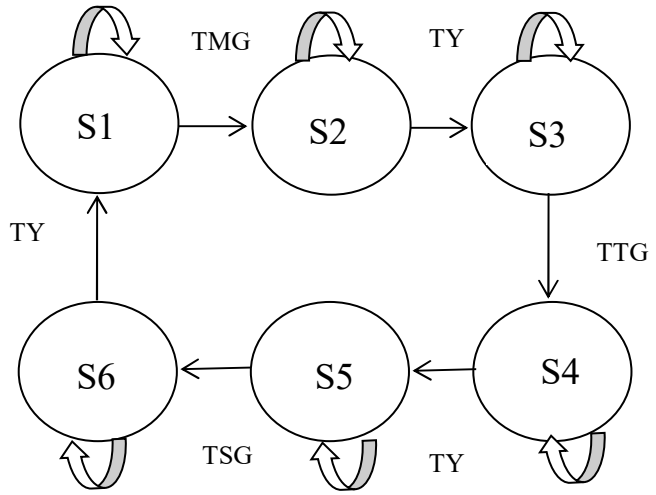


Fig. 3. Finite State Machine of Design.

Fig. 3 illustrates the transitions between each state in the system, with TMG, TY, TTG, and TSG representing the delays between states. These delays may be due to the physical characteristics of the system, such as the propagation delay of the logic gates, or they may be due to the desired behavior of the system, such as waiting for a certain amount of time before transitioning to the next state.

The FSM model provides a clear and concise way of representing the control flow between states. It is a state-based model, meaning that the system's behavior is determined by its current state and the inputs that it receives. The FSM model also includes the delays between states, which allows for a more accurate simulation and implementation of the system.

V. RESULTS

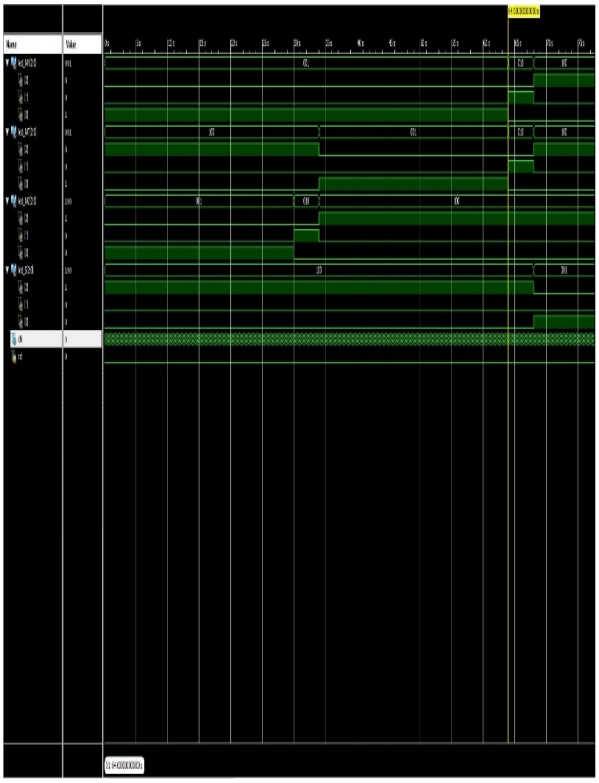


Fig. 4. Simulation Waveforms of Design.

From Fig. 4, The Traffic Light Switching System designed for a T-Intersection was created using Verilog. This design code was subsequently synthesized and simulated using Xilinx ISE 14.7 to generate waveforms, as shown in Fig. 4. The waveforms clearly demonstrate that each state transitions in accordance with the designed Finite State Machine (FSM) and adheres to precise timing definition.

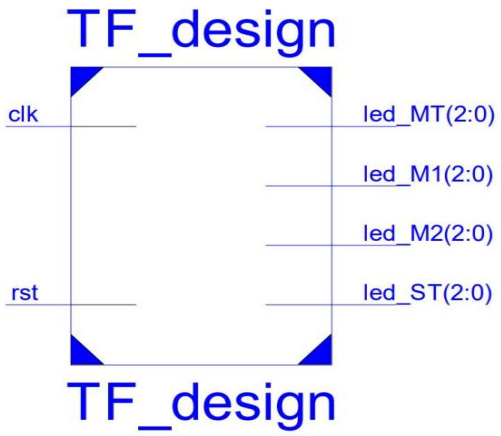
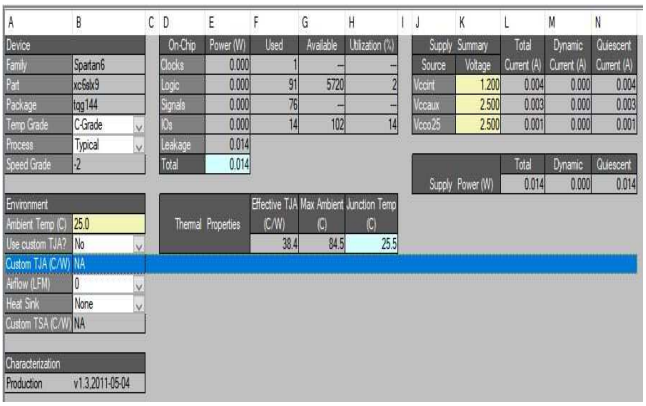


Fig. 5 Top Module of the Design.

Fig. 5. depicts the Top module of the Traffic Light Switching System design. The top module plays a critical role as it serves as the interface for inputs and outputs while also managing the internal operations of the processor. A processor is a device responsible for executing a sequence of instructions to perform specific task.



Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Spartan6	Clocks	0.000	1	--	--
Part	xc6slx9	Logic	0.000	91	5720	2
Package	tqg144	Signals	0.000	76	--	--
Temp Grade	C-Grade	IOs	0.000	14	102	14
Process	Typical	Leakage	0.014			
Speed Grade	-2	Total	0.014			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

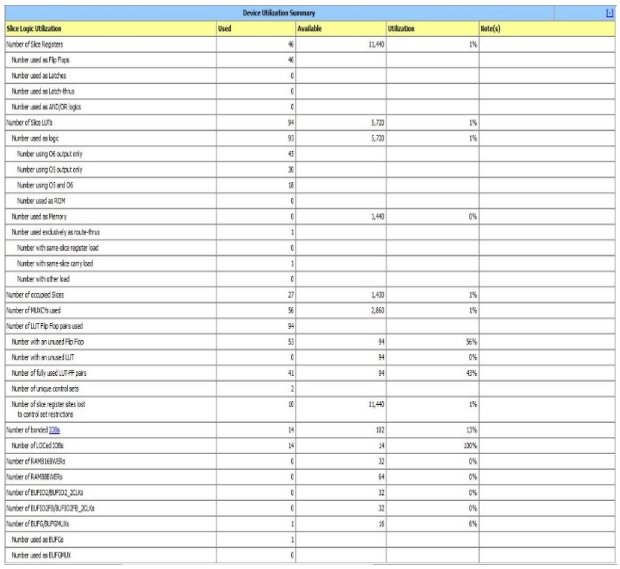
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.4	84.5	25.5

Characterization	
Production	v1.3,2011-05-04

Fig. 6. Power analysis of the design.

Fig. 6. The design has a power consumption of 0.014 watts per switching line, which is a decrease of over 99.99% from the existing system's maximum power consumption of 300 watts per switching line. This represents a significant improvement in energy efficiency, and it is likely to lead to significant savings in energy costs.In other words, the new system consumes less than one-thousandth of the power of the existing system. This is a remarkable achievement, and it is likely to have a major impact on the overall energy efficiency of the system.



Device Utilization Summary

Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	46	11,440	1%	
Number used as Flip Flops	46			
Number used as Latches	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	94	5,720	1%	
Number used as logic	93	5,720	1%	
Number using O6 output only	45			
Number using O5 output only	30			
Number using O5 and O6	18			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	27	1,430	1%	
Number of MUXCYs used	56	2,860	1%	
Number of LUT Flip Flop pairs used	94			
Number with an unused Flip Flop	53	94	56%	
Number with an unused LUT	0	94	0%	
Number of fully used LUT-FF pairs	41	94	43%	
Number of unique control sets	2			
Number of slice register sites lost to control set restrictions	10	11,440	1%	
Number of bonded IOBs	14	102	13%	
Number of LOCed IOBs	14	14	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Fig. 7. Area Report of the design.

From Fig. 7, The largest contributors to the design area are the following:

TABLE I. The Design Area

Parameter/Utilization	Available Area	Used(%)
Slice Logic	11440	94(1%)
Memory	1440	0(0%)
I/O Bound	132	14(13%)

Overall, the design area is well within the limits of the FPGA device. However, there are a few areas where the area utilization could be improved. For example, the memory usage could be reduced by using more efficient data structures. Additionally, the I/O usage could be reduced by using more efficient routing techniques.

Fig. 8. illustrates the estimated delay analysis for the design. The total delay computed is 5.464 nanoseconds, of

which 1.921 nanoseconds are attributed to logic delay and 3.543 nanoseconds to route delay.

```
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.464ns (frequency: 183.016MHz)
  Total number of paths / destination ports: 4445 / 57
-------------------------------------------------------------------------
Delay:               5.464ns (Levels of Logic = 12)
  Source:            count_23 (FF)
  Destination:       count_2 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: count_23 to count_2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             7   0.525   1.340  count_23 (count_23)
     LUT5:I0->O           0   0.254   0.000  Mcompar_n0003_lutdi1 (Mcompar_n0003_lutdi1)
     MUXCY:DI->O          1   0.181   0.000  Mcompar_n0003_cy<2> (Mcompar_n0003_cy<2>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<3> (Mcompar_n0003_cy<3>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<4> (Mcompar_n0003_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<5> (Mcompar_n0003_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<6> (Mcompar_n0003_cy<6>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<7> (Mcompar_n0003_cy<7>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<8> (Mcompar_n0003_cy<8>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<9> (Mcompar_n0003_cy<9>)
     MUXCY:CI->O          3   0.235   0.994  Mcompar_n0003_cy<10> (Mcompar_n0003_cy<10>)
     LUT6:I3->O          17   0.235   1.209  Mmux_state[2]_count[63]_wide_mux_24_OUT1101 (Mmux_state[2]_count[63]_wide_mux_24_OUT110)
     LUT2:I1->O           1   0.254   0.000  Mmux_state[2]_count[63]_wide_mux_24_OUT641 (state[2]_count[63]_wide_mux_24_OUT<9>)
     FDC:D                    0.074          count_9
    ----------------------------------------
    Total                     5.464ns (1.921ns logic, 3.543ns route)
                              (35.2% logic, 64.8% route)
```

Fig. 8. Delay Analysis of the Design.

Fig. 9. FPGA Implementation result.

Fig. 9. illustrates the implementation on the Spartan 6 FPGA board. The system's functionality has been verified through simulation and FPGA Prototyping. Following successful functional simulation and post-route simulation, FPGA Prototyping is carried out. It's noteworthy that the state transitions occur precisely according to the defined time parameters, and the desired set of outputs is generated as intended.

VI. Conclusion and Future Scope

A Traffic Light Switching System for a T-Intersection, implemented using Verilog, has been efficiently designed and synthesized within Xilinx ISE 14.7. This system has been successfully deployed on a SPARTAN-6 FPGA kit, boasting a minimal power consumption of 0.014 Watts and an impressively short delay time of 5.464 nanoseconds. Consequently, it offers an efficient solution to modern traffic control demands.

This integration into a compact chip has significantly reduced both the size and complexity of the system. In contrast, the current traffic light switching systems, which are embedded-based, demand substantial space, area, and consume more power. The adoption of this Verilog-based Traffic Light Control System for T-Intersections promises significant power and area savings.

Furthermore, this design can be enhanced with an emergency feature. For instance, during emergency situations like when an ambulance is stranded at a junction, the system can be programmed to prioritize traffic clearance. This could be considered as a potential avenue for future development within this project.

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