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Design and Implementation of Traffic Light Controller for T-Intersection on FPGA

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UNDER THE GUIDANCE OF

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ABSTRACT

Traffic control systems are essential for managing traffic flow and ensuring road safety. In recent years, the implementation of traffic control systems has been heavily reliant on digital electronics and computer-based technology. Verilog is a hardware description language, is widely used for designing digital circuits and systems, including traffic control systems. In this paper, describes an overview of the implementation of a Verilog design for T-Intersection traffic light control. The design includes a traffic light controller that utilizes a state machine to regulate the flow of traffic. The Verilog code is synthesized using a design compiler, and the design is then simulated using a hardware description language simulator. The design flow provides an insight into the implementation of the traffic light controller using Verilog. The implementation shows that Verilog is a powerful and efficient tool for designing traffic control systems. It allows for easy simulation and testing of the design before implementation, enabling designers to optimize the design for performance and reliability. In conclusion, this paper highlights the importance of Verilog in the development of traffic control systems and its potential to contribute to the future of intelligent transportation systems.

LITERATURE SURVEY

TITLE	AUTHOR	YEAR	INFERENCE
Designing of a Traffic Signalling System at T-Intersection	**Ramesh Surisetty**	2017	The signal is designed as per IRC guidelines so that the signal can justify the proper movement of the traffic. By providing signals, there will be a reduction in conflicts. And there will be orderly movement of traffic. The signal design procedure involves a few important steps: (1) Three Phase design (2) Determining of amber time and clearance time (3) Determined optimum cycle length (4) Apportioning of green time (5) The presentation estimate of the above design.
TRAFFIC LIGHT CONTROL SYSTEM USING VERILOG DESIGNING	**Akshay Bidwai Abhiyash Hodge Hrishikesh Humnabakar**	2018	traffic light signal controlling can be done using Verilog (hardware descriptive language). Bit Pattern to be used as RYG, RYG denotes (RED YELLOW GREEN). Transition from red light to green light requires more delay. That means the amount of time for the delay is more. Similarly transition from green light to yellow light requires moderate delay. Transition of yellow light to red light requires very small delay as compared to other delays.

TITLE	AUTHOR	YEAR	INFERENCE
International Journal of VLSI System Design and Communication Systems Volume.05, IssueNo.07, July-2017, Pages: 0657-0661:	**Sweatha, G Sai Prakash ,Prathyusha, Mahesh Shetkar**	2017	This is due to the large number of vehicles and the high dynamics of the traffic system. . Traffic Light Control (TLC) system also based on microcontroller and microprocessor. But the disadvantage of with microcontroller or microprocessor is that it works on fixed time, which is functioning according to the program that does not have the flexibility of modification on real time basis.
FPGA BASED TRAFFIC LIGHT CONTROLLER	**LalitaChoudhary Krishna Balram Parihari KamleshKumhar JitendraKumar**	2016	The methods that are used in this projects are proposing the circuit, write a code, simulate, synthesis and implement on the hardware. This paper presents the FPGA implemented low cost advance TLC system using chip scope pro and virtual input output.

INTRODUCTION

Traffic is the movement of vehicles, pedestrians, and other road users on a roadway. Managing traffic is essential to ensure safety and reduce congestion. A traffic controller is a device or system that regulates the flow of traffic at an intersection or along a roadway. Implementing a traffic controller involves designing and installing the system and ensuring that it is programmed and maintained properly. The implementation process involves analysing traffic patterns, selecting appropriate equipment and software, installing and configuring the system, and testing and validating its performance. Effective traffic management systems can create safer and more efficient transportation networks for communities.

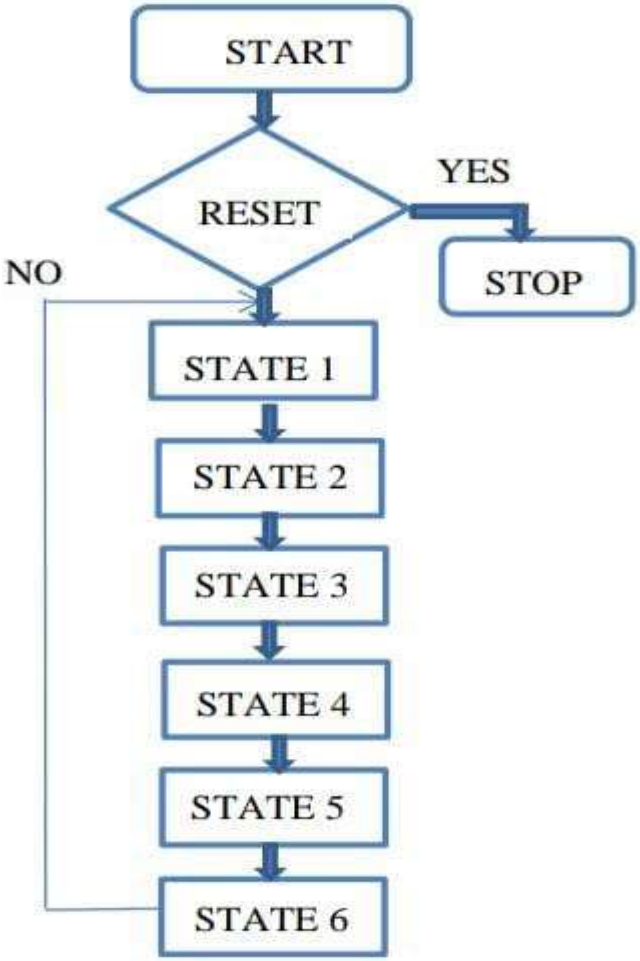
Problem Statement

The problem that arises in traffic management is the need to efficiently manage the movement of vehicles, pedestrians, and other road users while ensuring their safety and reducing congestion. The implementation of a traffic controller system aims to address this problem by regulating the flow of traffic at intersections and along roadways. However, the challenge is in designing and installing an effective traffic controller system that can adapt to changing traffic conditions and is programmed and maintained properly to ensure optimal performance.

OBJECTIVES

- The primary objective of a trafficlight controller is to regulate the movement of vehicles at intersection or along a roadway and to ensure efficient movement of vehicles and safety of pedestrians.
- The design can be optimised for delay and less power consumption.
- The area and complexity of the traffic light controller system can be reduced by implementing it on the FPGA Kit.

METHODOLOGY



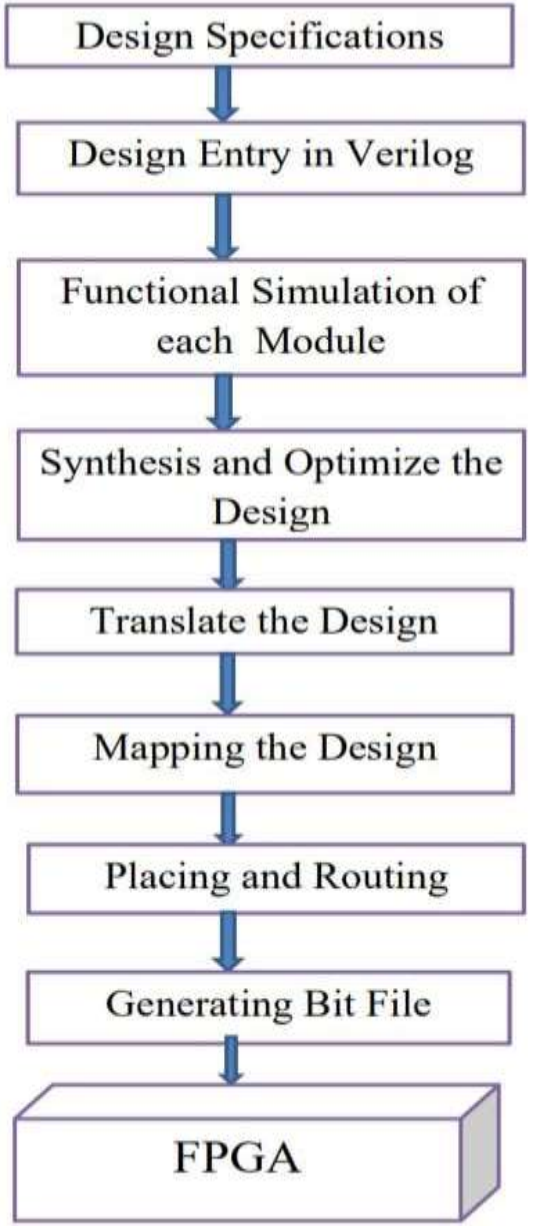
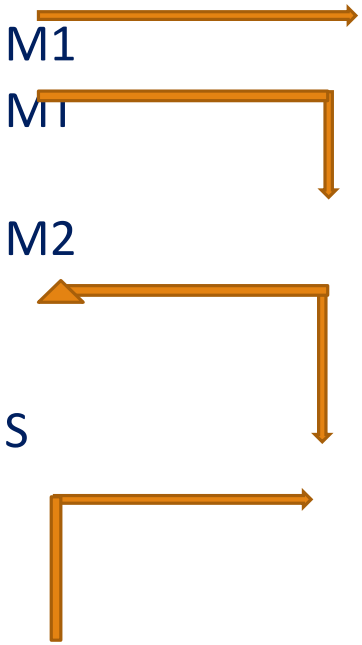
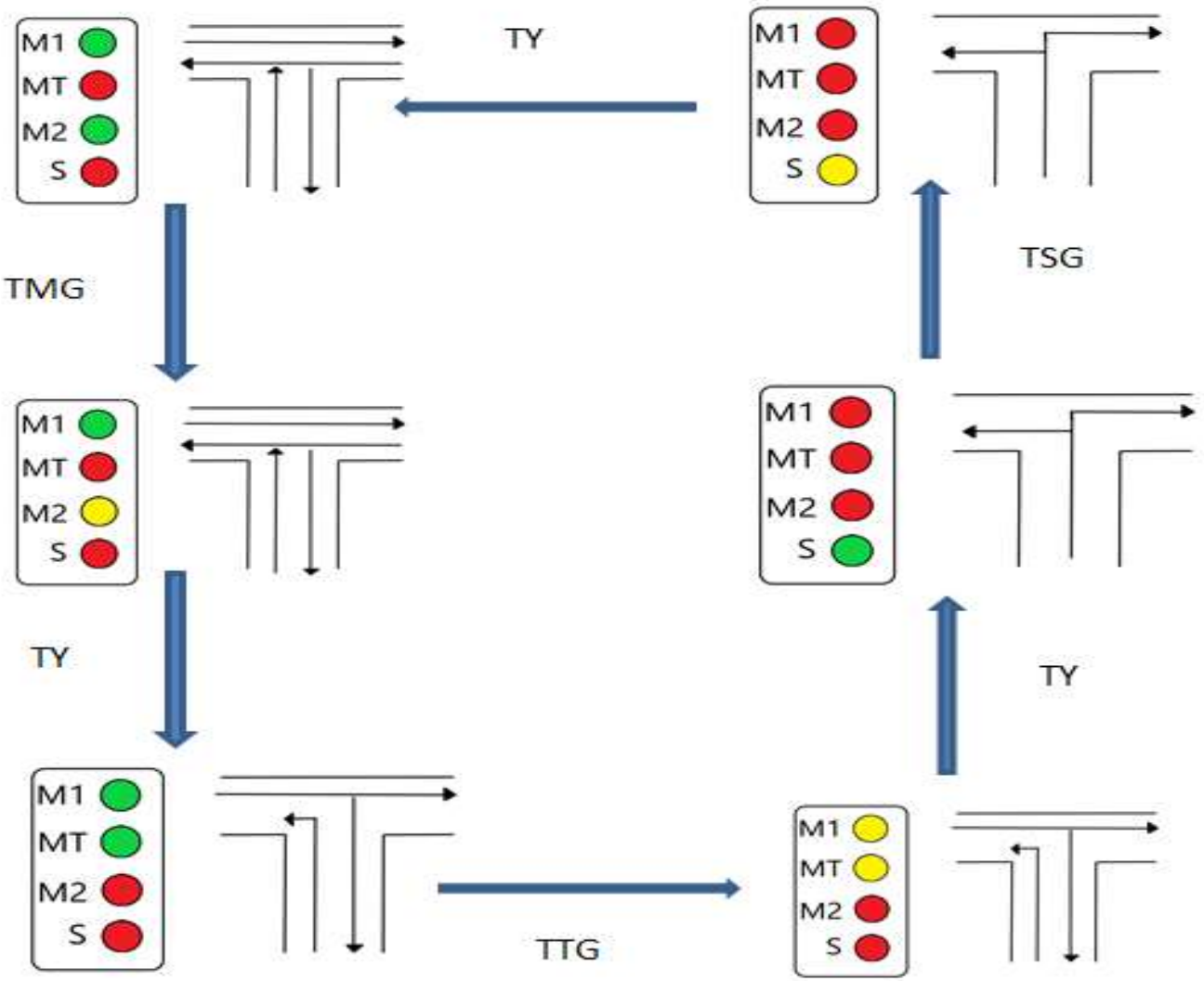


Fig : SYSTEM MODELLING and FLOW CHART

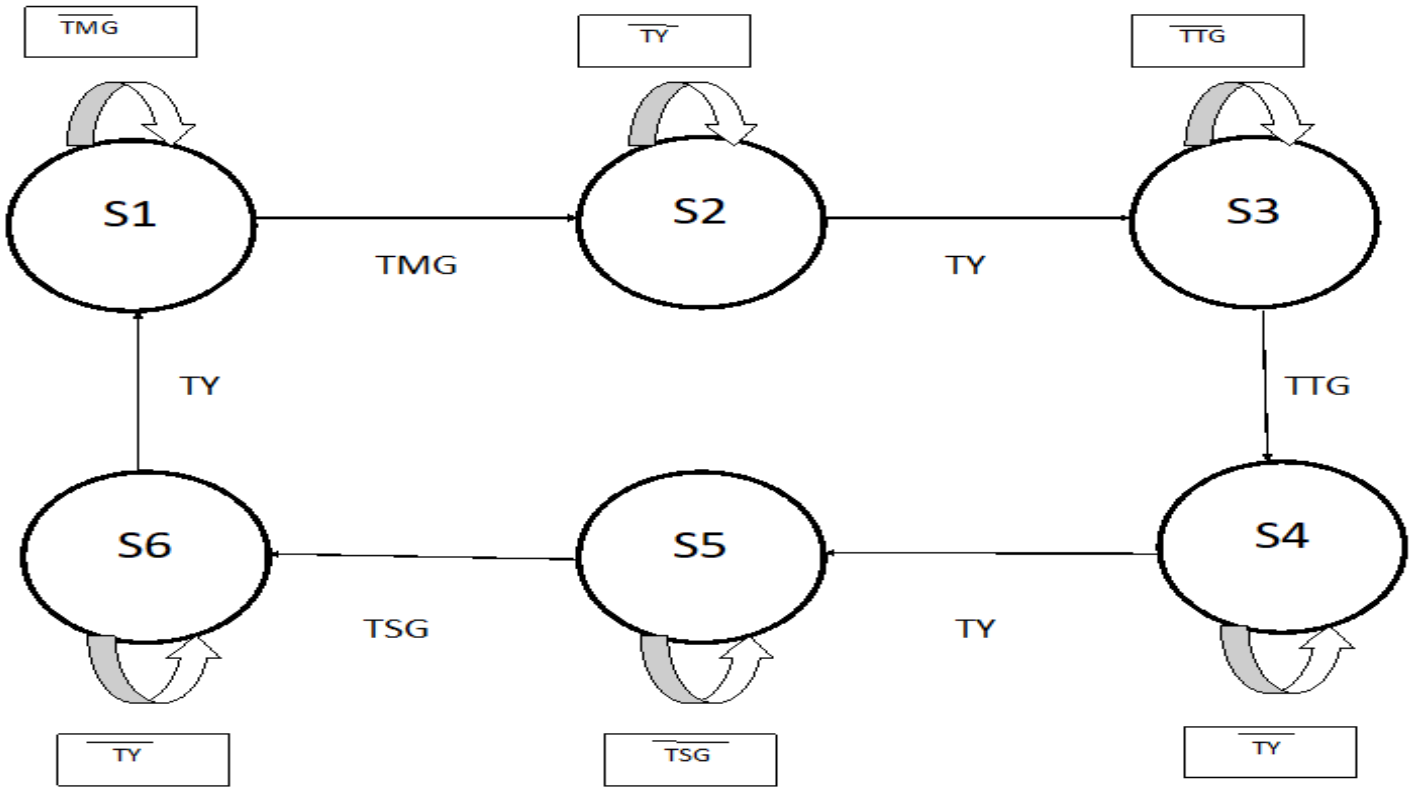
IMPLEMENTAION





FINITE STATE MACHINE (FSM)

TMG-30s , TY-4s, TTG-30s, TSG-20s



ADVANTAGES

1. Traffic control signals provide for an orderly movement of traffic.
2. They help in reducing the frequency of accidents of some special nature i.e., of Right-angle accidents.
3. They intercept heavy traffic to allow other traffic to cross the road intersection safely.
4. They provide authority to the drivers to move with confidence.
5. They control the speed of vehicles on main as well as on secondary roads.
6. They direct traffic on different routes without excessive congestion.
7. They provide economy over manual control at the intersection.

APPLICATIONS

Automatic traffic light controller have several applications in the field of traffic management and transportation. Here are some examples:

1. Intersection Control: Automatic traffic light controllers are used to regulate the flow of traffic at intersections. They ensure smooth and safe movement of vehicles by assigning right-of-way to different lanes based on traffic conditions.
2. Traffic Optimization: These controllers analyse traffic patterns and adjust signal timings accordingly to optimize traffic flow. They can prioritize high-traffic directions or dynamically adapt to changing traffic conditions, reducing congestion and minimizing delays.
3. Pedestrian Safety: Automatic traffic light controllers incorporate pedestrian detection systems and manage pedestrian signals. They provide safe crossing times, implement special phases for pedestrians, and synchronize pedestrian movements with vehicular traffic to enhance pedestrian safety.
4. Adaptive Signal Control: These controllers utilize real-time data to adapt signal timings based on current traffic conditions. By dynamically adjusting signal cycles, they optimize traffic flow and reduce congestion, especially during peak hours or in response to incidents.

These applications demonstrate the importance of automatic traffic light controllers in improving traffic safety, optimizing traffic flow, and enhancing overall transportation efficiency.

PROJECT REQUIREMENTS

SOFTWARE: XILINX ISE 14.7
HARDWARE: SPARTAN 6 FPGA BOARD

RESULT

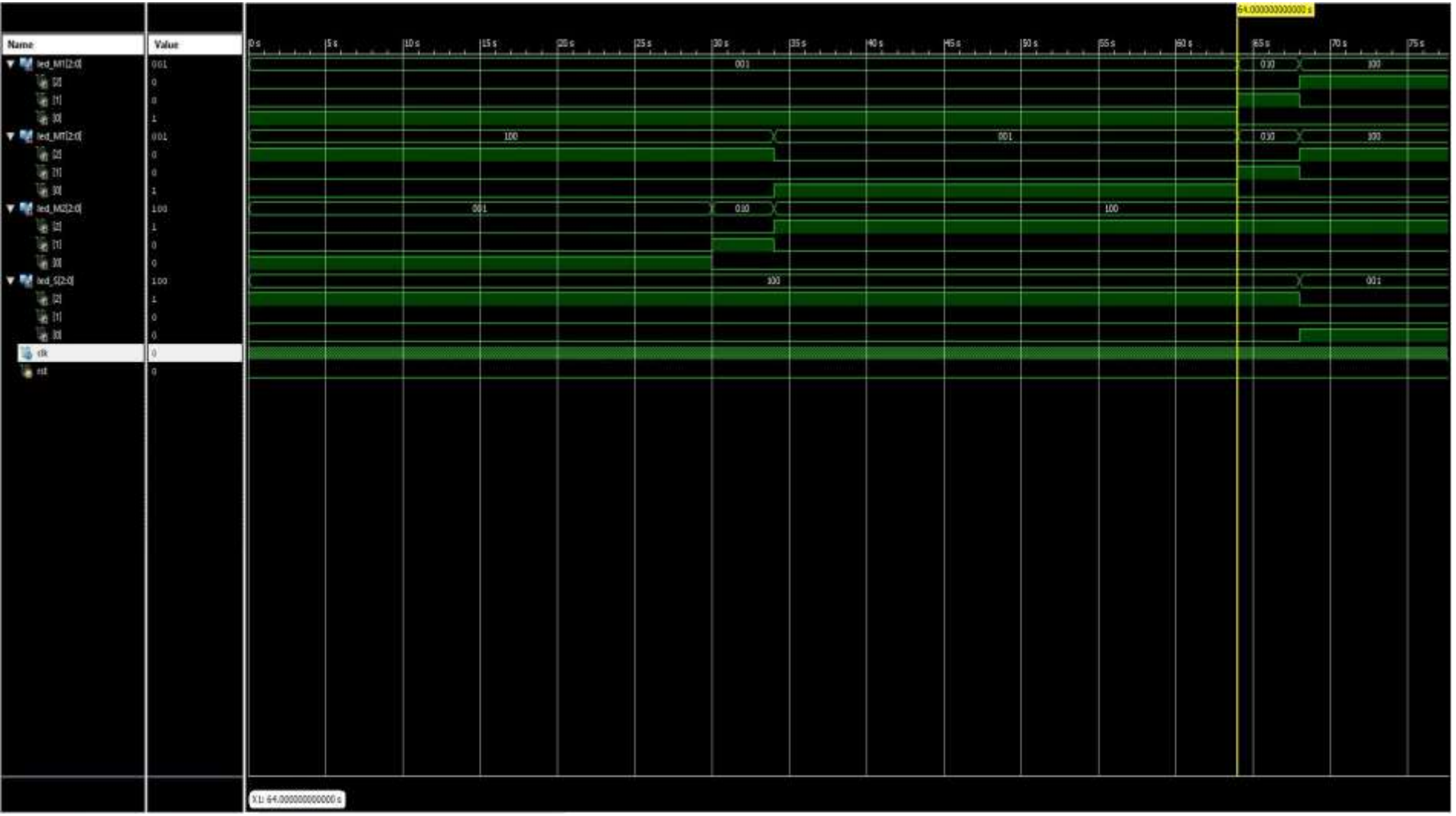


Fig1 : Simulation Waveforms

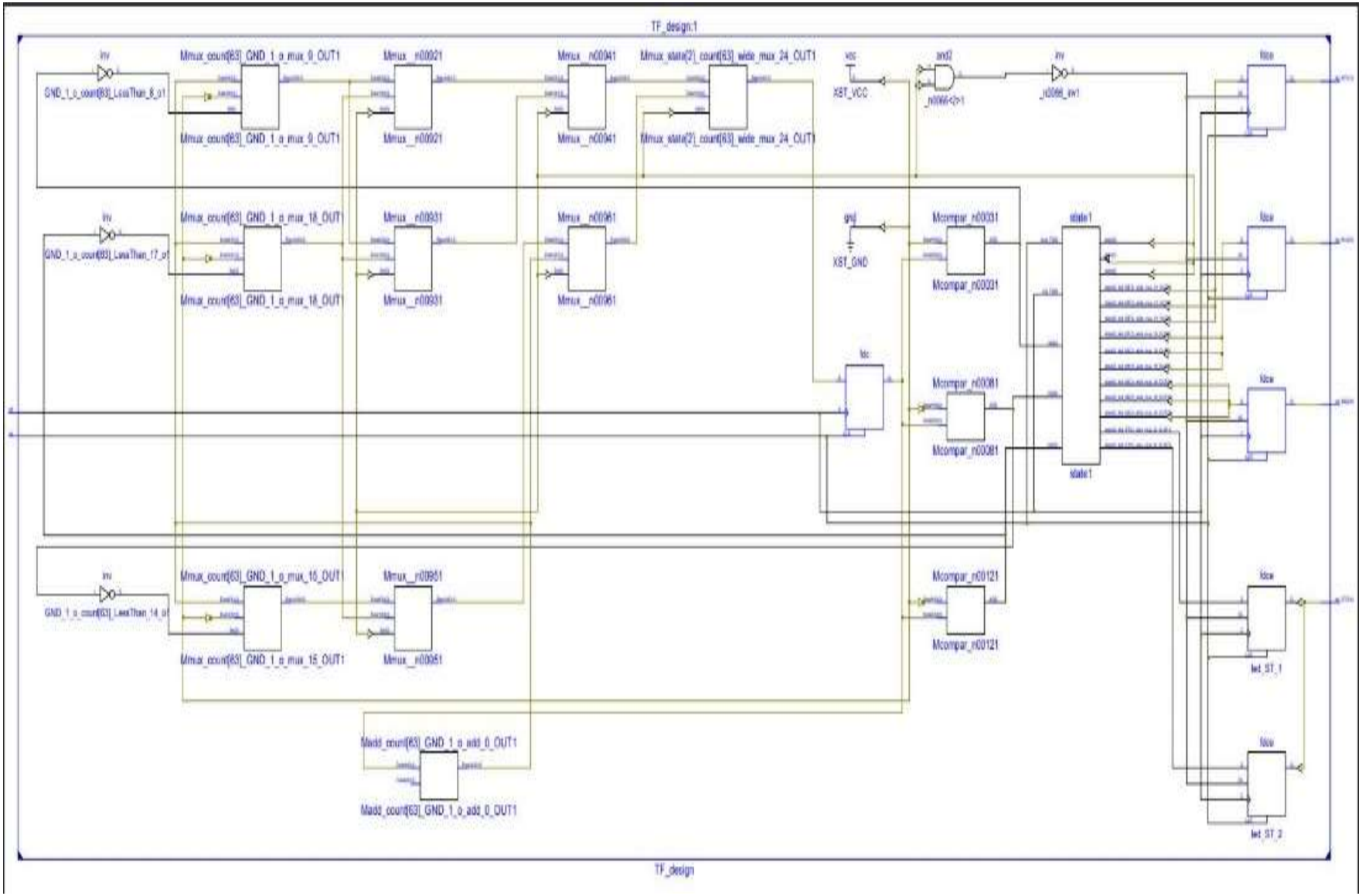


Fig 2: RTL SCHEMATIC of the Design

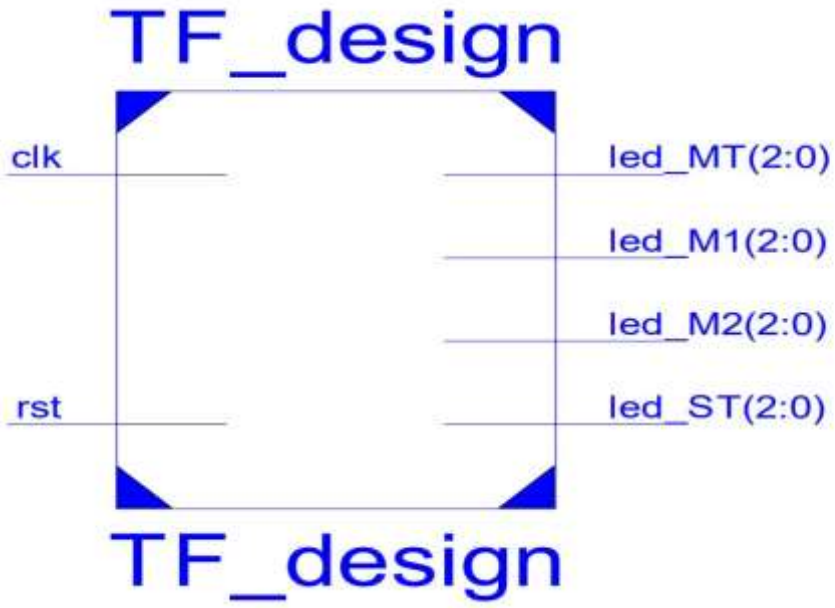


Fig 3 :TOP MODULE OF THE DESIGN

POWER ANALYSIS

Device	
Family	Spartan6
Part	xc6slx9
Package	tqg144
Temp Grade	C-Grade
Process	Typical
Speed Grade	-2

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	--	--
Logic	0.000	91	5720	2
Signals	0.000	76	--	--
IOs	0.000	14	102	14
Leakage	0.014			
Total	0.014			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.004	0.000	0.004
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.014	0.000	0.014

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Heat Sink	None
Custom TSA (C/W)	NA

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	38.4	84.5	25.5

Characterization	
Production	v1.3,2011-05-04

Fig3 : Power Report of the Design

AREA SUMMARY

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	46	11,440	1%	
Number used as Flip Flops	46			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	94	5,720	1%	
Number used as logic	93	5,720	1%	
Number using O6 output only	45			
Number using O5 output only	30			
Number using O5 and O6	18			
Number used as ROM	0			
Number used as Memory	0	1,440	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	27	1,430	1%	
Number of MUXCYs used	56	2,860	1%	
Number of LUT Flip Flop pairs used	94			
Number with an unused Flip Flop	53	94	56%	
Number with an unused LUT	0	94	0%	
Number of fully used LUT-FF pairs	41	94	43%	
Number of unique control sets	2			
Number of slice register sites lost to control set restrictions	10	11,440	1%	
Number of bonded IOBs	14	102	13%	
Number of LOCed IOBs	14	14	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Fig 4: Area Report of the Design

Delay Analysis

```
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.464ns (frequency: 183.016MHz)
  Total number of paths / destination ports: 4445 / 57
-------------------------------------------------------------------------
Delay:               5.464ns (Levels of Logic = 12)
  Source:            count_23 (FF)
  Destination:       count_2 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: count_23 to count_2
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             7   0.525   1.340  count_23 (count_23)
     LUT5:I0->O           0   0.254   0.000  Mcompar_n0003_lutdi1 (Mcompar_n0003_lutdi1)
     MUXCY:DI->O          1   0.181   0.000  Mcompar_n0003_cy<2> (Mcompar_n0003_cy<2>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<3> (Mcompar_n0003_cy<3>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<4> (Mcompar_n0003_cy<4>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<5> (Mcompar_n0003_cy<5>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<6> (Mcompar_n0003_cy<6>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<7> (Mcompar_n0003_cy<7>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<8> (Mcompar_n0003_cy<8>)
     MUXCY:CI->O          1   0.023   0.000  Mcompar_n0003_cy<9> (Mcompar_n0003_cy<9>)
     MUXCY:CI->O          3   0.235   0.994  Mcompar_n0003_cy<10> (Mcompar_n0003_cy<10>)
     LUT6:I3->O          17   0.235   1.209  Mmux_state[2]_count[63]_wide_mux_24_OUT1101 (Mmux_state[2]_count[63]_wide_mux_24_OUT110)
     LUT2:I1->O           1   0.254   0.000  Mmux_state[2]_count[63]_wide_mux_24_OUT641 (state[2]_count[63]_wide_mux_24_OUT<9>)
     FDC:D                    0.074          count_9
    ----------------------------------------
    Total                     5.464ns (1.921ns logic, 3.543ns route)
                              (35.2% logic, 64.8% route)
```

Fig 6: Delay Report of the Design

CONCLUSION AND FUTURE SCOPE

A Traffic Light controller for T-Intersection using Verilog was efficiently designed and synthesized in Xilinx ISE 14.7 and implemented on SPARTAN-6 FPGA kit with a power consumption of 0.014 Watt, and delay time of 5.464 nano seconds .Thus providing efficient solution for modern traffic control requirements. As the design is integrated in a small chip the size and complexity has reduced. At present the existing traffic light controller is embedded based which the system requires large space or area and more power consumption. By adopting this traffic light controller for T-Intersection we can reduce power and area.

Further the above Design can be added a feature in case of emergency situation. For example when an Ambulance stuck in a traffic the signal can be made traffic free this condition can be taken as a future work on this project.

THANK YOU!