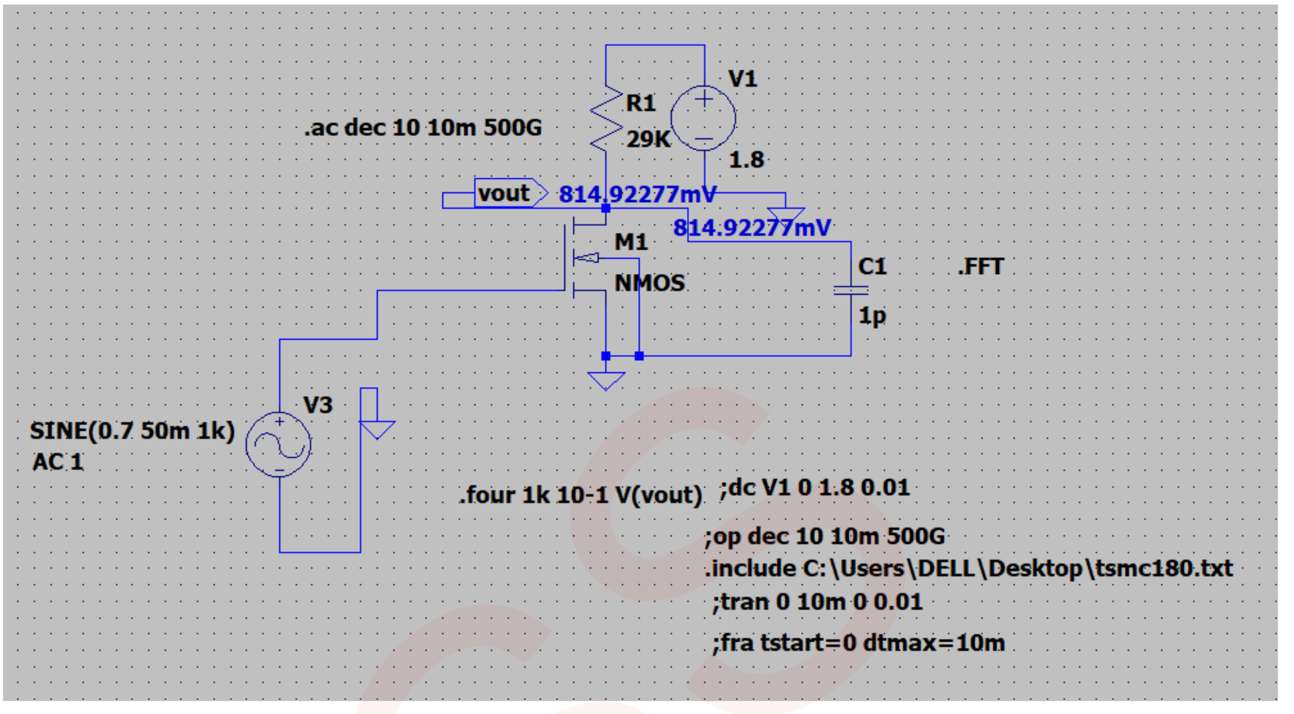
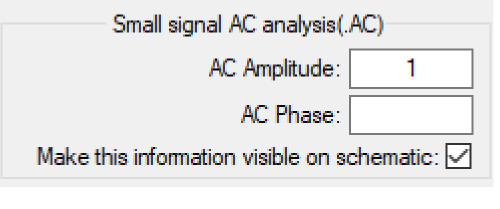
1. Design an NMOS input resistive loaded CS amplifier such that the small signal DC gain is anywhere between 5 to 15 (Excluding 5 and 15). The input DC bias voltage is 0.7 V. The output DC voltage can be anywhere between 0.7 V and 1.2 V. Perform the following experiments on the designed amplifier.

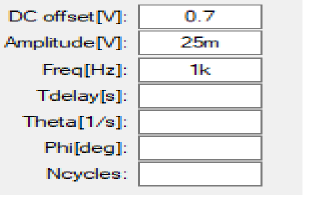
For gain to become 5.4 and output voltage to become 0.814 volt. The size of a mos device is taken as W=0.55μ and L=0.18 μ



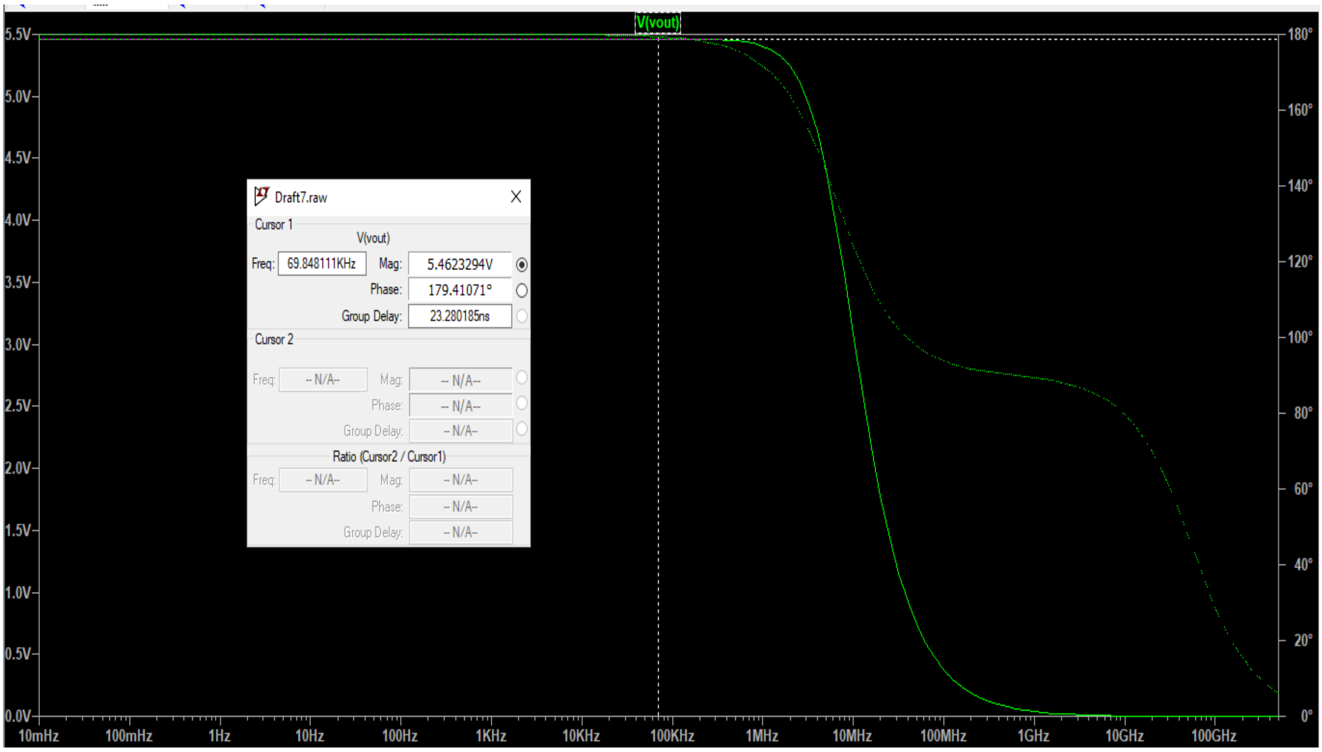

```
       Unknown control card
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM3 MOSFETS ---
Name:          m1
Model:        nmos
Id:         3.40e-05
Vgs:        7.00e-01
Vds:        8.15e-01
Vbs:        0.00e+00
Vth:        4.67e-01
Vdsat:      1.44e-01
Gm:         2.35e-04
Gds:        8.49e-06
```

Drain current comes out to be = 34 μA





(a) Frequency response of the amplifier. Find the small signal DC gain and bandwidth of the amplifier. Compare it with calculated value using the small signal parameters obtained from the DC operating point simulation. Also find the bandwidth of the amplifier.



Calculated gain-

$R_D = 29K$

$r_0 = \frac{1}{Gds}$

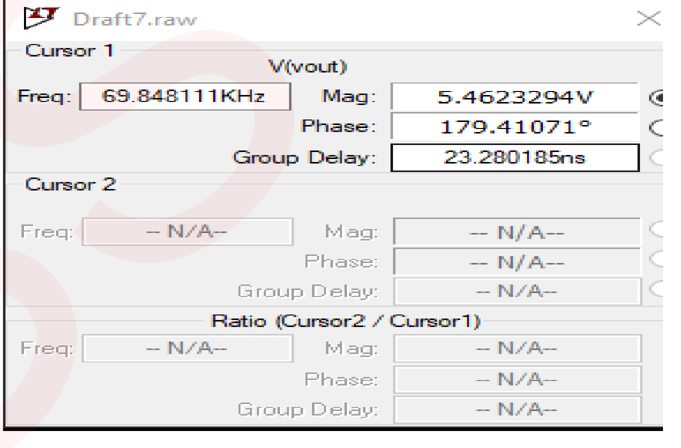
$r_0 = \frac{1}{8.49e-06} = 117.785k$

$R_D || r_0 = 23.27k$

$A_v = g_m (R_D || r_o)$

$A_v = 2.35 \times 10^{-4} \times 23.27\ k = 5.4$

Fig 1 – Gain in simulation



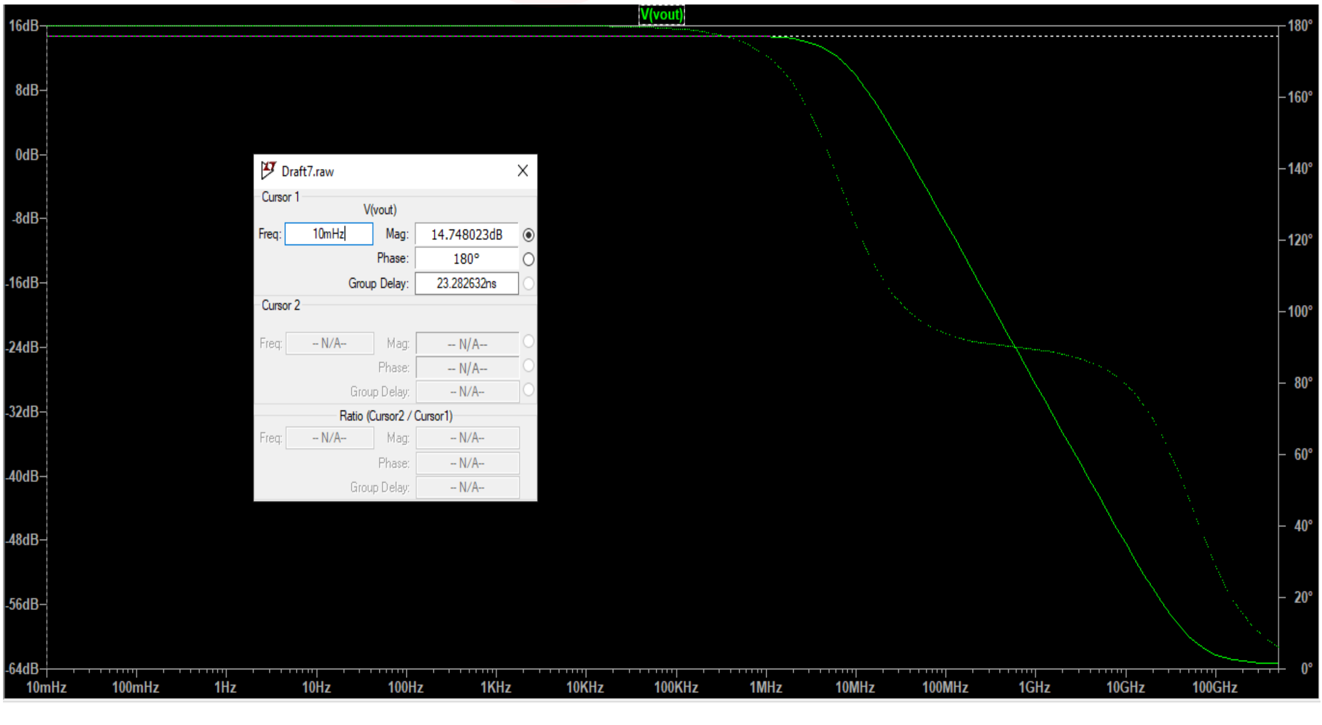


Fig -2 (Gain in decibel)

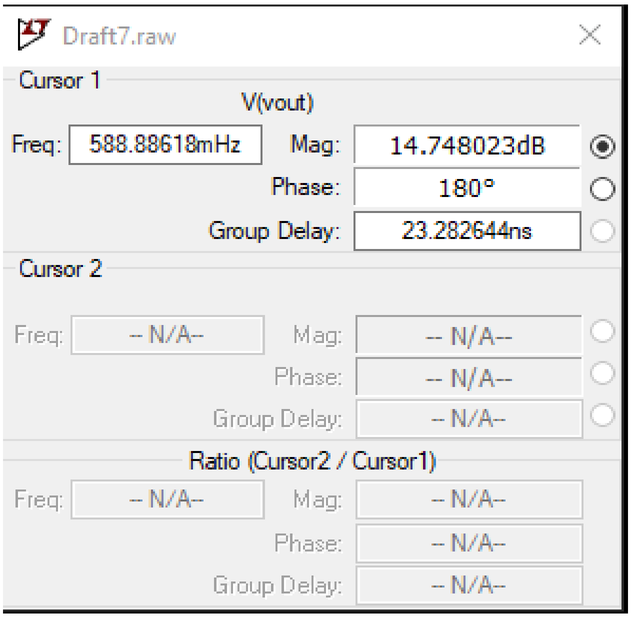
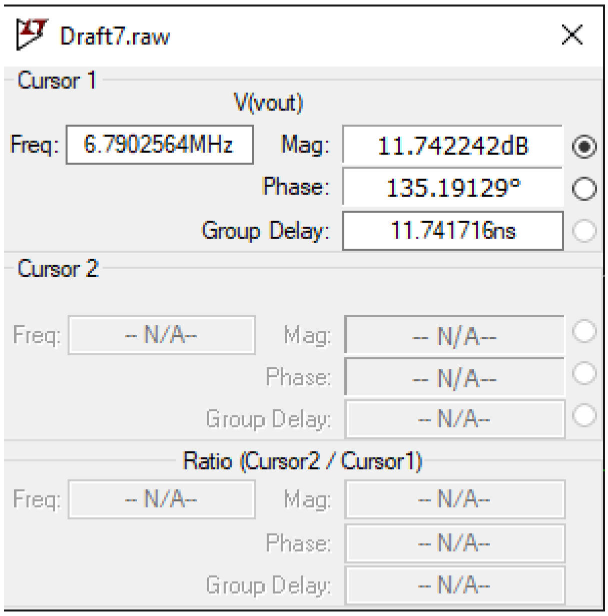


Fig -3 (Corresponding frequency)



For bandwidth:

Av=20log (gain)

=20log (5.4) =14.64 Decibel

For Bandwidth: (Simulation)

Gain in Db – 3dB= 14.74 – 3=11.74 dB

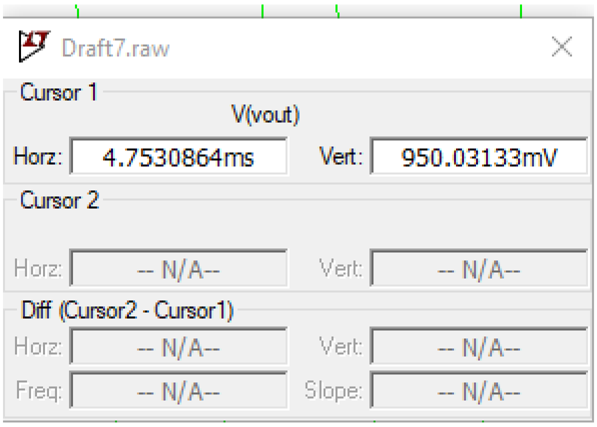
For 11.74 decibel the frequency is 6.79 MHz

Bandwidth= $f_1 - f_2$ = 6.79-0= 6.79 MHz

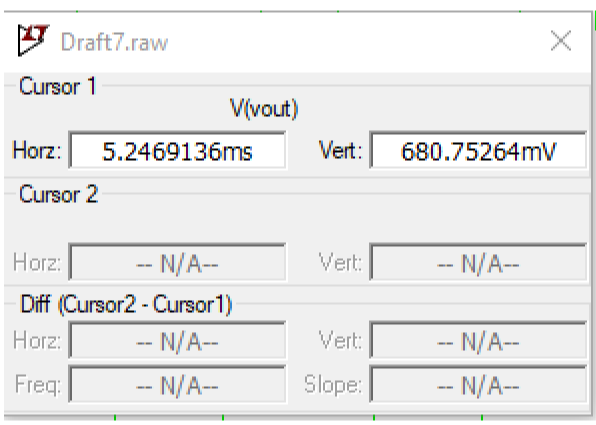
Parameter	Calculated	Simulation
Gain	5.4	5.46 (Fig 1)
Gain in dB	14.64dB	14.74 dB (Fig 2)
Bandwidth	6.94 MHz	6.79 MHz (Fig 3)

b) Excite the amplifier with a 50 mV peak-to-peak sine wave of frequency 1 kHz riding on the input DC bias voltage and obtain the output. What is the peak-to-peak voltage of the output?

- Here frequency in given as 1 KHz , DC offset is 0.7 V , Amplitude =25 millivolt



Maximum value of output voltage



Minimum value of Ouput voltage

For ouput-

$V_{(max)} = V\ (dc) + V_m$ $\qquad V_{(min)} = V(dc) - V_m$ $\qquad$ Adding this two-

$V_m(out) = [V_{(max)} - V_{(min)}]/2$

$V_m(out) = [950\ m\ V - 680.7\ m\ V]/2 = 134.65\ mv$

Peak to peak voltage of output=269.3 mv

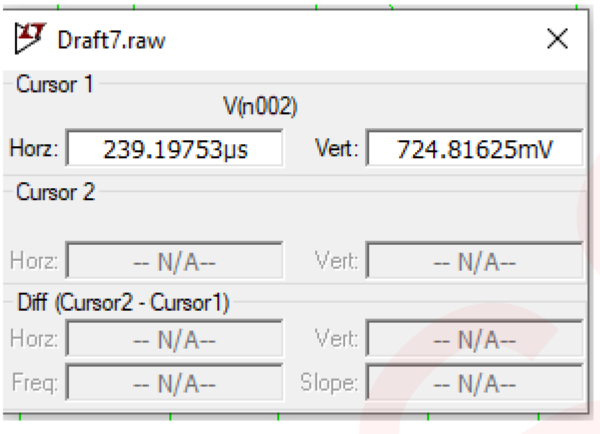
For input-

$V_{(max)} = V\ (dc) + V_m$ $\qquad V_{(min)} = V(dc) - V_m$ $\qquad$ Adding this two-

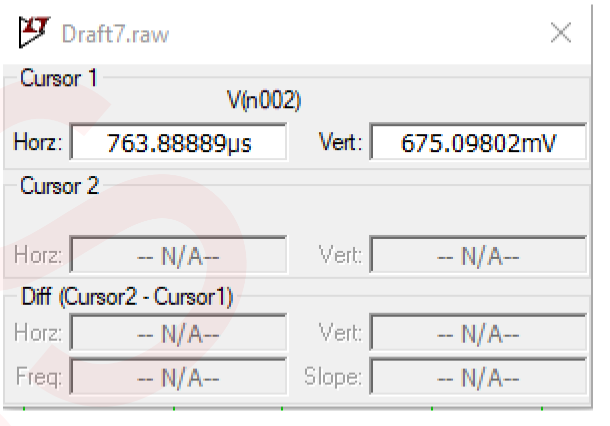
$V_m(in) = [V_{(max)} - V_{(min)}]/2$

$V_m(in) = [724.816\ m\ V - 675.09\ m\ V]/2 = 24.86\ mv$

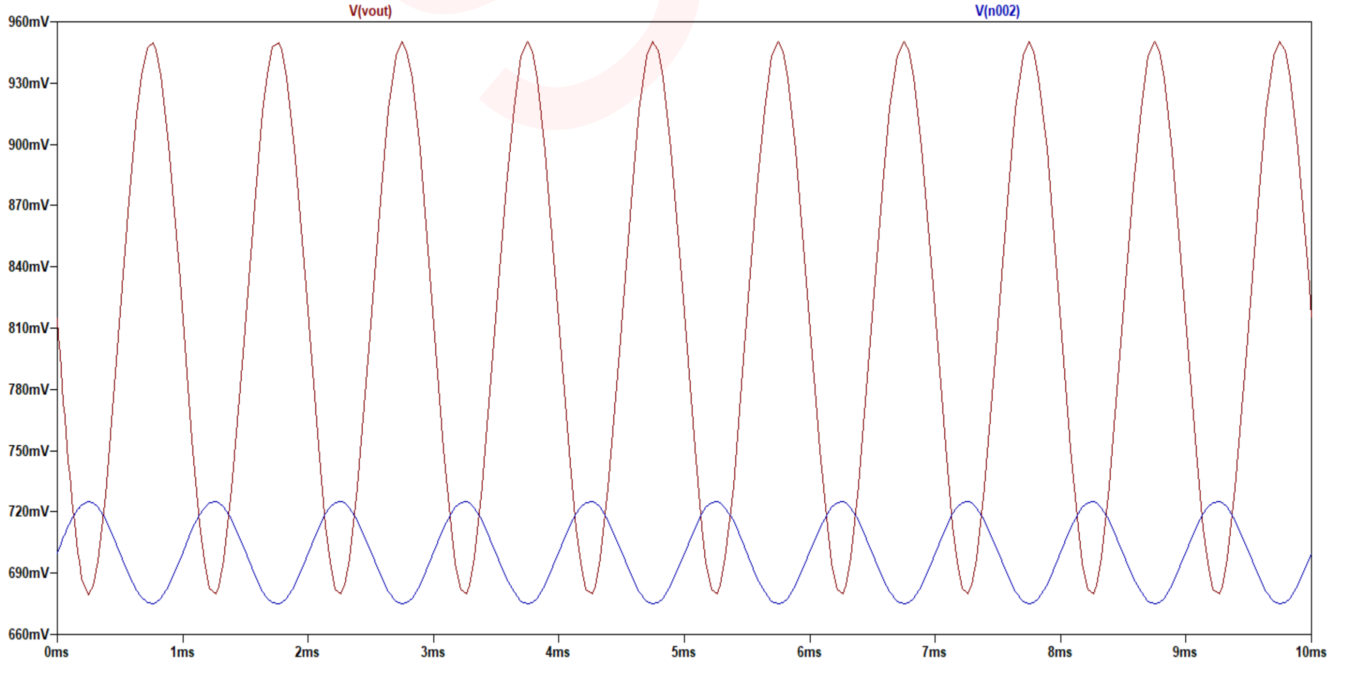
Gain $= \frac{output\ voltage}{input\ voltage} = \frac{134.65\ mV}{24.86\ mV} = 5.4$ which is exacly same as calculated earlier



Maximum Value of input voltage



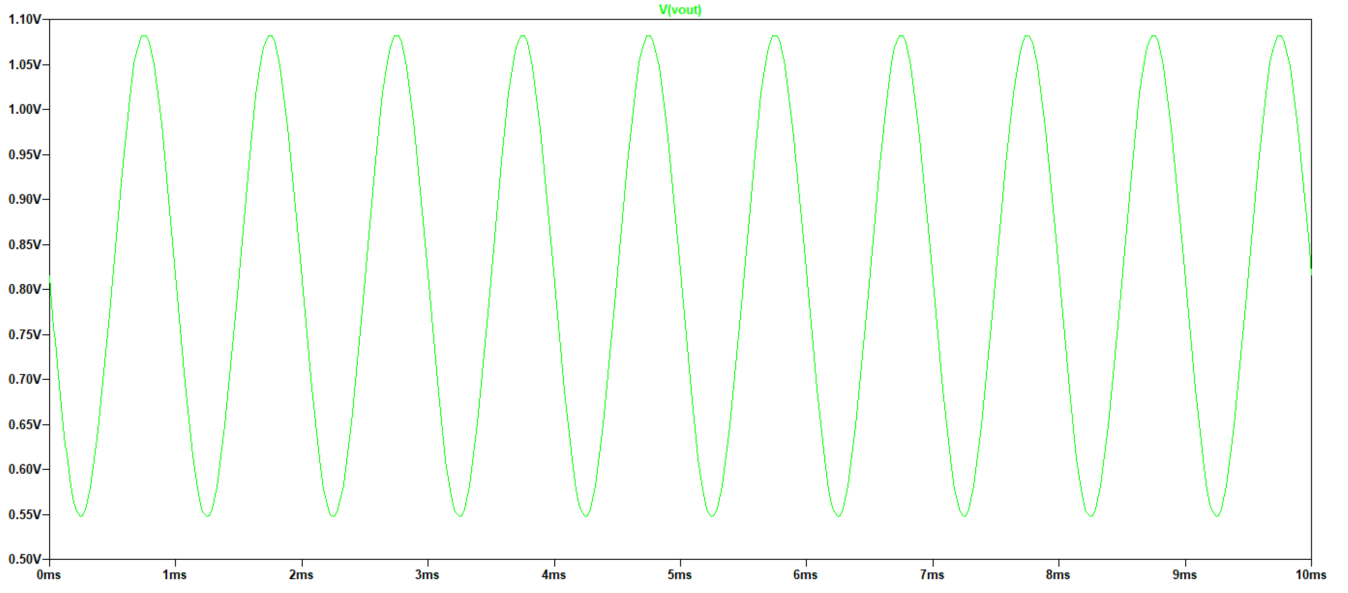
Minimum valoue of input voltage



Peak to peak voltage of output=269.3 mv

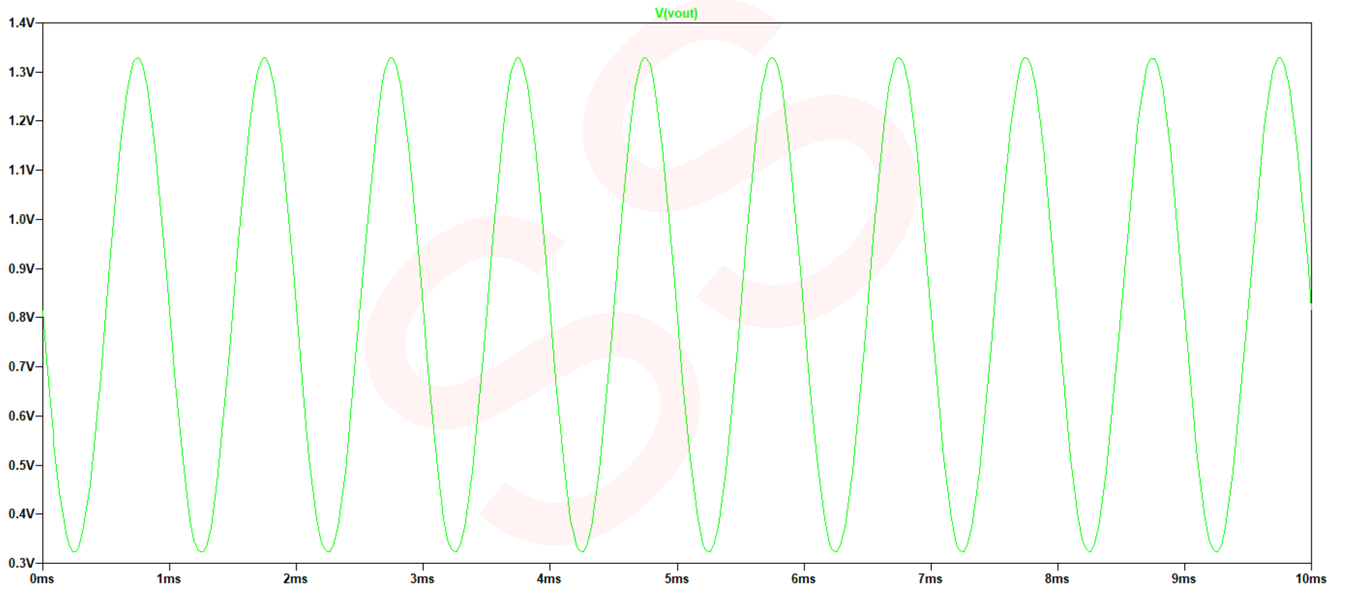
c) Repeat the transient analysis by increasing the input to 100 mVpp, 200 mVpp and 500 mVpp. Obtain the output and note down the peak-to-peak voltage. What do you observe and why?

For 100 mv peak to peak input:



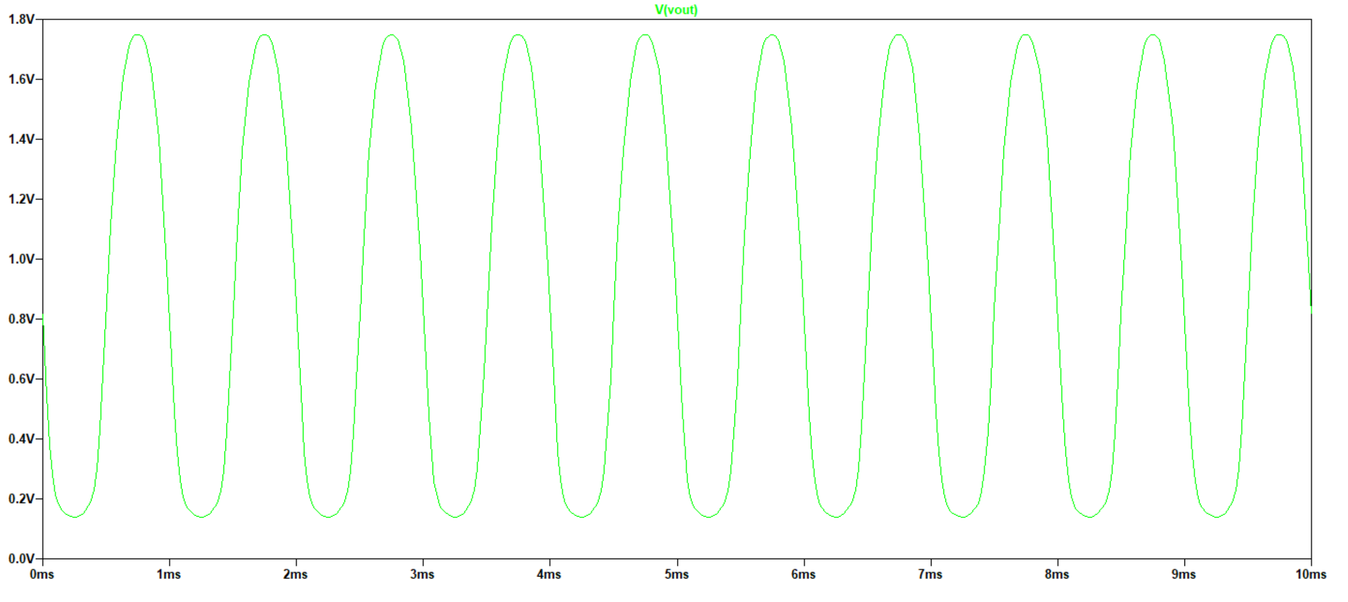
Output voltage peak to peak- 1.08 – 0.548 =0.532 volt, Vm=266mVolt

For 200 mv peak to peak input:



Output voltage peak to peak- 1.32 – 0.323 =0.997 v , Vm=498.5 mV

For 500 mv peak to peak input :



Output voltage peak to peak- 1.74 – 0.1398 =1.6 volt, Vm =800 mv

Observation –

we increase the amplitude of sinusoidal signal

1)The peak to peak output increases.

2)Minimum value decreases

3)maximum value increases

The output begins to saturate at supply voltage because our output cannot go beyond supply voltage 1.8 volt.

(d) Find the 1-dB compression point of the designed amplifier by performing total harmonic distortion (THD) analysis.

Fundamental component= $a_1V_m + \frac{3}{4}a_3V_m^3$

Third harmonic component= $\frac{1}{4}a_3V_m^3$

SPICE Error Log: C:\Users\DELL\AppData\Local\LTspice\Draft7.log

```
Circuit: * C:\Users\DELL\AppData\Local\LTspice\Draft7.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
N-Period=1
Fourier components of V(vout)
DC component:0.814934

Harmonic        Frequency       Fourier         Normalized
 Number          [Hz]           Component        Component
    1           1.000e+3        1.326e-1         1.000e+0
    2           2.000e+3        1.018e-4         7.672e-4
    3           3.000e+3        2.448e-3         1.846e-2
    4           4.000e+3        7.326e-5         5.523e-4
    5           5.000e+3        3.660e-4         2.759e-3
    6           6.000e+3        5.700e-5         4.297e-4
    7           7.000e+3        1.461e-4         1.101e-3
    8           8.000e+3        3.959e-5         2.984e-4
    9           9.000e+3        2.865e-4         2.160e-3
   10           1.000e+4        2.497e-5         1.882e-4
Partial Harmonic Distortion: 1.884950%
Total Harmonic Distortion:   1.921216%
```

Fundamental component= $a_1V_m + \frac{3}{4}a_3V_m^3$ =132.6m A

Third harmonic component=$\frac{1}{4}a_3V_m^3$ = 2.448 mA

1-dB compression point= $\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$

V_m=25mv

By calculating I get - a_3=626.68 , a_1=5.01

1-dB compression point $=\sqrt{[0.145 * 5.01]/626.68}$ = 0.034

2) Now the gain of the CS amplifier is required to be increased three folds without changing the main transistor and power supply. Retain the input and output DC voltages in the first CS amplifier. How will you modify the design? You are free to change the resistor, add any transistor and/or current source. Perform all the analysis mentioned in the first problem statement (above).

Gain obtained in first CS amplifier = 5.4

Now three times = 5.4×3
= 16.2

$$\left(\frac{V_o}{V_{in}}\right) = A_v = g_m (R_D \| r_o)$$

$$g_m (R_D \| r_o) = 16.2$$

$$2.35\times10^{-4}\,\frac{(R_D \times 117.785k)}{R_D + 117.785k} = 16.2$$

$$\frac{R_D \times 117.785k}{R_D + 117.785k} = \frac{16.2}{2.35\times10^{-4}}$$

$$R_D + 117.785k = 1.7 R_D$$

$$0.7 R_D = 117.785\ k\Omega$$

$$R_D = 168.26\ k\Omega$$

Drain current in previous amplifier = 34 μA , $V_{out} = 0.814V$

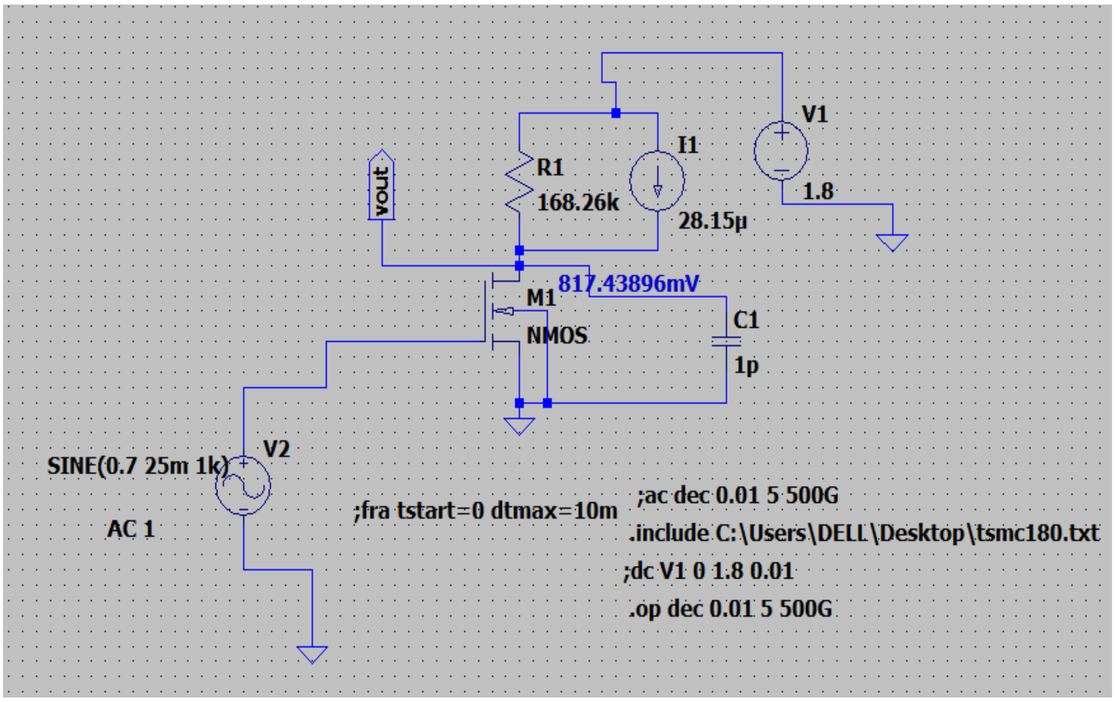
$$\therefore\ 34\mu A = \frac{1.8 - 0.814}{168.26k} + I$$

$$34\mu A = 5.85\mu A + I$$

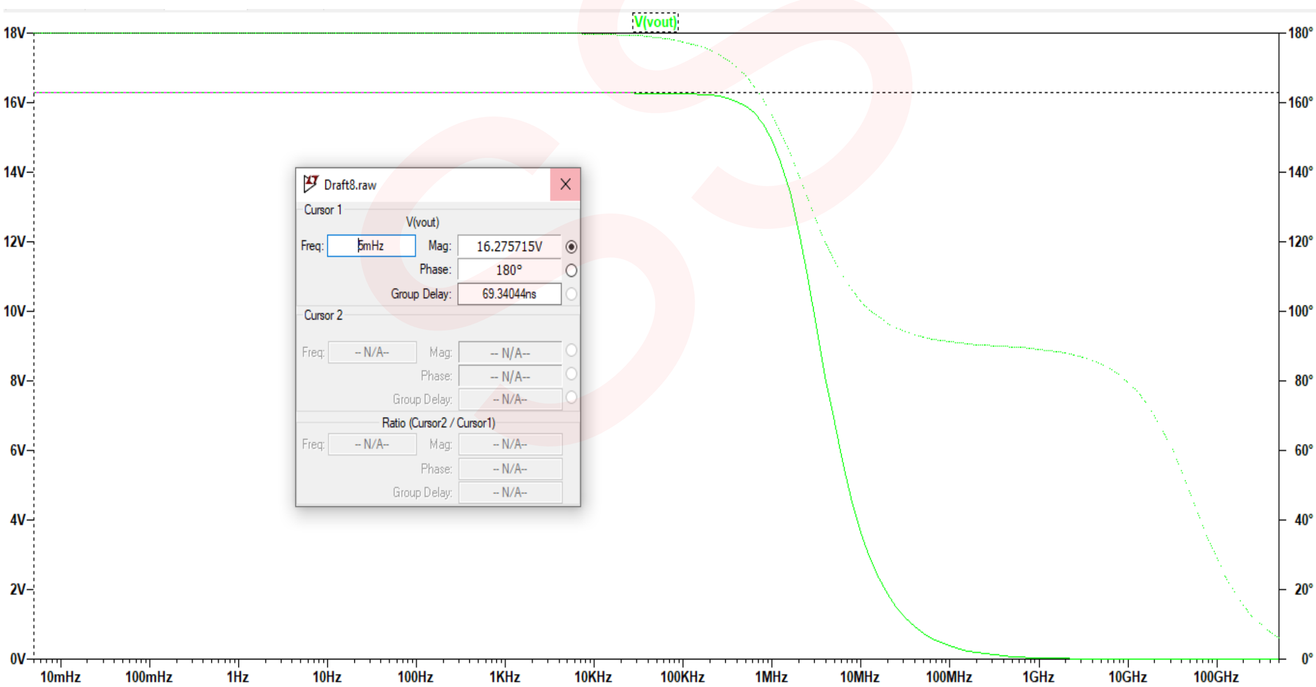
$$I = 28.15\mu$$

The drain current was 34μA and voltage as 0.814 Volt.
We get new drain resistor as 168.26 Kohm for 3 times gain (5.4).
By above calculation based on 3 times gain as 16.2 we get addition current of 28.15 μA
So we put current source as 28.15μA parallel to drain resistor 168.26 K ohm

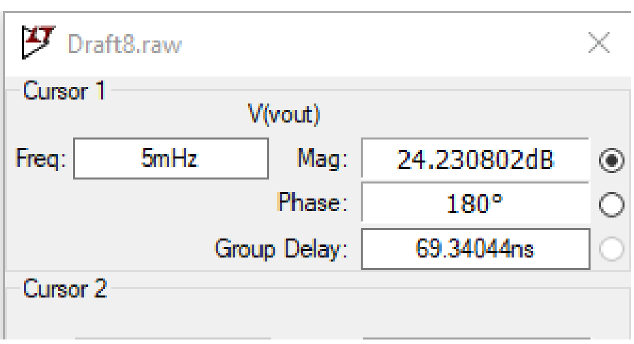
The circuit with 28.15μA current source parallel to drain resistance is below.



a) Frequency response



We can see in simulation also that our gain is 3 times that of previous gain which is 16.275



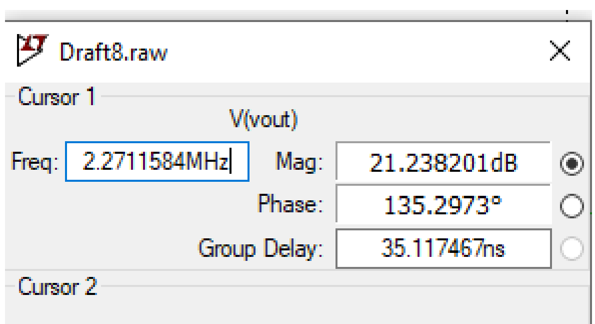


Fig 4 **For bandwidth (Fig 5)**

In db we get 20 log 16.2= 24.2dB

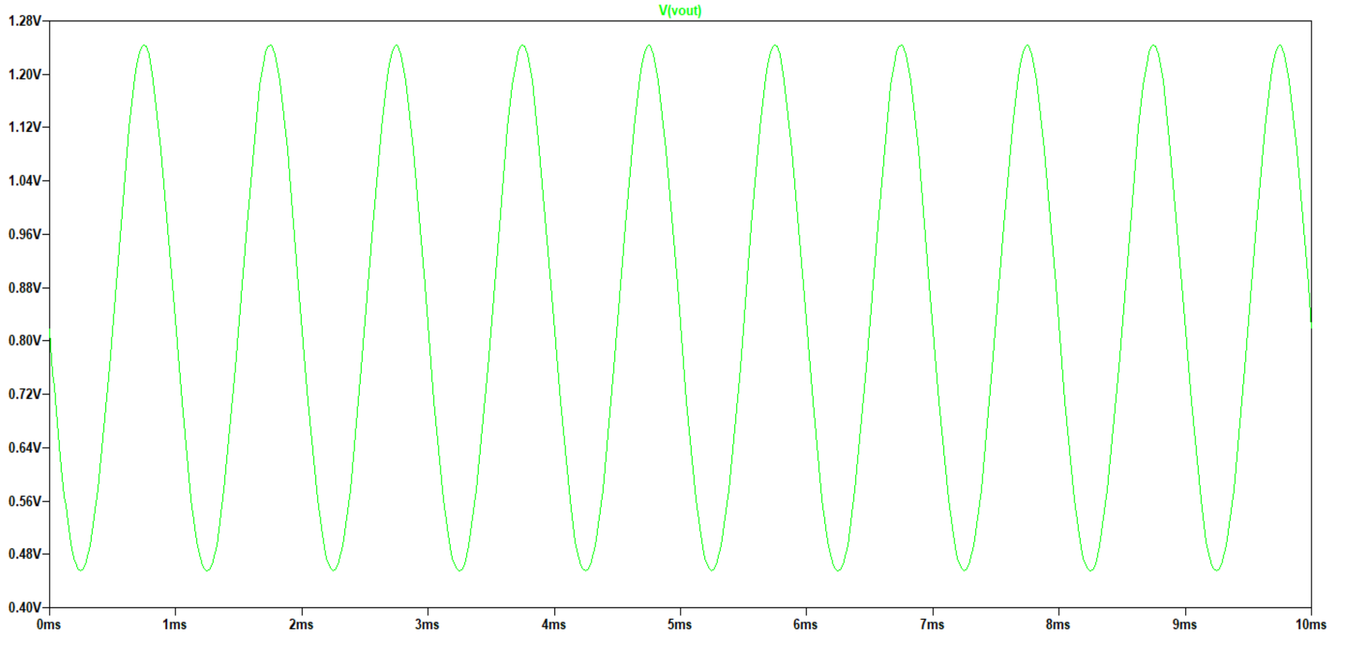
In dB-

For bandwidth=24.23 dB -3 dB =21.23dB For this see the frequency.

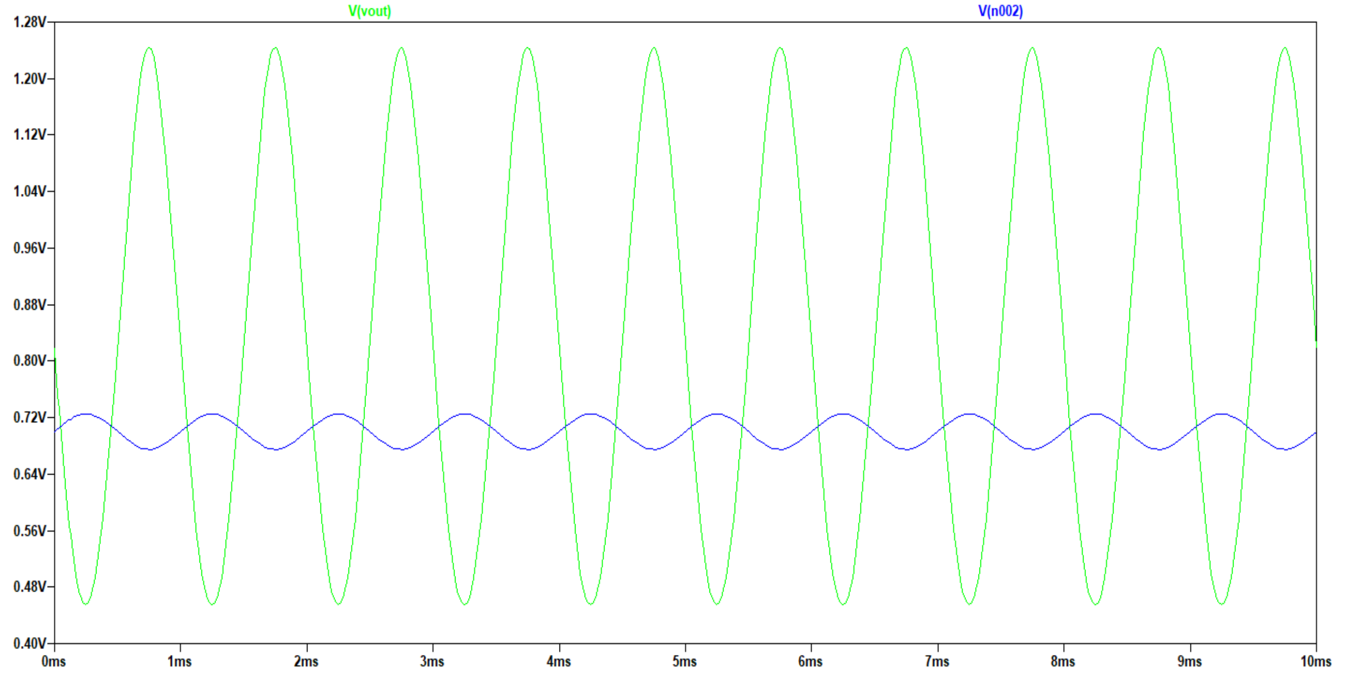
Tabulation-

Parameter	Calculated	Simulation
Gain	16.2	16.275 above
Gain in dB	24.19dB	24.23 dB (Fig 4)
Bandwidth	2.29 MHz	2.271 MHz (Fig 5)

b) Obtain the output voltage-



Peak to peak= 1.243 v- 0.455 v= 0.788 volt



Vm(output)=[0.788/2] = 0.394 volt

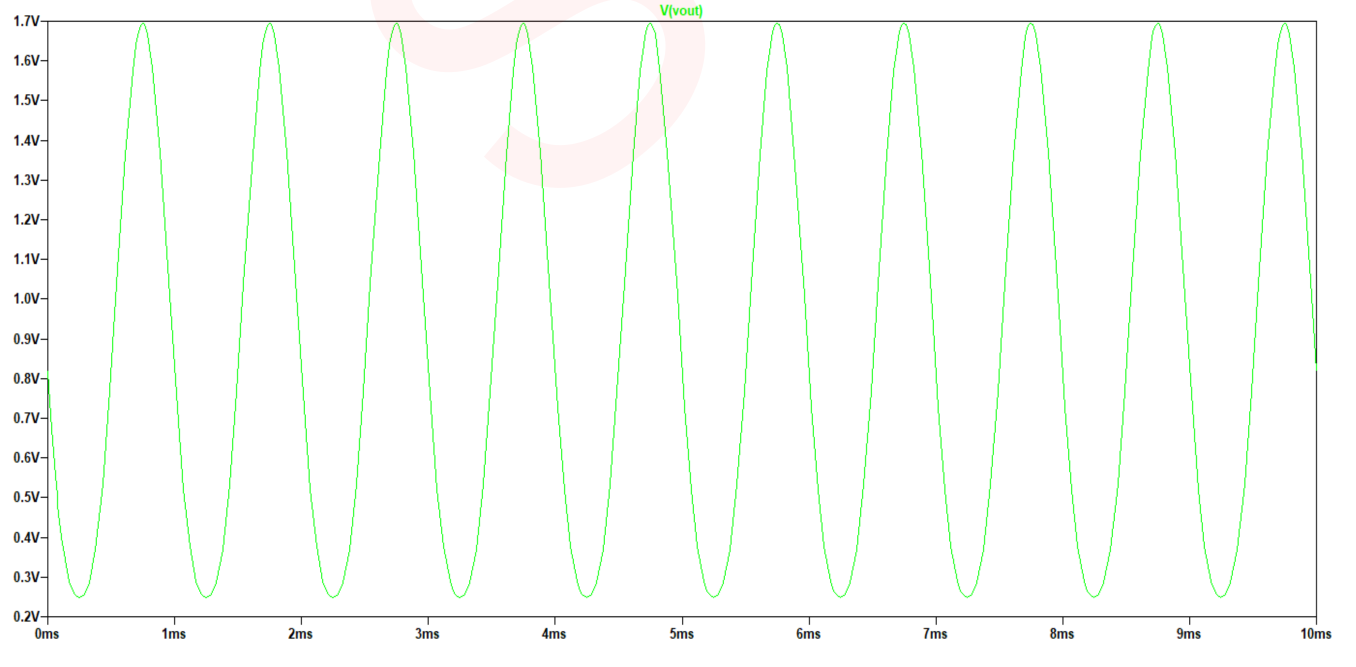
Vm(input)=[724mv-675mv]/2 =0.0499/2=0.02495volt

Gain= 0.394/0.02495=15.8

20log15.8= 24dB

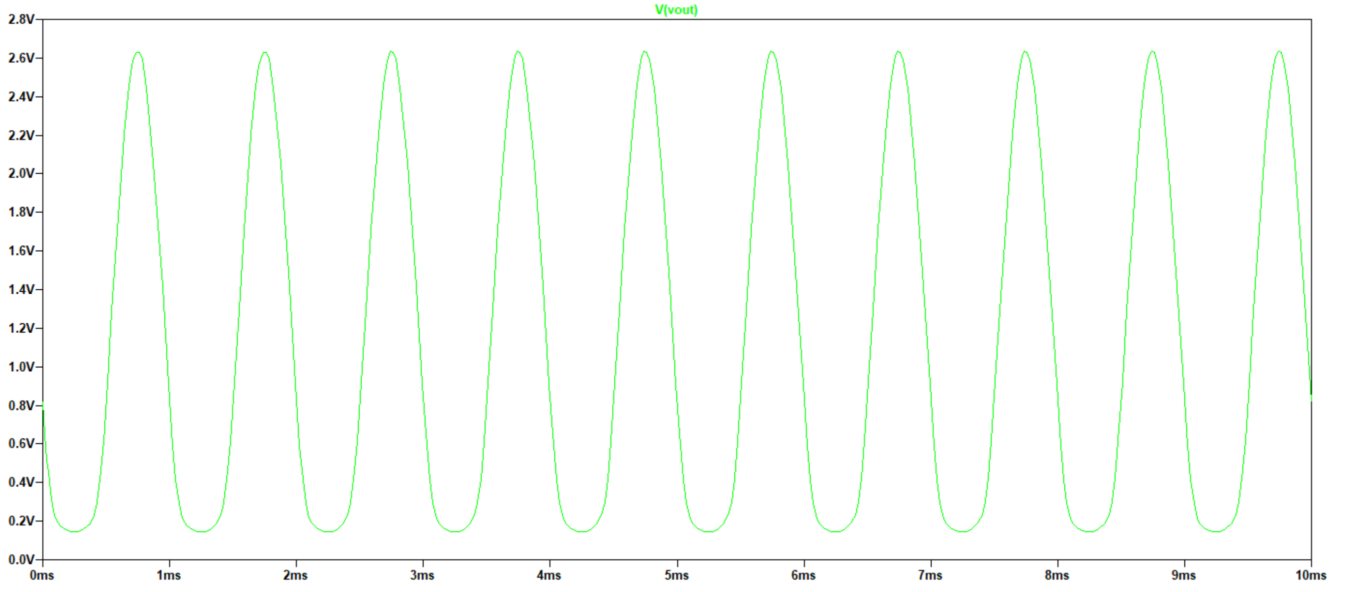
c) Repeat for 100 mVpp, 200 mVpp and 500 mVpp.

for 100 mv peak to peak



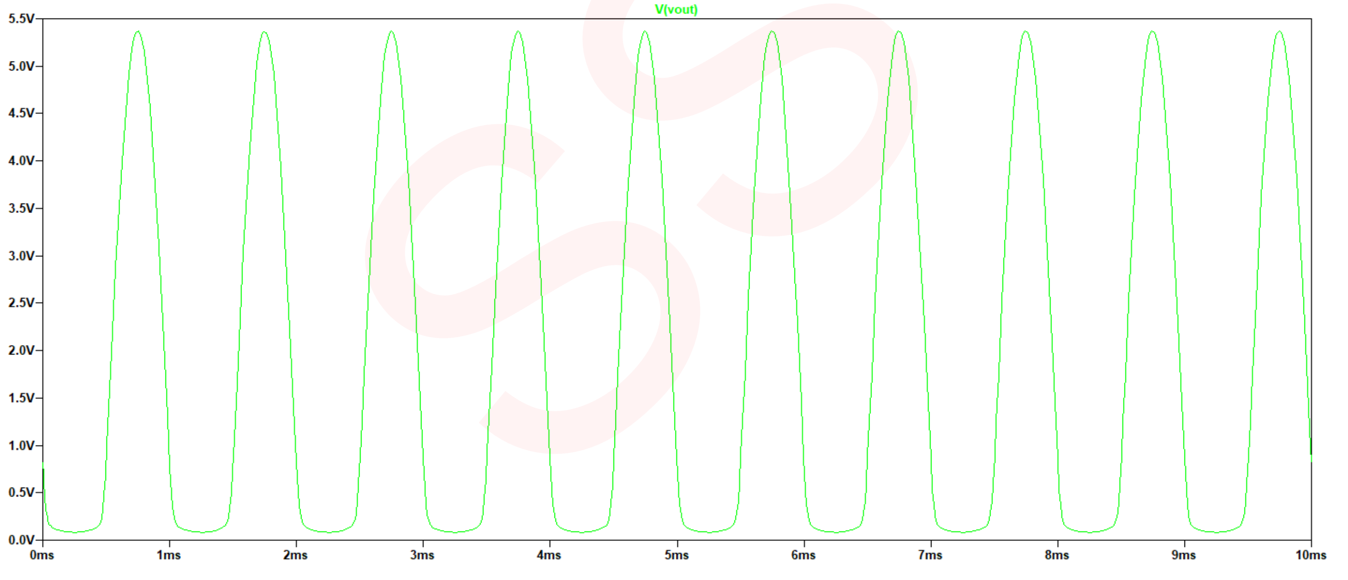
1.69-0.249=1.441v

For 200mv peak to peak



2.63-0.145=2.631 volt

For 500mv peak to peak-



5.36 v-84.26mv = 5.285 volt

d) 1 –dB Gain compression

```
Circuit: * C:\Users\DELL\AppData\Local\LTspice\Draft8.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
N-Period=1
Fourier components of V(vout)
DC component:0.834565

Harmonic      Frequency      Fourier       Normalized
 Number         [Hz]        Component      Component
    1        1.000e+3       3.882e-1       1.000e+0
    2        2.000e+3       1.352e-2       3.482e-2
    3        3.000e+3       6.726e-3       1.732e-2
    4        4.000e+3       9.478e-4       2.441e-3
    5        5.000e+3       4.295e-4       1.106e-3
    6        6.000e+3       4.186e-4       1.078e-3
    7        7.000e+3       3.471e-4       8.939e-4
    8        8.000e+3       1.686e-4       4.343e-4
    9        9.000e+3       6.670e-4       1.718e-3
   10        1.000e+4       1.320e-4       3.399e-4
Partial Harmonic Distortion: 3.905394%
Total Harmonic Distortion:   3.920800%
```

Fundamental component= $a_1V_m + \frac{3}{4}a_3V_m^3$ =3.882 x 10^{-1} =0 .3882

Third harmonic component=$\frac{1}{4}a_3V_m^3$ = 6.726 x 10^{-3}

a_3=1721.85

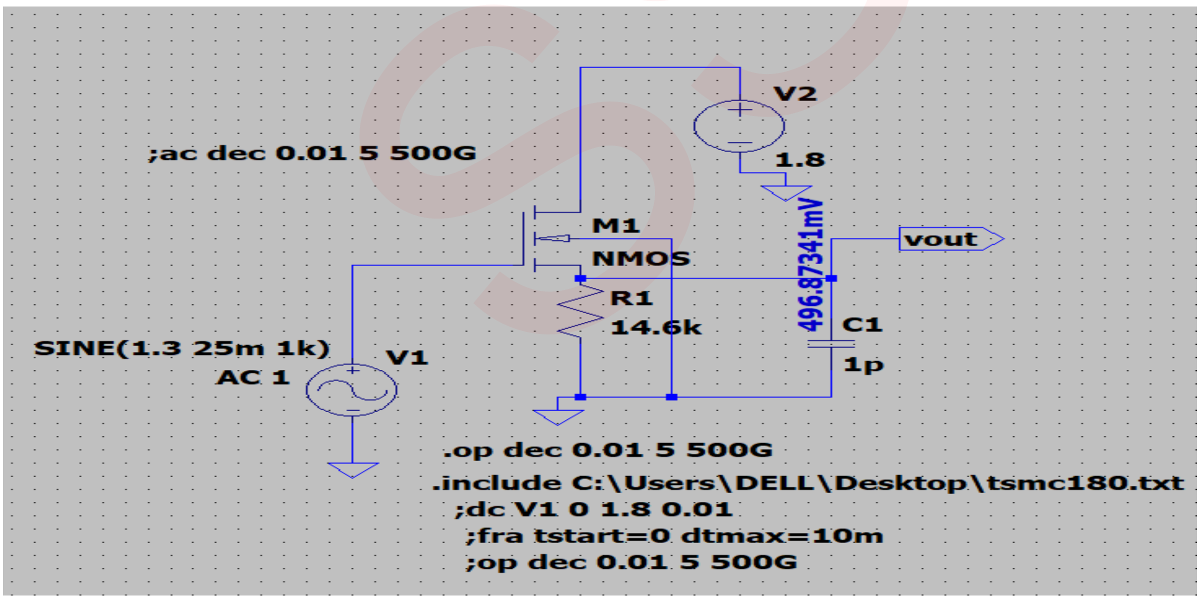
a_1=14.72

1-dB compression point= $\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$

1-dB compression point = 0.035

3) Realize a NMOS CD amplifier using the same transistor designed (sized) in problem 1 above. Keep the same DC bias current. Set the input DC bias voltage to 1.3 V. Perform the following experiments on the designed amplifier.

= Earlier our DC bias current was 34µA so by calculating we get the source resistance as 14.6 Kohm




```
Circuit: * C:\Users\DELL\AppData\Local\LTspice\Draft9.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM3 MOSFETS ---
Name:          m1
Model:        nmos
Id:          3.40e-05
Vgs:         8.03e-01
Vds:         1.30e+00
Vbs:        -4.97e-01
Vth:         5.94e-01
Vdsat:       1.44e-01
Gm:          2.44e-04
Gds:         7.89e-06
Gmb          5.49e-05
```

Calculation of gain for CD amplifier theoretically is shown below-

In CD amplifier body and source are not connected to each other so we have to take Gmb also in consideration.

Total =Gmb + Gds

$=5.49 \times 10^{-5} + 7.89 \times 10^{-6} = 62.79 \times 10^{-6}$

gm= 2.44×10^{-4}

Here:-

$$r_o = \frac{1}{G_{mb}+G_{ds}} \qquad g_m = 2.44\times10^{-4}$$

$$= \frac{1}{62.79\times10^{-6}}$$

$$= 15.92\ k\Omega$$

$$R_D \| r_o = 14.6k \| 15.92k$$

$$= \frac{14.6k\times15.92k}{14.6k+15.92k}$$

$$= 7.61\ k\Omega$$

$$A_v = \frac{g_m(R_D\|r_o)}{1+g_m(R_D\|r_o)}$$

$$= \frac{2.44\times10^{-4}\times7.61\times10^{3}}{1+2.44\times10^{-4}\times7.61\times10^{3}}$$

$$= \frac{1.856}{1+1.856} = 0.650$$

(a) Frequency response of the amplifier. Find the small signal DC gain and bandwidth of the amplifier. Compare with the values calculated using the small signal parameters obtained from the DC operating point simulation.

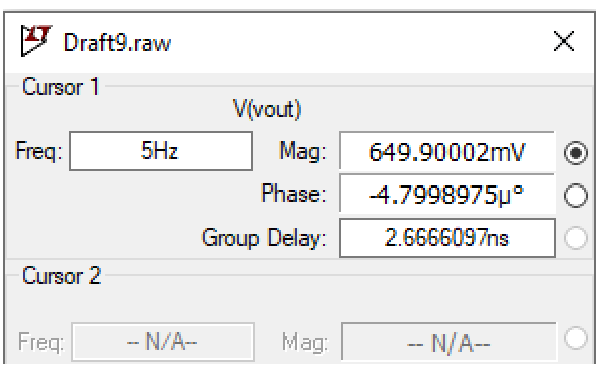


Fig 6

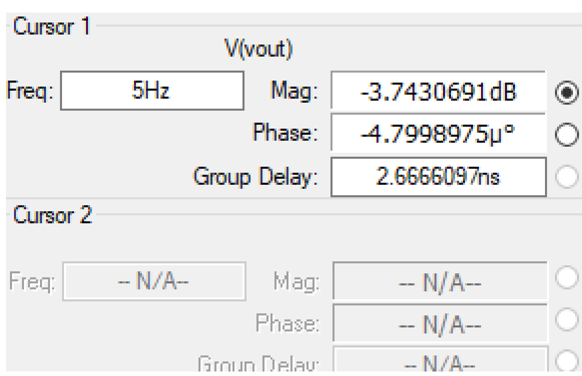
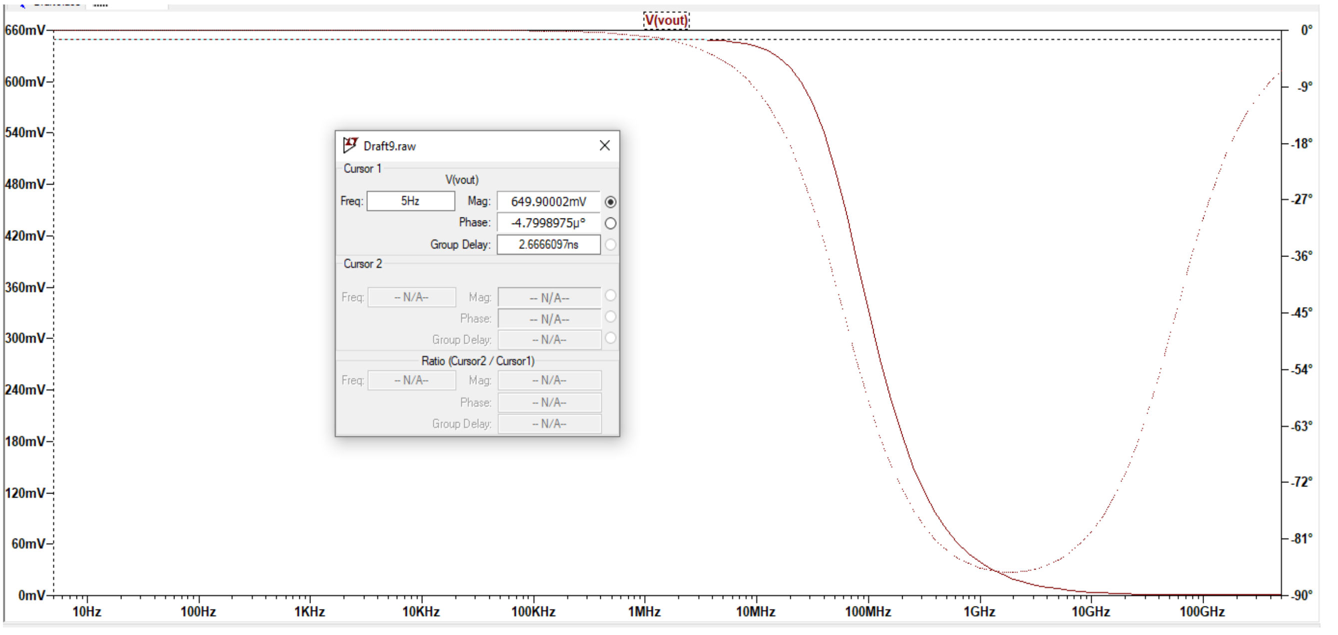
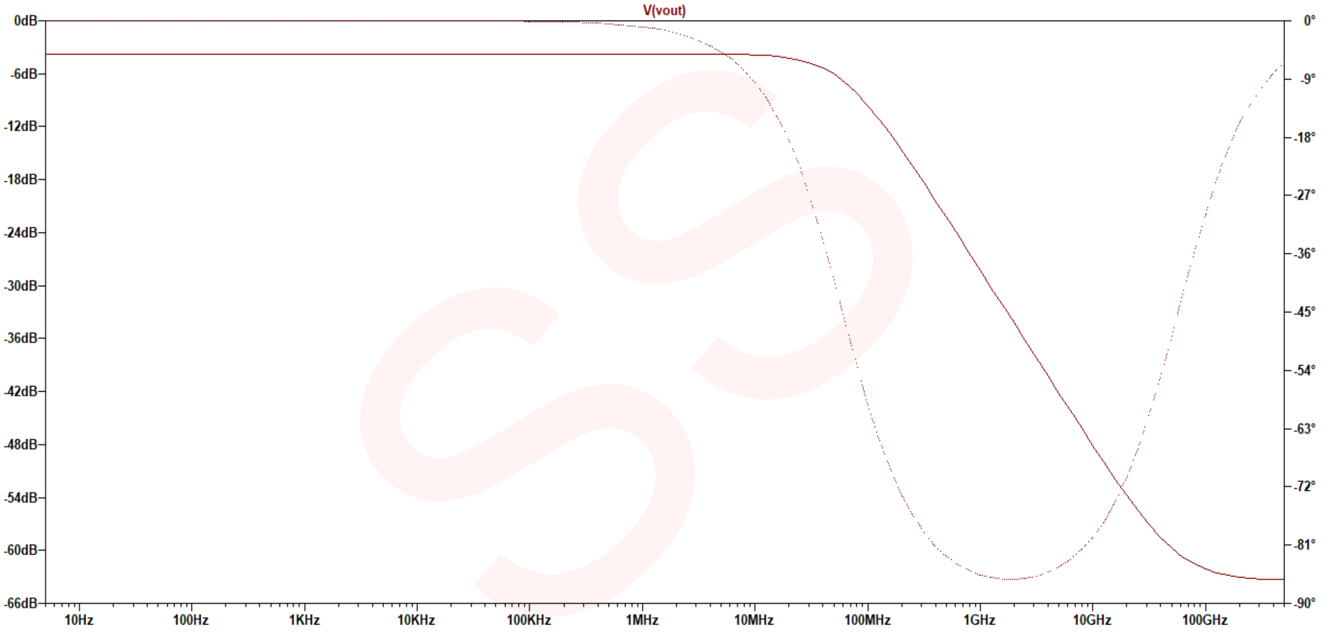


Fig 7



The gain is coming out to be 0.649 which is same as 0.650



For bandwidth:

Av=20log (gain)

=20log (0.650) =-3.741 Decibel

For Bandwidth: (Simulation)

Gain in Db – 3dB= -3.741 – 3= -6.741 dB

For 11.74 decibel the frequency is 59.14 MHz

Bandwidth= $f_1 - f_2$ = 59.14-0= 59.14 MHz

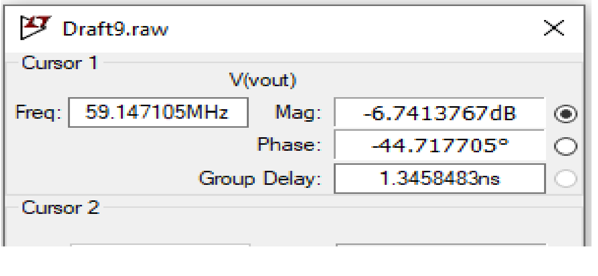
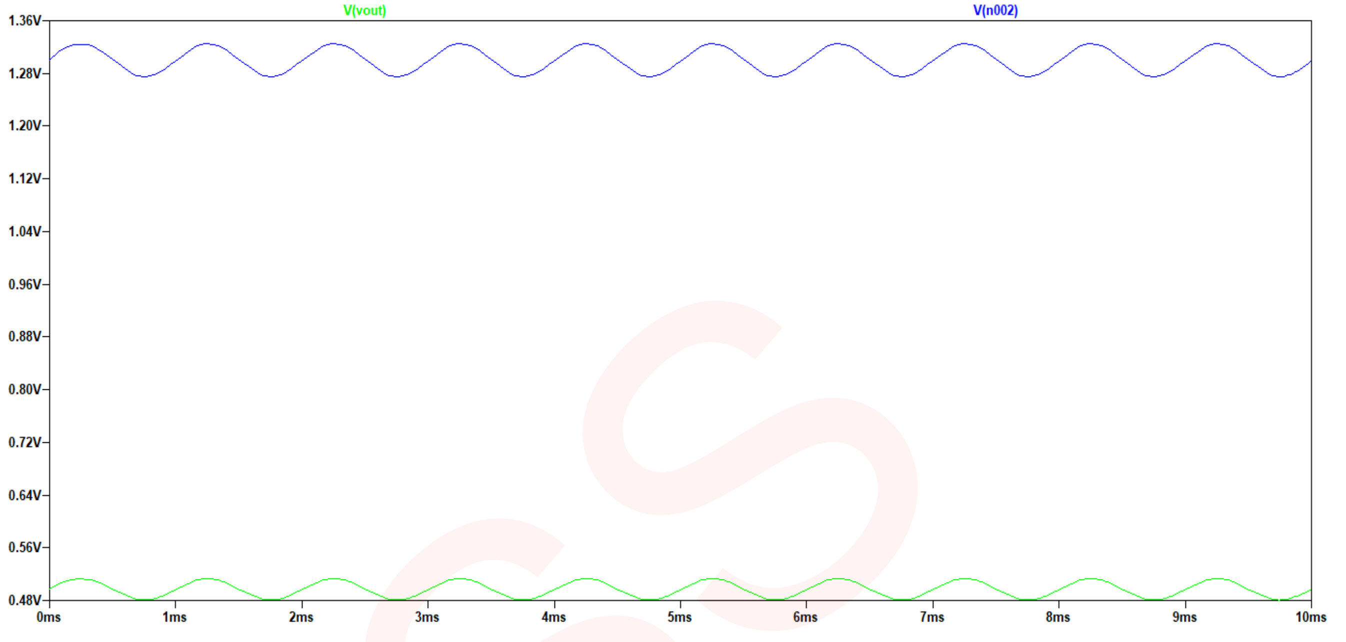


Fig 8

Tabulation-

Parameter	Calculated	Simulation
Gain	0.650	0.649 (Fig 6)
Gain in dB	-3.741 dB	-3.743 dB (Fig 7)
Bandwidth	59.14 MHz	59.14 MHz (Fig 8)

b) Excite the amplifier with a 50 mV peak-to-peak sine wave of frequency 1 kHz riding on the input DC bias voltage and obtain the output. What is the peak-to-peak voltage of the output?



Blue one is for input and other one is for output.

Peak to peak output= 31.8 millivolt (Fig 9)

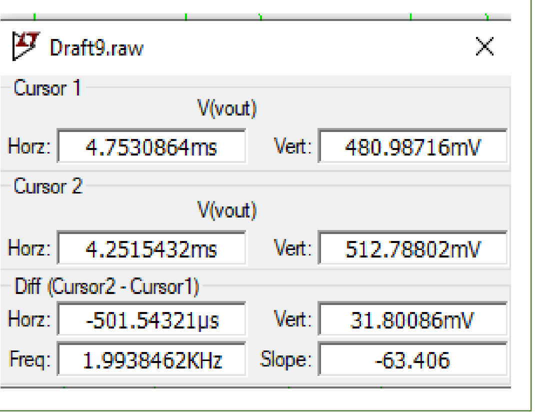
Vm (out)= 15.9 millivolt

Vm (in)=25 millivolt

Gain=$\frac{V(out)}{V(in)} = \frac{15.9\ mV}{25\ mV} = 0.636$

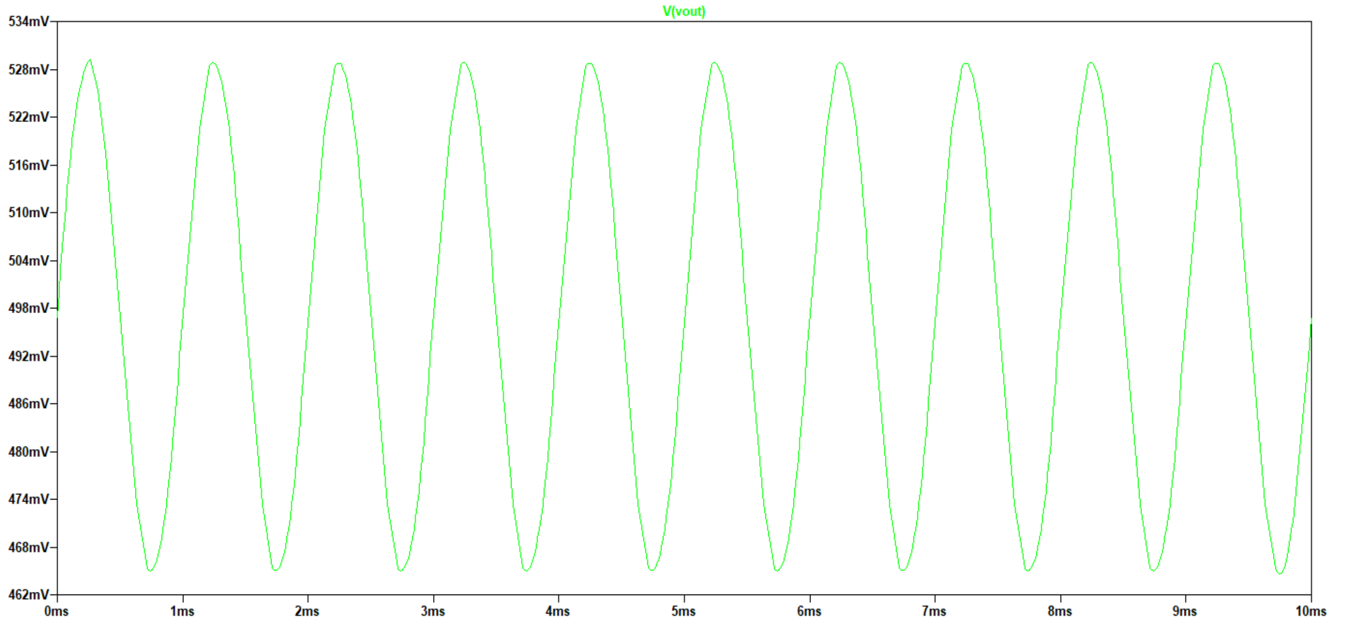
The gain we can clearly see is same as calculated theoretically as well as frequency response.

Fig 9



C) Repeat the transient analysis by increasing the input to 100 mVpp, 200 mVpp and 500 mVpp. Obtain the output and note down the peak-to-peak voltage. What do you observe and why? How does the waveform compare with that of the CS amplifier? Comment on it.

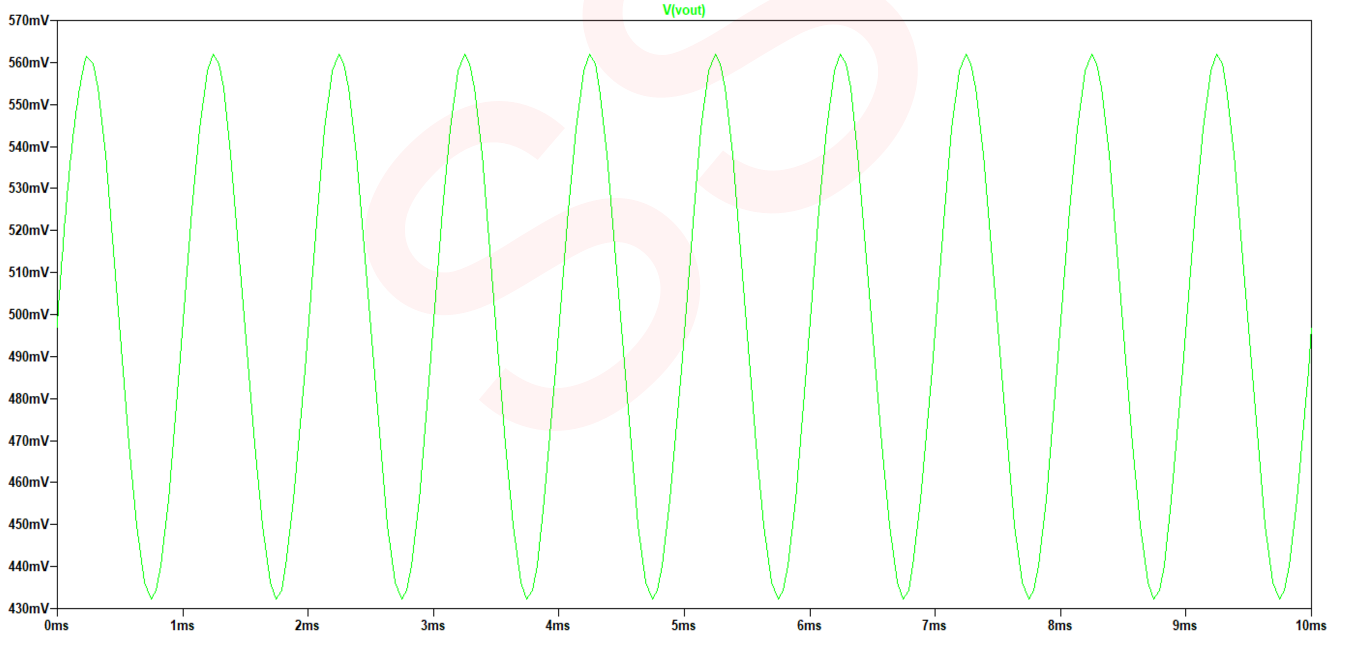
For 100mV peak to peak input:



Peak to peak output voltage= 63.81 millivolt

Output voltage=31.905 millivolt

For 200mV peak to peak input:



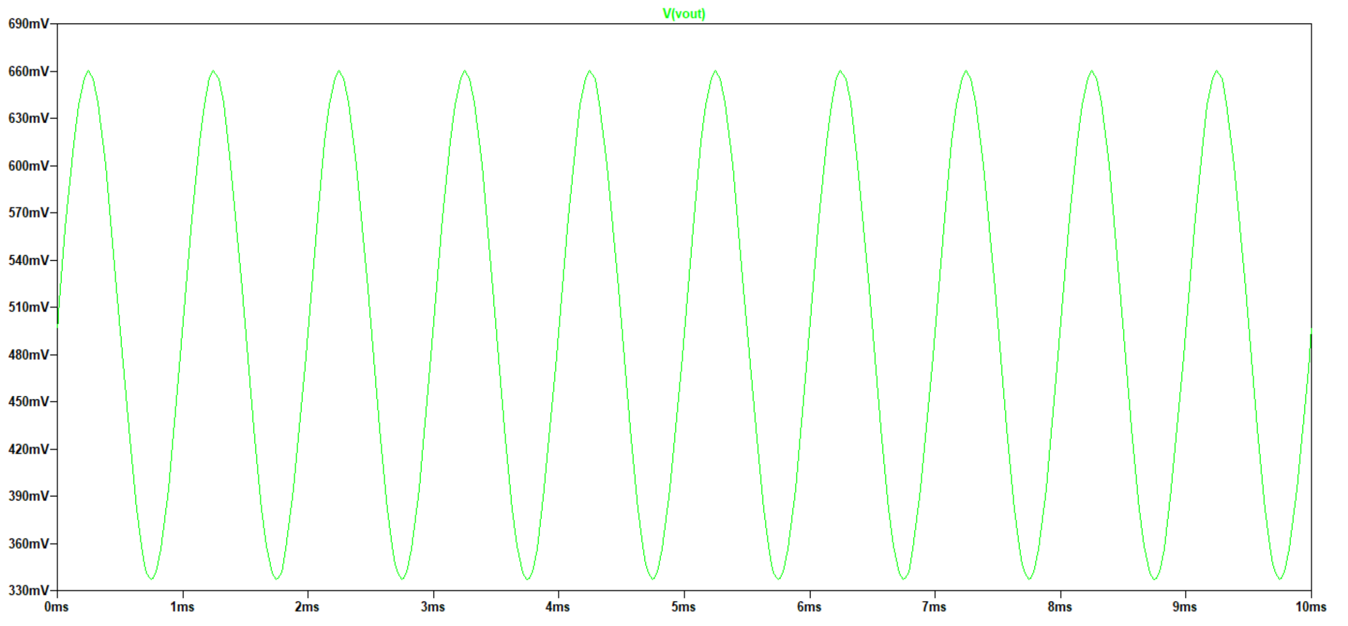
Peak to peak output voltage= 128.81 millivolt

Output voltage=64.4 millivolt

For 500 mV peak to peak input:

Peak to peak output voltage= 322.22 millivolt

Output voltage=161.11 millivolt



Obsevation-

d) Find the 1-dB compression point of the amplifier by performing total harmonic distortion (THD) analysis. How does it compare with the CS amplifier? Comment on it.

SPICE Error Log: C:\Users\DELL\AppData\Local\LTspice\Draft9.log

```
Circuit: * C:\Users\DELL\AppData\Local\LTspice\Draft9.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.
N-Period=1
Fourier components of V(vout)
DC component:0.496953

Harmonic          Frequency        Fourier          Normalized
 Number             [Hz]           Component         Component
    1             1.000e+3         1.579e-2          1.000e+0
    2             2.000e+3         1.935e-4          1.226e-2
    3             3.000e+3         4.435e-4          2.809e-2
    4             4.000e+3         1.478e-4          9.361e-3
    5             5.000e+3         2.554e-4          1.618e-2
    6             6.000e+3         5.305e-5          3.360e-3
    7             7.000e+3         6.240e-5          3.953e-3
    8             8.000e+3         4.194e-5          2.657e-3
    9             9.000e+3         4.489e-5          2.843e-3
   10             1.000e+4         1.716e-5          1.087e-3
Partial Harmonic Distortion: 3.649871%
Total Harmonic Distortion:   3.677104%
```

Fundamental component= $a_1V_m + \frac{3}{4}a_3V_m^3 \quad =1.579 \times 10^{-2}$

Third harmonic component=$\frac{1}{4}a_3V_m^3 = 4.435 \times 10^{-4}$

a_3=113.536

A1=0.5784

1-dB compression point= $\sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}$

1-dB Compression point= 5.335