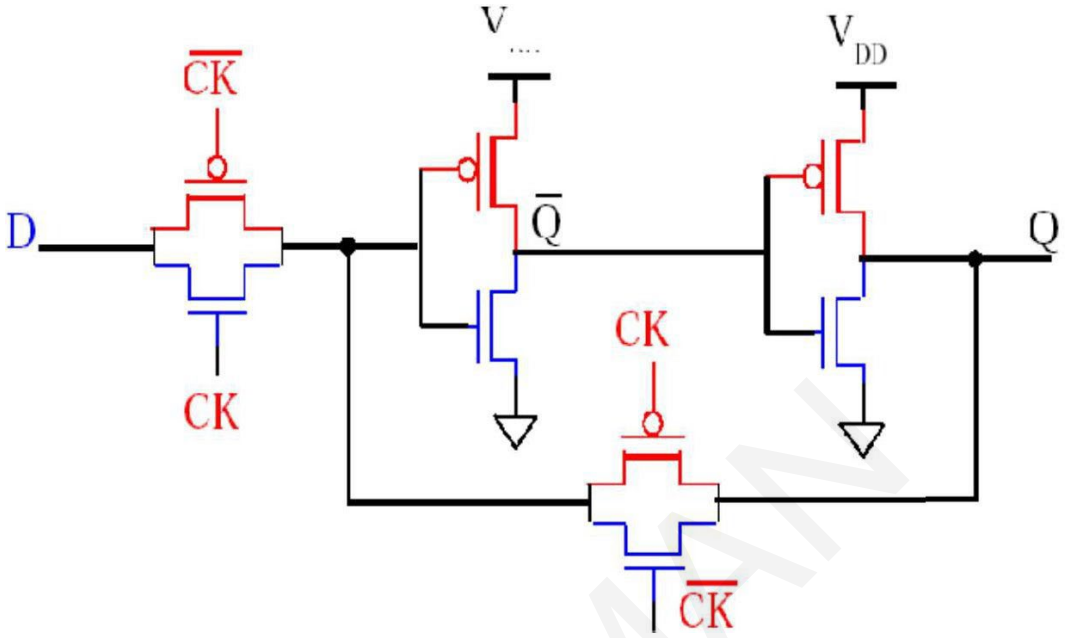
MAGIC LAYOUT BY S.SUMAN

Q3. Draw the optimized layout of the given circuit using magic. Use 0.25µm Technology and Vdd = 5V. Build register by appropriately modifying the given circuit and cascading two of them. Finally calculate the following things after simulation of the extracted layout

i) Average clock to q delay

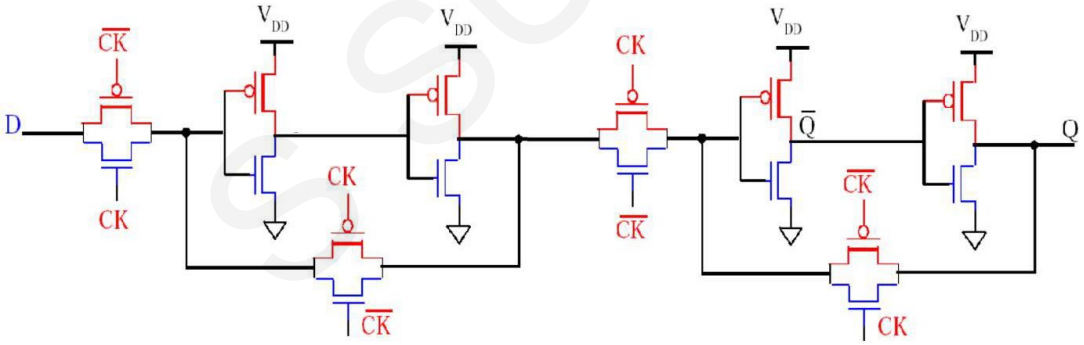
ii) Peak power consumption

iii) Total area occupied by the cell

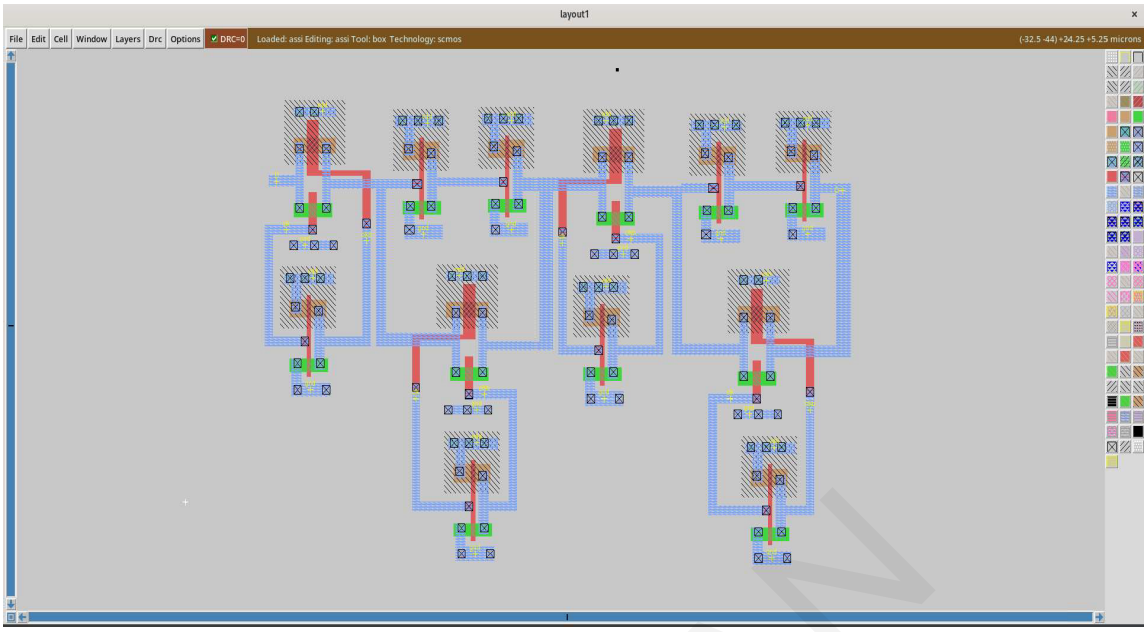


Ans:

Modified and Cascaded circuit will be as follows.



Layout of above circuit from Magic Software:
The layout is drawn on .25 um technology file.



IRSIM simulation-

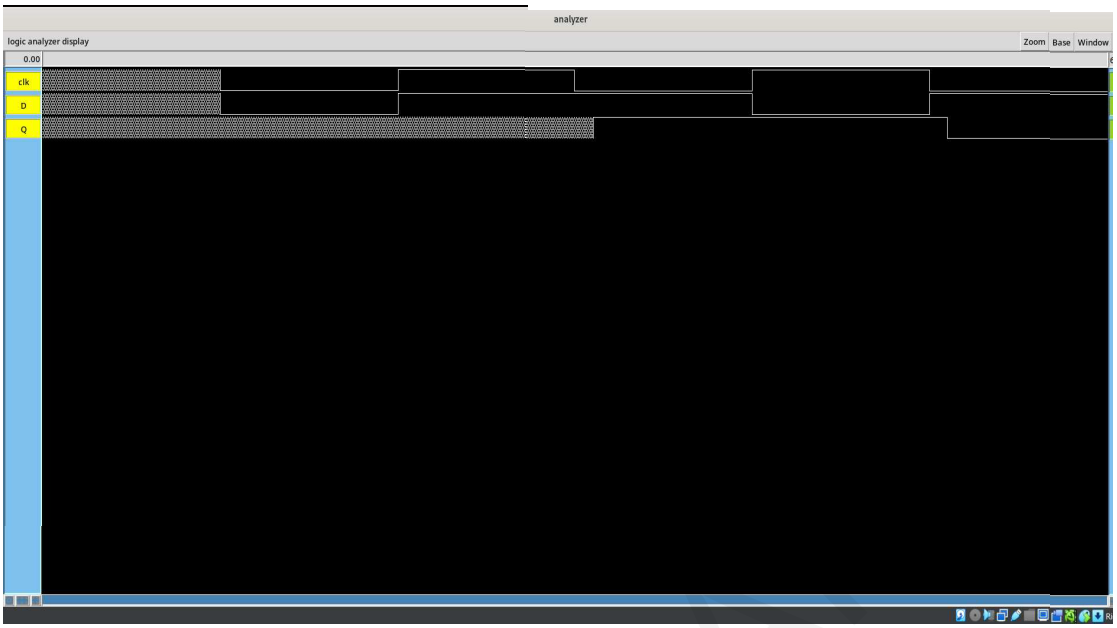
Output of irsim

Default step size in 10 ns .

Time(ns)	clk	D	Q
10	x	x	x
20	0	0	x
30	1	1	x
40	0	1	1
50	1	0	1
60	0	1	0

Analyzer output: -

We analyze our simulation from analyzer so that we can check whether our layout is giving desired value.



Above is the simulation result which shows the desired output.

On the low phase of the clock, the master stage is *transparent,* and the *D* input is passed to the master stage output, *QM*. During this period, the slave stage is in the *hold* mode, keeping its previous value using feedback. On the rising edge of the clock, the master slave stops sampling the input, and the slave stage starts sampling. During the high phase of the clock, the slave stage samples the output of the master stage (*QM*), while the master stage remains in a *hold* mode.

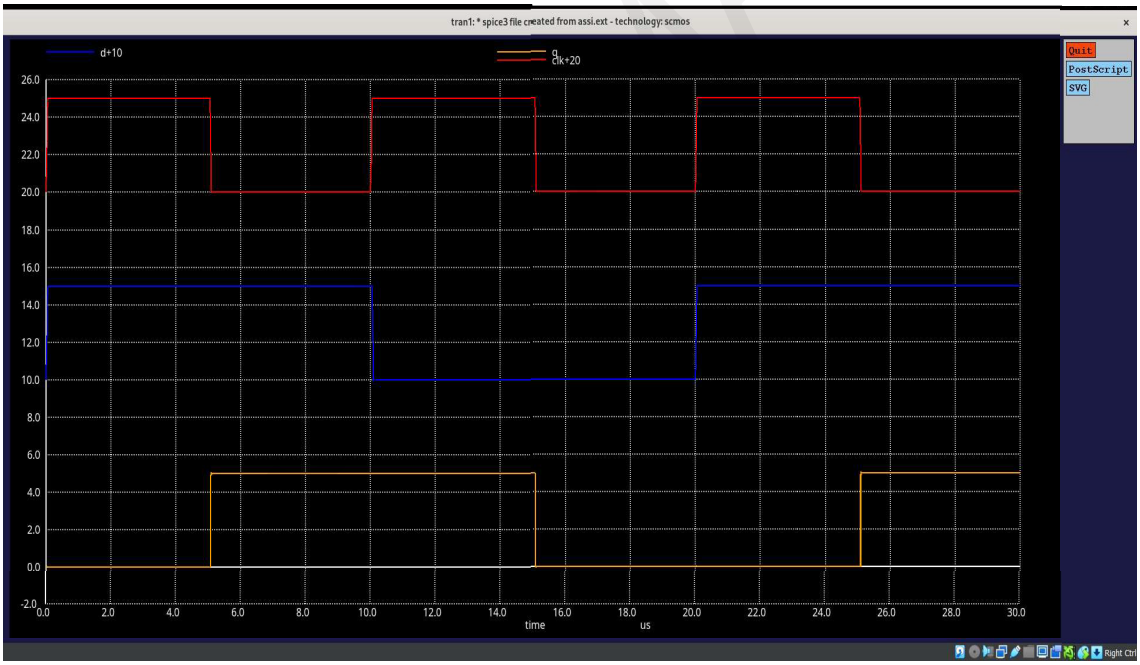
Ngspice output be as follows:

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
clkb                                         5
clk                                          0
q                                  5.63869e-09
d                                            0
vdd                                          5
v_clk#branch                                 0
v_in#branch                        5.01001e-12
v_dd#branch                       -1.79829e-10


No. of Data Rows : 202
Warning: Missing charsets in String to FontSet conversion
tplh                =  2.691258e-10 targ=  5.075269e-06 trig=  5.075000e-06
tphl                =  -5.898496e-09 targ=  1.506910e-05 trig=  1.507500e-05
clk2q_delay = 3.083811e-09
energy              =  5.10990e-10 from=  4.00000e-06 to=  2.40000e-05
power = 2.554950e-05
Error: no block to end.
Warning: ignoring previous error
```

Output waveform-



First one(RED) is Clock, second one (blue) is D input and Q output is third one.

For area we first select the layout and type box command in magic terminal window(tcl).

Observation:

Parameter	Value
Average clock to Q delay	3.08 ns
Peak power consumption	25.55 uW
Total area occupied by the cell	4106.125 um^2

Ngspice netlist

Let “assi.spice” file be as follows.

```
* SPICE3 file created from assi.ext - technology: scmos
.include ./t14y_tsmc_025_level3.txt
.option scale=0.25u

M1000 clkb clk gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1001 Q clk a_76_6# Gnd cmosn w=6 l=4
+  ad=48p pd=28u as=48p ps=28u
M1002 clkb clk gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1003 a_n174_2# clkb D vdd cmosp w=7 l=6
+  ad=63p pd=32u as=49p ps=28u
M1004 Q clkb a_76_6# vdd cmosp w=7 l=6
+  ad=63p pd=32u as=49p ps=28u
M1005 a_n112_n10# a_n174_2# vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1006 clkb clk vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1007 a_133_n6# a_76_6# gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1008 a_n86_n86# clkb a_n174_2# Gnd cmosn w=6 l=4
+  ad=48p pd=28u as=48p ps=28u
M1009 a_133_n6# a_76_6# vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1010 a_76_6# clkb a_n86_n86# Gnd cmosn w=6 l=4
+  ad=48p pd=28u as=48p ps=28u
M1011 Q a_133_n6# gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1012 clkb clk vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1013 clkb clk gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1014 a_n86_n86# a_n112_n10# gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1015 Q a_133_n6# vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1016 clkb clk gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
M1017 clkb clk vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1018 a_76_6# clk a_n86_n86# vdd cmosp w=7 l=6
+  ad=49p pd=28u as=63p ps=32u
M1019 a_n86_n86# a_n112_n10# vdd vdd cmosp w=8 l=2
+  ad=64p pd=32u as=72p ps=34u
M1020 a_n174_2# clk D Gnd cmosn w=6 l=4
+  ad=48p pd=28u as=48p ps=28u
M1021 a_n112_n10# a_n174_2# gnd Gnd cmosn w=6 l=2
+  ad=54p pd=30u as=54p ps=30u
```

```
M1022 a_n86_n86# clk a_n174_2# vdd cmosp w=7 l=6
+  ad=49p pd=28u as=63p ps=32u
M1023 clkb clk vdd vdd cmosp w=8 l=2
+ ad=64p pd=32u as=72p ps=34u
C0 vdd clk 2.331628f
C1 clkb vdd 2.045978f
*C2 gnd 0 5.78388f FLOATING
*C3 clk 0 14.45634f FLOATING
*C4 clkb 0 12.94498f FLOATING
*C5 Q 0 3.76741f FLOATING
*C6 a_76_6# 0 4.9698f FLOATING
*C7 a_n174_2# 0 4.96634f FLOATING
*C8 a_n86_n86# 0 7.01028f FLOATING
*C9 vdd 0 37.3745f FLOATING

v_dd VDD 0 5
v_in D 0 dc 2.5 pulse(0 5 0 0.05u 0.05u 10u 20u)
v_clk clk 0 dc 2.5 pulse(0 5 0 0.05u 0.05u 5u 10u)

.control
tran 0.5u 30u
**gave offset for differentiating all nets in single plot
plot clk+20 D+10 Q

** following cmd measures tplh and tphl delay between "clk" and "Q"
meas tran tplh trig clk val=2.5 fall=1 targ v(Q) val=2.5 rise=1
meas tran tphl trig clk val=2.5 fall=2 targ v(Q) val=2.5 fall=1
** following cmd calculates clock to Q delay and power
let clk2Q_delay = (tplh-tphl)*0.5
print clk2Q_delay
let p = 5*-v_dd#branch
meas tran energy integ p from=4u to=24u
let power = energy/20u
print power
end
.endc
**
.end
```

The code is extracted from layout and the t14y_tsmc_025_level3.txt file included in the code at the top. Now the code is written in the extracted spice code for the things to be calculated.
By default, extracted code comes as nfet and pfet but in our model file it is written cmosp and cmosn so replace all nfet and pfet with cmosn and cmosp respectively.

Conclusion :-

1) We learned to design D-Latch using magic layout design.
2) We learned how to test the working of layout design using irsim tool and learned how to test the design using ngspice and find out the time delay and power consumption.