NGSPICE

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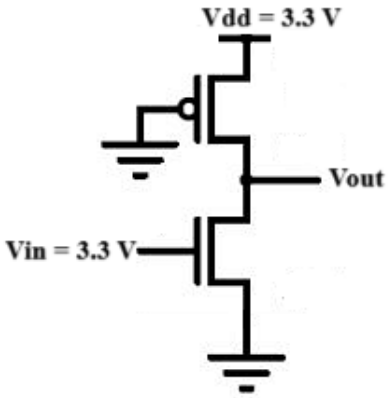
2. a) Simulate and plot the DC transfer characteristics of the Pseudo NMOS inverter with the following specifications. Use inverting device (pull-down) has L=0.8µm and W=1.2 µm., and V_{OL}< 0.4V for V_{in}=3.3V. What is the required value of W and L of load? transistor?

Supply voltage is V_{dd}=3.3 V

Circuit-



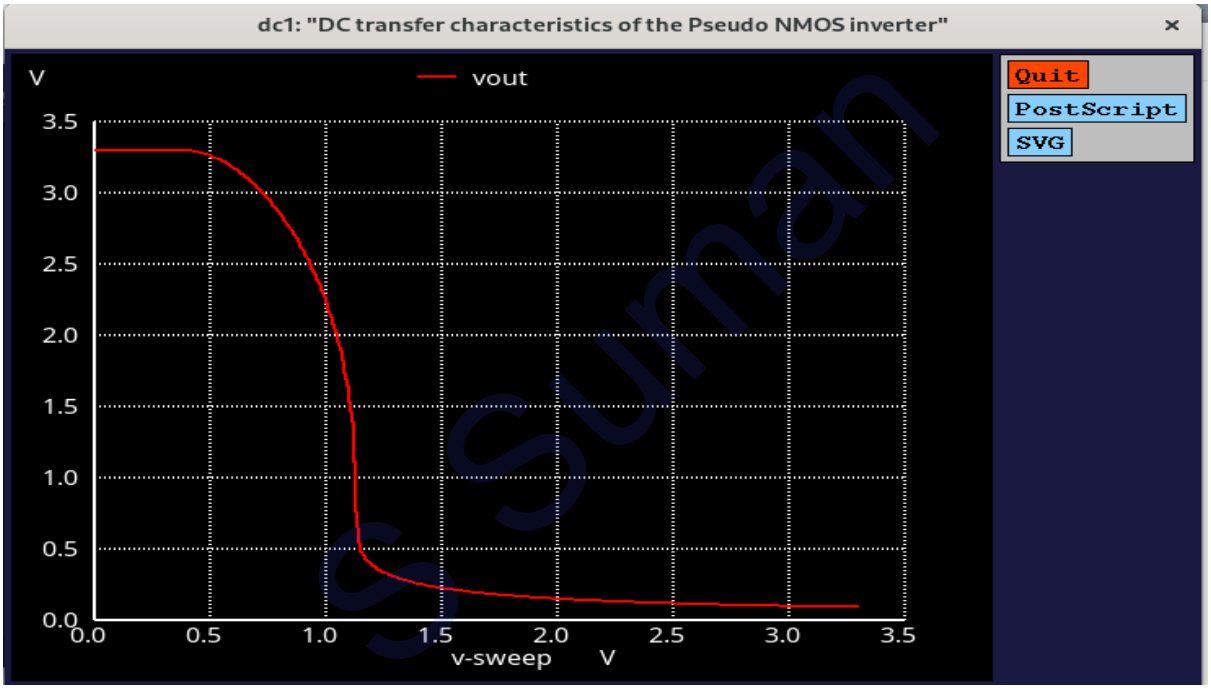
Netlist-

For width 0.5u

```
*Pseudo NMOS Inverter Design(Vol<0.4V)
 *including the 0.25 µm level 3 model file for simulation
.include ./t14y_tsmc_025_level3.txt
 *netlist description
m1 Vout Vin 0 0 cmosn l=0.8u w=1.2u
m2 Vout 0 Vdd Vdd cmosp l=0.8u w=0.5u
*DC excitations
V_in Vin 0 3.3
V_dd Vdd 0 3.3
.control
dc V_in 0 3.3 0.01
let d_Vout=deriv(Vout)
meas dc VOH find Vout when d_Vout=-1 fall=1
meas dc VOL find Vout when d_Vout=-1 rise=1
meas dc VIL find Vin when Vout=VOH
meas dc VIH find Vin when Vout=VOL

let NML=VIL-VOL
let NMH=VOH-VIH
print VOH VIH NMH
print VIL VOL NML
setplot
plot Vout title "DC transfer characteristics of the Pseudo NMOS inverter"
plot d_Vout 0-1 title "locating slope = -1"
.endc
```

```
Circuit:  *pseudo nmos inverter design(vol<0.4v)

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 331
voh                  =  3.199115e+00
vol                  =  3.615173e-01
vil                  =  5.786782e-01
vih                  =  1.222381e+00
voh = 3.199115e+00
vih = 1.222381e+00
nmh = 1.976734e+00
vil = 5.786782e-01
vol = 3.615173e-01
```

Waveform-



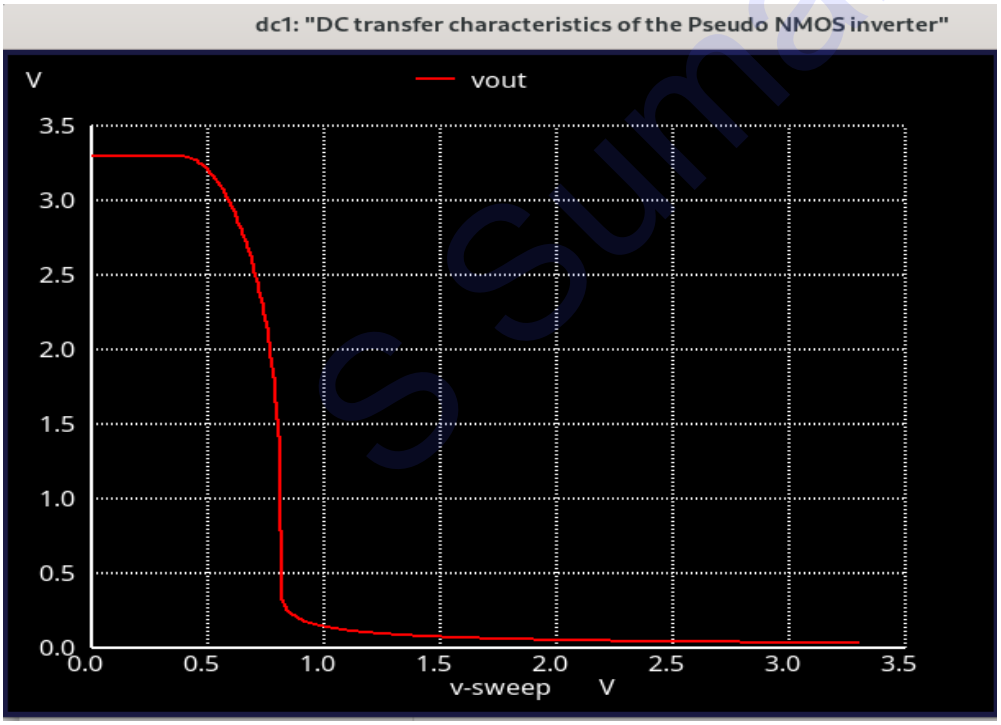
For width 0.2u-
Netlist -

```
*Pseudo NMOS Inverter Design(Vol<0.4V)
 *including the 0.25 µm level 3 model file for simulation
 .include ./t14y_tsmc_025_level3.txt
 *netlist description
 m1 Vout Vin 0 0 cmosn l=0.8u w=1.2u
 m2 Vout 0 Vdd Vdd cmosp l=0.8u w=0.2u
 *DC excitations
 V_in Vin 0 3.3
 V_dd Vdd 0 3.3
 .control
 dc V_in 0 3.3 0.01
 let d_Vout=deriv(Vout)
 meas dc VOH find Vout when d_Vout=-1 fall=1
 meas dc VOL find Vout when d_Vout=-1 rise=1
 meas dc VIL find Vin when Vout=VOH
 meas dc VIH find Vin when Vout=VOL
```

```
let NML=VIL-VOL
let NMH=VOH-VIH
print VOH VIH NMH
print VIL VOL NML
setplot
plot Vout title "DC transfer characteristics of the Pseudo NMOS inverter"
plot d_Vout 0-1 title "locating slope = -1"
.endc
```

```
No. of Data Rows : 331
voh                 =  3.264284e+00
vol                 =  2.162822e-01
vil                 =  4.533699e-01
vih                 =  8.701448e-01
voh = 3.264284e+00
vih = 8.701448e-01
nmh = 2.394139e+00
vil = 4.533699e-01
vol = 2.162822e-01
```

Waveform-



FOR width 0.05

```
No. of Data Rows : 331
voh                 =  3.262271e+00
vol                 =  9.407958e-02
vil                 =  4.091491e-01
vih                 =  5.914620e-01
voh = 3.262271e+00
vih = 5.914620e-01
nmh = 2.670809e+00
vil = 4.091491e-01
vol = 9.407958e-02
```

Tabluation

Pmos width (W) in µm	Pmos length (L) in µm	Vol
0.5	0.8	0.361 volt
0.2	0.8	0.216 volt
0.05	0.8	0.094 volt

Conclusion-

1) we noticed that by decreasing the width size of pmos we are able to decrease Vol. Here V_{ol} must be below 0.4 based on that we got the value of pmos size.
2) By decreasing Pmos size VTC curve shift left hand side.
3) Decrease in V_{ol} will cause decrease in pmos width size and this results in decrease in static power dissipation.

(b) Design a inverter chain to drive a large load capacitance of 1pF. Assume that the first stage has to be a minimum sized inverter with matched N and P delays (i.e. for the first stage choose Ln= Lp=0.8 µm and Wn= 1.2 µm and Wp=3.6 µm. (This inverter has a gate capacitance of about 13 fF for the technology you are using). Through simulations, estimate the optimum number of stages and the corresponding stage ratio which minimizes the propagation delay from input to the output of the inverter chain. What is the rising delay falling delay and average delay.

Netlist

```
*single stage inverter
 *including the 0.25 µm level 3 model file for simulation
.include ./t14y_tsmc_025_level3.txt
 *netlist
 *stage-1
 mn1 Vout1 Vin 0 0 cmosn l=0.8u w=1.2u
 mp1 Vout1 Vin Vdd Vdd cmosp l=0.8u w=3.6u
 *load capacitance
 cl Vout1 0 1p

 *dc excitations
 V_dd Vdd 0 3.3
 V_in Vin 0 pulse(0 3.3 0 0 0 50n 100n)

 .control
 tran 0.1n 200n
 meas tran tphl trig Vin val=1.65 rise=2 targ Vout1 val=1.65 fall=2
 meas tran tplh trig Vin val=1.65 fall=1 targ Vout1 val=1.65 rise=1
 meas tran tr trig Vout1 val=0.33 rise=2 targ Vout1 val=2.97 rise=2
 meas tran tf trig Vout1 val=2.97 fall=2 targ Vout1 val=0.33 fall=2
 print tphl tplh tr tf
 let tpd=(tphl+tplh)/2
 let tdavg=(tr+tf)/2
 print tpd tdavg
 setplot
 plot Vout1 Vin
 .endc
```

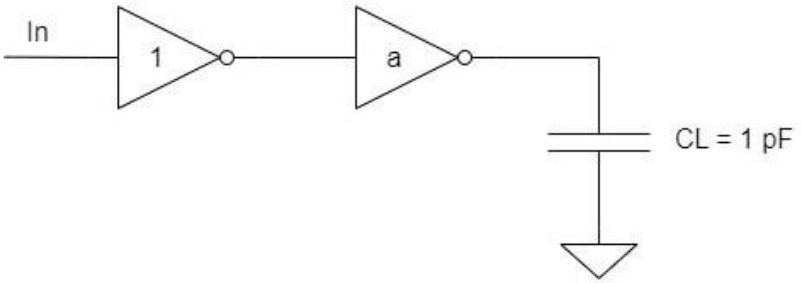
Output Waveform

Simulation Result

```
tphl                   =  3.507339e-09 targ=  1.035573e-07 trig=  1.000500e-07
tplh                   =  3.801649e-09 targ=  5.395165e-08 trig=  5.015000e-08
tr                     =  7.815076e-09 targ=  1.587592e-07 trig=  1.509442e-07
tf                     =  6.465012e-09 targ=  1.072703e-07 trig=  1.008053e-07
tphl = 3.507339e-09
tplh = 3.801649e-09
tr = 7.815076e-09
tf = 6.465012e-09
tpd = 3.654494e-09
tdavg = 7.140044e-09
```

Rise time	7.81 ns
Fall time	6.46 ns
Average delay	7.14 ns
Propagation delay	3.65 ns

Transistor Sizing for N=2



Given first stage has to be a minimum sized inverter with

$$W_n = 1.2\ \mu m\ W_p = 3.6\ \mu m$$

Delay is minimized when each stage has the same fanout. The total fanout is

$$F = \frac{CL}{Cin} = \frac{1pF}{13fF} = \frac{1000}{13}$$

Fanout per stage

$$f = \sqrt[N]{F} = \sqrt[2]{1000/13} = 8.77$$

$$C_a = \frac{C_L}{f} = \frac{1000}{13 * 8.77} C_{in} = 8.77 C_{in} \Rightarrow a = 8.77$$

$$W_n = 8.77 * 1.2\ \mu m = 10.524\ \mu m$$

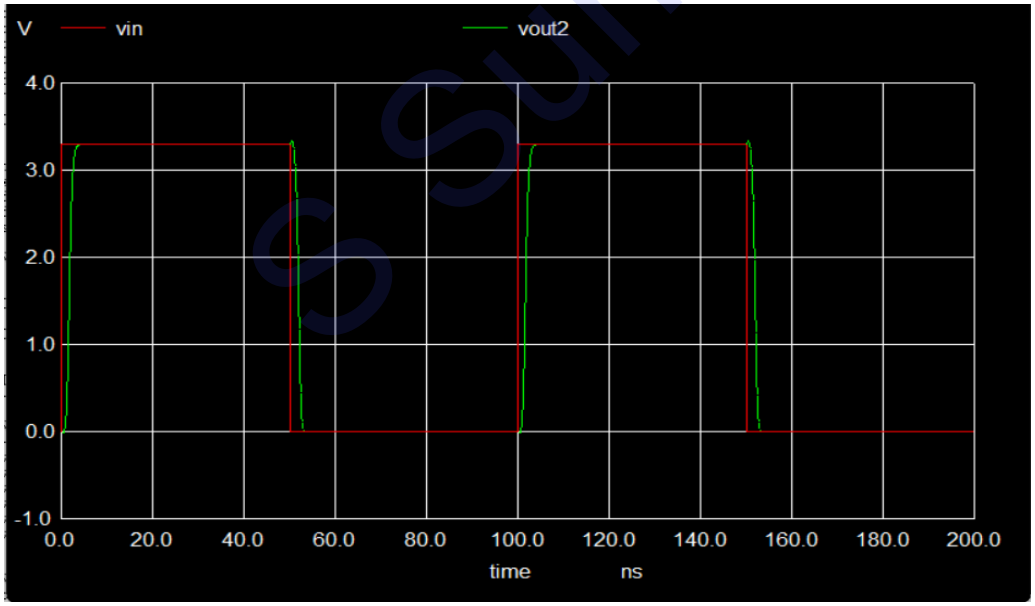
$$W_p = 8.77 * 3.6\ \mu m = 31.572\ \mu m$$

Netlist for 2-stage (N=2)

```
*Two stage inverter
 *including the 0.25 µm level 3 model file for simulation
.include ./t14y_tsmc_025_level3.txt
 *netlist
 *stage-1
 mn1 Vout1 Vin 0 0 cmosn l=0.8u w=1.2u
 mp1 Vout1 Vin Vdd Vdd cmosp l=0.8u w=3.6u
 *stage-2
 mn2 Vout2 Vout1 0 0 cmosn l=0.8u w=10.52u
 mp2 Vout2 Vout1 Vdd Vdd cmosp l=0.8u w=31.57u
 *load capacitance
cl Vout2 0 1p
 *dc excitations
 V_dd Vdd 0 3.3
```

```
V_in Vin 0 pulse(0 3.3 0 0 0 50n 100n)
.control
tran 0.1n 200n
meas tran tphl trig Vin val=1.65 rise=2 targ Vout2 val=1.65 rise=2
meas tran tplh trig Vin val=1.65 fall=2 targ Vout2 val=1.65 fall=2
meas tran tr trig Vout2 val=0.33 rise=2 targ Vout2 val=2.97 rise=2
meas tran tf trig Vout2 val=2.97 fall=2 targ Vout2 val=0.33 fall=2
print tphl tplh tr tf
let tpd=(tphl+tplh)/2
let tdavg=(tr+tf)/2
print tpd tdavg
setplot
plot Vout2 Vin
.endc
```

Output Waveform

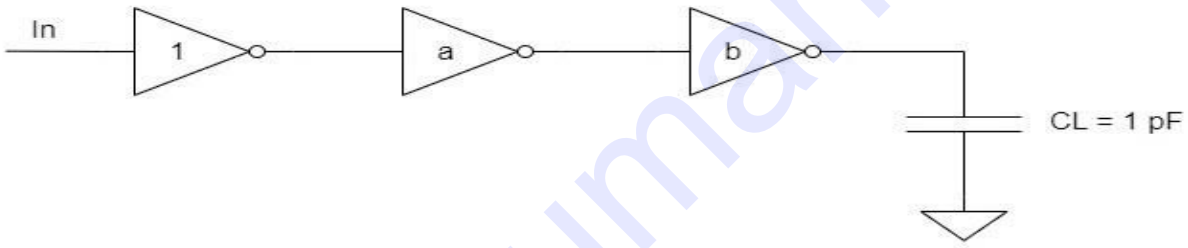


Simulation Result

```
tphl                   =  1.692385e-09 targ=  1.017424e-07 trig=  1.000500e-07
tplh                   =  1.813309e-09 targ=  1.519633e-07 trig=  1.501500e-07
tr                     =  1.338750e-09 targ=  1.024923e-07 trig=  1.011535e-07
tf                     =  1.207237e-09 targ=  1.525039e-07 trig=  1.512966e-07
tphl = 1.692385e-09
tplh = 1.813309e-09
tr = 1.338750e-09
tf = 1.207237e-09
tpd = 1.752847e-09
tdavg = 1.272994e-09
```

Rise time	1.33 ns
Fall time	1.20 ns
Average delay	1.27 ns
Propagation delay	1.75 ns

Transistor sizing for N=3



Given first stage has to be a minimum sized inverter with

$$W_n = 1.2\ \mu m\ W_p = 3.6\ \mu m$$

Delay is minimized when each stage has the same fanout. The total fanout is

$$F = \frac{CL}{Cin} = \frac{1pF}{13fF} = \frac{1000}{13}$$

Fanout per stage

$$f = \sqrt[N]{F} = \sqrt[3]{1000/13} = 4.25$$

Sizing of inverters

$$C_b = \frac{C_L}{f} = \frac{1000}{13 * 4.25} C_{in} = 18.1 C_{in} \Rightarrow b = 18.1$$

$$W_n = 18.1 * 1.2\ \mu m = 21.72\ \mu m$$

$$W_p = 18.1 * 3.6\ \mu m = 65.16\ \mu m$$

$$C_a = \frac{C_b}{f} = \frac{18.1 C_{in}}{4.25} = 4.26 \Rightarrow a = 4.26$$

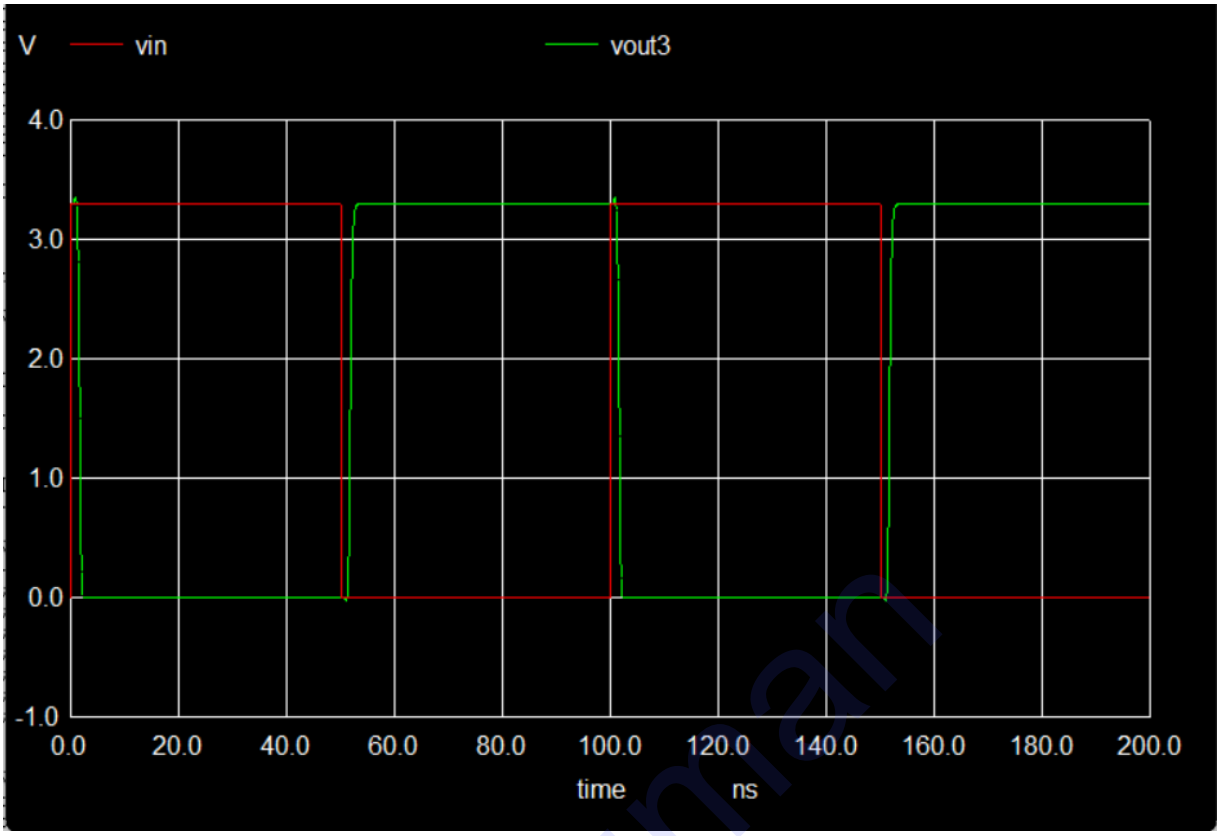
$$W_n = 4.26 * 1.2\ \mu m = 5.112\ \mu m$$

$$W_p = 4.26 * 3.6\ \mu m = 15.336\ \mu m$$

Netlist for 3-stage (N=3)

```
*Three stage inverter
 *including the 0.25 µm level 3 model file for simulation
.include ./t14y_tsmc_025_level3.txt

 *netlist
 *stage-1
mn1 Vout1 Vin 0 0 cmosn l=0.8u w=1.2u
mp1 Vout1 Vin Vdd Vdd cmosp l=0.8u w=3.6u
*stage-2
mn2 Vout2 Vout1 0 0 cmosn l=0.8u w=5.1u
mp2 Vout2 Vout1 Vdd Vdd cmosp l=0.8u w=15.31u
*stage-3
mn3 Vout3 Vout2 0 0 cmosn l=0.8u w=21.7u
mp3 Vout3 Vout2 Vdd Vdd cmosp l=0.8u w=65.11u
*load capacitance
cl Vout3 0 1p
*dc excitations
V_dd Vdd 0 3.3
V_in Vin 0 pulse(0 3.3 0 0 0 50n 100n)
.control
tran 0.1n 200n
meas tran tphl trig Vin val=1.65 rise=2 targ Vout3 val=1.65 fall=2
meas tran tplh trig Vin val=1.65 fall=1 targ Vout3 val=1.65 rise=1
meas tran tr trig Vout3 val=0.33 rise=2 targ Vout3 val=2.97 rise=2
meas tran tf trig Vout3 val=2.97 fall=2 targ Vout3 val=0.33 fall=2
print tphl tplh tr tf
let tpd=(tphl+tplh)/2
let tdavg=(tr+tf)/2
print tpd tdavg
setplot
plot Vout3 Vin
.endc
```

Output Waveform

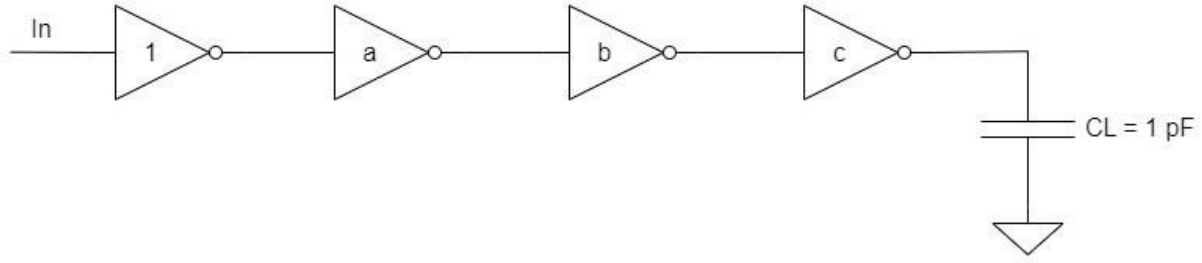


Simulation Result

```
tphl                   =  1.579605e-09 targ=  1.016296e-07 trig=  1.000500e-07
tplh                   =  1.626787e-09 targ=  5.177679e-08 trig=  5.015000e-08
tr                     =  7.657305e-10 targ=  1.522181e-07 trig=  1.514523e-07
tf                     =  6.246678e-10 targ=  1.019161e-07 trig=  1.012914e-07
tphl = 1.579605e-09
tplh = 1.626787e-09
tr = 7.657305e-10
tf = 6.246678e-10
tpd = 1.603196e-09
tdavg = 6.951991e-10
```

Rise time	0.765 ns
Fall time	0.624 ns
Average delay	0.695 ns
Propagation delay	1.60 ns

Transistor sizing for N=4



Given first stage has to be a minimum sized inverter with

$$W_n = 1.2\ \mu m$$
$$W_p = 3.6\ \mu m$$

Delay is minimized when each stage has the same fanout. The total fanout is

$$F = \frac{CL}{Cin} = \frac{1pF}{13fF} = \frac{1000}{13}$$

Fanout per stage

$$f = \sqrt[N]{F} = \sqrt[4]{1000/13} = 2.96$$

Sizing of inverters

$$C_c = \frac{C_L}{f} = \frac{1000C_{in}}{13 * 2.96} = 25.98C_{in} \Rightarrow c = 25.98$$
$$W_n = 25.98 * 1.2\ \mu m = 31.176\ \mu m$$
$$W_p = 25.98 * 3.6\ \mu m = 93.528\ \mu m$$
$$C_b = \frac{C_c}{f} = \frac{25.98C_{in}}{2.96} = 8.78C_{in} \Rightarrow b = 8.78$$
$$W_n = 8.78 * 1.2\ \mu m = 10.536\ \mu m$$
$$W_p = 8.78 * 3.6\ \mu m = 31.608\ \mu m$$
$$C_a = \frac{C_b}{f} = \frac{8.78C_{in}}{2.96} = 2.96C_{in} \Rightarrow a = 2.97$$
$$W_n = 2.97 * 1.2\ \mu m = 3.564\ \mu m$$
$$W_p = 2.97 * 3.6\ \mu m = 10.692\ \mu m$$

Netlist for 4-stage (N=4)

*Four stage inverter

*including the 0.25 µm level 3 model file for simulation

.include ./t14y_tsmc_025_level3.txt

*netlist

*stage-1

mn1 Vout1 Vin 0 0 cmosn l=0.8u w=1.2u

mp1 Vout1 Vin Vdd Vdd cmosp l=0.8u w=3.6u

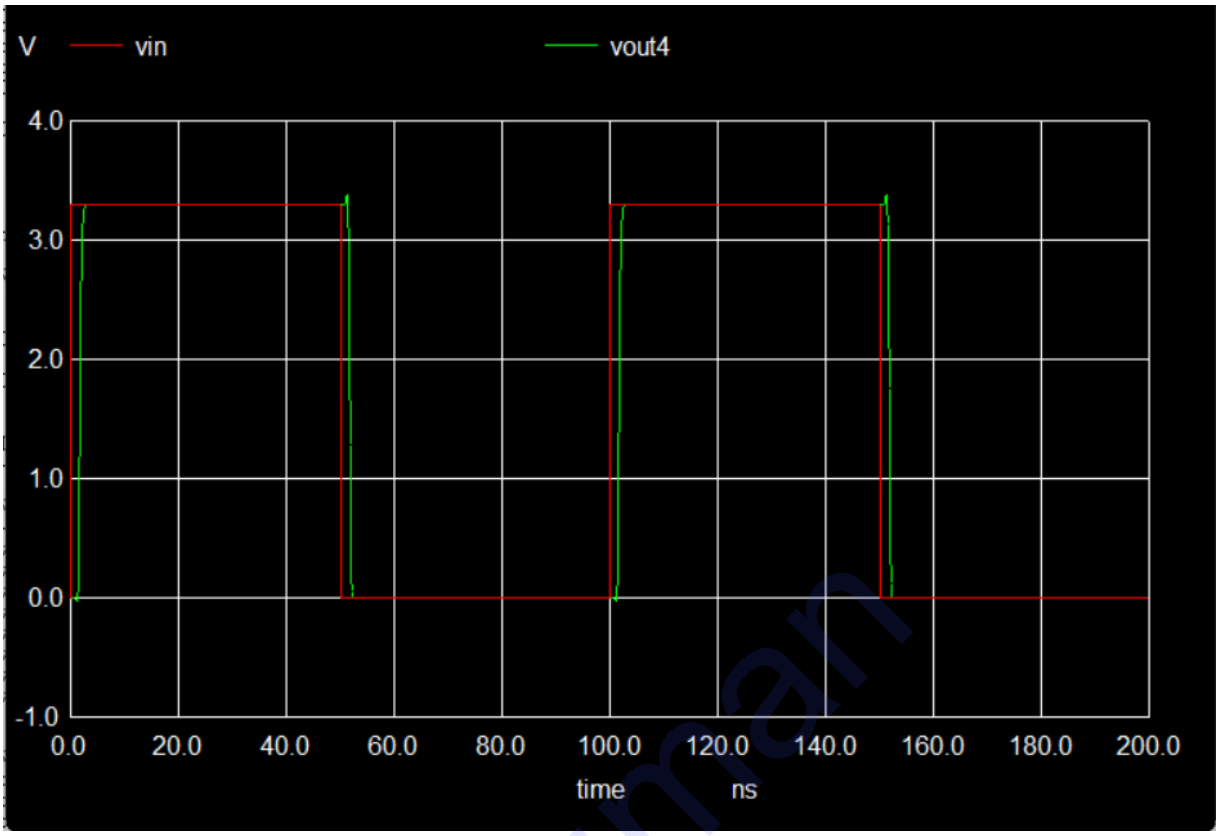
*stage-2

mn2 Vout2 Vout1 0 0 cmosn l=0.8u w=3.55u

mp2 Vout2 Vout1 Vdd Vdd cmosp l=0.8u w=10.66u

```
*stage-3
mn3 Vout3 Vout2 0 0 cmosn l=0.8u w=10.51u
mp3 Vout3 Vout2 Vdd Vdd cmosp l=0.8u w=31.54u
*stage-4
mn4 Vout4 Vout3 0 0 cmosn l=0.8u w=31.12u
mp4 Vout4 Vout3 Vdd Vdd cmosp l=0.8u w=93.36u
*load capacitance of 1pf
cl Vout4 0 1p
*dc excitations
V_dd Vdd 0 3.3
V_in Vin 0 pulse(0 3.3 0 0 0 50n 100n)
 .control
tran 0.1n 200n
meas tran tphl trig Vin val=1.65 rise=2 targ Vout4 val=1.65 rise=2
meas tran tplh trig Vin val=1.65 fall=2 targ Vout4 val=1.65 fall=2
meas tran tr trig Vout4 val=0.33 rise=2 targ Vout4 val=2.97 rise=2
meas tran tf trig Vout4 val=2.97 fall=2 targ Vout4 val=0.33 fall=2
print tphl tplh tr tf
let tpd=(tphl+tplh)/2
let tdavg=(tr+tf)/2
print tpd tdavg
setplot
plot Vout4 Vin
.endc
```

Output Waveform

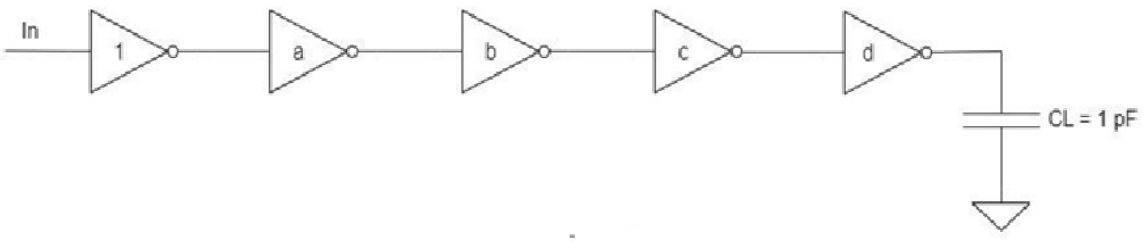


Simulation Result

```
tphl                   =  1.676709e-09 targ=  1.017267e-07 trig=  1.000500e-07
tplh                   =  1.695863e-09 targ=  1.518459e-07 trig=  1.501500e-07
tr                     =  6.082358e-10 targ=  1.020919e-07 trig=  1.014837e-07
tf                     =  4.732935e-10 targ=  1.520629e-07 trig=  1.515896e-07
tphl = 1.676709e-09
tplh = 1.695863e-09
tr = 6.082358e-10
tf = 4.732935e-10
tpd = 1.686286e-09
tdavg = 5.407647e-10
```

Rise time	0.608 ns
Fall time	0.473 ns
Average delay	0.540 ns
Propagation delay	1.68 ns

Transistor sizing for N=5



Given first stage has to be a minimum sized inverter with

$$W_n = 1.2\ \mu m$$
$$W_p = 3.6\ \mu m$$

Delay is minimized when each stage has the same fanout. The total fanout is

$$F = \frac{CL}{Cin} = \frac{1pF}{13fF} = \frac{1000}{13}$$

Fanout per stage

$$f = \sqrt[N]{F} = \sqrt[4]{1000/13} = 2.96$$

Sizing of inverters

$$C_d = \frac{C_L}{f} = \frac{1000C_{in}}{13 * 2.38} = 32.32C_{in} \Rightarrow d = 32.32$$
$$W_n = 32.32 * 1.2\ \mu m = 38.784\ \mu m$$
$$W_p = 32.32 * 3.6\ \mu m = 116.352\ \mu m$$
$$C_c = \frac{C_L}{f} = \frac{32.32C_{in}}{2.38} = 13.58C_{in} \Rightarrow c = 13.58$$
$$W_n = 13.58 * 1.2\ \mu m = 16.296\ \mu m$$
$$W_p = 13.58 * 3.6\ \mu m = 48.888\ \mu m$$
$$C_b = \frac{C_c}{f} = \frac{13.58C_{in}}{2.38} = 5.70C_{in} \Rightarrow b = 5.70$$
$$W_n = 5.7 * 1.2\ \mu m = 6.84\ \mu m$$
$$W_p = 5.7 * 3.6\ \mu m = 20.52\ \mu m$$
$$C_a = \frac{C_b}{f} = \frac{5.7C_{in}}{2.38} = 2.39C_{in} \Rightarrow a = 2.39$$
$$W_n = 2.39 * 1.2\ \mu m = 2.868\ \mu m$$
$$W_p = 2.39 * 3.6\ \mu m = 8.604\ \mu m$$

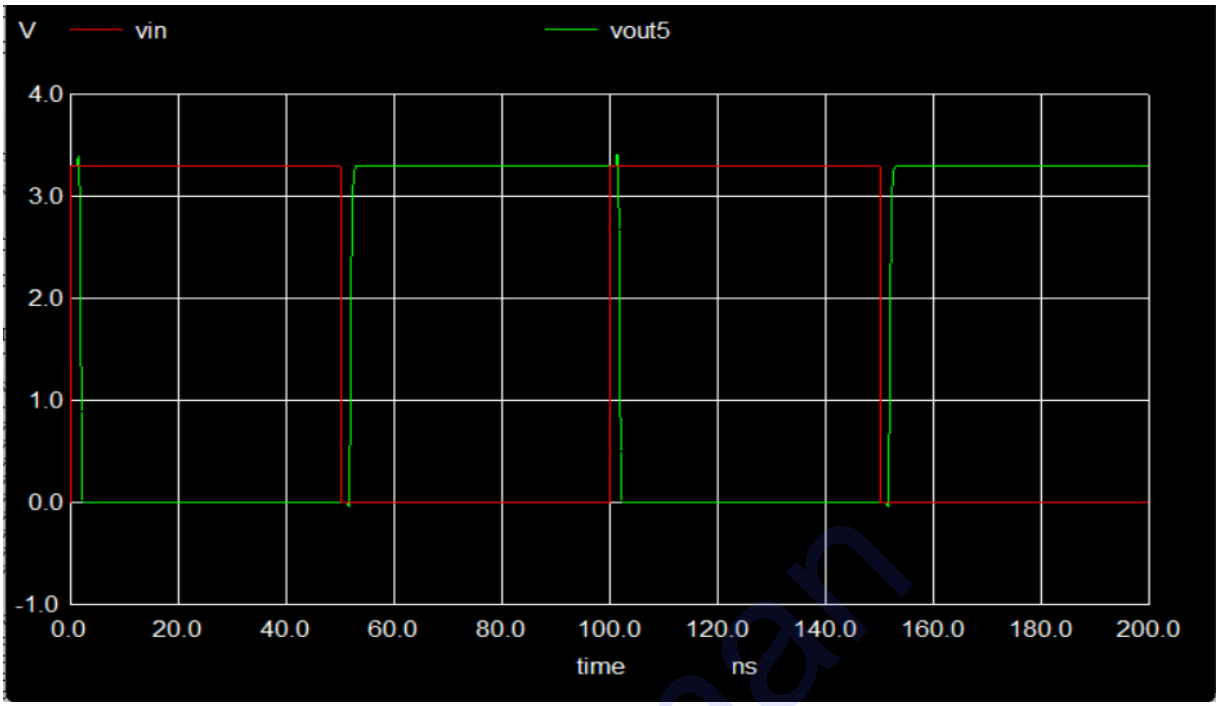
Netlist for 5-stage (N=5)

```
*Five stage inverter
 *including the 0.25 µm level 3 model file for simulation
.include ./t14y_tsmc_025_level3.txt

 *netlist
 *stage-1
 mn1 Vout1 Vin 0 0 cmosn l=0.8u w=1.2u
 mp1 Vout1 Vin Vdd Vdd cmosp l=0.8u w=3.6u
 *stage-2
 mn2 Vout2 Vout1 0 0 cmosn l=0.8u w=2.86u
 mp2 Vout2 Vout1 Vdd Vdd cmosp l=0.8u w=8.58u
 *stage-3
 mn3 Vout3 Vout2 0 0 cmosn l=0.8u w=6.81u
 mp3 Vout3 Vout2 Vdd Vdd cmosp l=0.8u w=20.44u
 *stage-4
 mn4 Vout4 Vout3 0 0 cmosn l=0.8u w=16.24u
 mp4 Vout4 Vout3 Vdd Vdd cmosp l=0.8u w=48.72u
 *stage-5
 mn5 Vout5 Vout4 0 0 cmosn l=0.8u w=38.69u
 mp5 Vout5 Vout4 Vdd Vdd cmosp l=0.8u w=116.09u
 *load capacitance of 1pf
 cl Vout5 0 1p
 *dc excitations
 V_dd Vdd 0 3.3
 V_in Vin 0 pulse(0 3.3 0 0 0 50n 100n)
 .control
 tran 0.1n 200n
 meas tran tphl trig Vin val=1.65 rise=2 targ Vout5 val=1.65 fall=2
 meas tran tplh trig Vin val=1.65 fall=1 targ Vout5 val=1.65 rise=1
 meas tran tr trig Vout5 val=0.33 rise=2 targ Vout5 val=2.97 rise=2
 meas tran tf trig Vout5 val=2.97 fall=2 targ Vout5 val=0.33 fall=2
 print tphl tplh tr tf
 let tpd=(tphl+tplh)/2
 let tdavg=(tr+tf)/2
 print tpd tdavg

 setplot
```

plot Vout5 Vin

.endc

Output Waveform



Simulation Result

```
tphl                   =  1.802795e-09 targ=  1.018528e-07 trig=  1.000500e-07
tplh                   =  1.838274e-09 targ=  5.198827e-08 trig=  5.015000e-08
tr                     =  5.309703e-10 targ=  1.523065e-07 trig=  1.517756e-07
tf                     =  3.911672e-10 targ=  1.020386e-07 trig=  1.016474e-07
tphl = 1.802795e-09
tplh = 1.838274e-09
tr = 5.309703e-10
tf = 3.911672e-10
tpd = 1.820535e-09
tdavg = 4.610687e-10
```

Rise time	0.530 ns
Fall time	0.391 ns
Average delay	0.461 ns
Propagation delay	1.82 ns

Conclusion

Parameters	N=1	N=2	N=3	N=4	N=5
Rise time	7.81 ns	1.33 ns	0.765 ns	0.608 ns	0.530 ns
Fall time	6.46 ns	1.20 ns	0.624 ns	0.473 ns	0.391 ns
Average delay	7.14 ns	1.27 ns	0.695 ns	0.540 ns	0.461 ns
Propagation delay	3.65 ns	1.75 ns	1.60 ns	1.68 ns	1.82 ns

The propagation delay is brought to a minimum in a 3-stage inverter setup. Therefore, it is established that the most favourable number of stages for minimizing the propagation delay across the entire inverter chain, from input to output, is N=3.