Layout of Full Adder Circuit With Transmission Gate Logic

Objective

- Perform Layout of a 1-bit full adder in Cadence Virtuoso.
- Simulate and verify the circuit.
- Create a cell of the given circuit and give the test input to verify result.

Introduction

1 bit full adder architecture consists of XOR gate for sum and for carry “AND” and “OR”. Those gate logic are replaced by CMOS logic such as Transmission gate logic and CMOS inverter. In summary, the full adder circuit combines two binary numbers along with a carry input to produce the sum of the numbers along with a carry output, making it a crucial building block in digital arithmetic circuits.

Application

- -ALUs (Arithmetic logic unit) of CPU
- -Program Counter
- -Graphical processing unit

Given Circuit

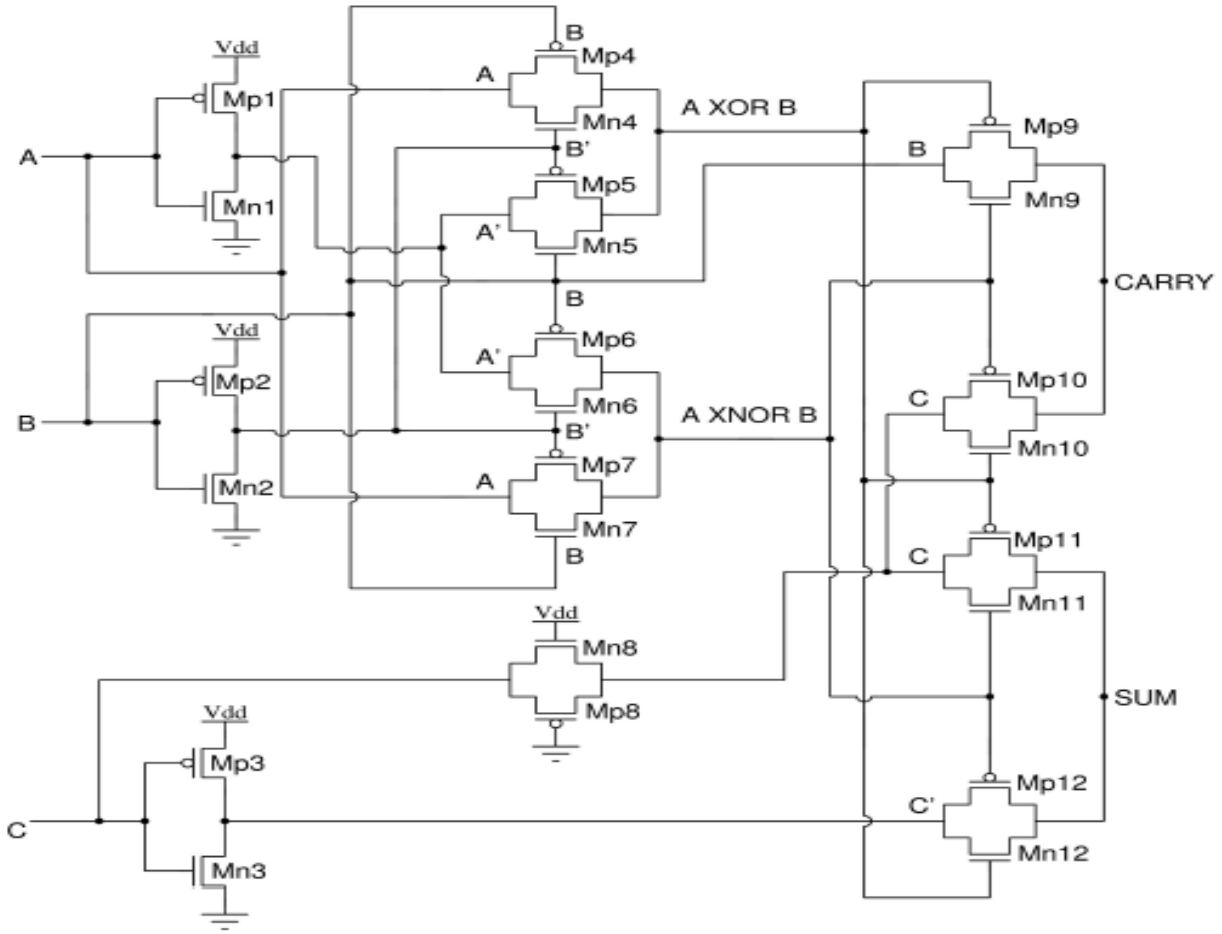

Fig 1- Circuit

Sizing of Transistor-

- Circuit-2 Sizing with Umc 65 nm Technology :Reference Size:

PMOS width = NMOS width = 155nm, Gate length = 70 nm

Inverters:

PMOS (Mp1, Mp2, Mp3) sized as multiples of reference NMOS (Mn1):

Mp1: 2x reference size (PMOS double the size of NMOS)

Mp2: 8x reference size

Mp3: 4x reference size

Transmission Gates:

Standard: Mp4-7, Mp10-12, Mn4-7, Mn10-12 use reference size.

Delay-adjusted:

Mp8/Mn8: reference width, but 2x gate length (match C & $\bar{C}$ delays).

Mp9/Mn9: reference width, but 3x gate length (match B & C to carry output)

Schematic of given circuit-

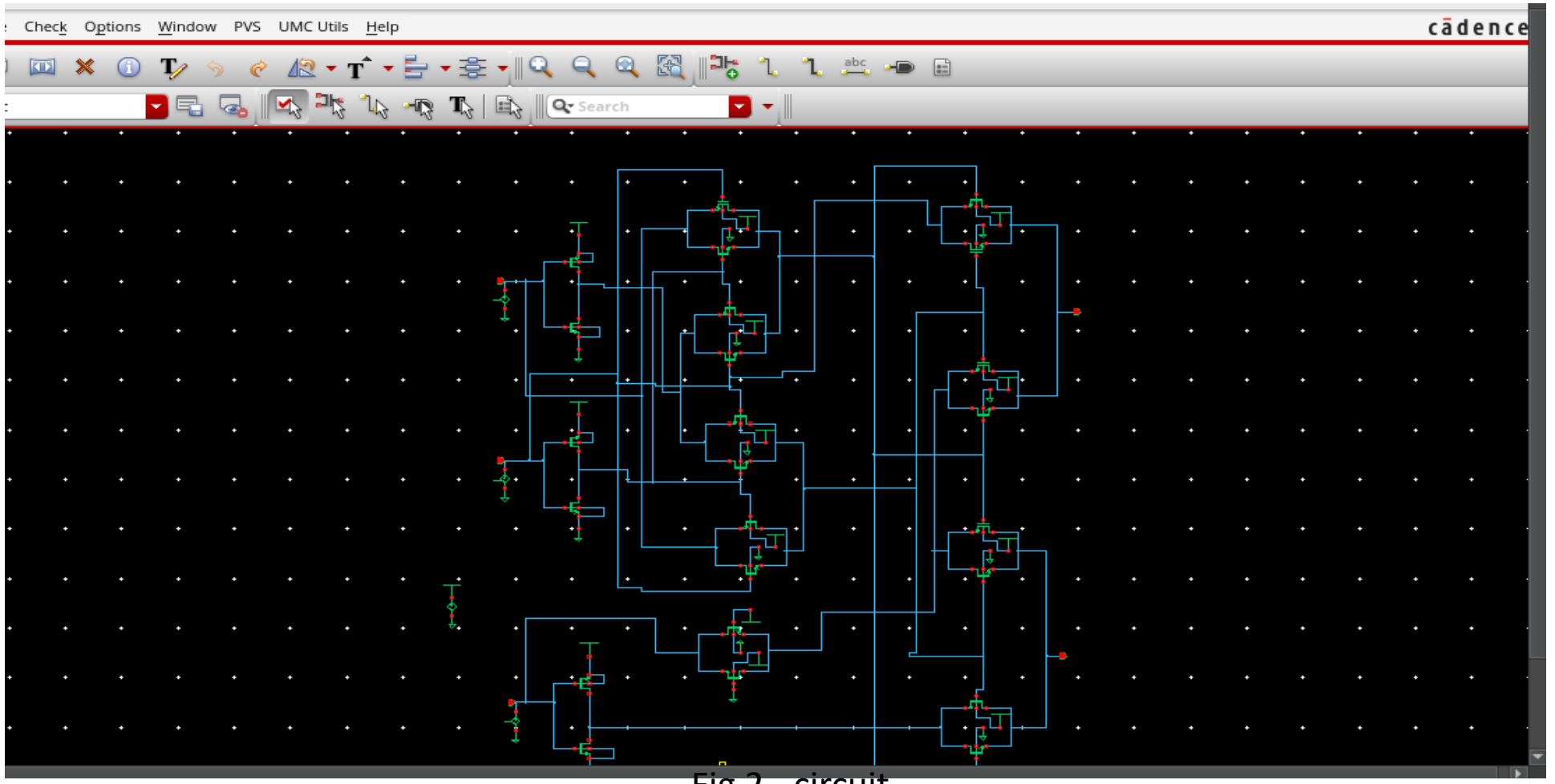

Fig 2 - circuit

Result-

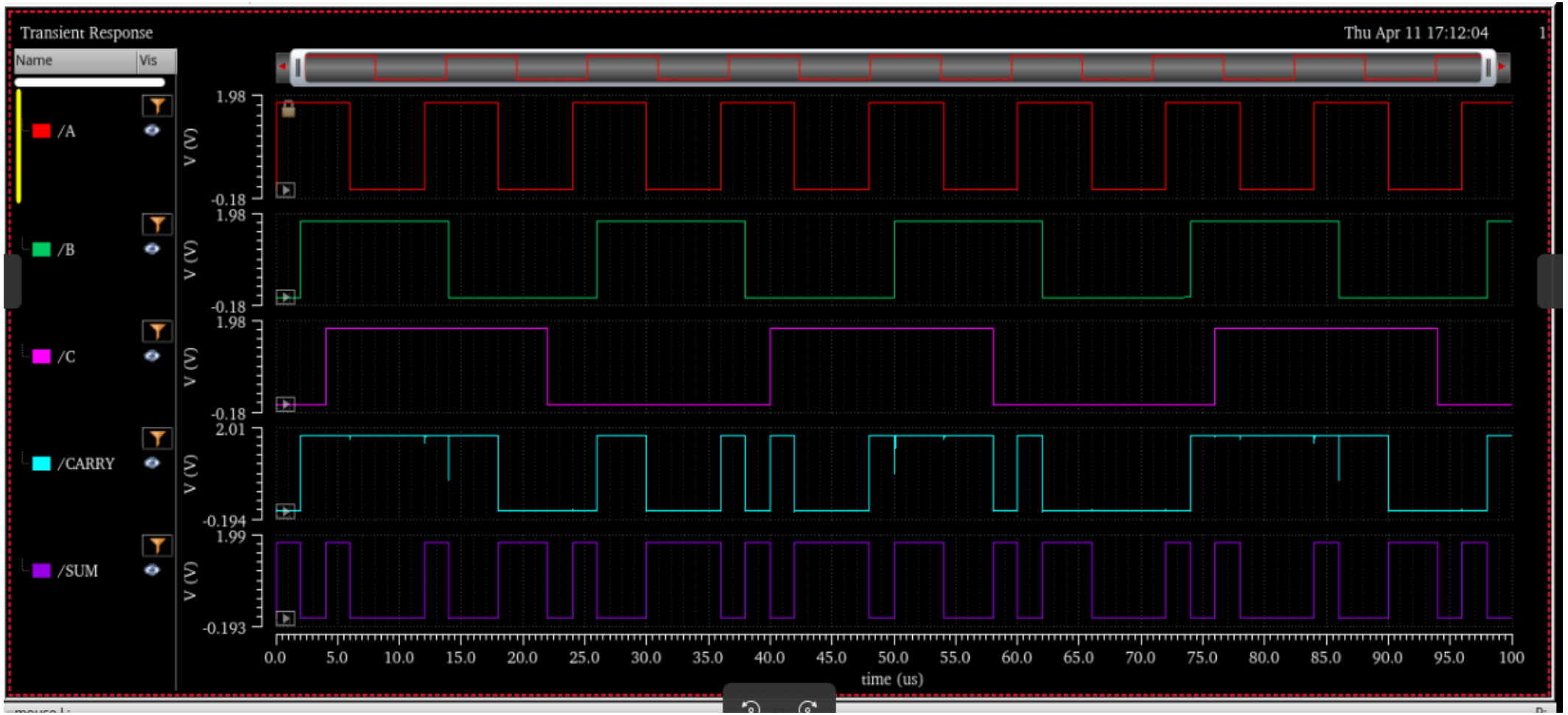

Fig 2 - Waveforms

Performed Layout-

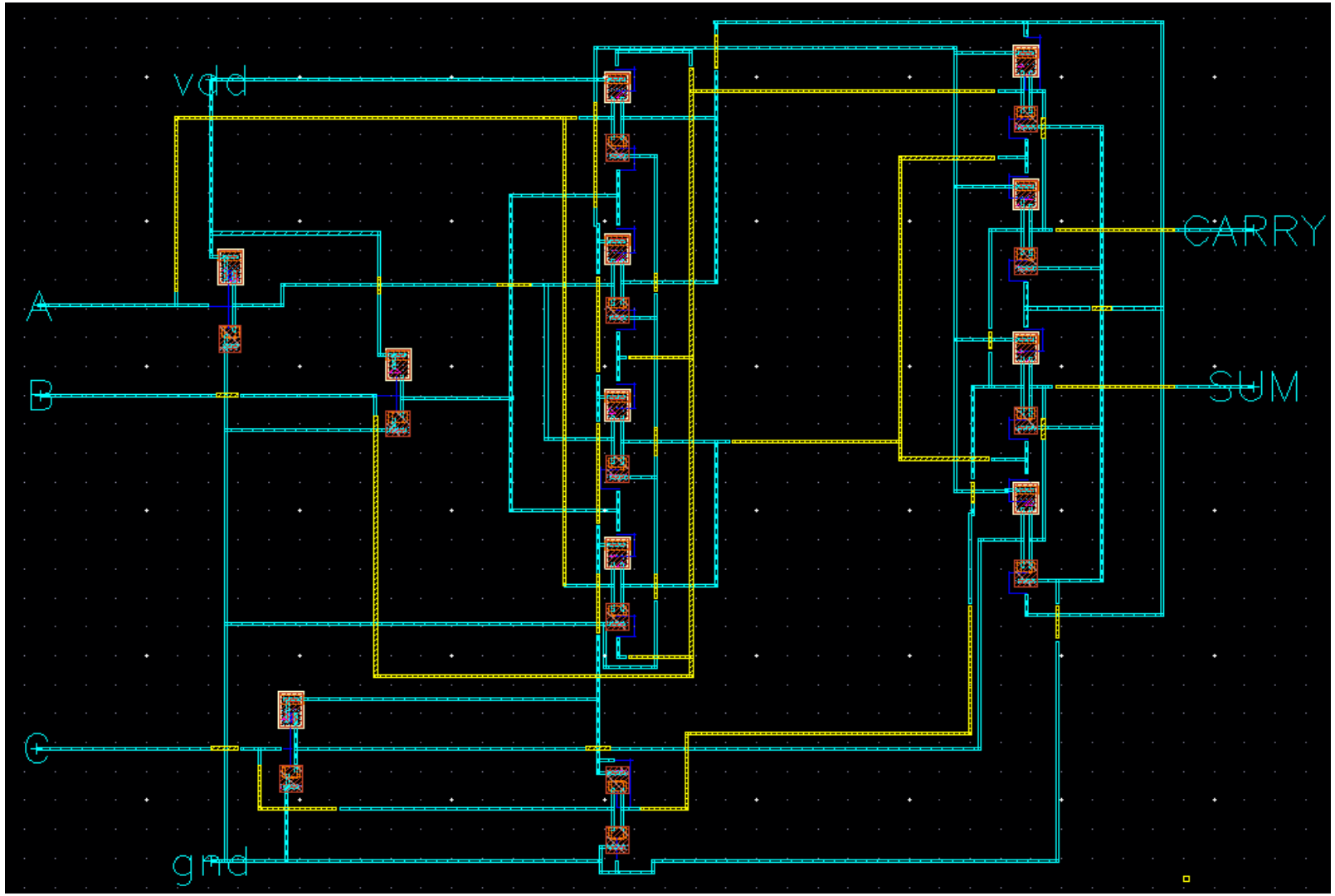

Fig 2 - Layout

Schematic simulation result-

Delay

Sum- 69.17ps

Carry- 74.1 ps

Power- 10 .28 nW

Conclusion

- It demonstrates better speed while also consuming less power and offering an improved PDP on simulation done in Ltspice.
- Consequently, this architecture is well-suited for high-speed applications that prioritize power efficiency.

Reference

[1] Chiou-Kou Tung, Shao-Hui Shieh, Yu-Cherng Hung, and Ming-Chien Tsai (2006) High-Performance Low-Power Full-Swing Full Adder Cores with Out-put Driving Capability, 2006 IEEE Asia Pacic Conference on Circuits and Systems.(APCCAS-2006)

[2] Anantha P. Chandrakasan and Jan M. Rabaey (2016) Digital Integrated Circuits:A Design Perspective, Pearson Education India.