Abstract

This project tackles the pressing challenge of achieving high-speed 1-bit full adders in digital design. As a critical building block of digital circuits, the 1-bit full adder underpins arithmetic and logical operations within microprocessors, microcontrollers, and signal processing units. By introducing a novel architecture, this project aims to dramatically reduce the delay in 1-bit full adders, ultimately enhancing performance. Leveraging a strategic blend of CMOS and Transmission Gate logic, the proposed design offers a promising path forward. The project entails meticulously crafting a circuit layout and rigorously simulating it using Cadence tools. By optimizing delay characteristics, this research holds the potential to revolutionize the efficiency of digital systems, offering valuable insights for optimizing arithmetic operations in electronic devices.

Contents

Chapter 1

OBJECTIVES

The main objectives of this project are:

- Design high speed 1-Bit Full Adder architecture by decreasing the parasitic effect of capacitance.
- Create circuit layout and carry out simulation using Cadence tools.
- Achieve optimization of 1-bit full adder for better speed, area and minimize wire length to avoid problem in fabrication.

Chapter 2

INTRODUCTION

1-Bit Full Adder

A full adder is a fundamental digital logic circuit that performs the addition of three binary digits (bits) and outputs two binary digits. It is essentially an extension of a half adder, which can only add two bits. It accounts for the carry-in from the previous addition, making it suitable for multi-bit addition operations. Figure 1(a) shows the block diagram and Figure 1(b) shows the gate level implementation for a 1-bit full adder. Full adders are constructed using basic logic gates like XOR and OR. They are the building blocks of arithmetic logic units (ALUs) in processors and other digital circuits performing arithmetic operations.

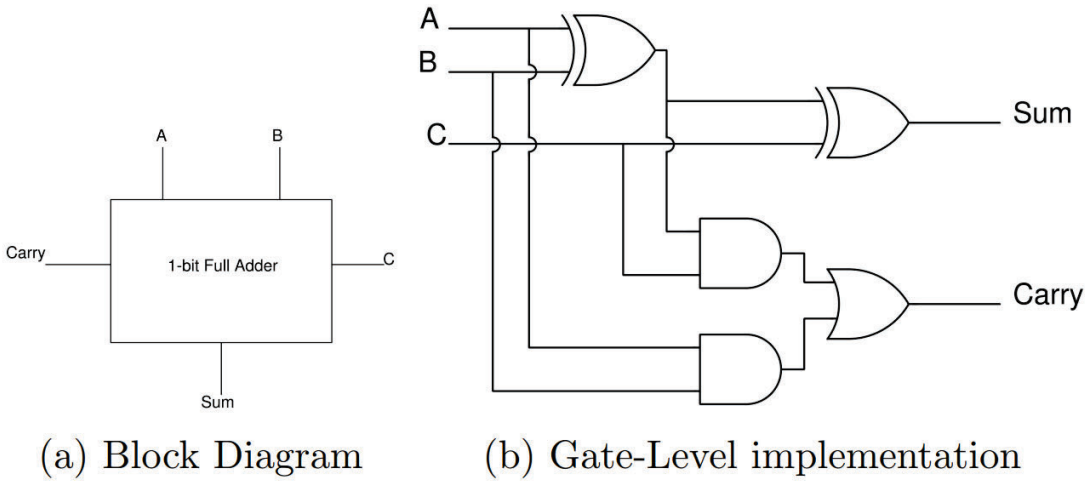

Figure 1: Full Adder

First binary digit (bit) A second binary digit (bit) B and C the Carry-in bit from the previous addition stage (optional, can be 0 or 1) are added to results in two outputs Sum and Carry. Sum represents the actual sum of the three input bits while Carry indicates whether the addition resulted in a carry that needs to be propagated to the next addition stage.

The truth-table for full adder is given in Table 1 shows the output (Sum and Carry) for all possible combinations of inputs (A, B, and C)

Table 1: Truth Table of a 1-bit Full Adder

A	**B**	**C**	**Sum**	**Carry**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The relation between input and output of the full adder is given in eq. (1) & (2)

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = A.B + B.C + A.C = A.B + C.\ (A \oplus B) \quad (2)$$

Chapter 3

High Speed Full Adder Architectures

This chapter presents one of the proposed circuits of 1- bit full adder which gives the best results and a reliable waveform.

3.1 Proposed Circuit

Proposed 1-bit full adder-II

Source: “Optimization and Characterization of 1-bit Full Adder Circuits for use in High Speed Standard Cell Library” by Chinmay Malkhandi under the guidance of Dr. Rathnamala Rao in May,2022

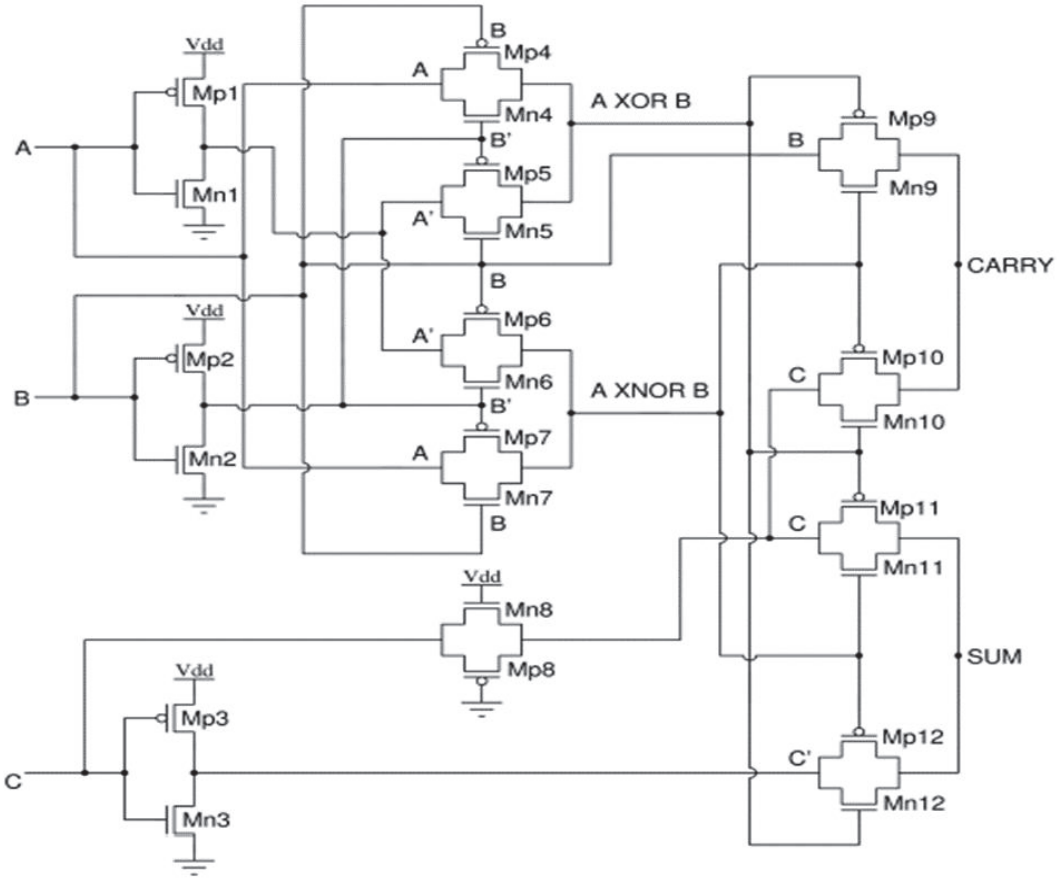

Figure 2: Circuit level implementation of the Proposed 1-bit full adder-2

3.2 Sub-Modules of the Proposed Circuits

This section shows the different blocks used for the design of the proposed circuits. The proposed circuit is implemented by are three modules, the XOR-XNOR module, the Sum module, and the Carry module.

3.2.1 XOR-XNOR Module

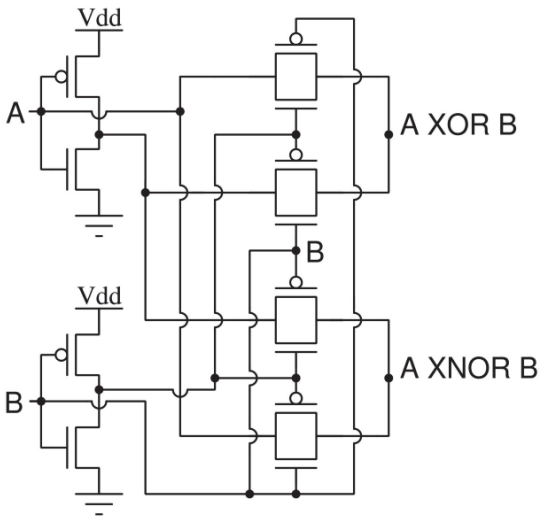

Figure 3: XOR-XNOR Module

3.2.2 Sum Module

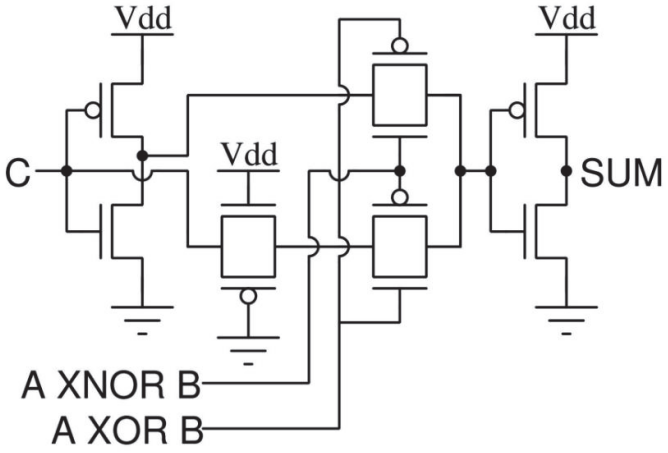

Figure 4: Sum Module-1

3.2.3 Carry Module

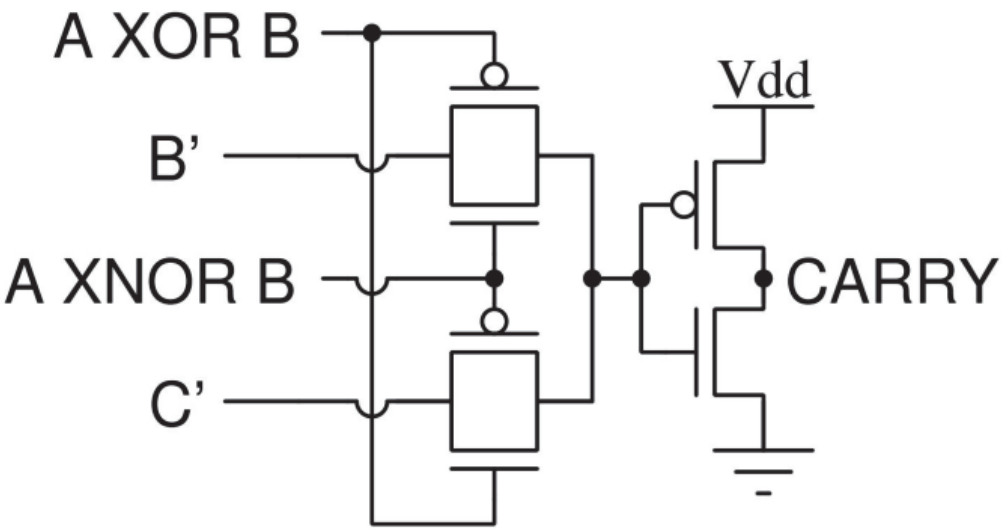

Figure 5: Carry Module-1

3.3 Simulation Result

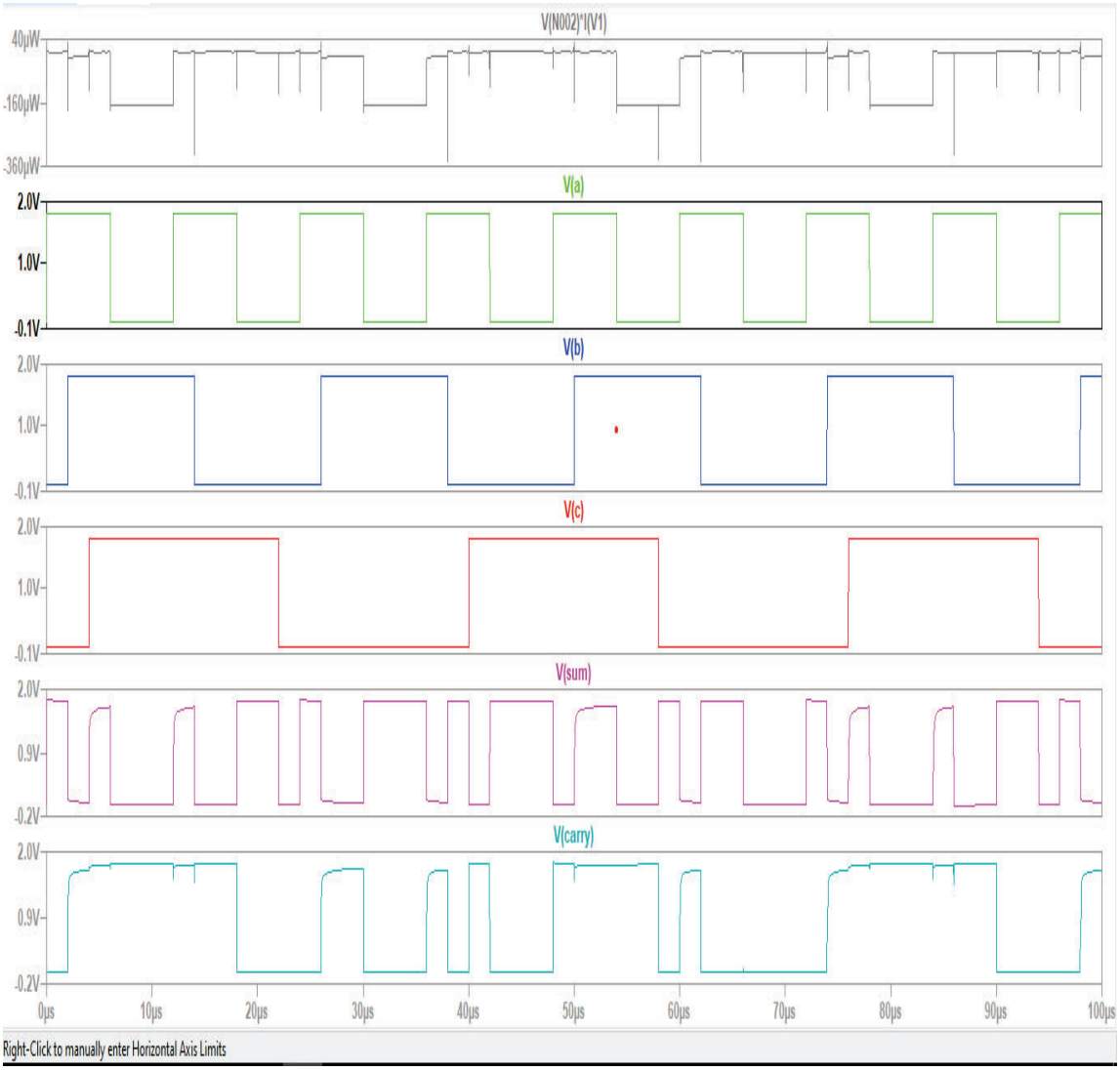

Figure 6: LT Spice Simulation Result

Chapter 4

CONCLUSION

This project explored the design of high-speed full adder architectures. Simulated in TSMC 180-nm CMOS technology using LT Spice, the proposed circuit demonstrates its functionality through waveforms showcasing the sum and carry outputs. However, these waveforms also reveal a degree of delay in both outputs. Additionally, the simulation quantifies the power dissipation of the circuit.