Abstract

A rapid growth in semiconductor technology due to which existing transistor switches face major drawbacks because of variation in various device parameters, manufacturing process and short channel effect. so, to overcome drawbacks we have to come up with a device which can enhance the device performance significantly. For this a Dual Material Gate (DMG) Junction less FINFET is a prominent solution which has a benefits of Dual material Gate as well as Junction less. In this thesis we will investigate how with the help of dual material gate we have a better electrostatic control over channel. We will also deal with effect on electrical performance due to various variation in geometrical parameters of device.

We are using Synopsis Sentaurus TCAD tool simulations, we analyzed the influence of variation in gate length, fin width, Work function between two different gate material. Key performance metrics analyzed include threshold voltage for various variation such as metal length to gate length ratio ,gate length , doping concentration and gate oxide thickness .The current characteristic for all these variation are recorded .Our results reveal that while the DMG structure inherently improves control over short-channel effects and exhibits robustness against certain dimensional variations, it remains sensitive to fluctuations in gate material properties.

It is demonstrated that the dual material gate configuration lessens the effects of fin width and gate length fluctuation, resulting in a more constant drive current and threshold voltage. However, the electrostatic integrity and threshold voltage stability of the device are greatly impacted by differences in the work function difference between the dual gate materials. The need for exact control over material parameters during manufacturing is highlighted by this sensitivity.

The findings from this study provide valuable insights into the design optimization of DMG Junctionless FinFETs. By identifying the critical parameters that influence device variability, this research aids in developing strategies to enhance manufacturing tolerances and improve overall device reliability.

Keywords: Dual material gate (DMG), Short channel effect, Junctionless, Threshold voltage, TCAD, Work function

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ABBREVIATIONS

SCE	-	Short channel effect
TCAD	-	Technology Computer Aided Design
JLT	-	Junction less transistor
DMG	-	Dual Material Gate
DIBL	-	Drain induced barrier lowering

Chapter 1

Introduction

Transistor architectures have advanced significantly as a result of the constant scaling of semiconductor devices in an effort to achieve greater performance and reduced power consumption. Alternative device topologies have been investigated since traditional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) face constraints at nanoscale dimensions. The Dual Material Gate (DMG) Junctionless FinFET is one of these that has shown promise in addressing the issues of variability, leakage currents, and short-channel effects in nanoscale devices [1].

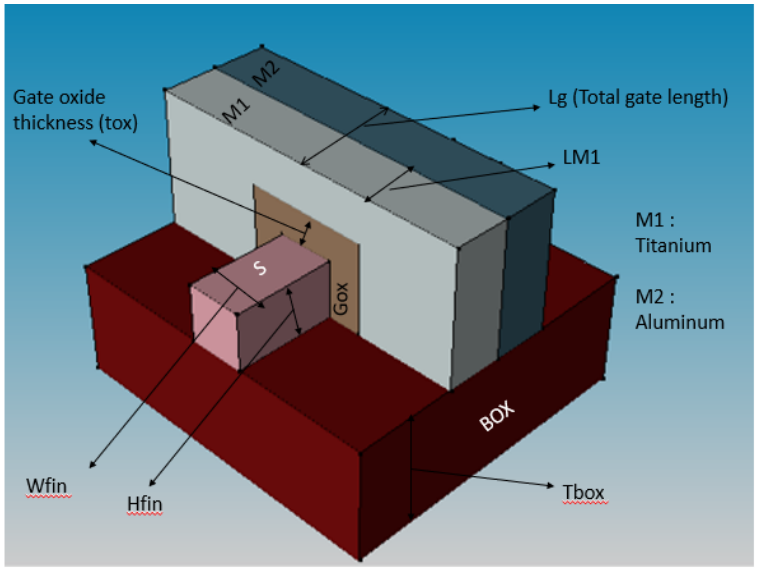

Figure 1.1: Dual material Gate Junction less FinFET

The Junctionless FinFET, characterized by its elimination of junctions between the source, drain, and channel, offers simplified fabrication processes and reduced doping-related variability. By combining this architecture with a Dual Material Gate, which employs two different gate materials with varying work functions, the electrostatic control of the channel is significantly enhanced.We will see that how DIBL (Drain induced barrier lowering) gets reduced and how overall device performance is getting improved.

The focus of this project is to conduct a variability study of DMG Junctionless FinFETs, investigating how process-induced variations affect the device's performance. Variation in Gate length, fin width , oxide thickness, work function difference etc are analyzed and shown that how this variation affect the performance and characteristics. [2].

This report contributes to the understanding and optimization of DMG Junctionless FinFETs. The insights gained from this study will aid in mitigating variability-related challenges and enhancing the robustness of nanoscale transistors, thereby supporting the continued scaling of semiconductor devices.

This project is structured to provide a comprehensive analysis, starting from the fundamental concepts of DMG Junctionless FinFETs, through the methodology employed for variability studies, to the results and design guidelines derived from the findings.

1.1 Motivation

The semiconductor industry has continuously pushed the boundaries of miniaturization, enabling faster, more efficient, and compact electronic devices. However, as transistor dimensions scale into the nanometer regime, traditional MOSFET architectures face critical challenges such as short-channel effects, high leakage currents, and increased process-induced variability. These issues threaten the reliability and performance of nanoscale devices, necessitating the exploration of innovative transistor designs.

The Junctionless FinFET stands out as a strong candidate to replace traditional junction-based MOSFETs, thanks to its several advantages. By removing the need for source and drain junctions, the manufacturing process becomes more straightforward, which is especially beneficial for developing devices at the nanoscale. Incorporating a Dual Material Gate (DMG) design further boosts its performance by enhancing control over the electric field and minimizing short-channel effects. This combination of technologies provides a promising approach to overcoming the challenges found in conventional transistor designs.

Although Dual Material Gate Junctionless FinFETs show great promise, variations in process parameters like gate length, fin size, oxide layer thickness, and material work functions present major challenges for their practical use. It's essential to understand how these fluctuations affect device performance to ensure they remain reliable, scalable, and suitable for manufacturing. This highlights the importance of a thorough study on variability to help improve and optimize the design[3].

1.2 Objectives

To Examine how variations caused during the manufacturing process—such as changes in gate length, fin width, oxide thickness, and differences in material work func-

tions—impact key device characteristics like threshold voltage, subthreshold slope, drive current, and leakage current.

Assess how using a Dual Material Gate setup improves control over the electric field, helps minimize short-channel effects, and boosts the overall reliability of the device when compared to junctionless FinFETs with a single gate material.

Carry out comprehensive simulations using TCAD software to study how Dual Material Gate Junctionless FinFETs perform under different conditions and to gain valuable insights into their behavior and variability.

Chapter 2

Literature Review

Fin Field-Effect Transistors (FinFETs) have emerged as a prominent solution to mitigate short-channel effects (SCEs) in nanoscale regimes. Among the various FinFET architectures, the dual-material gate (DMG) and junctionless (JL) structures have garnered significant attention due to their potential in enhancing device performance and manufacturability. This survey explores the existing literature on the variability studies of dual-material gate junctionless FinFETs (DMG-JLFETs), highlighting the key findings and identifying gaps for future research.

2.1 Junctionless Transistor Technology

Junctionless transistors, first proposed, eliminate the need for junctions between the source, drain, and channel, simplifying the fabrication process and reducing doping-related variability. Unlike conventional MOSFETs, where charge carriers are confined by p-n junctions, junctionless devices rely on the gate to control conduction. Studies have highlighted the following benefits:

- Reduced Short-Channel Effects: Tight gate control in junctionless architectures improves electrostatic integrity, mitigating issues such as threshold voltage roll-off and drain-induced barrier lowering (DIBL).

- Improved Variability Tolerance: Junctionless devices are less sensitive to random dopant fluctuations, offering enhanced uniformity and reliability.

- Fabrication Simplicity: The absence of junctions reduces doping gradients and diffusion complexities, making junctionless devices easier to manufacture at nanoscale dimensions [4].

2.2 Structure of device

FinFETs, with their three-dimensional (3D) fin structure, have become the standard for sub-22nm technologies. Their vertical channel design enhances gate control, reduces leakage currents, and minimizes short-channel effects. Junctionless FinFETs leverage the advantages of both junctionless and FinFET technologies:

- Better Electrostatic Control: The 3D structure improves gate control over the channel.

- Scalability: FinFETs are well-suited for further scaling due to their excellent electrostatic performance and reduced parasitic effects.

2.3 Dual Material Gate (DMG) Technology

The Dual Material Gate concept, introduced by Long et al., employs two different gate materials with varying work functions to improve device performance. The DMG structure provides [5]:

- Improved Electrostatic Control: The work function difference between both gate materials creates a step potential, reducing DIBL and improving threshold voltage stability.

- Enhanced Drive Current: The step potential accelerates carrier flow, increasing the drive current.

- Reduced Short-Channel Effects: DMG technology mitigates threshold voltage roll-off, making it suitable for nanoscale devices.

2.4 Variability Challenges in Nanoscale Devices

Process-induced variability, such as fluctuations in gate length, fin dimensions, oxide thickness, and material properties, significantly impacts device performance. Key findings from prior research include [6]:

- Threshold Voltage Variability: Variations in gate material work function and fin dimensions lead to significant threshold voltage fluctuations, affecting device reliability

- Impact of Oxide Thickness: Inconsistent gate oxide thickness introduces variability in gate capacitance, impacting device performance.

- Work Function Variability: Differences in gate material properties in DMG structures amplify variability concerns, requiring precise material control during fabrication.

2.5 Simulation and Modeling Techniques

Technology Computer-Aided Design (TCAD) tools are widely used to model and analyze the behavior of nanoscale devices. Research has demonstrated that TCAD simulations are effective in:

- Providing insights into electrostatic potential distribution and current flow in DMG Junctionless FinFETs.

2.6 Comparative Analysis

Comparisons between DMG-JLFETs and other FinFET architectures indicate that the dual-material gate junctionless approach offers enhanced immunity to variability. The straightforward fabrication of Junctionless devices minimizes sources of variation, and the Dual Material Gate structure enhances control over the electric field. Together, these features lead to better overall performance and greater reliability of the device.

2.7 Challenges and Gaps

While DMG-JLFETs offer several promising benefits, there are still unresolved challenges in fully grasping their variability. Much of the current understanding is based on simulation results, with limited experimental data available for validation. Moreover, the effects of factors like line edge roughness and changes in fin width remain underexplored. Further research is also needed to examine how high-k dielectrics and metal gate integration influence device variability.

Chapter 3

Dual Material Gate Junctionless FinFET

3.1 Introduction

Synopsys Sentaurus TCAD is an all-encompassing simulation platform that facilitates the modeling of semiconductor devices across process, device, and system levels. It enables in-depth analysis of device performance by solving core semiconductor equations, integrating different physical models, and handling intricate geometries. In this project, Sentaurus TCAD was used to design and simulate a dual-material gate junctionless FinFET (DMG-JLFET), offering valuable insights into its electrical behavior and variability factors.

3.2 Threshold voltage extraction

A dual-material gate junctionless FinFET's threshold voltage is a crucial component that establishes the voltage at which the device begins to conduct a discernible quantity of current. Analyzing and improving the device's performance requires knowing the threshold voltage.
In this thesis threshold voltage is extracted by gate voltage at which the current through the transistor is $\frac{effectivefinwidth}{totalgatelength}$ X 10^{-7} A/um .An effective fin width = 2hfin + wfin [1].

In a dual-material gate setup, the threshold voltage is affected by the work function difference between the two gate materials, leading to a non-uniform electric field across the channel. This distinctive characteristic helps mitigate short-channel effects, reduce leakage current, and boost overall device performance. Accurate extraction and optimization of the threshold voltage are crucial for designing high-performance and reliable devices.

3.3 Device Structure Design

The DMG-JLFET was designed with a 3D structure to effectively model the impacts of the fin geometry and dual-material gate. The primary dimensions and materials

selected for the device are as follows: [1]:

Parameter	Dimension
Total gate length (Lg)	10nm
Fin height (Hfin)	5nm
Fin width (Wfin)	5nm
Gate Oxide Thickness (tox)	3nm
Gate metal 1 length (LM1)	5nm
Gate metal 2 length (LM2)	5nm
Gate oxide (Gox)	HfO2
Burried oxide (Box)	Sio2
Channel dopant type	donor
Channel dopant concentration	10e+18
source drain length	9nm

Table 3.1: Dimension and material of the given 3d structure of dual material gate junctionless finFET

3.4 Doping Profile

- Uniform Doping: n type , doped with phosphorus
- Source and Drain Regions: The device uses the junctionless principle, which means that there is no extra doping and that the doping is consistent across the source, channel, and drain.

3.5 Device Layout

The device was created using Sentaurus Structure Editor (SDE), allowing precise control over the geometric parameters. The dual-material gate was meticulously defined to accurately reflect the work function difference along the channel length.
This image displays a 3D device model generated with the Sentaurus Structure Editor (SDE), a widely used tool for designing and simulating semiconductor structures. The visualization highlights a FinFET-like geometry, with clearly defined layers and regions that represent various materials and functional components of the device.
The structure consists of multiple elements, including the substrate at the bottom, the fin, and surrounding layers that represent the metal contacts and dielectric regions. The substrate, shown in red, serves as the base layer, providing mechanical support and acting as the bulk material. The fin, depicted as a vertical structure in the center, functions as the main channel for carrier transport. On either side of the fin are gate

and dielectric layers that regulate the conductivity of the channel, as illustrated in Figures 3.1 and 3.2.

The colors and shapes in the structure suggest that the materials used include Aluminum and Titanium, as detailed in the command log at the bottom of the image. These metals are commonly chosen for gate and contact formation due to their advantageous electrical properties, such as work function and conductivity. The gray area at the top likely represents the gate material, while the brown and pink regions indicate specific parts of the metal stack or interconnects, as shown in Figure 3.1.

This structured modeling approach is essential for evaluating the device's electrical characteristics and performance across different operating conditions.

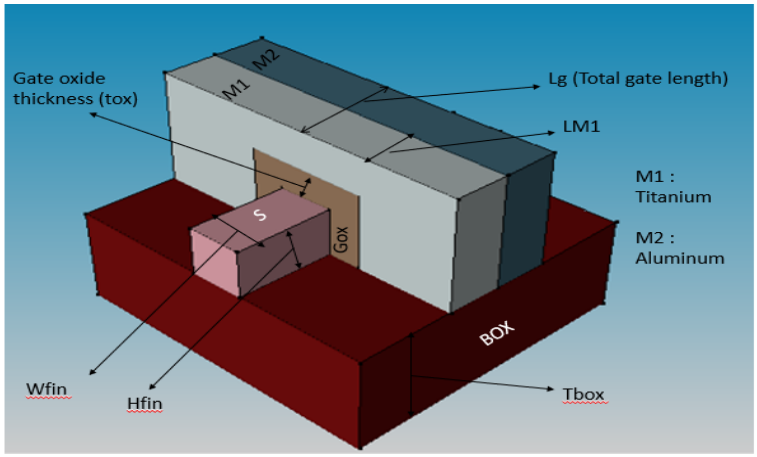

Figure 3.1: 3D Structure of FinFET

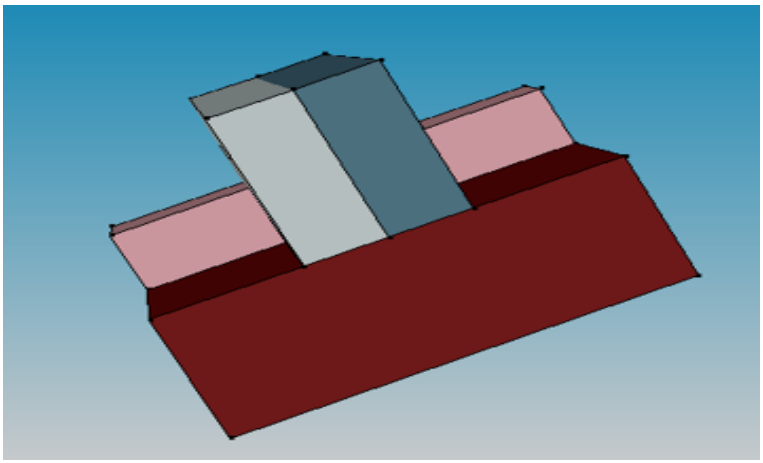

Figure 3.2: Other side view of FinFET

3.6 Meshing Strategy

A non-uniform mesh was employed to optimize simulation accuracy and computational efficiency.Fine Mesh Regions in the channel, gate and Around the fin edges and

at the interface between two metals of gate.The metal M1 is titanium and metal M2 is aluminium. The titanium is having higher workfunction so that side is source and lower workfunction side which is aluminium is drain . The meshing strategy ensured that critical regions with high electric field gradients were adequately resolved. Higher meshing grid points will give more accurate results but will take more time to execute. In this project more than 10000 grid points has been taken [7].

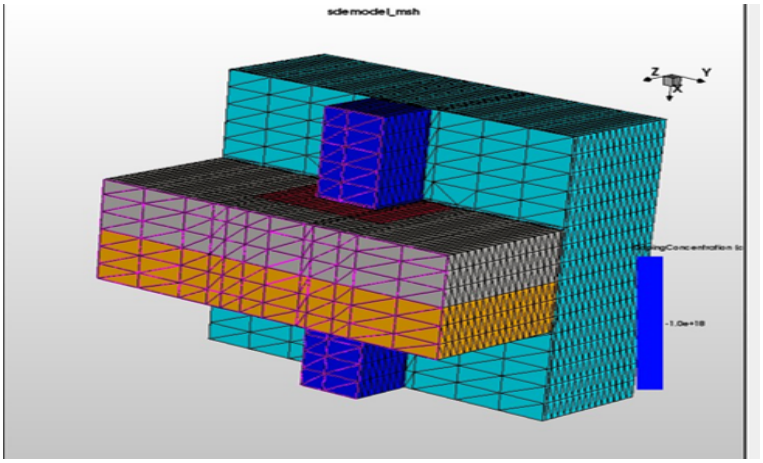

Figure 3.3: Meshing of finFET

This figure depicts a 3D meshed model of a FinFET structure, which is commonly used in semiconductor device simulations. The visualization represents the spatial discretization of the device geometry into smaller finite elements or meshes, enabling numerical analysis of the physical and electrical properties using simulation tools.
The structure consists of distinct regions with different colors and mesh densities, each representing specific parts of the FinFET. For example, the vertical region in the middle corresponds to the fin, which is the channel through which current flows. The base and surrounding areas indicate the source and drain terminals, while the top region corresponds to the gate terminal that modulates the channel conductivity. The color gradient within certain regions corresponds to doping concentrations, as indicated by the color legend on the right-hand side. The blue shading with the annotation "1.0e+18" signifies a high doping concentration which is typical for heavily doped source/drain regions to ensure efficient carrier injection as shown in figure 3.3.

3.7 Physics Model

Accurate simulation of semiconductor devices requires the incorporation of comprehensive physical models that capture the behavior of carriers under various operating conditions. In the simulation of the dual-material gate junctionless FinFET using Synopsys Sentaurus TCAD, several critical physics models were employed to ensure realistic representation of device performance. This section details the following models: Field dependent mobility model, generation-recombination model and band to band tunneling model, quantum effects [8].

3.8 Contacts

For standard operation,both metals were electrically shorted to form a single gate contact. Source and drain also have contact as shown in figure 3.4.

3.9 Sentaurus tool flow

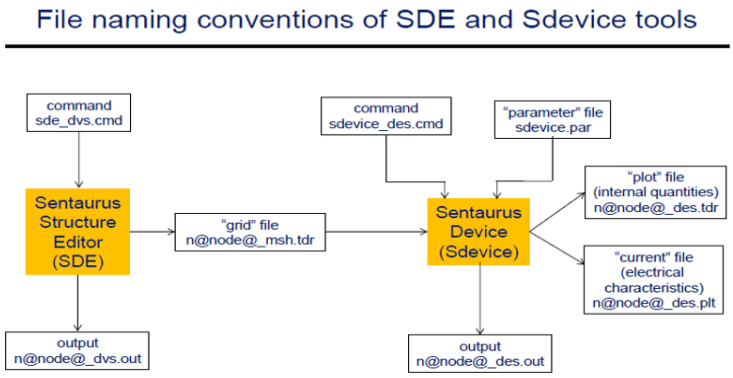

Figure 3.4: Simulation tool flow

The diagram explains the file naming conventions and workflow for Sentaurus Structure Editor (SDE) and Sentaurus Device (Sdevice) tools, commonly used in TCAD simulations for semiconductor device modeling and analysis.

3.9.1 Sentaurus Structure Editor (SDE)

Purpose: SDE is used to define the physical structure of the device (e.g., materials, regions, and geometries).

- The sdedvs.cmd file holds the commands and parameters required to define the device structure.
- The "grid file" named n@node@msh.tdr is generated by SDE, containing the meshing details of the device structure. This file is then used by the Sdevice tool for simulation.

3.10 Work function defined in sdevice script

The work function values for the metals chosen in this study were based on their material properties and their relevance to the experimental setup. Aluminum, with a work function of 4.28 eV, and Titanium, with a work function of 4.66 eV, were selected as the primary metals. These values indicate the energy required to detach an electron from the metal's surface to the vacuum level, which is essential for understanding the metals' behavior in the device. The choice of these materials was influenced by their

compatibility with the device structure and their impact on overall performance. A drain-to-source voltage (Vds) of 0.7 V and a gate-to-source voltage (Vgs) of 1.2 V were applied to the FinFET device.

Physics (Material = "Aluminum")
MetalWorkfunction (Workfunction= 4.28)
Physics (Material = "Titanium")
MetalWorkfunction (Workfunction= 4.66)

3.11 Transfer Characteristic

The relationship between a dual-material-gate (DMG) junctionless FinFET's drain current and gate-to-source voltage is depicted in this graph. When examining the device's performance, the plot offers important information about its current conduction properties as a function of the applied gate voltage.

The curve displays a FinFET's predicted behavior. Since there is not enough gate voltage to cause conduction in the channel, the drain current is initially very small at low gate voltages. The subthreshold operation, in which the current grows exponentially with gate voltage, is represented by this region. The channel becomes conductive and the drain current rapidly increases as the gate voltage rises above the threshold voltage, signaling the change to the linear and saturation periods of operation.

The device has attained its maximum current drive capability for the specified bias circumstances, as seen in figure 3.5, when the current in the saturation zone steadily increases due to the short channel effect as the gate voltage keeps increasing.

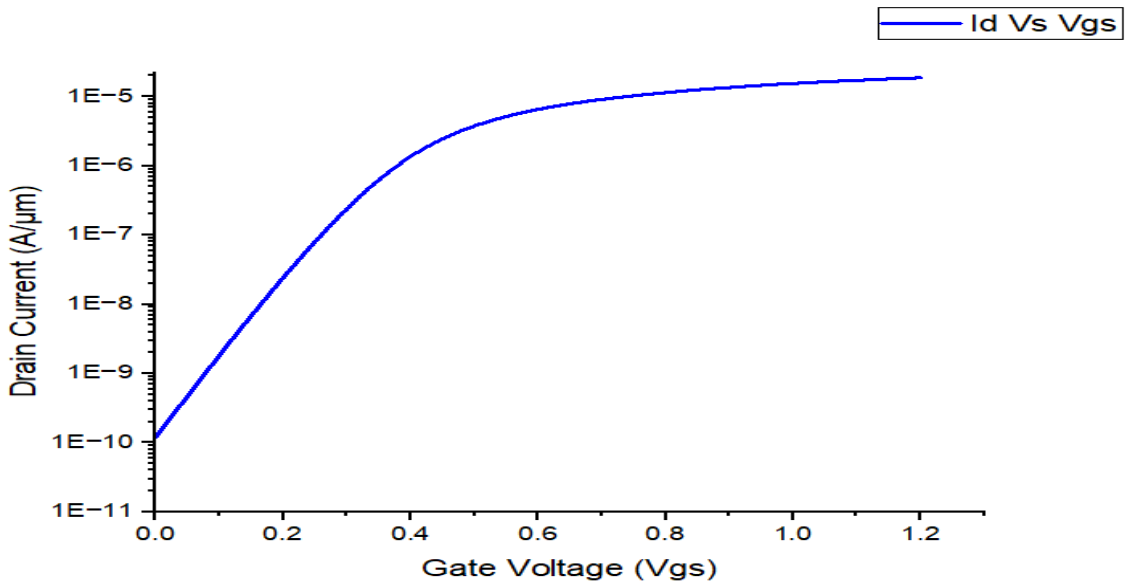

Figure 3.5: I-V characateristic

Chapter 4

Simulation Results for variation in different parameter

4.1 Transfer Characteristic of Various doping concentration

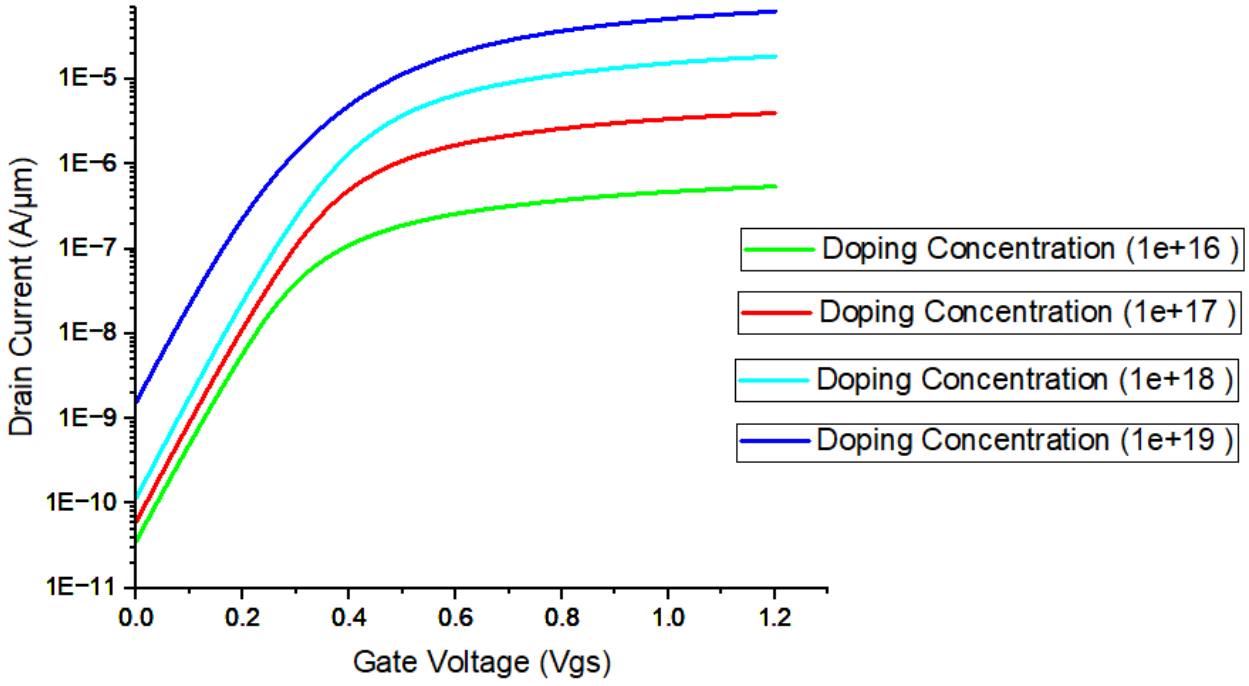

Figure 4.1: Transfer characteristic of various doping concentration

This graph represents the relationship between the gate-to-source voltage and drain current for a dual-material-gate (DMG) junctionless FinFET across various doping concentrations. The curves illustrate how the doping concentration in the device's channel impacts its electrical characteristics, particularly the drain current, for a given gate voltage as shown in figure 4.1.

- Impact of Doping on Current: The drain current at a given gate voltage rises with increasing doping concentration. This is due to the fact that higher doping levels increase the channel's carrier availability, which raises current flow.
- Threshold Voltage Behavior: The drain current begins to increase noticeably at higher gate to source voltages with lower doping concentrations, suggesting a bigger threshold voltage.
- For higher doping concentrations, the current starts increasing at lower gate to source voltage which implies a reduction in the threshold voltage.
- Saturation and On-State Current: The curves tend to saturate at increasing gate voltages, signifying the maximum current that the device is capable of producing. Higher doping levels result in an increase in the saturation current.

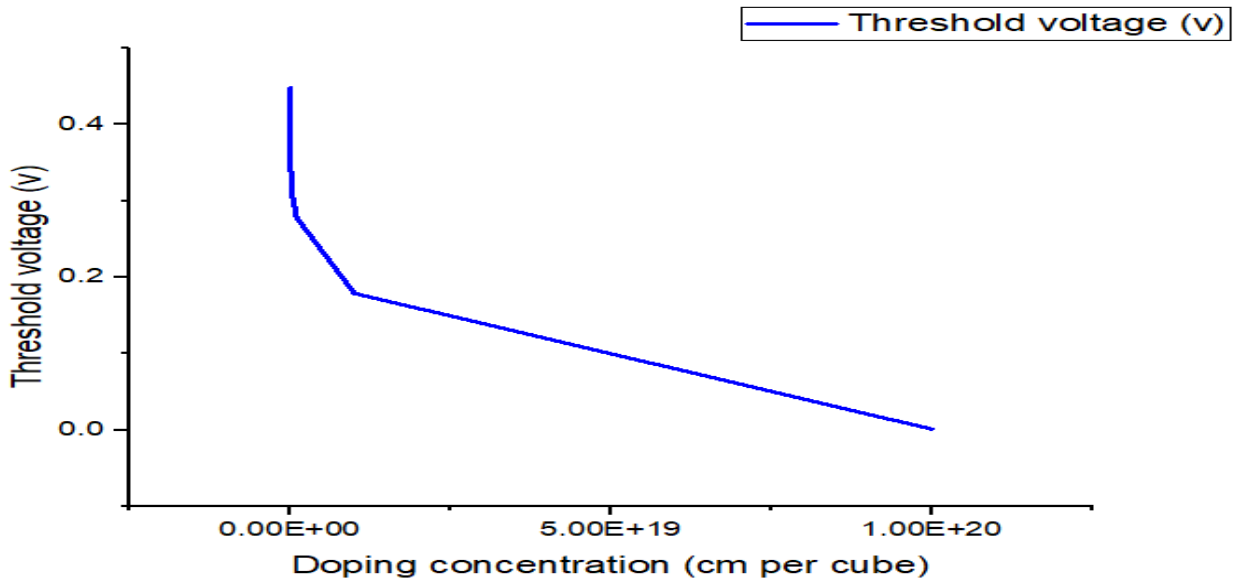

Figure 4.2: Threshold voltage vs doping concentration

The graph illustrates the relationship between the threshold voltage and the doping concentration for a dual-material-gate (DMG) junctionless FinFET. This plot is critical for understanding how the doping level in the channel influences the device's threshold voltage, a key parameter for its electrical performance.

The threshold voltage is plotted on the vertical axis, measured in volts (V), while the doping concentration is plotted on the horizontal axis in units of per cm cube as shown in figure 4.2.

The graph shows a clear trend: as the doping concentration increases, the threshold voltage decreases. This behavior can be attributed to the physics of the junctionless FinFET. In a junctionless design, the conduction channel is created directly in the doped silicon without a junction, and the gate voltage modulates the carriers in the

channel. At higher doping concentrations, the carrier density is naturally higher, which reduces the gate voltage required to induce conduction, thereby lowering the threshold voltage.

At lower doping concentrations, the threshold voltage is relatively high, meaning a higher gate voltage is required to activate the device. However, as the doping concentration increases to approximately 10 to the power 19 per cubic centimeter, the threshold voltage starts to decrease more sharply

The reduction in threshold voltage with increasing doping concentration illustrates a key trade-off in designing DMG junctionless FinFETs. Although higher doping concentrations lower the threshold voltage, improving the device's performance in high-speed and low-voltage applications, they can also result in higher leakage current and other negative effects, such as diminished gate control over the channel.

This analysis is essential for designing dual-material-gate junctionless FinFETs, as doping concentration has a direct impact on the device's electrical properties. It highlights the importance of optimizing the doping concentration in DMG junctionless FinFETs to strike the right balance between a low threshold voltage and effective control over the channel, ensuring efficient and reliable operation across different applications.

Table 4.1: Doping Concentration effect on Threshold Voltage

Doping concentration (cm^{-3})	Threshold voltage (V)
10^{16}	0.4483
10^{17}	0.316
10^{18}	0.278
10^{19}	0.179

4.2 Transfer characteristic of various Gate oxide thickness (tox)

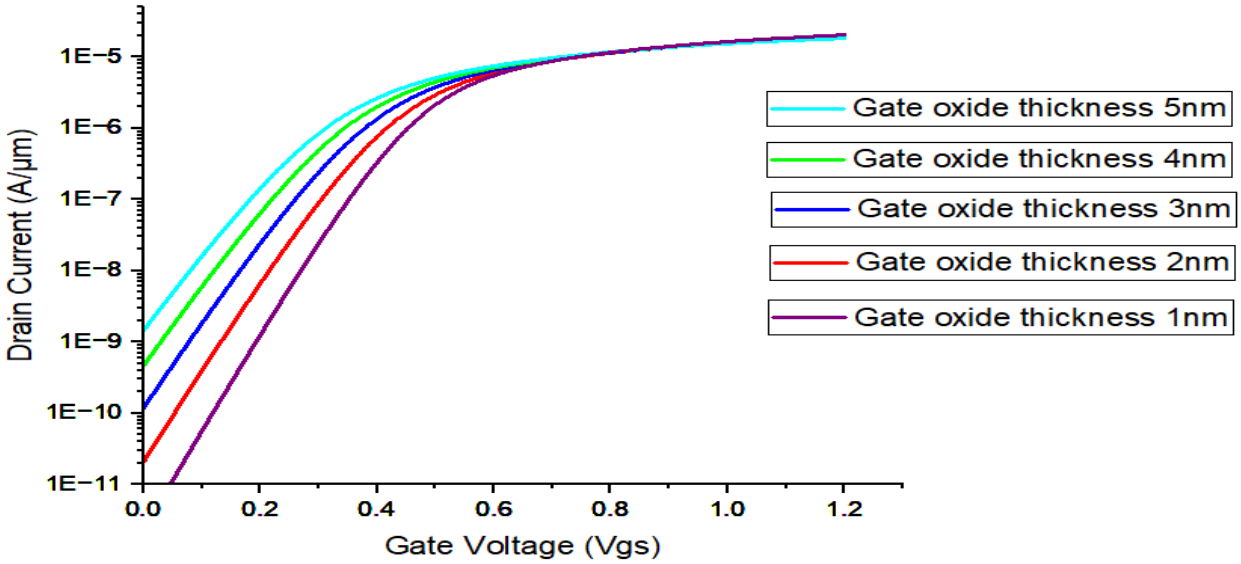

Figure 4.3: Transfer characteristic of various gate oxide

The graph shows how a dual-material-gate (DMG) junctionless FinFET's drain current and gate-to-source voltage relate to one another, emphasizing the impact of variations in gate oxide thickness. Because it affects the gate's control over the channel, the oxide thickness plays a crucial role in defining the electrical performance of the device.

According to the caption, the curves depict various gate oxide thicknesses, which range from 1 nm to 5 nm. Each graph shows how the device's current response to changes in gate-to-source voltage is affected by variations in the gate oxide thickness.

The graph shows that for a given gate voltage, the drain current increases as the gate oxide thickness decreases. Thinner oxide layers give the gate more control over the channel, which explains this phenomenon. Higher current flow results from a more efficient regulation of the carrier concentration in the channel caused by a thinner oxide, which also improves the coupling between the gate voltage and the channel.

For devices with thicker gate oxides (e.g., 5 nm), the drain current is relatively lower for the same gate to source voltage as the gate's electric field is less effectively transmitted to the channel. This results in reduced gate control, requiring higher gate voltages to achieve similar levels of current compared to devices with thinner oxides as shown in figure 4.3.

The saturation region, where the drain current reaches at higher gate to source voltage, also shifts with oxide thickness, reflecting the varying impact of the gate control strength on the device's performance. Devices with thinner oxides saturate

at higher current levels, which is advantageous for high-speed and low-power applications.

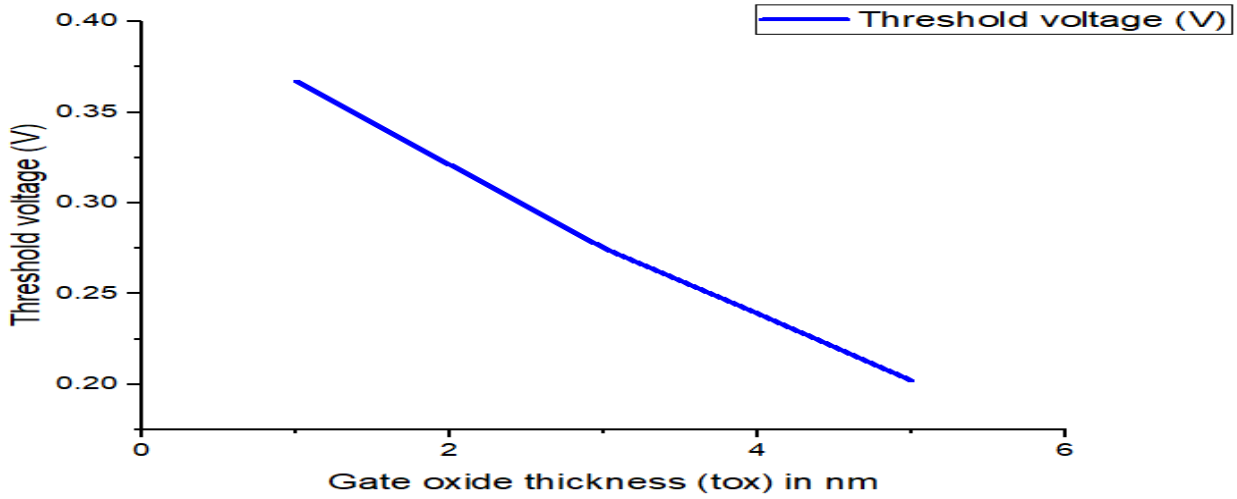

Figure 4.4: Threshold voltage vs gate oxide

Table 4.2: Gate oxide thickness (tox) on Threshold Voltage

Gate oxide thickness (tox) in nm	Threshold voltage (V)
1	0.367
2	0.321
3	0.275
4	0.239
5	0.202

This graph emphasizes the critical role of gate oxide thickness in optimizing the performance of DMG junctionless FinFETs. While thinner oxides improve gate control and current drive capabilities, they may also lead to increased leakage currents and reliability concerns due to higher electric fields. Therefore, selecting an appropriate oxide thickness as shown in figure 4.4.

This graph illustrates the relationship between the threshold voltage and the gate oxide thickness.

When the gate oxide is thinner, the gate's electric field couples more strongly to the channel, enhancing its ability to control the carrier concentration. This stronger coupling requires a higher voltage to deplete the channel completely, leading to a higher threshold voltage. Conversely, as the oxide thickness increases, the electric field from the gate is less effectively transmitted to the channel, weakening the gate's control. This results in a reduction of the threshold voltage, as less voltage is needed to modulate the channel's carrier concentration.

4.3 Varying the length ratio of Metal 1 (M1) to the total gate width

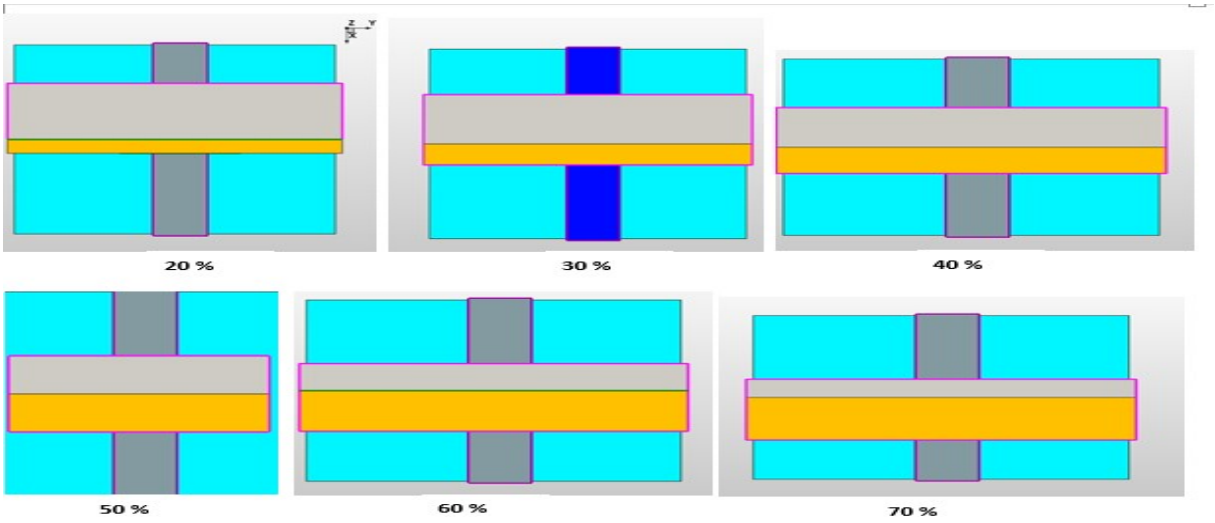

Figure 4.5: Variation in gate length ratio

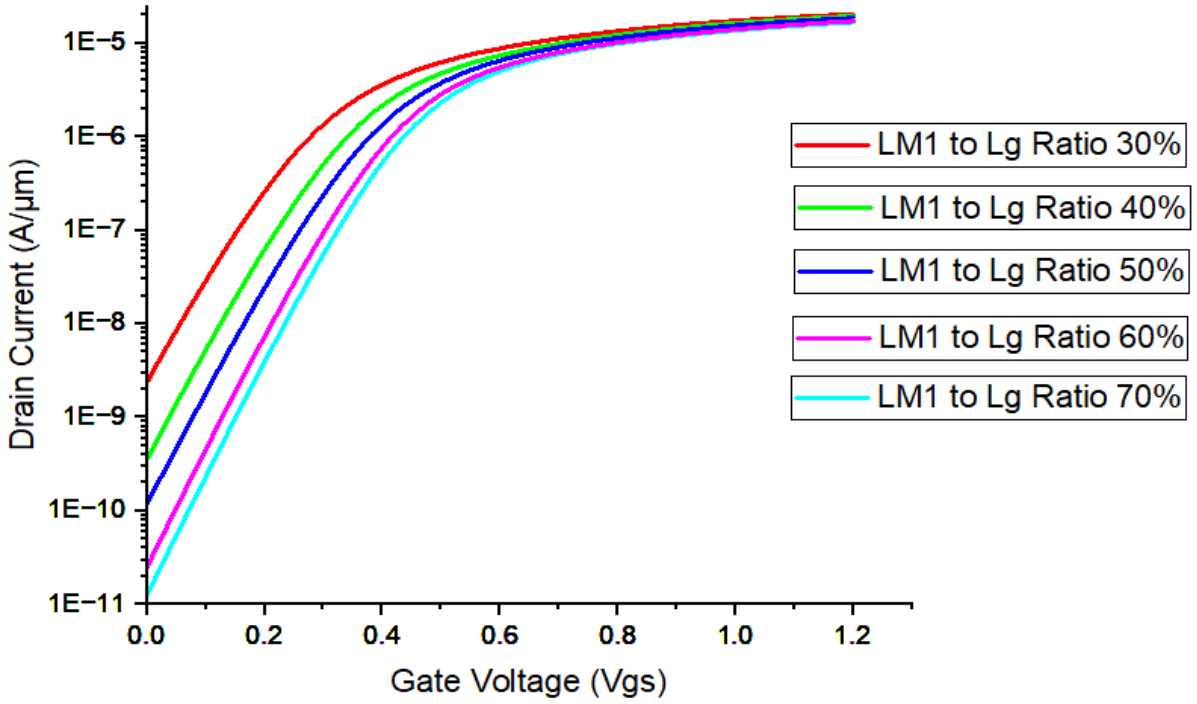

Figure 4.6: Variation in gate length ratio

The relationship between the gate-to-source voltage and drain current for a dual-material-gate junctionless FinFET is depicted in the graph in figure 4.5. The analysis

explores the impact of varying the length ratio of Metal 1 (LM1) to the total gate length (Lg) on the device's electrical performance. In this structure, Metal 1 (M1), made of titanium, is located closer to the source terminal, while Metal 2 (M2) is aluminium which completes the remaining portion of the gate length, forming the total gate length.

Each curve corresponds to a different LM1 to Lg ratio, ranging from 30% to 70%, as specified in the plot. The variation in the ratio alters the distribution of the gate's electrostatic influence over the channel, thereby affecting the device's current response.

The graph as shown in figure 4.5 reveals that as the M1-to-total gate length ratio increases, the drain current for a given gate to source voltage decreases. When M1 occupies a smaller fraction of the total gate length (e.g., 30%), the contribution of M2, which has a different work function, dominates the gate control. This configuration leads to higher carrier modulation and, consequently, a higher drain current. On the other hand, as the M1-to-total gate length ratio increases (e.g., 70%), the influence of M1 grows, reducing the overall gate control effectiveness due to the weaker contribution of M2.

The dual-material-gate design takes advantage of the differing work functions of the metals (titanium for M1 and another metal for M2) to create an electric field gradient along the channel. This gradient helps improve the carrier transport and reduces short-channel effects. The exact ratio of M1 to total gate length significantly impacts the threshold voltage and on state current.

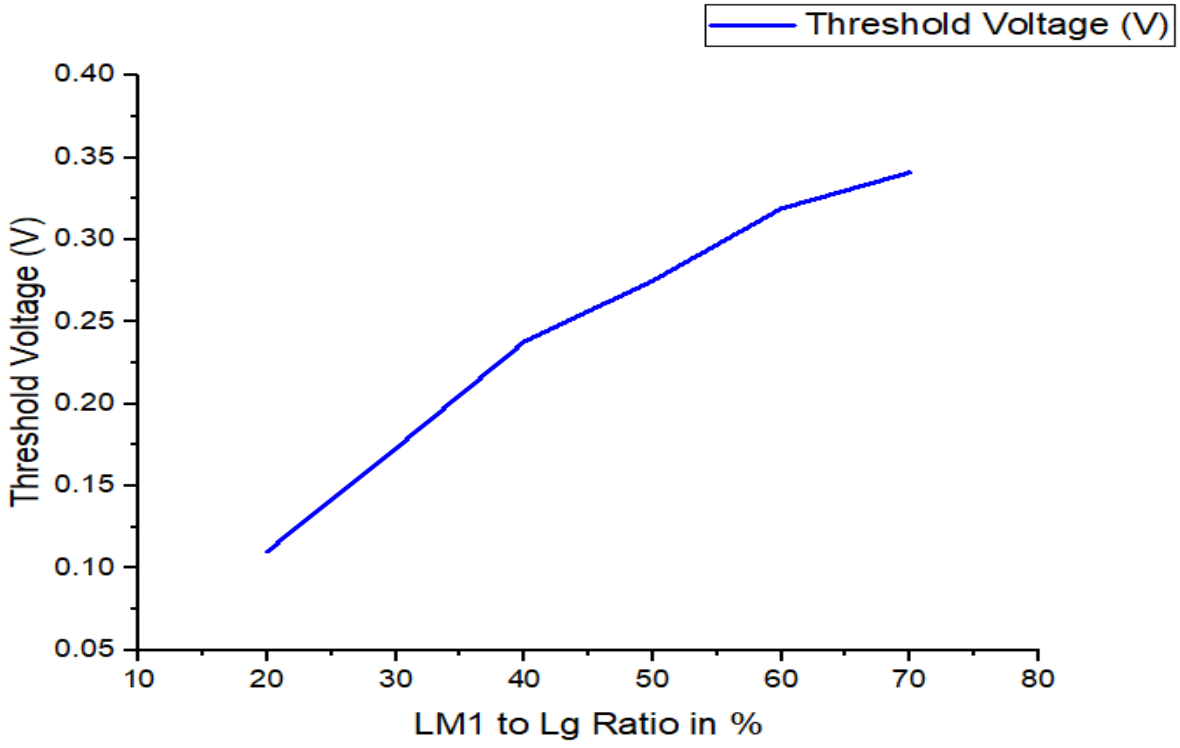

Figure 4.7: Threshold voltage vs LM1 to Lg ratio

Table 4.3: LM1 to Lg Ratio in % effect on Threshold Voltage

LM1 to Lg Ratio in %	Threshold voltage (V)
20	0.1104
30	0.173
40	0.238
50	0.275
60	0.319
70	0.341

This graph as shown in figure 4.6 illustrates the relationship between the threshold voltage and the ratio of Metal 1 (M1) length to the total gate length in a dual-material-gate (DMG) junctionless FinFET. The horizontal axis represents the LM1 to Lg ratio in percentage, while the vertical axis shows the threshold voltage in volts (V).

The curve as shown in figure 4.6 indicates that the threshold voltage increases as the LM1 to Lg ratio grows. This trend is directly linked to the electrostatic effects caused by the relative proportions of Metal 1 and Metal 2 in the dual-material-gate structure. Metal 1, positioned closer to the source, has a specific work function that influences the electric field distribution and, subsequently, the channel's carrier modulation.

Because of its greater fraction in the gate, Metal 2's contribution predominates when the LM1 to Lg ratio is low (for example, 20–30%). The threshold voltage is lowered by this arrangement because it produces a higher electric field gradient along the channel. Metal 1 takes up more space in the gate when the LM1 to Lg ratio rises. Due to its distinct work function, Metal 1's growing dominance causes the electric field gradient to decrease and its influence over the channel to deteriorate, raising the threshold voltage.

This graph underscores the importance of optimizing the M1-to-total gate length ratio in dual-material-gate junctionless FinFETs. A lower ratio enhances current drive and improves performance, while a higher ratio may offer better control over leakage and other undesirable effects.

4.4 Drain Induced Barrier Lowering (DIBL)

A device's short-channel effect is called DIBL. As the drain voltage increases V_{DS}, the threshold voltage V_{th} decreases as a result of the drain voltage's influence on the potential barrier at the source.

The basic idea is that the drain's depletion region extends closer to the source in short-channel devices. The barrier for electrons (or holes) to move from the source to the drain is essentially lowered by this interaction, which also lessens the gate control

over the channel. Consequently, at larger drain voltages, the gadget switches on more readily.

4.4.1 Calculation of DIBL

Two different V_{DS} value is supplied as V_{DS1} = 0.1VDD and V_{DS2} =VDD. VDD is 0.7 V and 0.1VDD is 0.07 V.The threshold voltage correspond to V_{DS1} is suppose V_{th1} and V_{DS2} is V_{th2}. Change in threshold voltage ΔV_{th} = V_{th1} - V_{th2} and ΔV_D = V_{VDD} - $V_{0.1VDD}$. DIBL is calculated by formula $\frac{change\ in\ threshold\ voltage}{change\ in\ drain\ voltage(0.7-0.07=0.63)}$.

4.4.2 DIBL value with Variation of LM1 to Lg length ratio

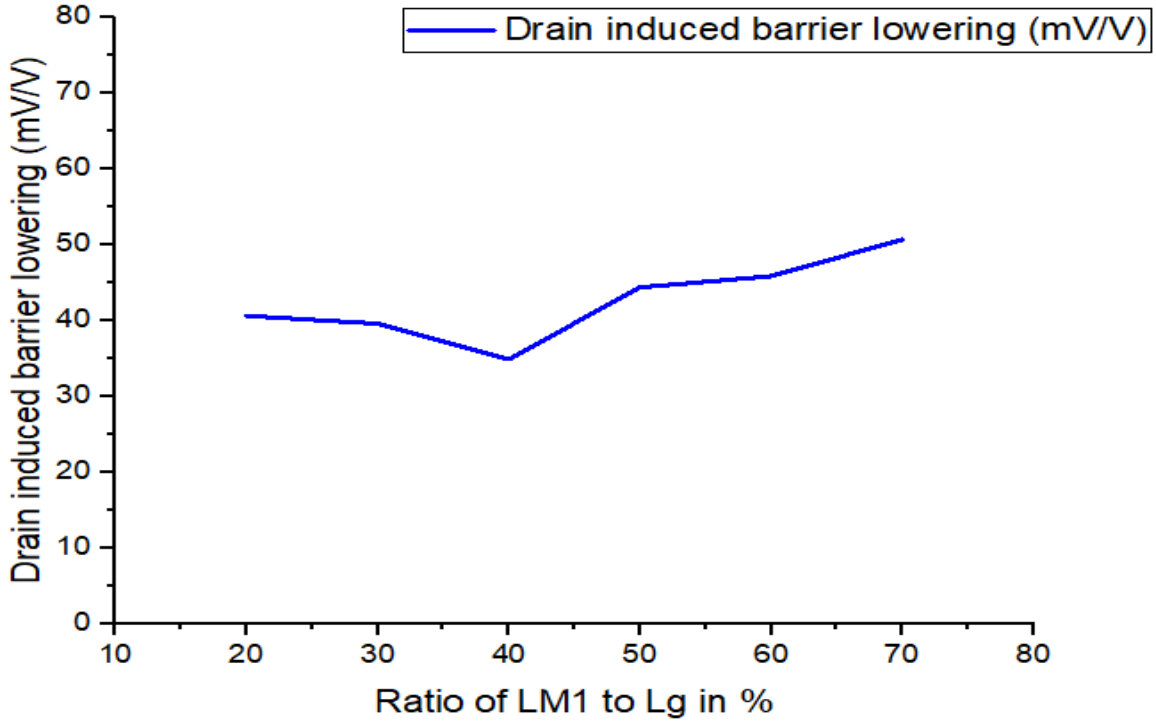

Figure 4.8: DIBL value at various Ratio of LM1 to Lg ratio

The graph as shown in fig 4.7 demonstrates the relationship between Drain-Induced Barrier Lowering (DIBL) and the percentage ratio of Metal 1 Length (LM1) to the total Gate Length (Lg) in a Dual Material Gate Junctionless FinFET structure. Here, Metal 1 is Titanium, and Metal 2 is Aluminum.

As the proportion of LM1 to Lg changes, DIBL exhibits a non-linear trend. At smaller LM1 ratios, DIBL initially remains low, indicating effective gate control. As the ratio increases, DIBL decreases slightly, reaching a minimum value, showcasing the optimal configuration for minimizing short-channel effects. However, beyond this optimal ratio, DIBL begins to rise steadily, implying that an excessive contribution from Metal 1 (Titanium) weakens the gate's ability to suppress the effect of drain

voltage on the source-to-channel potential barrier.

Increasing the proportion of Titanium beyond a certain point reduces the beneficial effects of the dual-gate configuration, leading to higher DIBL.

This behavior underscores the importance of achieving the right balance between the lengths of the two gate materials to optimize device performance, minimizing DIBL while maintaining strong electrostatic control in the channel.

Table 4.4: LM1 to Lg Ratio effect on Drain induced barrier lowering

Ratio of LM1 to Lg in %	Drain induced barrier lowering (mV/V)
20	40.63
30	39.6
40	34.9
50	44.4
60	45.87
70	50.7

Chapter 5

Conclusion

The project titled **"Dual-Material Gate Junctionless FinFET"** ,this study offers an in-depth analysis of how design parameters affect the threshold voltage and overall device performance. By employing a dual-material gate structure with Titanium (Metal 1) and Aluminum (Metal 2), the research investigates improvements in electrostatic control, reduction of short-channel effects, and optimization of the device for nanoscale applications. The selection of these materials is key to achieving the desired work function difference, which is critical for fine-tuning the device's characteristics.

Finding the threshold voltage from the device's transfer characteristics—specifically, the drain current against gate-to-source voltage curves—is the main goal of the study. Key parameters, including doping concentration, gate oxide thickness, and the ratio of Metal 1 gate length to the total gate length (M1:Lg), were carefully varied in simulations to provide a comprehensive knowledge of the behavior of the dual-material gate junctionless FinFET. The findings unequivocally demonstrate that these parameters affect the threshold voltage:

- **Doping Concentration**: Changes in channel doping have a notable effect on the threshold voltage, with higher doping concentrations causing a shift in the threshold voltage. This highlights the importance of precise doping control to optimize performance and ensure the device operates reliably under various conditions.

- **Gate Oxide Thickness**: The simulations show that decreasing the gate oxide thickness improves the electrostatic coupling between the gate and the channel, which lowers the threshold voltage and enhances gate control. This finding emphasizes the trade-off between adjusting the threshold voltage and managing leakage, which is vital for designing nanoscale devices.

- **M1:Lg Ratio**: The dual-material gate structure allows for customized adjustments to the threshold voltage via the M1:Lg ratio. By fine-tuning the lengths of the Titanium and Aluminum gates, the device achieves a more favorable electrostatic potential distribution and enhances the suppression of short-channel effects, a key challenge in contemporary transistor design.

The findings of this study underscore the advantages of the dual-material gate architecture in enhancing device performance and reliability. The ability to control

the threshold voltage by tuning material properties and structural parameters makes the DMG junctionless FinFET a promising candidate for high-performance and low-power applications. Furthermore, the methodology employed for threshold voltage extraction, combined with the analysis of parameter variations, provides a systematic approach for device optimization.

In conclusion, this project highlights the versatility of dual-material gate junctionless FinFETs while deepening the understanding of how material and structural decisions impact transistor behavior at the nanoscale. The findings from this study provide a solid foundation for future improvements in FinFET design, helping to pave the way for the development of efficient and reliable electronic devices in next-generation technologies.

5.1 Future Scope

The future scope of the study on **Dual-Material Gate (DMG) Junctionless FinFETs** is vast, with numerous opportunities for advancements and applications in the realm of nanoscale semiconductor devices. The insights gained from this project can serve as a foundation for further exploration in the following areas:

- **Scaling Challenges:** As technology nodes continue to scale down, further studies on the impact of extreme scaling on DMG junctionless FinFETs are necessary. The exploration of sub-5 nm nodes could provide valuable insights into the physical and quantum mechanical effects that dominate at these scales.

- **Multi-Material Gates:** Extending the dual-material gate concept to multi-material gate structures could enable even greater flexibility in threshold voltage tuning and device optimization for specific applications such as analog, digital, or mixed-signal circuits.

- **Thermal and Reliability Studies:** Future research could focus on the thermal stability of the DMG junctionless FinFET, particularly with materials like Titanium and Aluminum, and investigate how these devices perform under prolonged operation and high-temperature conditions. Reliability studies on device degradation mechanisms such as hot carrier injection (HCI) and bias temperature instability (BTI) will be crucial.

- **Low-Power Applications:** The findings of this study can be extended to design ultra-low-power devices for applications in the Internet of Things (IoT), wearable electronics, and biomedical devices. The ability to fine-tune the threshold voltage makes DMG junctionless FinFETs suitable for energy-efficient applications.

- **Circuit-Level Implementation:** Future research could explore the integration of DMG junctionless FinFETs in circuit-level designs, such as SRAM cells, logic gates, and analog circuits. This would involve understanding the impact of device-level improvements on system-level performance.

- **Simulation and Modeling Enhancements:** Improved compact models and simulation techniques can be developed to better predict the behavior of DMG junctionless FinFETs under various operating conditions. This could include incorporating advanced quantum effects, parasitics, and reliability factors into device models.

In summary, the DMG junctionless FinFET has the potential to address critical challenges in semiconductor technology and pave the way for innovative applications. The insights from this project offer a robust starting point for extending this research into cutting-edge device designs and systems for next-generation electronics.

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