Sanjeen Suman

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Professional Summary

VLSI Engineer with strong fundamentals in Digital Logic, CMOS Design, and the complete VLSI flow. Skilled in RTL coding (Verilog), Synthesis, STA, and Physical Design. Proficient in EDA tools, device modeling, SRAM memory layout, and Spice/testbench simulations. Seeking an opportunity to apply my skills and contribute to innovative projects in the semiconductor industry.

Education

National Institute Of Technology, Surathkal (NITK) 70 %
M.Tech in VLSI Design *Aug. 2023 – May 2025*

SRM Institute of Science and Technology KTR, Chennai, TN 80.59 %
B.Tech in Electrical and Electronics Engineering. *June 2016 – June 2020*

Experience

Laboratory Assistant August 2024 – March 2025
National Institute Of Technology, Surathkal (NITK) *Karnataka*

Projects

Modeling and Variability Analysis of 10 nm Dual Material Gate Junctionless FinFET December 2024

- Dual material gate Junctionless FinFET with 10 nm gate length is designed on Structure Editor of Synopsys Sentaurus TCAD Tool.
- Implemented and configured essential physics models in the SDEVICE script of Sentaurus TCAD to accurately simulate semiconductor device behavior.
- Automated Id–Vg curve plotting and extraction of parameters such as threshold voltage, DIBL, subthreshold slope, leakage current is done using SVisual scripting in Sentaurus TCAD.
- Extracted key device parameters and conducted comparative analysis with conventional FinFETs under variations in channel doping concentration, gate oxide thickness, metal gate length ratio, fin width, and dual-metal gate materials.

Characterization of 7nm FinFET based Inverter and bandgap reference circuit August 2025

- Designed and simulated the Inverter in an open source tool using 7nm FinFET with ASAP7 PDK.
- Analyzed V-I characteristics, switching behavior, performance metrics, trans-conductance and gain of inverter
- Designed and simulated 7nm FinFET based bandgap reference circuit and checked performance with supply and temperature variation.

Design and Layout of Full adder circuit using Transmission gate in Cadence March 2024

- Designed a schematic and performed a layout of a Transmission Gate Logic based Full Adder using Cadence Virtuoso with UMC 65nm CMOS technology and calculated the delay and power.

Pre and Post Layout Simulation of 6T SRAM cell with Read/Write Speed Analysis August 2025

- Performed layout design of 6T SRAM cell with DRC/LVS verification and parasitic extraction using open source tool.
- Calculated write/read speed and verified the functionality of cell in both pre layout as well as post layout simulation.

RV32 Single-Cycle RISC-V CPU Architecture Implementation in Verilog March 2024

- Designed and Implemented a 32 bit RISC-V processor capable of executing R, I,B and S-type instructions, focusing on efficient datapath and control logic design. Developed a strong understanding of RISC V architecture, functionality and interaction of each block in the architecture.

Implementation of Synchronous FIFO for Efficient Data Buffering July 2025

- Designed and implemented a synchronous FIFO memory using Verilog for smooth data flow within the same clock module.
- Verified functionality and timing using testbench simulations ensuring correct FIFO operation.

Skills

Technical Skills: UART protocol, Static Timing Analysis, Spice simulation, Cell layout and characterization, CMOS VLSI, RTL Design, Physical Design, Digital IC Design, Linux, RTL Synthesis, Device physics
Practical Skills: Characterization of D latch, CMOS Inverter, MOSFET, SRAM cell and FinFET, RTL synthesis using Yosys, Device modeling by Sentaurus TCAD, Spice simulation using Ngspice, Circuit Schematic using LTSpice/XSchem/Cadence spectre, STA using OpenSTA tool and LVS check using Netgen, Layout using Magic VLSI/Cadence Virtuoso
Tools: Synopsys Sentaurus TCAD tool, Cadence Virtuoso, Cadence Spectre, Intel Quartus Prime, Magic VLSI, Xilinx Vivado, LTSpice, NgSpice, ModelSim, Yosys, XSchem, Netgen, OpenRoad, OpenSTA tool, Origin Pro, QuestaSim
Language: Verilog

Course

NPTEL: VLSI Design Flow - IIIT Delhi, Digital IC Design -IIT Madras Janakiraman, VLSI Physical Design With Timing Analysis -IIT Roorkee, Hardware modeling using Verilog - IIT Kharagpur
Academic Course: CMOS VLSI, Digital Design Using FPGA, Analog IC Design, Physical Design, High Performance Computer Architecture (HPCA)

Publication

Appl. Sci. Eng.: Development of a New Pseudo-DC Link Type DC-Decoupled Transformerless Inverter (Electrical)-Power Electronics
IJRTE: Economic Load Dispatch in the Power System (Electrical)

ACHIEVEMENT

- Qualified Gate in 2023 and 2025
- Selected for the position of Assistant Professor in Electronics Department