Module 2 Assignment

7nm FinFET Device and Inverter Characterization

For my username Sanjeen the ASCII sum in mv is 0.516

So, voltage is taken as 0.516

1. Simulate the inverter using the provided SPICE deck (Inverter.sp).

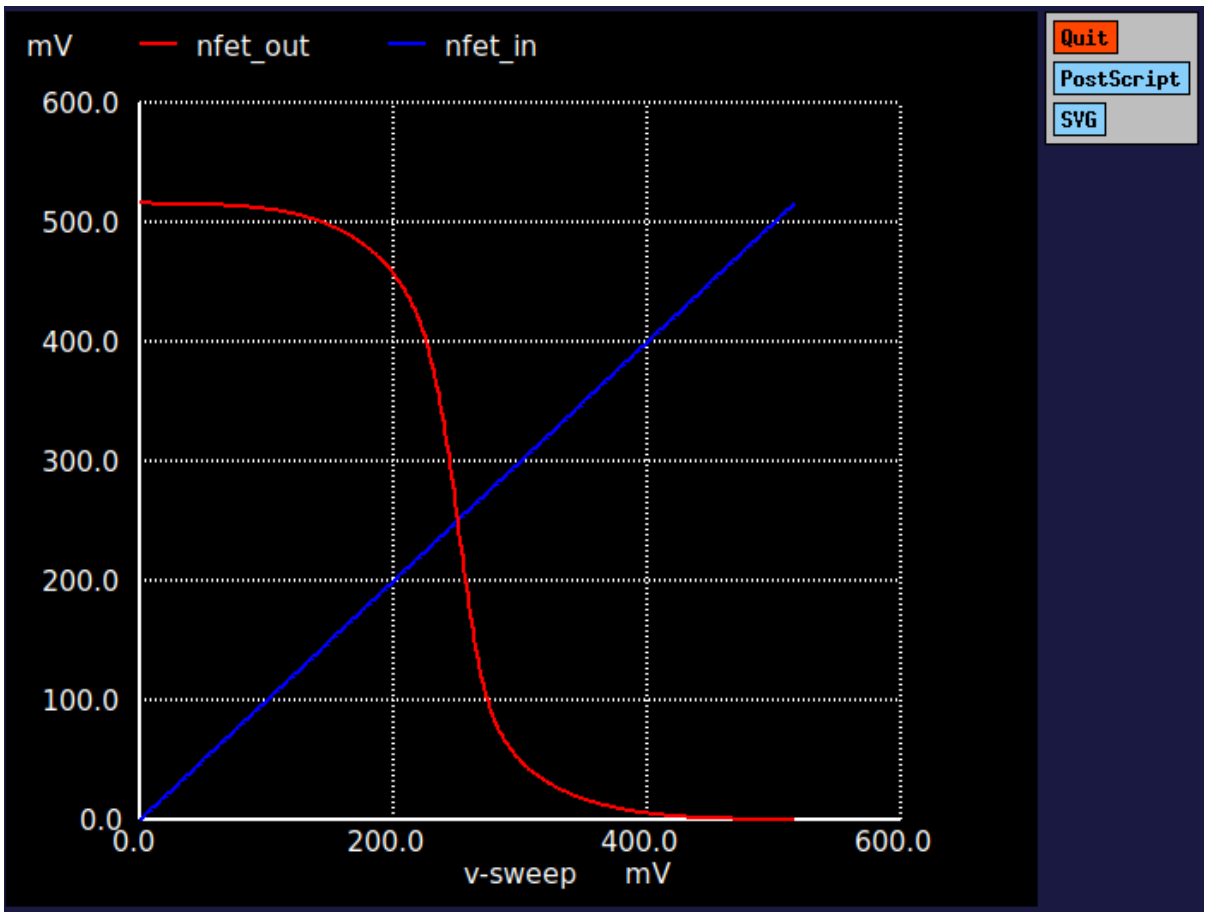

Fig 2.1 VTC Curve

Y axis is output voltage **(nfet_out)** and X axis is input voltage **(nfet_in).** The point where input voltage is equal to output voltage or the point where blue line intersect red line is known as switching threshold (denoted here by v_th).

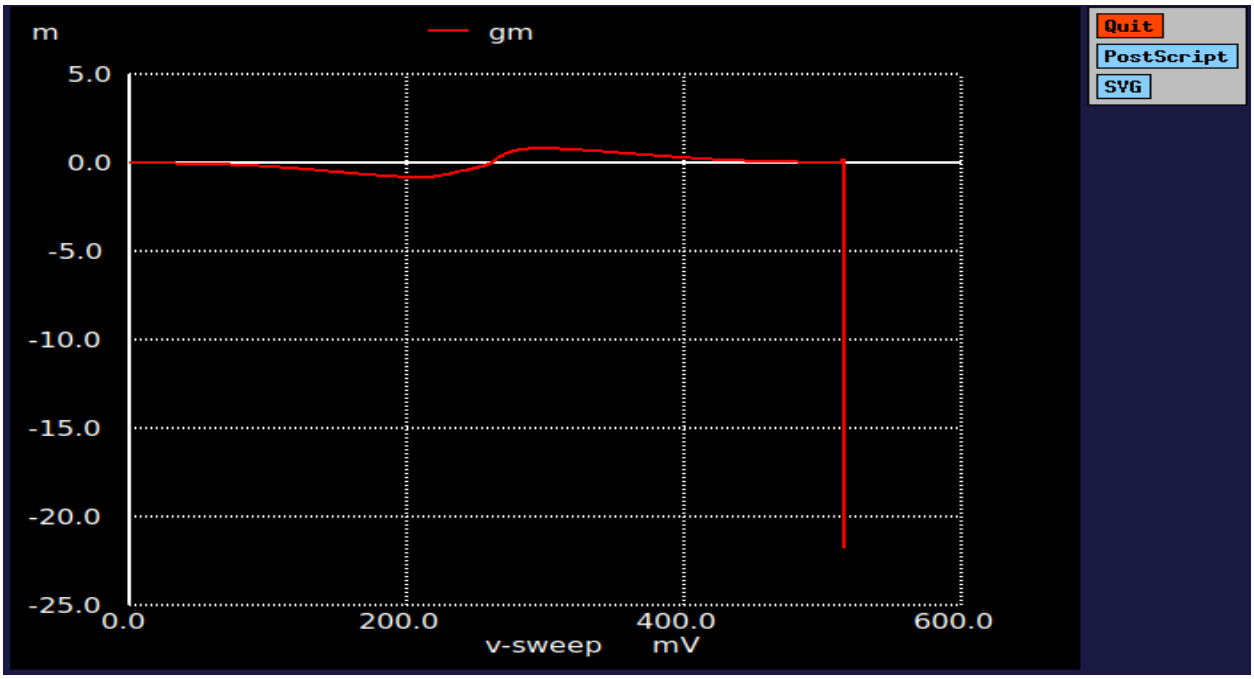

Fig 2.2 Transconductance (Gm)

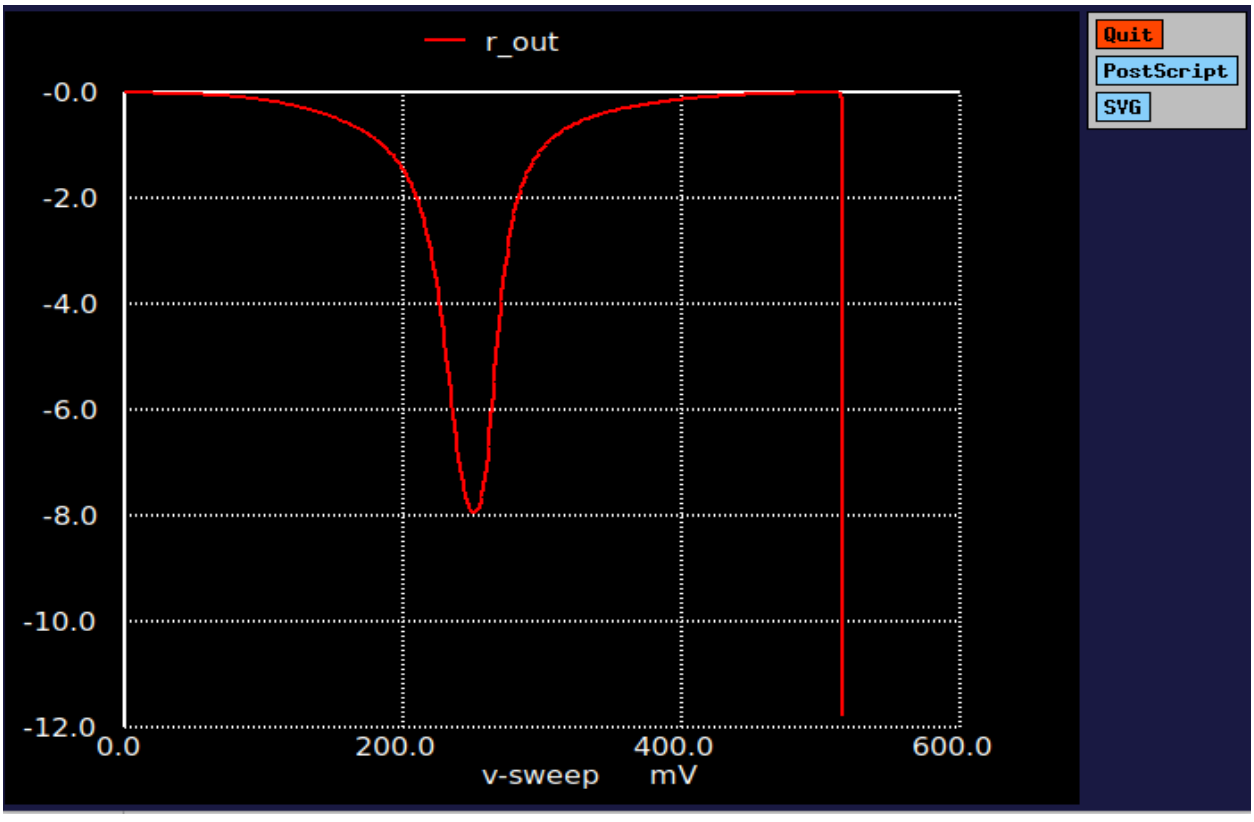

Fig 2.3 Output Resistance

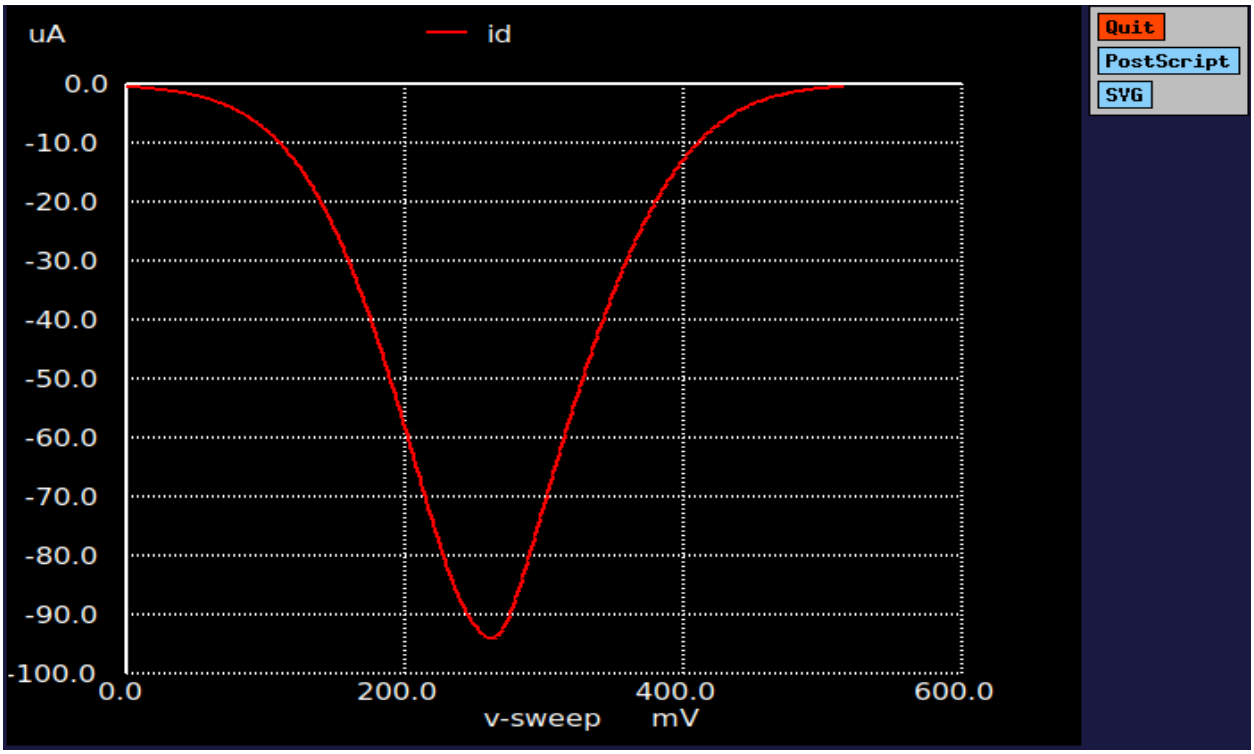

Fig 2.4 Drain current

2)

When width of pfet increased -

Parameter	**comment**
Switching threshold	increase
Maximum gain	decrease
Maximum Transconductance	increase
Power	increase
Propagation delay	Slightly increase