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Release 14.7 Trace  (nt64)
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C:\Xilinx\14.7\ISE_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3
-n 3 -fastpaths -xml Async_FIFO.twx Async_FIFO.ncd -o Async_FIFO.twr
Async_FIFO.pcf -ucf Async_FIFO.ucf

Design file:              Async_FIFO.ncd
Physical constraint file: Async_FIFO.pcf
Device,package,speed:     xc7a100t,csg324,C,-3 (PRODUCTION 1.10 2013-10-13)
Report level:             verbose report

Environment Variable      Effect
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NONE                      No environment variables were set
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INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths
   option. All paths that are not constrained will be reported in the
   unconstrained paths section(s) of the report.
INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on
   a 50 Ohm transmission line loading model.  For the details of this model,
   and for more information on accounting for different loading conditions,
   please see the device datasheet.



Data Sheet report:
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All values displayed in nanoseconds (ns)

Setup/Hold to clock rd_clk
------------+------------+------------+------------+------------+------------------+--------+
            |Max Setup to|  Process   |Max Hold to |  Process   |                  | Clock  |
Source      | clk (edge) |   Corner   | clk (edge) |   Corner   |Internal Clock(s) | Phase  |
------------+------------+------------+------------+------------+------------------+--------+
reset       |    0.409(R)|      FAST  |    1.205(R)|      SLOW  |rd_clk_BUFGP      |   0.000|
------------+------------+------------+------------+------------+------------------+--------+

Setup/Hold to clock wr_clk
------------+------------+------------+------------+------------+------------------+--------+
            |Max Setup to|  Process   |Max Hold to |  Process   |                  | Clock  |
Source      | clk (edge) |   Corner   | clk (edge) |   Corner   |Internal Clock(s) | Phase  |
------------+------------+------------+------------+------------+------------------+--------+
reset       |    1.292(R)|      FAST  |    0.756(R)|      SLOW  |wr_clk_BUFGP      |   0.000|
------------+------------+------------+------------+------------+------------------+--------+

Clock rd_clk to Pad
------------+-----------------+------------+-----------------+------------+------------------+--------+
            |Max (slowest) clk|  Process   |Min (fastest) clk|  Process   |                  | Clock  |
Destination |  (edge) to PAD  |   Corner   |  (edge) to PAD  |   Corner   |Internal Clock(s) | Phase  |
------------+-----------------+------------+-----------------+------------+------------------+--------+
data_out<0> |         9.903(R)|      SLOW  |         4.260(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<1> |         9.760(R)|      SLOW  |         4.169(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<2> |         9.746(R)|      SLOW  |         4.140(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<3> |         9.824(R)|      SLOW  |         4.212(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<4> |         9.858(R)|      SLOW  |         4.241(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<5> |         9.804(R)|      SLOW  |         4.198(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<6> |         8.988(R)|      SLOW  |         3.695(R)|      FAST  |rd_clk_BUFGP      |   0.000|
data_out<7> |         9.444(R)|      SLOW  |         4.014(R)|      FAST  |rd_clk_BUFGP      |   0.000|
r_empty     |         9.665(R)|      SLOW  |         3.777(R)|      FAST  |rd_clk_BUFGP      |   0.000|
------------+-----------------+------------+-----------------+------------+------------------+--------+

Clock wr_clk to Pad
------------+-----------------+------------+-----------------+------------+------------------+--------+
            |Max (slowest) clk|  Process   |Min (fastest) clk|  Process   |                  | Clock  |
Destination |  (edge) to PAD  |   Corner   |  (edge) to PAD  |   Corner   |Internal Clock(s) | Phase  |
------------+-----------------+------------+-----------------+------------+------------------+--------+
data_out<0> |         9.167(R)|      SLOW  |         4.043(R)|      FAST  |wr_clk_BUFGP      |   0.000|
data_out<1> |         9.003(R)|      SLOW  |         3.936(R)|      FAST  |wr_clk_BUFGP      |   0.000|
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w_full      |        10.009(R)|      SLOW  |         4.015(R)|      FAST  |wr_clk_BUFGP      |   0.000|
------------+-----------------+------------+-----------------+------------+------------------+--------+

Clock to Setup on destination clock rd_clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
rd_clk         |    1.861|         |         |         |
wr_clk         |    1.941|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock wr_clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
rd_clk         |    2.464|         |         |         |
wr_clk         |    2.859|         |         |         |
---------------+---------+---------+---------+---------+


Analysis completed Sat Aug 14 13:09:48 2021
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Trace Settings:
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Trace Settings

Peak Memory Usage: 5002 MB
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