```
Release 14.7 - xst P.20131013 (nt64)
Copyright (c) 1995-2013 Xilinx, Inc.  All rights reserved.
--> Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.25 secs

--> Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.26 secs

--> Reading design: Async_FIFO.prj

TABLE OF CONTENTS
  1) Synthesis Options Summary
  2) HDL Parsing
  3) HDL Elaboration
  4) HDL Synthesis
       4.1) HDL Synthesis Report
  5) Advanced HDL Synthesis
       5.1) Advanced HDL Synthesis Report
  6) Low Level Synthesis
  7) Partition Report
  8) Design Summary
       8.1) Primitive and Black Box Usage
       8.2) Device utilization summary
       8.3) Partition Resource Summary
       8.4) Timing Report
            8.4.1) Clock Information
            8.4.2) Asynchronous Control Signals Information
            8.4.3) Timing Summary
            8.4.4) Timing Details
            8.4.5) Cross Clock Domains Report


=========================================================================
===
*                      Synthesis Options
Summary                          *
=========================================================================
===
---- Source Parameters
Input File Name                    : "Async_FIFO.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "Async_FIFO"
```

```
Output Format                      : NGC
Target Device                      : xc7a100t-3-csg324

---- Source Options
Top Module Name                    : Async_FIFO
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Shift Register Extraction          : YES
ROM Style                          : Auto
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Shift Register Minimum Size        : 2
Use DSP Block                      : Auto
Automatic Register Balancing       : No

---- Target Options
LUT Combining                      : Auto
Reduce Control Sets                : Auto
Add IO Buffers                     : YES
Global Maximum Fanout              : 100000
Add Generic Clock Buffer(BUFG)     : 32
Register Duplication               : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Auto
Use Synchronous Set                : Auto
Use Synchronous Reset              : Auto
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Power Reduction                    : NO
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
```

```
DSP48 Utilization Ratio            : 100
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================
===


=========================================================================
===
*                           HDL
Parsing                                  *
=========================================================================
===
Analyzing Verilog file "F:\Software files\Quartus files\self
projects\FIFO\transmitter.v" into library work
Parsing module <transmitter>.
Analyzing Verilog file "F:\Software files\Quartus files\self
projects\FIFO\Async_FIFO.v" into library work
Parsing module <Async_FIFO>.

=========================================================================
===
*                             HDL
Elaboration                                *
=========================================================================
===

Elaborating module <Async_FIFO>.
WARNING:HDLCompiler:413 - "F:\Software files\Quartus files\self
projects\FIFO\Async_FIFO.v" Line 31: Result of 6-bit expression is
truncated to fit in 5-bit target.
WARNING:HDLCompiler:413 - "F:\Software files\Quartus files\self
projects\FIFO\Async_FIFO.v" Line 32: Result of 9-bit expression is
truncated to fit in 8-bit target.

Elaborating module <transmitter>.
WARNING:HDLCompiler:413 - "F:\Software files\Quartus files\self
projects\FIFO\Async_FIFO.v" Line 52: Result of 6-bit expression is
truncated to fit in 5-bit target.

=========================================================================
===
*                           HDL
Synthesis                                 *
=========================================================================
===

Synthesizing Unit <Async_FIFO>.
    Related source file is "F:\Software files\Quartus files\self
```

```
projects\FIFO\Async_FIFO.v".
        ptr = 4
        width = 8
        depth = 16
    Found 16x8-bit dual-port RAM <Mram_mem> for signal <mem>.
    Found 8-bit register for signal <transmitter_ptr>.
    Found 5-bit register for signal <rd_ptr>.
    Found 5-bit register for signal <wr_ptr>.
    Found 5-bit register for signal <read_s1>.
    Found 5-bit register for signal <read_s2>.
    Found 5-bit register for signal <write_s1>.
    Found 5-bit register for signal <write_s2>.
    Found 5-bit adder for signal <wr_ptr[4]_GND_1_o_add_1_OUT>
created at line 31.
    Found 8-bit adder for signal
<transmitter_ptr[7]_GND_1_o_add_2_OUT> created at line 32.
    Found 5-bit adder for signal <rd_ptr[4]_GND_1_o_add_12_OUT>
created at line 52.
    Found 5-bit comparator equal for signal <r_empty> created at
line 65
    Found 5-bit comparator equal for signal <w_full> created at line
73
    Summary:
        inferred   1 RAM(s).
        inferred   3 Adder/Subtractor(s).
        inferred  38 D-type flip-flop(s).
        inferred   2 Comparator(s).
        inferred   1 Multiplexer(s).
Unit <Async_FIFO> synthesized.

Synthesizing Unit <transmitter>.
    Related source file is "F:\Software files\Quartus files\self
projects\FIFO\transmitter.v".
WARNING:Xst:647 - Input <wr_ptr<7:7>> is never used. This port will
be preserved and left unconnected if it belongs to a top-level block
or it belongs to a sub-block and the hierarchy of this sub-block is
preserved.
WARNING:Xst:2999 - Signal 'input_RAM', unconnected in block
'transmitter', is tied to its initial value.
    Found 128x8-bit single-port Read Only RAM <Mram_input_RAM> for
signal <input_RAM>.
    Summary:
        inferred   1 RAM(s).
Unit <transmitter> synthesized.

=========================================================================
===
HDL Synthesis Report

Macro Statistics
```

```
# RAMs                                                 : 2
 128x8-bit single-port Read Only RAM                  : 1
 16x8-bit dual-port RAM                               : 1
# Adders/Subtractors                                   : 3
 5-bit adder                                          : 2
 8-bit adder                                          : 1
# Registers                                            : 7
 5-bit register                                       : 6
 8-bit register                                       : 1
# Comparators                                          : 2
 5-bit comparator equal                               : 2
# Multiplexers                                         : 1
 1-bit 2-to-1 multiplexer                             : 1
# Xors                                                 : 10
 1-bit xor2                                           : 8
 5-bit xor2                                           : 2

=========================================================================
===

=========================================================================
===
*                      Advanced HDL
Synthesis                           *
=========================================================================
===


Synthesizing (advanced) Unit <Async_FIFO>.
The following registers are absorbed into counter <rd_ptr>: 1
register on signal <rd_ptr>.
The following registers are absorbed into counter <transmitter_ptr>:
1 register on signal <transmitter_ptr>.
The following registers are absorbed into counter <wr_ptr>: 1
register on signal <wr_ptr>.
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_mem> will be implemented
on LUTs either because you have described an asynchronous read or
because of currently unsupported block RAM features. If you have
described an asynchronous read, making it synchronous would allow
you to take advantage of available block RAM resources, for
optimized device usage and improved timings. Please refer to your
documentation for coding guidelines.

-------------------------------------------------------------------------
-
    | ram_type           | Distributed
|          |

-------------------------------------------------------------------------
-
```

```
    | Port
A                                                                  |
    |     aspect ratio   | 16-word x 8-bit
|          |
    |     clkA           | connected to signal <wr_clk>        |
rise     |
    |     weA            | connected to internal node          |
high     |
    |     addrA          | connected to signal <wr_ptr<3:0>>
|          |
    |     diA            | connected to signal <data_in>
|          |

-----------------------------------------------------------------------
-
    | Port
B                                                                  |
    |     aspect ratio   | 16-word x 8-bit
|          |
    |     addrB          | connected to signal <rd_ptr<3:0>>
|          |
    |     doB            | connected to signal <data_out>
|          |

-----------------------------------------------------------------------
-
Unit <Async_FIFO> synthesized (advanced).

Synthesizing (advanced) Unit <transmitter>.
INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram_input_RAM> will be
implemented on LUTs either because you have described an
asynchronous read or because of currently unsupported block RAM
features. If you have described an asynchronous read, making it
synchronous would allow you to take advantage of available block RAM
resources, for optimized device usage and improved timings. Please
refer to your documentation for coding guidelines.

-----------------------------------------------------------------------
-
    | ram_type           | Distributed
|          |

-----------------------------------------------------------------------
-
    | Port
A                                                                  |
    |     aspect ratio   | 128-word x 8-bit
|          |
    |     weA            | connected to signal <GND>           |
high     |
```

```
    |     addrA           | connected to signal <wr_ptr>
|           |
    |     diA             | connected to signal <GND>
|           |
    |     doA             | connected to internal node
|           |

-----------------------------------------------------------------------
-
Unit <transmitter> synthesized (advanced).

=========================================================================
===
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 2
 128x8-bit single-port distributed Read Only RAM       : 1
 16x8-bit dual-port distributed RAM                    : 1
# Counters                                             : 3
 5-bit up counter                                      : 2
 8-bit up counter                                      : 1
# Registers                                            : 20
 Flip-Flops                                            : 20
# Comparators                                          : 2
 5-bit comparator equal                                : 2
# Xors                                                 : 10
 1-bit xor2                                            : 8
 5-bit xor2                                            : 2

=========================================================================
===

=========================================================================
===
*                           Low Level
Synthesis                               *
=========================================================================
===
INFO:Xst:2146 - In block <Async_FIFO>, Counter <transmitter_ptr>
<wr_ptr> are equivalent, XST will keep only <transmitter_ptr>.
WARNING:Xst:2677 - Node <transmitter_ptr_7> of sequential type is
unconnected in block <Async_FIFO>.

Optimizing unit <Async_FIFO> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Async_FIFO, actual
ratio is 0.
```

```
Final Macro Processing ...

Processing Unit <Async_FIFO> :
        Found 2-bit shift register for signal <write_s2_4>.
        Found 2-bit shift register for signal <read_s2_0>.
        Found 2-bit shift register for signal <read_s2_4>.
Unit <Async_FIFO> processed.

=========================================================================
===
Final Register Report

Macro Statistics
# Registers                                             : 26
 Flip-Flops                                             : 26
# Shift Registers                                       : 3
 2-bit shift register                                   : 3

=========================================================================
===

=========================================================================
===
*                            Partition
Report                             *
=========================================================================
===

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

-------------------------------

=========================================================================
===
*                             Design
Summary                              *
=========================================================================
===

Top Level Output File Name         : Async_FIFO.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 58
#      GND                         : 1
#      INV                         : 1
```

```
#      LUT1                          : 5
#      LUT2                          : 14
#      LUT3                          : 4
#      LUT5                          : 1
#      LUT6                          : 17
#      MUXCY                         : 6
#      MUXF7                         : 1
#      VCC                           : 1
#      XORCY                         : 7
# FlipFlops/Latches                  : 29
#      FD                            : 14
#      FDC                           : 3
#      FDCE                          : 9
#      FDE                           : 3
# RAMS                               : 3
#      RAM32M                        : 1
#      RAM32X1D                      : 2
# Shift Registers                    : 3
#      SRLC16E                       : 3
# Clock Buffers                      : 2
#      BUFGP                         : 2
# IO Buffers                         : 11
#      IBUF                          : 1
#      OBUF                          : 10

Device utilization summary:
---------------------------

Selected Device : 7a100tcsg324-3


Slice Logic Utilization:
 Number of Slice Registers:             29  out of  126800     0%
 Number of Slice LUTs:                  53  out of  63400      0%
    Number used as Logic:               42  out of  63400      0%
    Number used as Memory:              11  out of  19000      0%
       Number used as RAM:               8
       Number used as SRL:               3

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    62
   Number with an unused Flip Flop:     33  out of     62    53%
   Number with an unused LUT:            9  out of     62    14%
   Number of fully used LUT-FF pairs:   20  out of     62    32%
   Number of unique control sets:        7

IO Utilization:
 Number of IOs:                         13
 Number of bonded IOBs:                 13  out of    210     6%
```

```
Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                2  out of     32     6%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


=========================================================================
===
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
rd_clk                             | BUFGP                  | 15    |
wr_clk                             | BUFGP                  | 20    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 2.357ns (Maximum Frequency: 424.322MHz)
   Minimum input arrival time before clock: 1.544ns
   Maximum output required time after clock: 1.939ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
===
Timing constraint: Default period analysis for Clock 'rd_clk'
  Clock period: 2.029ns (frequency: 492.805MHz)
```

```
  Total number of paths / destination ports: 128 / 12
-------------------------------------------------------------------------
---
Delay:               2.029ns (Levels of Logic = 2)
  Source:            write_s2_2 (FF)
  Destination:       rd_ptr_1 (FF)
  Source Clock:      rd_clk rising
  Destination Clock: rd_clk rising

  Data Path: write_s2_2 to rd_ptr_1
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               2   0.361   0.697  write_s2_2 (write_s2_2)
     LUT6:I0->O            5   0.097   0.398  r_empty51_SW0 (N6)
     LUT6:I4->O            2   0.097   0.283  r_empty_inv1
(r_empty_inv)
     FDCE:CE                   0.095          rd_ptr_1
    ----------------------------------------
    Total                      2.029ns (0.650ns logic, 1.379ns route)
                                       (32.0% logic, 68.0% route)

=========================================================================
===
Timing constraint: Default period analysis for Clock 'wr_clk'
  Clock period: 2.357ns (frequency: 424.322MHz)
  Total number of paths / destination ports: 226 / 40
-------------------------------------------------------------------------
---
Delay:               2.357ns (Levels of Logic = 2)
  Source:            transmitter_ptr_0 (FF)
  Destination:       Mram_mem1 (RAM)
  Source Clock:      wr_clk rising
  Destination Clock: wr_clk rising

  Data Path: transmitter_ptr_0 to Mram_mem1
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             8   0.361   0.715  transmitter_ptr_0
(transmitter_ptr_0)
     LUT6:I1->O            3   0.097   0.389  w_full53_SW1 (N11)
     LUT6:I4->O            3   0.097   0.289  Mmux_BUS_000311
(BUS_0003)
     RAM32M:WE                 0.408          Mram_mem1
    ----------------------------------------
    Total                      2.357ns (0.963ns logic, 1.394ns route)
                                       (40.9% logic, 59.1% route)

=========================================================================
```

```
===
Timing constraint: Default OFFSET IN BEFORE for Clock 'wr_clk'
  Total number of paths / destination ports: 10 / 10
-------------------------------------------------------------------------
---
Offset:              1.544ns (Levels of Logic = 2)
  Source:            reset (PAD)
  Destination:       Mram_mem1 (RAM)
  Destination Clock: wr_clk rising

  Data Path: reset to Mram_mem1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             13   0.001   0.749  reset_IBUF (reset_IBUF)
     LUT6:I0->O             3   0.097   0.289  Mmux_BUS_000311
(BUS_0003)
     RAM32M:WE                  0.408          Mram_mem1
    ----------------------------------------
    Total                       1.544ns (0.506ns logic, 1.038ns route)
                                        (32.8% logic, 67.2% route)

=========================================================================
===
Timing constraint: Default OFFSET IN BEFORE for Clock 'rd_clk'
  Total number of paths / destination ports: 5 / 5
-------------------------------------------------------------------------
---
Offset:              0.685ns (Levels of Logic = 1)
  Source:            reset (PAD)
  Destination:       rd_ptr_1 (FF)
  Destination Clock: rd_clk rising

  Data Path: reset to rd_ptr_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             13   0.001   0.335  reset_IBUF (reset_IBUF)
     FDCE:CLR                   0.349          rd_ptr_1
    ----------------------------------------
    Total                       0.685ns (0.350ns logic, 0.335ns route)
                                        (51.1% logic, 48.9% route)

=========================================================================
===
Timing constraint: Default OFFSET OUT AFTER for Clock 'wr_clk'
  Total number of paths / destination ports: 24 / 9
-------------------------------------------------------------------------
---
Offset:              1.939ns (Levels of Logic = 3)
```

```
  Source:            transmitter_ptr_0 (FF)
  Destination:       w_full (PAD)
  Source Clock:      wr_clk rising

  Data Path: transmitter_ptr_0 to w_full
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDCE:C->Q             8   0.361   0.715  transmitter_ptr_0
(transmitter_ptr_0)
     LUT6:I1->O            3   0.097   0.389  w_full53_SW1 (N11)
     LUT6:I4->O            1   0.097   0.279  w_full53 (w_full_OBUF)
     OBUF:I->O                 0.000          w_full_OBUF (w_full)
    ----------------------------------------
    Total                      1.939ns (0.555ns logic, 1.384ns route)
                                       (28.6% logic, 71.4% route)

==========================================================================
===
Timing constraint: Default OFFSET OUT AFTER for Clock 'rd_clk'
  Total number of paths / destination ports: 48 / 9
--------------------------------------------------------------------------
---
Offset:              1.930ns (Levels of Logic = 3)
  Source:            write_s2_2 (FF)
  Destination:       r_empty (PAD)
  Source Clock:      rd_clk rising

  Data Path: write_s2_2 to r_empty
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               2   0.361   0.697  write_s2_2 (write_s2_2)
     LUT6:I0->O            5   0.097   0.398  r_empty51_SW0 (N6)
     LUT6:I4->O            1   0.097   0.279  r_empty51 (r_empty_OBUF)
     OBUF:I->O                 0.000          r_empty_OBUF (r_empty)
    ----------------------------------------
    Total                      1.930ns (0.555ns logic, 1.375ns route)
                                       (28.8% logic, 71.2% route)

==========================================================================
===

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock rd_clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
```

```
---------------+---------+---------+---------+---------+
rd_clk         |    2.029|         |         |         |
wr_clk         |    0.887|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock wr_clk
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
rd_clk         |    0.915|         |         |         |
wr_clk         |    2.357|         |         |         |
---------------+---------+---------+---------+---------+

=========================================================================
===


Total REAL time to Xst completion: 19.00 secs
Total CPU time to Xst completion: 18.75 secs

-->

Total memory usage is 4617532 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    6 (   0 filtered)
Number of infos    :    3 (   0 filtered)
```