KTU NOTES

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MODULE 4

SEQUENTIAL CIRCUITS

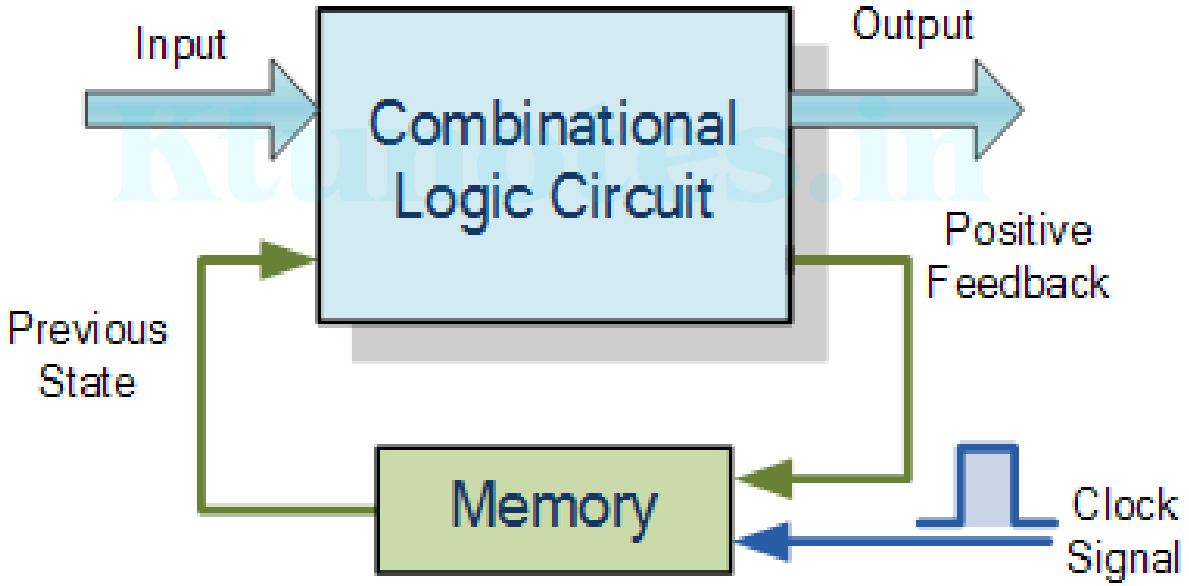
Sequential Circuits

- Output state of a “sequential logic circuit” is a function of following three states, “present input”, “past input” and/or “past output”
- *Sequential Logic circuits* remember these conditions and stay fixed in their current state until next clock signal changes one of states, giving sequential logic circuits “Memory”
- Sequential logic circuits are generally termed as *two state* or Bistable devices which can have their output or outputs set in one of two basic states, a logic level “1” or a logic level “0”

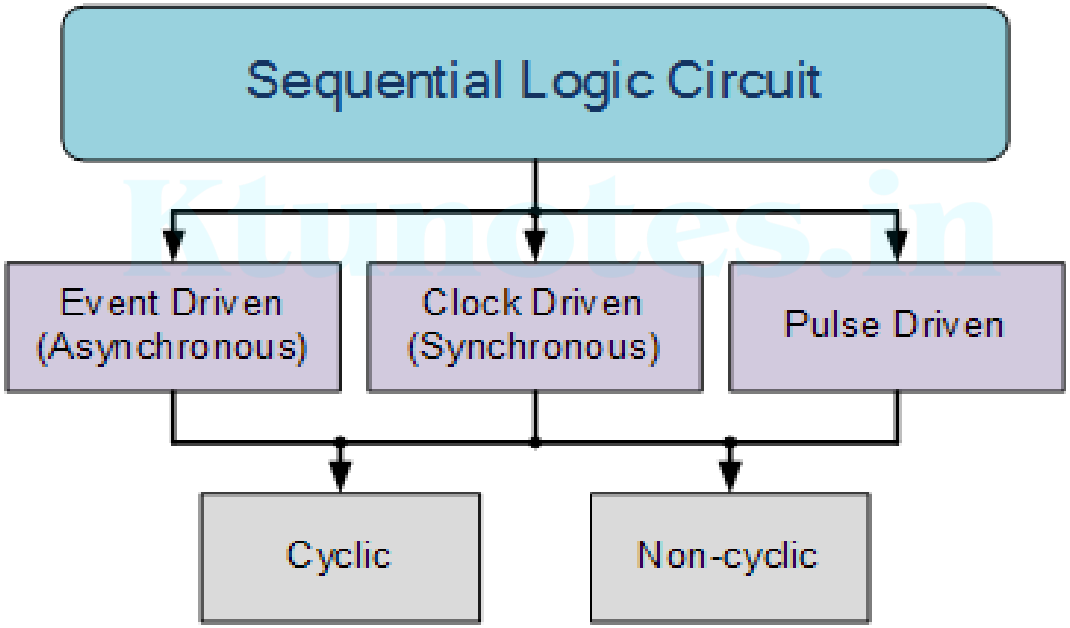
Sequential Circuits

- It will remain “latched” (hence name latch) indefinitely in this current state or condition until some other input trigger pulse or signal is applied which will cause bistable to change its state once again
- Word “Sequential” means that things happen in a “sequence”, one after another and in **Sequential Logic** circuits, the actual clock signal determines when things will happen next
- Simple sequential logic circuits can be constructed from standard **Bistable** circuits such as: *Flip flops*, *Latches* and *Counters*

Sequential Logic Representation



Classification of Sequential Logic



Classification of Sequential Logic

1. Event Driven – asynchronous circuits that change state immediately when enabled
2. Clock Driven – synchronous circuits that are synchronised to a specific clock signal
3. Pulse Driven – which is a combination of two that responds to triggering pulses

Flip Flops

- A flip flop is an electronic circuit with two stable states that can be used to store binary data
- Stored data can be changed by applying varying inputs
- Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems

Flip Flops

- Types
  1. SR Flip Flop
  2. JK Flip Flop
  3. D Flip Flop
  4. T Flip Flop

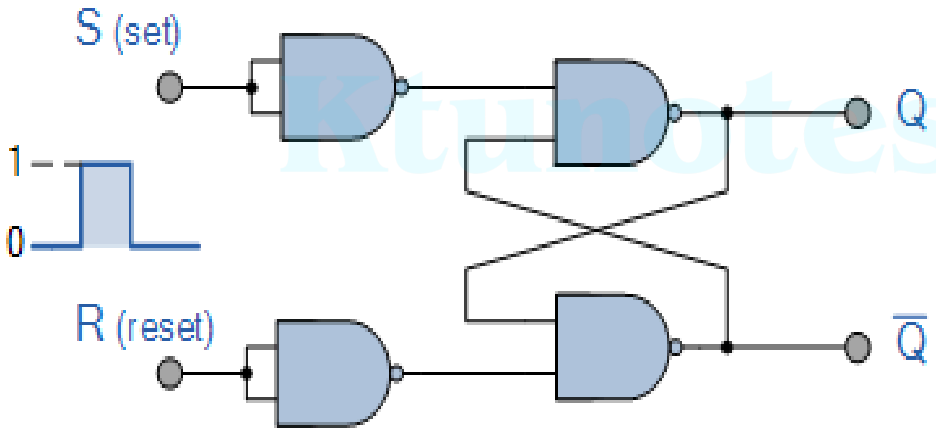
SR Flip-Flop

- **SR flip-flop**, also known as a *SR Latch*
- One of most basic sequential logic circuit
- SR description stands for “Set-Reset”
- It is basically a one-bit memory bistable device that has two inputs
  - ❖ One will “SET” device (meaning output = “1”), and is labelled **S**
  - ❖ One will “RESET” device (meaning output = “0”), labelled **R**

SR Flip-Flop

- SR flip-flop actually has three inputs, Set, Reset and its current output Q relating to it's current state or history
- Term "Flip-flop" relates to actual operation of device, as it can be "flipped" into one logic Set state or "flopped" back into opposing logic Reset state

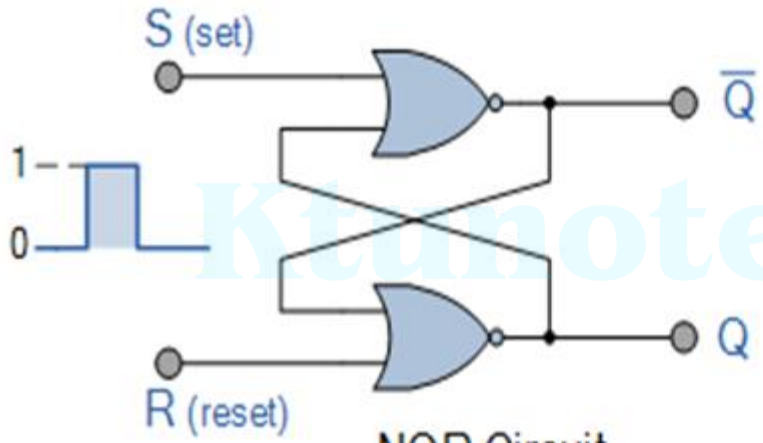
NAND Gate SR Flip-flop



NAND Circuit

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	X	X
		(Invalid)	

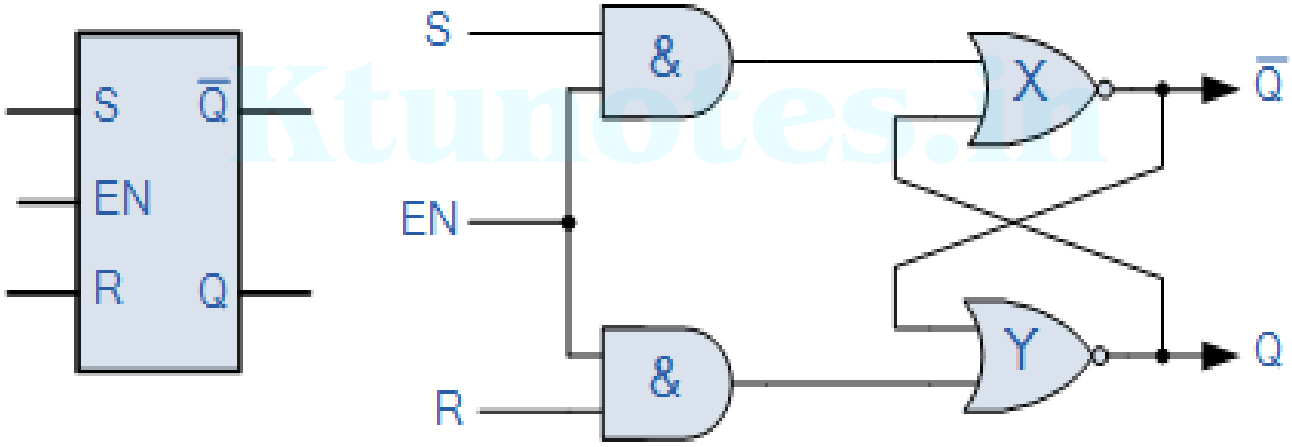
NOR Gate SR Flip-flop



NOR Circuit

S	R	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	X	X
		(Invalid)	

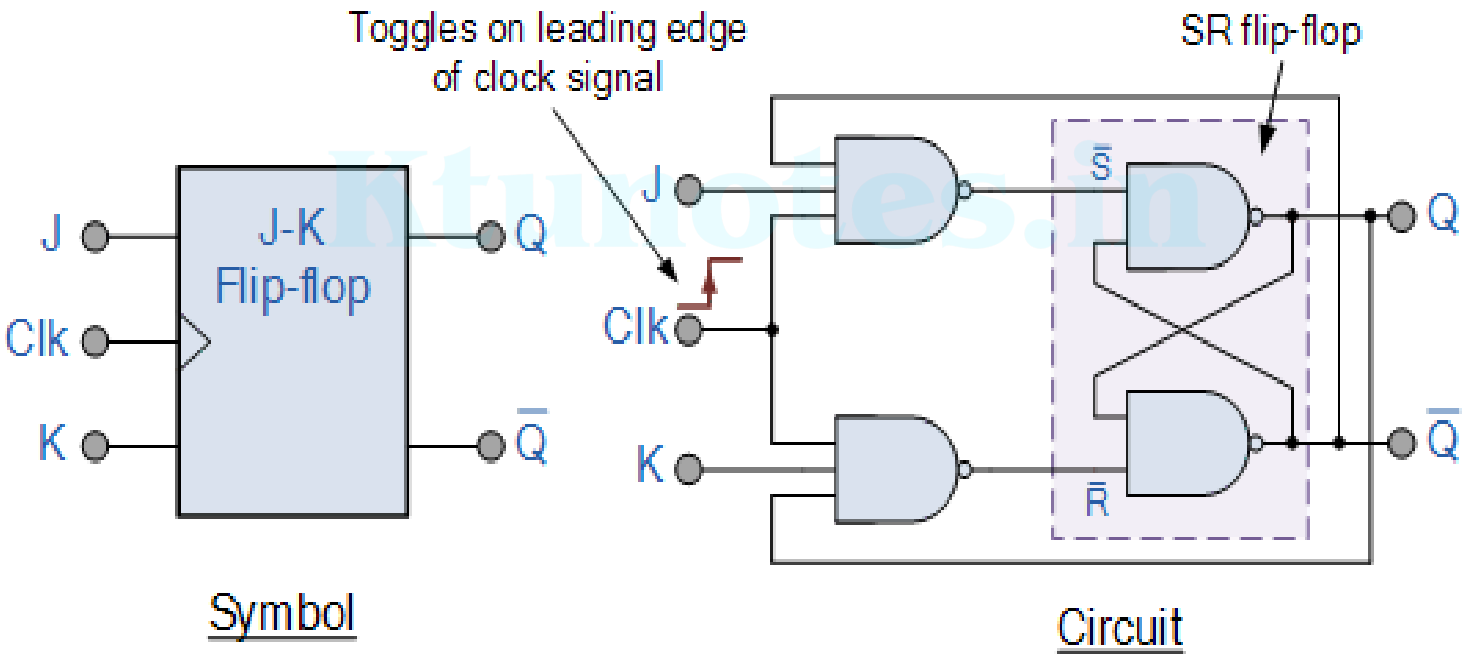
Gated or Clocked SR Flip-Flop



JK Flip Flop

- **JK flip flop** is basically a gated SR flip-flop with addition of a clock input circuitry that prevents illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”
- Due to this additional clocked input, a JK flip-flop has four possible output combinations, “logic 1”, “logic 0”, “no change” and “toggle”
- JK flip-flop is a universal flip-flop, because it can be configured to work as an SR flip-flop, a D flip-flop, or a T flip-flop

JK Flip Flop


Toggles on leading edge
of clock signal
SR flip-flop
J
Clk
K
J-K
Flip-flop
Q
$\overline{Q}$
$\overline{S}$
$\overline{R}$
Symbol
Circuit

JK Flip Flop

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

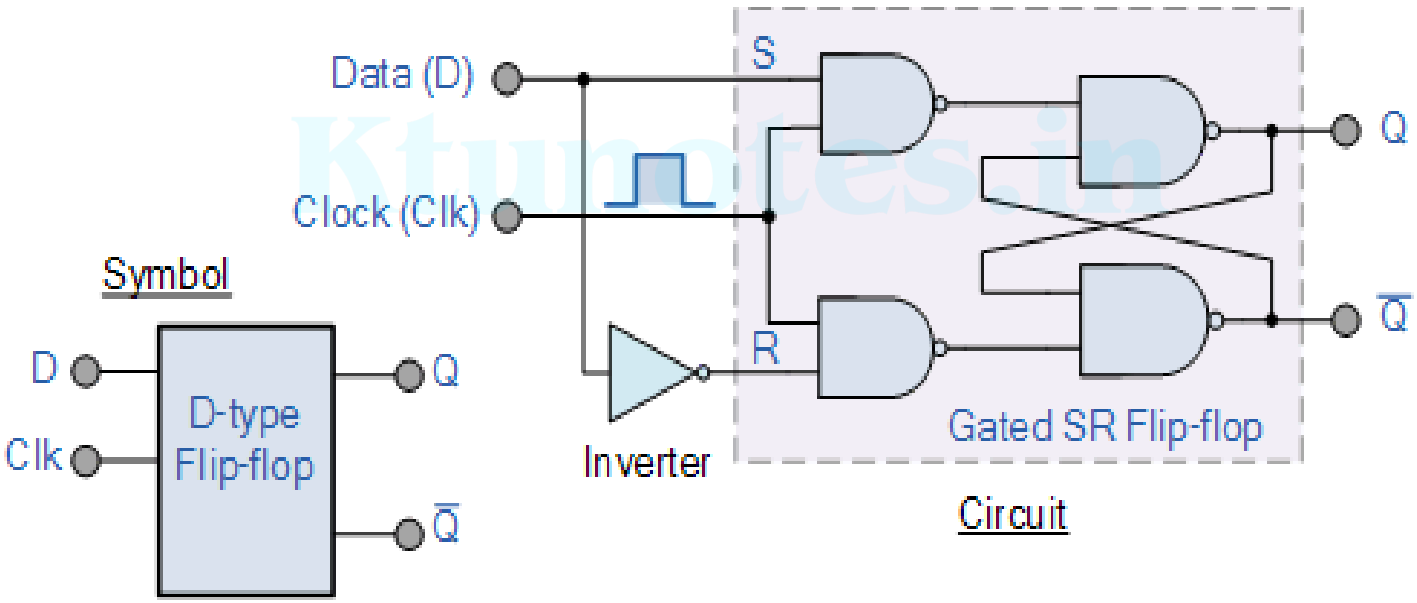
D Flip Flop

- **D Flip Flop** is by far most important of clocked flip-flops as it ensures that ensures that inputs S and R are never equal to one at same time
- D-type flip flop are constructed from a gated SR flip-flop with an inverter added between the S and R inputs to allow for a single D (Data) input
- Then this single data input, labelled “D” and is used in place of the “Set” signal, and the inverter is used to generate the complementary “Reset” input

D Flip Flop

- In D flip flop input and output is same but output comes out after moving into loop of d flip flop that's why delay is introduces
- Also known as a *Data Latch*, *Delay flip flop*, *D-type Bistable*, *D-type Flip Flop*

D Flip Flop


Data (D)
Clock (Clk)
S
R
Q
$\overline{Q}$
Inverter
Gated SR Flip-flop
Circuit
Symbol
D
Clk
D-type
Flip-flop
Q
$\overline{Q}$

D Flip Flop

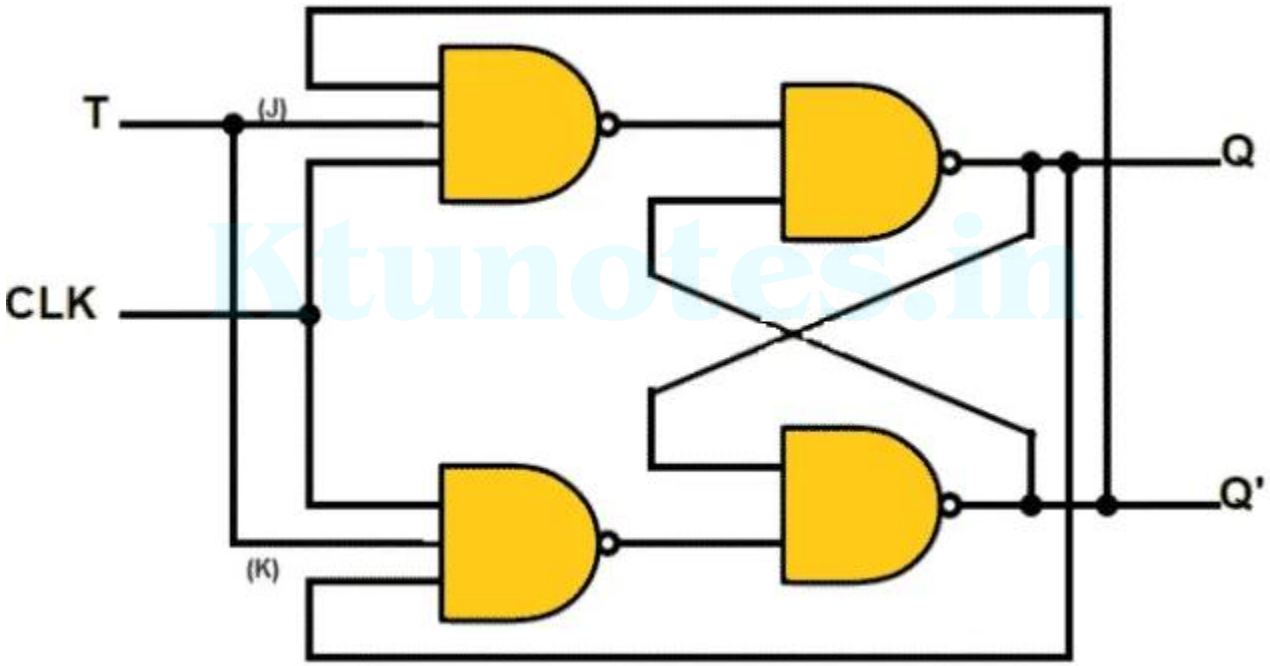
Truth Table for the D-type Flip Flop

Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

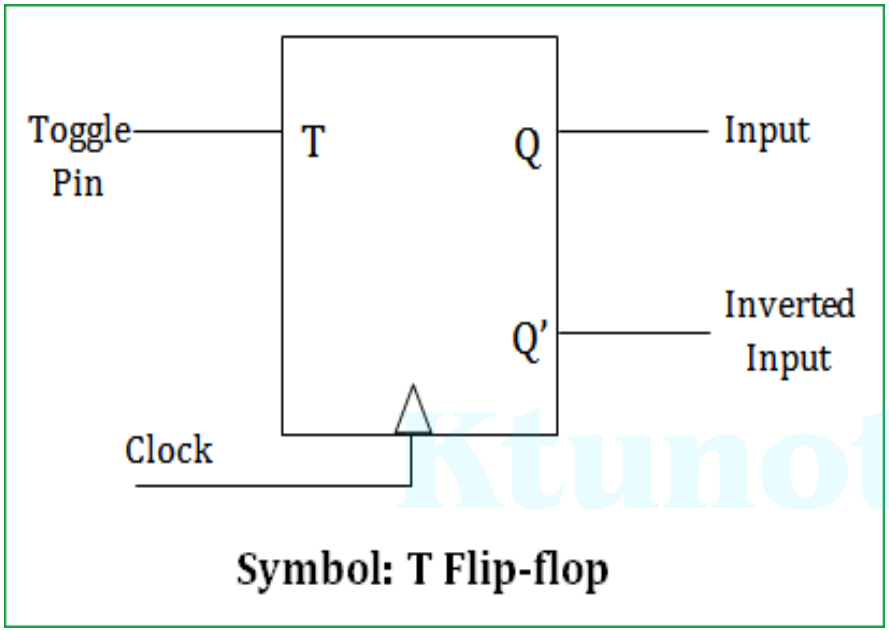
T Flip Flop

- T flip flop is also known as “Toggle Flip flop”
- To avoid occurrence of intermediate state in SR flip flop, we should provide only one input to flip flop called Trigger input or Toggle input (T)
- Then flip flop acts as a Toggle switch
- Toggling means ‘Changing next state output to complement of present state output’
- T flip flop is a single input device and hence by connecting J and K inputs together and giving them with single input called T we can convert a JK flip flop into T flip flop

T Flip Flop



T Flip Flop



Symbol: T Flip-flop

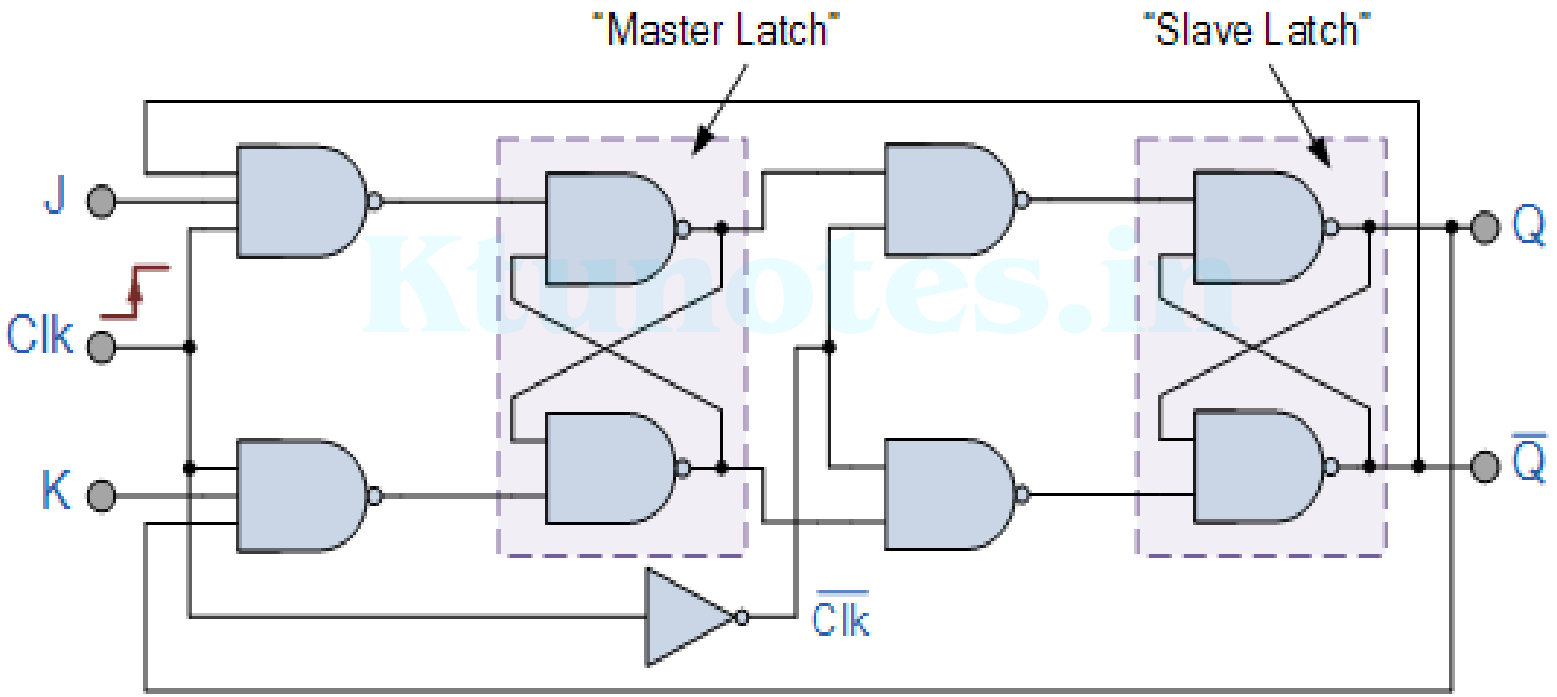
T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

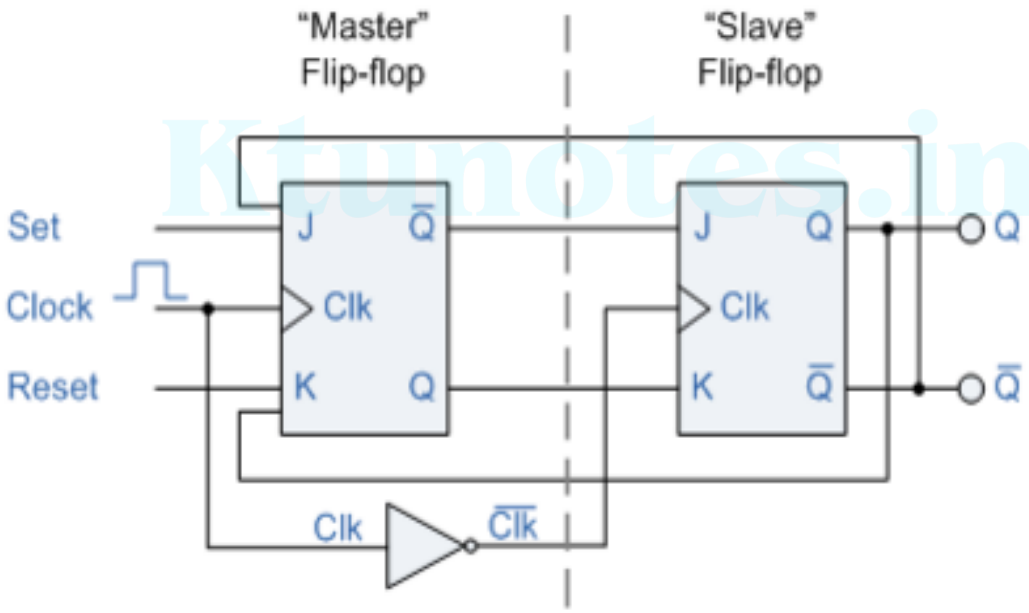
Master-Slave JK Flip Flop

- In "JK Flip Flop", when both inputs and CLK set to 1 for a long time, then Q output toggle until CLK is 1’
- Thus, uncertain or unreliable output produces
- This problem is referred to as a race-round condition in JK flip-flop and avoided by ensuring that CLK set to 1 only for a very short time
- Master-slave flip flop is designed in such a way that output of the "master" flip flop is passed to both inputs of "slave" flip flop
- Output of "slave" flip flop is passed to inputs of master flip flop

Master-Slave JK Flip Flop



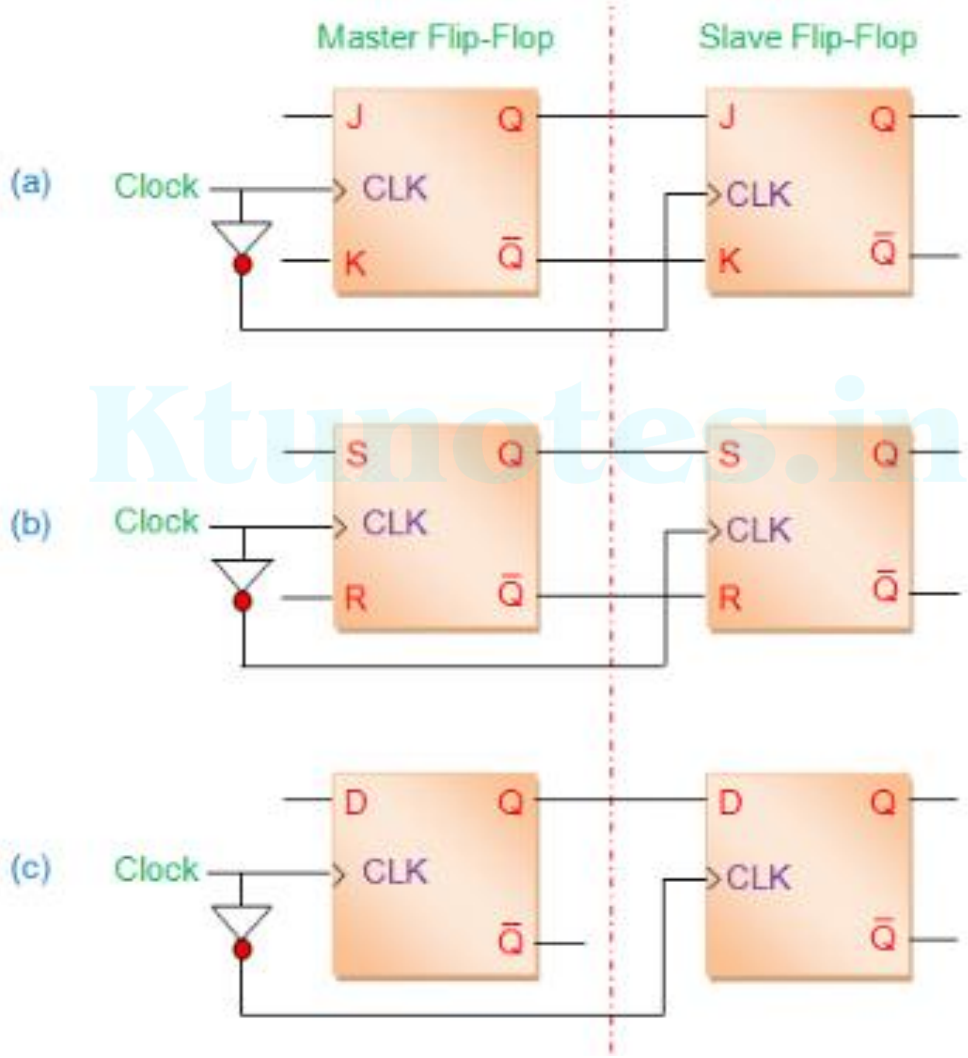
Master-Slave JK Flip Flop



Master-Slave JK Flip Flop

- Input signals J and K are connected to gated “master” SR flip flop which “locks” input condition while clock (Clk) input is “HIGH” at logic level “1”
- Outputs from “master” flip flop are only “seen” by gated “slave” flip flop when clock input goes “LOW” to logic level “0”
- When clock is “LOW”, outputs from the “master” flip flop are latched , gated “slave” flip flop now responds to state of its inputs passed over by “master” section
- **Master-Slave JK Flip flop** is a “Synchronous” device as it only passes data with timing of clock signal

Master-Slave Flip Flops



Triggering of Flip Flops

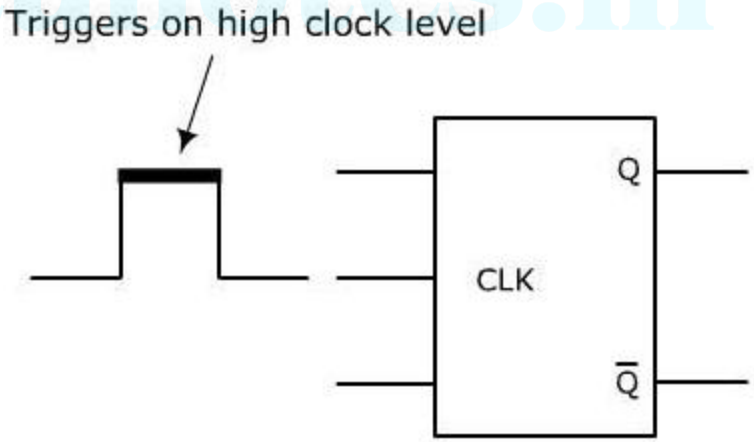
- Output of a flip flop can be changed by bring a small change in input signal
- This small change can be brought with help of a clock pulse or commonly known as a trigger pulse
- When such a trigger pulse is applied to input, output changes and thus the flip flop is said to be triggered

Triggering of Flip Flops

- There are mainly TWO types of pulse-triggering methods
  1. Edge triggering
  2. Level Triggering

High Level Triggering

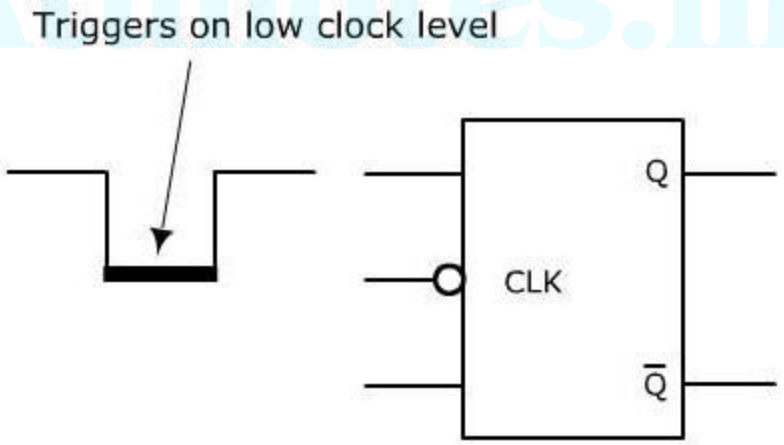
- When a flip flop is required to respond at its HIGH state, a HIGH level triggering method is used
- It is mainly identified from the straight lead from the clock input



High Level Triggering

Low Level Triggering

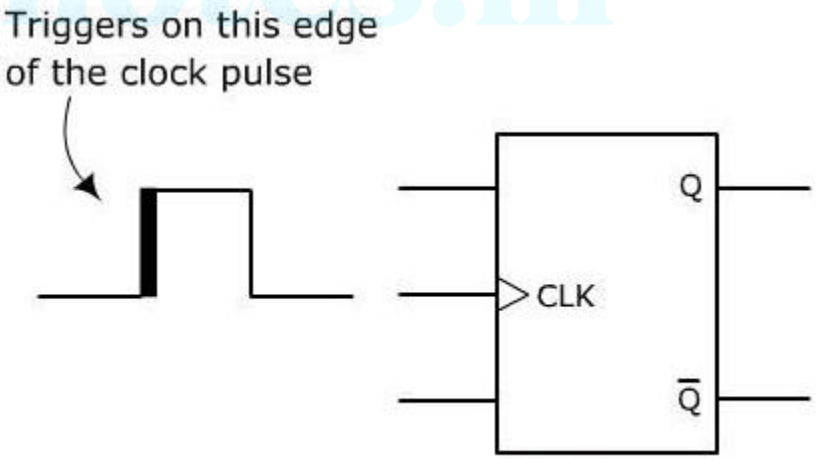
- When a flip flop is required to respond at its LOW state, a LOW level triggering method is used
- It is mainly identified from the clock input lead along with a low state indicator bubble



Low Level Triggering

Positive Edge Triggering

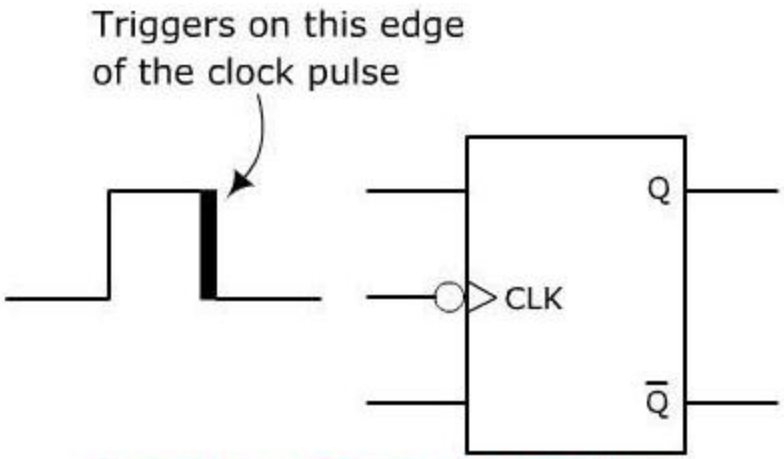
- When a flip flop is required to respond at a LOW to HIGH transition state, POSITIVE edge triggering method is used
- It is mainly identified from the clock input lead along with a triangle



Positive Edge Triggering

Negative Edge Triggering

- When a flip flop is required to respond during the HIGH to LOW transition state, a NEGATIVE edge triggering method is used
- It is mainly identified from the clock input lead along with a low-state indicator and a triangle



Negative Edge Triggering

Excitation Table And Characteristics Equation Of Flip Flops

- For a given combination of present state Q_n and next state Q_{n+1}, excitation table tell inputs required
- A characteristic function which gives next state in terms of current state and output

SR Flip Flop

INPUTS			OUTPUTS
S	R	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Indeterminate
1	1	1	Indeterminate

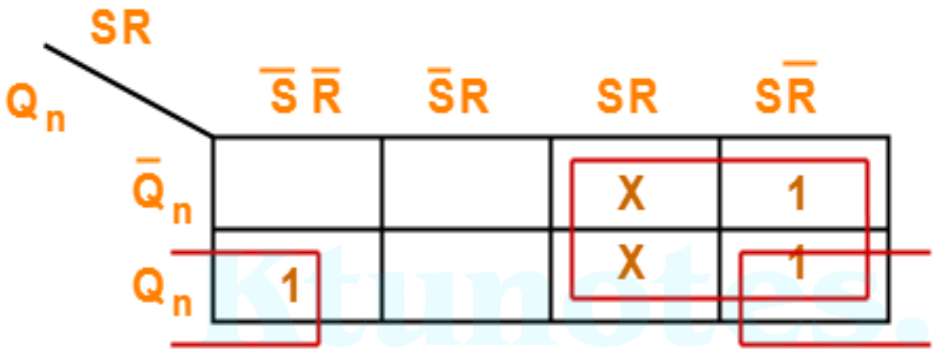
Truth Table

SR Flip Flop

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Excitation Table

SR Flip Flop



K Map

Characteristic equation: $Q_{n+1} = S + Q_nR'$

JK Flip Flop

INPUTS			OUTPUTS
J	K	Q_n (Present State)	Q_{n+1} (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

JK Flip Flop

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

JK Flip Flop

K Map

Characteristic equation: $Q_{n+1} = Q_n' J + Q_n K'$

D Flip Flop

- Truth table

D	$Q_{(next)}$
0	0
1	1

D Flip Flop

- Excitation Table

Q	$Q_{(next)}$	D
0	0	0
0	1	1
1	0	0
1	1	1

Characteristic equation: Q(next) = D

T Flip Flop

- Truth table

T	$Q_{(next)}$
0	Q
1	Q'

T Flip Flop

- Excitation table

Q	$Q_{(next)}$	T
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic equation: Q(next) = TQ' + T'Q

Registers

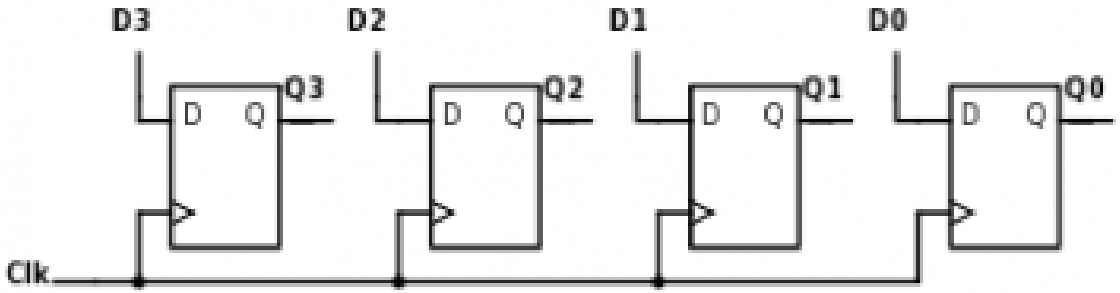
- Flip-flop is a 1 bit memory cell which can be used for storing digital data
- To increase storage capacity in terms of number of bits, we have to use a group of flip-flop
- Such a group of flip-flop is known as a **Register**
- **n-bit register** will consist of **n** number of flip-flop and it is capable of storing an **n-bit** word
- Binary data in a register can be moved within register from one flip-flop to another
- Registers that allow such data transfers are called as **shift registers**

Registers with Parallel load

- Parallel-load registers are a type of register where individual bit values in register are loaded simultaneously
- More specifically, every flip-flop within register takes an external data input, and these inputs are loaded into flip-flops on same edge in a clock cycle

Registers with Parallel load

- Pictured below is a simple 4-bit parallel-load register where *D0*, *D1*, *D2*, and *D3* are individual data bits
- *Q0*, *Q1*, *Q2*, and *Q3* form output value (as a 4-bit word *Q3 Q2 Q1 Q0*); and *Clk* is single clock signal



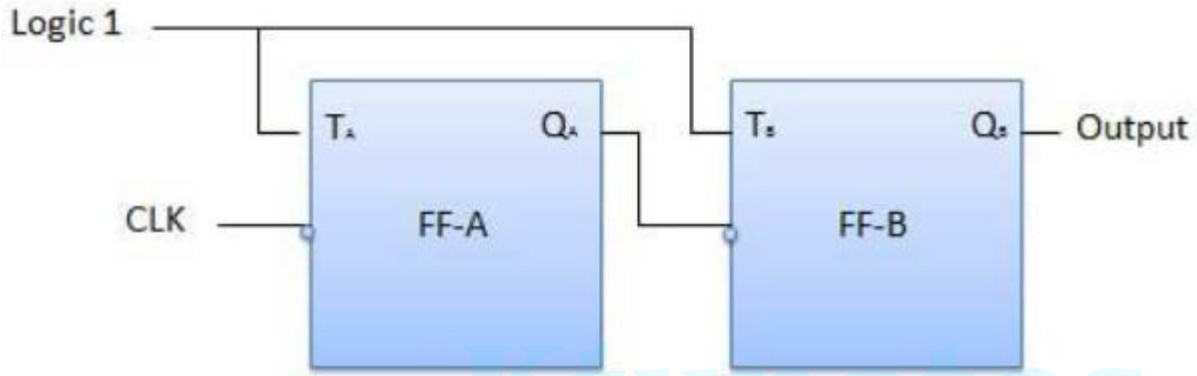
Counters

- Counter is a sequential circuit
- A digital circuit which is used for a counting pulses is known counter
- Counter is the widest application of flip-flops
- It is a group of flip-flops with a clock signal applied
- Counters are of two types
  1. Asynchronous or ripple counters
  2. Synchronous counters

Asynchronous or ripple counters

- Logic diagram of a 2-bit ripple up counter is shown in figure
- Toggle (T) flip-flop are being used
- But we can use the JK flip-flop also with J and K connected permanently to logic 1
- External clock is applied to clock input of flip-flop A and Q_A output is applied to clock input of next flip-flop i.e. FF-B

Asynchronous or ripple counters

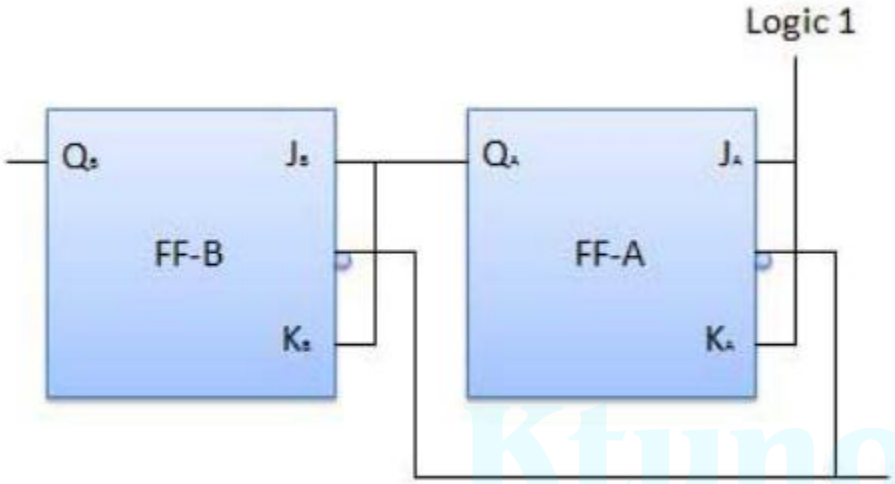


Clock	Counter output		State number	Deciimal Counter output
	Q	Q		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

Synchronous counters

- If "clock" pulses are applied to all flip-flops in a counter simultaneously, then such a counter is called as synchronous counter
- Logic diagram of a 2-bit synchronous up counter is shown in figure
- J_A and K_A inputs of FF-A are tied to logic 1
- So FF-A will work as a toggle flip-flop
- The J_B and K_B inputs are connected to Q_A

Synchronous counters



Clock	Counter output		State number	Deciimal Counter output
	Q_B	Q_A		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

Classification of counters

- Depending on way in which counting progresses, synchronous or asynchronous counters are classified as follows
  1. Up counters
  2. Down counters
  3. Up/Down counters