2021 Asian Conference on Innovation in Technology (ASIANCON)
Pune, India. Aug 28-29, 2021

Low Power and Area Efficieny ALU With Different Type of Low Power in Full Adders

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2021 Asian Conference on Innovation in Technology (ASIANCON) | 978-1-7281-8402-9/21/$31.00 ©2021 IEEE | DOI: 10.1109/ASIANCON51346.2021.9544561

***Abstract*—This paper presents a low power area efficient of a ALU using different low power full adders .Classified as XNOR logic, pass transistor, 2T XOR logic. The 4-bit ALU design is compared with respect in their power consumption and area .ALU is an operating system named as Arithmetic and Logic Unit, which perform arithmetic operation like ADD, SUB, PASS THROUGH TWO'S COMPLEMENT etc. and logic operation like AND,OR,EXCULSIVE OR,EXCLUSIVE NOR etc. We introduce different types of full adders, which are taken as 6T XNOR logic, 6T 2t XOR Logic and pass transistors using 6T to produce sum and multiplexers are used for carry .Full adder is a part of an ALU, it can be used with varying Transistors .By reducing full adder power, we can reduce the power of ALU .Compared with existing technique power can be decreased by <50% by changing full adders .The simulation is carried in cadence virtuoso 90nm technology. Compared with the previous design of gate diffusion input, the results shows area efficient and low power with existing work.**

Keywords—Gate Diffusion Input Technique; XNOR logic ;2T XOR logic; Pass Transistors

I. INTRODUCTION

Varying the VLSI circuits perform at low power with high accurate speed .The ALU (arithmetic and logic unit) operations are the parts that produce for low power with high speed advantages to produce different sections digital signal processing, microprocessor ,VLSI, microcontroller, etc. ALU is used for all arithmetic and logic operations.ALU has different parts to produce output they are full adder,2x1, 4x1 multiplexer circuits. The 1-bit full adder circuit is mapped using 2T XNOR logic ,2T XOR logic, PASS TRANSISTORS. 2x1 multiplexer and 4x1 multiplexer circuits are designed using Gate Diffusion Input technique. The count of transistors and power is reduced in 2T XNOR ,2T XOR logic and pass transistors also with respect to there Gate Diffusion Input Technique .This paper gives you a mature quality of produced results in 2T XNOR ,2T XOR logics and Pass transistors for full adder in the layout of Arithmetic and logic units .

The parts of paper is divided as courses Section II explains the existing methodology . Section III consists of the justification of method used in the existing work. In the section IV rationalizes the operation arithmetic and logic unit design .Section V sector represents the simulation result and analysis .Further conclusion is at in section V.

II. PREVIOUS WORKS

The previous paper presents a existing work Gate Diffusion Input technique (GDI), Which is a approach for lowering the power with area. ALU can be designed in N number of types. The previous work used a ALU as 4x1 multiplexer, 2x1 multiplexer and full adder .GDI cell has one PMOS and one NMOS .GDI cell has three inputs and one output. This 2x1, 4x1 MUX and full adder are implemented using Gate Input technique.

This works has given a amount of power consumed by every part of ALU as 2x1 multiplexer based gate diffusion input technique are implemented using two transistors and consumes the powers of 2.338nW .4x1 multiplexers using six transistors and consumes the power of 2.456nW .Full adder based Gate Diffusion Input technique has 10 transistors and consumes the power of 2.085nW .ALU based GDI technique has consumed the power of . The low power of full adder using 2T XNOR logic consumes power of1.953nW .Low power in full adder using 2T XOR logic consumes power of 2.342nW . The low power based full adder using pass transistors logic consumes power of 2.067nW.Based on the full adder implementation of sum using XOR-XNOR and COUT using NMOS-PMOS logic, which gives the improved conclusion in speed, Power and threshold loss problem.

III. GATE DIFFUSION INPUT TECHNOLOGY

GATE DIFFUSION TECHNIQUE is an recent useful method in the VLSI, it is used to reduce both power and area. It consists of G,P,N inputs and a output.

The G is a common gate input, P represent Selection input and N represents basic input. The G can have either '0' or '1'.The N can have either '0' or '1', when P input is '1',it performs A'+B operation or else it perform AND operation. When N,P,G has neither '0' nor '1' input, it performs MUX operation. When N input is '0', P input is '1' and G has neither '0' nor '1', it performs NOT operation. It can be seen in TABLE 1.

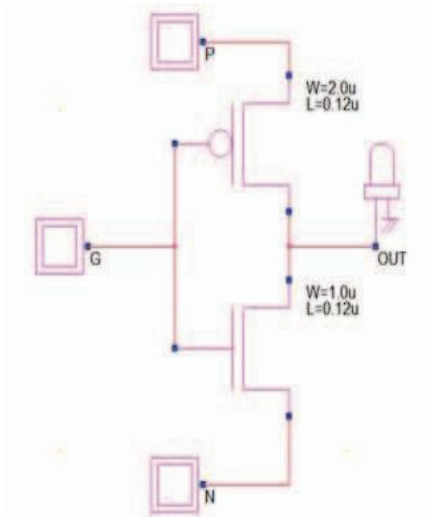

Fig. 1. Basic GDI Cell

TABLE I. LOGIC FUNCTIONS OF GDI CELL

S.No	N I/P	P I/P	G I/P	OUTPUT	FUNCTION
1	0	B	A	A'B	F1
2	B	1	A	A'+B	F2
3	1	B	A	A+B	OR
4	B	0	A	AB	AND
5	C	B	A	A'B+AC	MUX
6	0	1	A	A'	NOT

A. GDI Based 2X1 Multiplexer

Multiplexer acts as an switch . Multiplexer has n selection line and 2^n input line. For 2x1 multiplexer ,it consists of two input and one selection with a output .

In this we can see a one PMOS and NMOS .MOS contains drain gain and source .In PMOS ,the source is opposite to the gate and for NMOS ,the source moves towards the gate. The gates are connected to selection input 'S' and drain of PMOS is given as input 'A' and source of PMOS and NMOS drain are connected and given as a output. In NMOS ,source with an input 'B' .

The PMOS acts as switch off and NMOS is connected as switch ON. When the selection line '0', the PMOS will be 'on'. When the selection line is '1',the NMOS will be 'on'.

TABLE II. .TRUTH TABLE OF 2X1 MULTIPLEXER

S	A	B	OUT
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

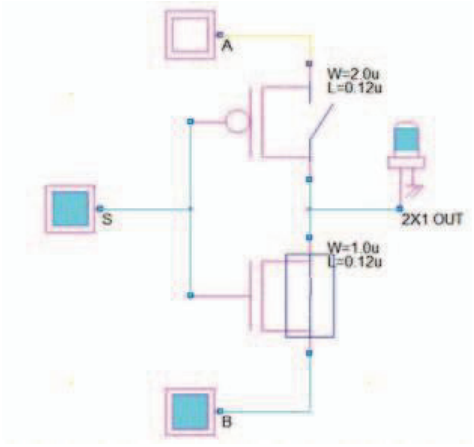

Fig. 2. 2x1 multiplexer based GDI technique

B. GDI Based 4 X 1 Multiplexer

4X1 multiplexer consists of 4 inputs and 2 selection line respectively. It has six transistors, depending on the two selection line, the output will be generated. When s0 s1='0', then A input is taken as an output .When s0='0' & s1='1',then B input is given to the output. When s0/s1='1', then C input is given to the output. When s0/s1='1',then C input is given to the output .When s0 s1='1', then D input is taken as an output.

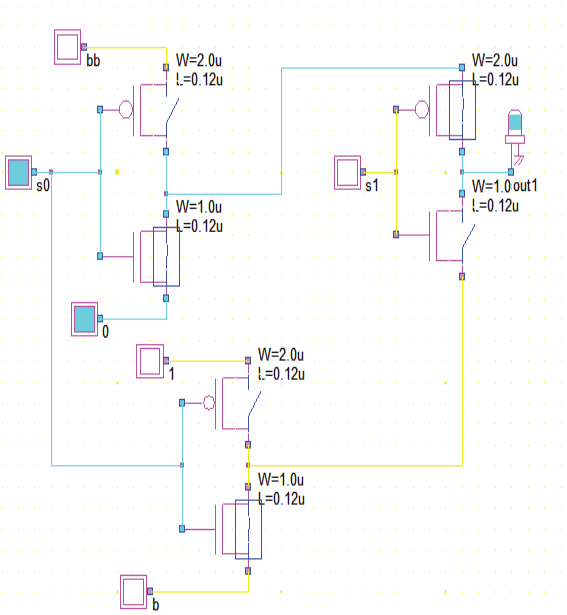

Fig. 3. 4x1 mutiplexer using GDI technique.

C. XNOR Technique

XNOR gate is the basic architecture section for full adder circuit. The 3 Transistor XNOR module consumes the less power than the XOR module. When A and B input is zero, it gives the output value as '1'. When A=0/1 and B=0/1, it gives the output value as '0'. When A and B input is one, then it gives the output value as '1'.

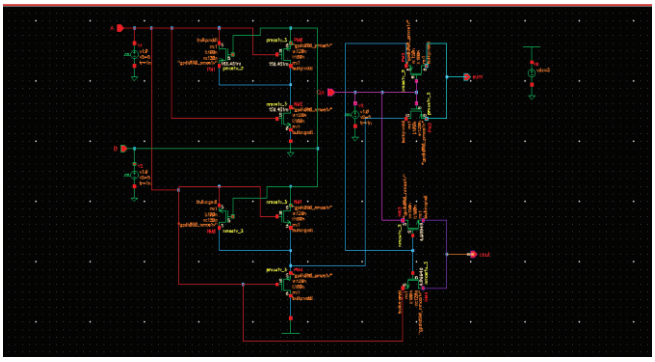

Fig. 4. Schematic diagram of GDI technique using cadence virtuoso technology 90nm

D. FULL ADDER BASED 2T XNOR TECHNIQUE.

Full adder based XNOR technique has 6 transistors, it consist of two defined 2T XNOR module generates the SUM as output and multiplexer generates the CARRY output. Full adder is a basic component for an ALU. Depending on the three input A,B,C, the sum and carry output can be generated. Full adder based XNOR technique consumes the power 1.983nW. Voltage given as 5V and delay as 1ns in input.

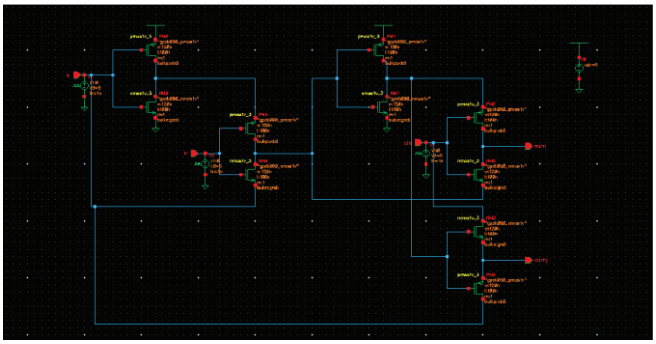

Fig. 5. schematic diagram of 2T XNOR (6T) technique using cadence virtuoso technology 90nm

E. Full Adder Using 2T XOR Technique

Full adder based XOR technique has 6 transistors, it consist of two 2T XOR modules which generates the SUM as output and multiplexer generates the CARRY output respectively. Full adder is a basic component for an ALU. Depending on the three input A,B,C, the sum and carry output can be generated. Full adder based XOR technique consumes the power 1.961nW. Voltage given as 5V and delay as 1ns in input.

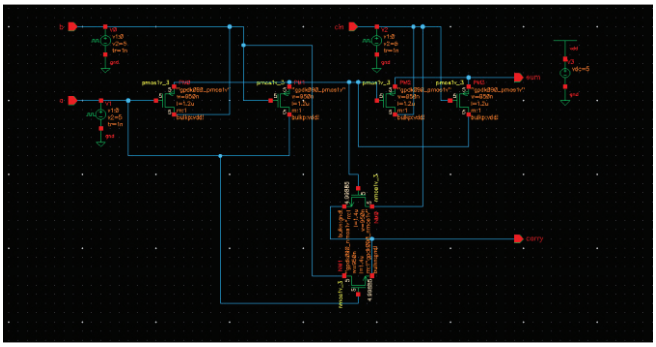

Fig. 6. schematic diagram of 2T XOR (6T) technique using cadence virtuoso technology 90nm

F. Full Adder Using Pass Transistors Technique

Full adder based PASS TRANSISTORS technique has 6 transistors, it consists of pass transistors generates, the SUM and CARRY outputs same as other techniques. Full adder is a defined component for an ALU. Depending on the three input A,B,C, the sum and carry output can be generated. Full adder based pass transistors technique consumes the power 2.067nW. Voltage given as 5V and delay as 1ns in input.

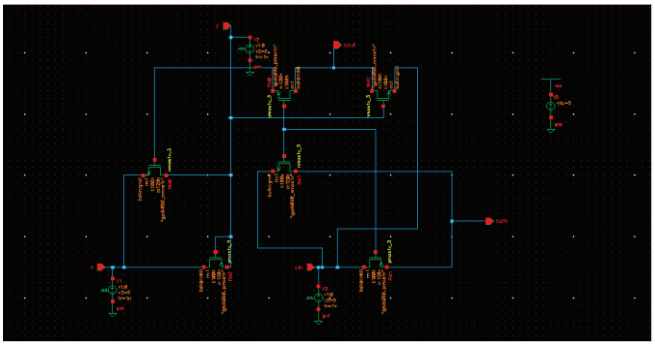

Fig. 7. schematic diagram of PASS TRANSISTORS (6T) technique using cadence virtuoso technology 90nm

G. Design Of Alu Using Different Type Of Low Power Full Adders

An arithmetic and logic unit ia a fundamental block for different processors in different aspects .It performs many operations like addition, Subtraction, XOR, XNOR, NAND, OR etc. The 1-bit ALU operation can be implemented using two 4x1 multiplexer, one 2x1 multiplexers and full adder taken one .In 4-bit ALU operation is designed using eight 4x1 multiplexers, Four full adders, Four 2x1 multiplexers. Depends on the three input factors that is selection lines s2,s1,s0.the arithmetic and logic operation can be performed.

The block of 4x1 multiplexer consists of four input, which is logic 0,logic 1,b and bb. Depends upon the s0 and s1 selection line, the required output will be generated. These output can be indicate as the B .This acts as an 'B' input for the full adder. Then the full adder operation can be performed using different techniques by inserting 2T XNOR,2T XOR, PASS TRANSISTORS to give results as output .

After this, further in the next stage of 4x1 multiplexer has the input of full adder of sum , which is EXOR ,EXNOR, AND, OR. Depends on the selection lines, the output can be generated .it acts as an input for the 2x1 multiplexer. Another input of 2x1 multiplexer is the full adder sum output. Finally, the output stage of 2x1 multiplexer can be generated using s2 selection line.

TABLE III. OPERATIONS OF ALU

S2	S1	S0	OPERATIONS
0	0	0	Buffer
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBTRACTION
1	1	0	BITWISE NAND
1	1	1	Inverter

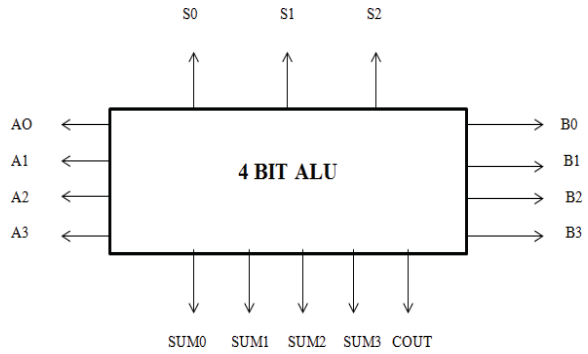

Fig. 8. Logic repersentation of ALU

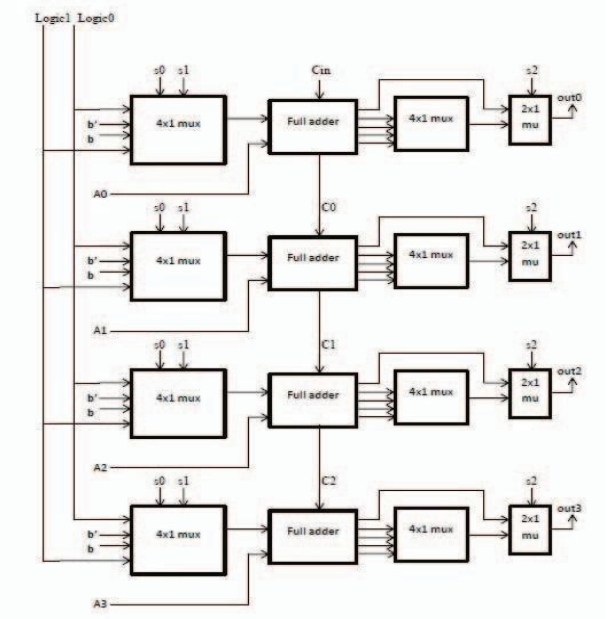

Fig. 9. Process of 4bit ALU

Multiplexer's logic at the input stage consists of 4x1, 2x1 multiplexers. Depends upon the selection line of s0,s1 and s2, the output of full adder has been computed. Depends upon the selection line of s0,s1 and s2,the output of ALU has been computed. Input stage multiplexer consists of VDD, GND, b and bb . The output stage multiplexer consists of EXOR,EXNOR,AND and OR input.

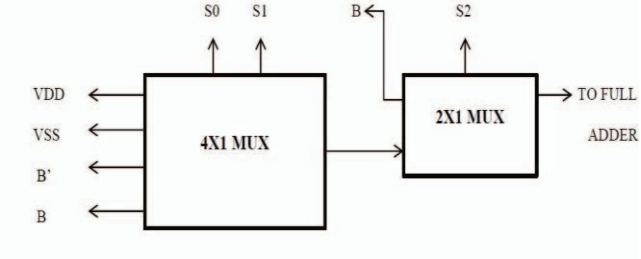

Fig. 10. Architecture of multiplexer's logic at the input stage

This paper as better technique of modified XNOR,XOR,PASS TRANSISTORS with just 6Transistors The schematic of 4bit ALU has been implemented using cadence virtuoso platform.

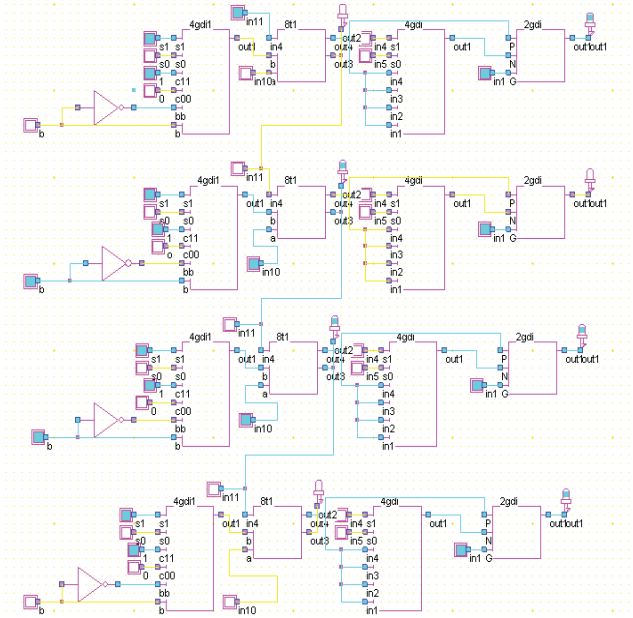

Fig. 11. Basic design of 4bit ALU

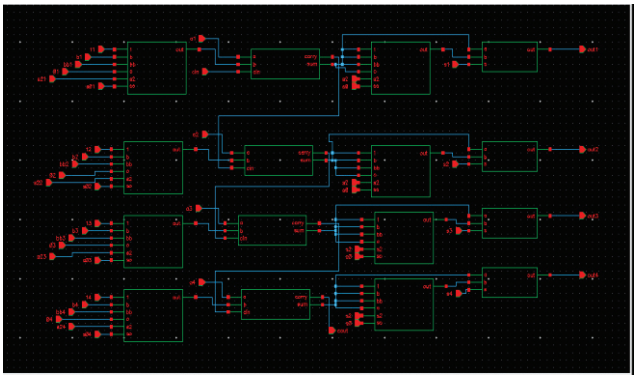

Fig. 12. schematic diagram of a ALU using full adder with different techniques

IV. SIMULATION RESULTS AND ANALYSIS

The process as the execution of the a layout using cadence virtuoso platform on 90nm technology. The simulation results shows the output of 2x1 multiplexer, 4x1 multiplexer, full adder's of XNOR-XOR, 2T XNOR, 2T XOR, PASS TRANSISTORS and complete 4-bit ALU design graph .The bar chart for power consumption and number of transistor.

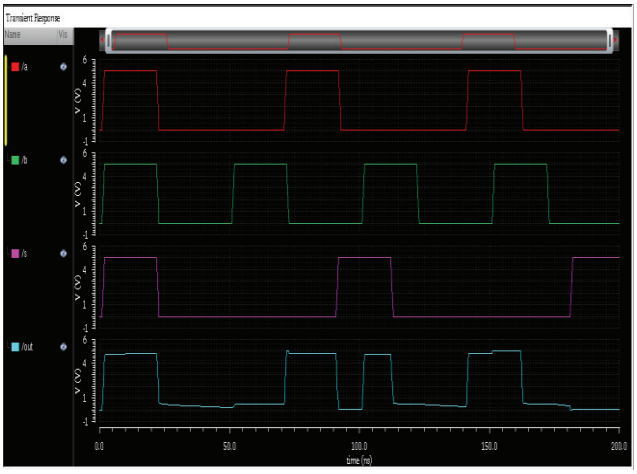

Fig. 13. Produced output of 2x1 Multiplexer

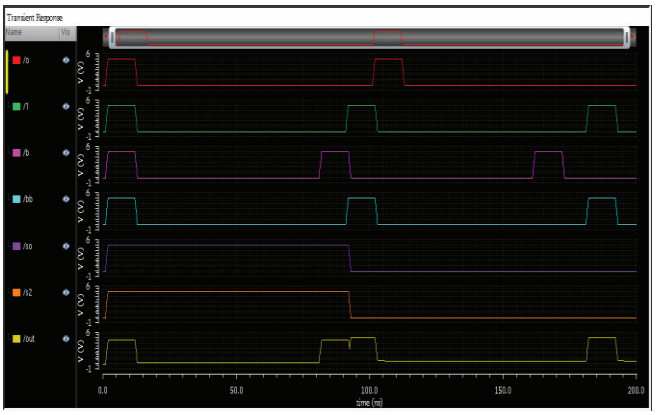

Fig. 14. Produced output of 4x1 Multiplexer

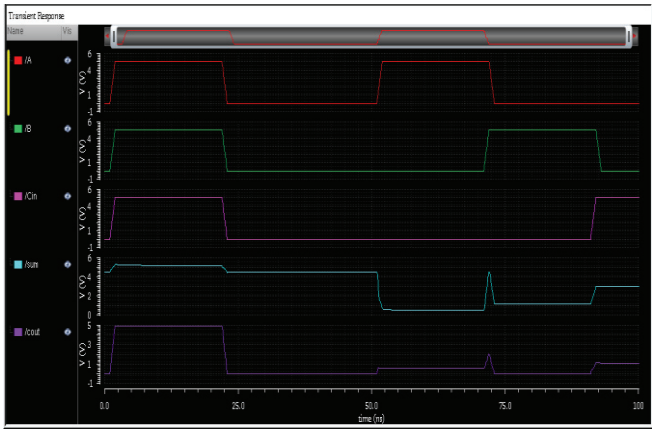

Fig. 15. Produced output of existing XNOR-XOR

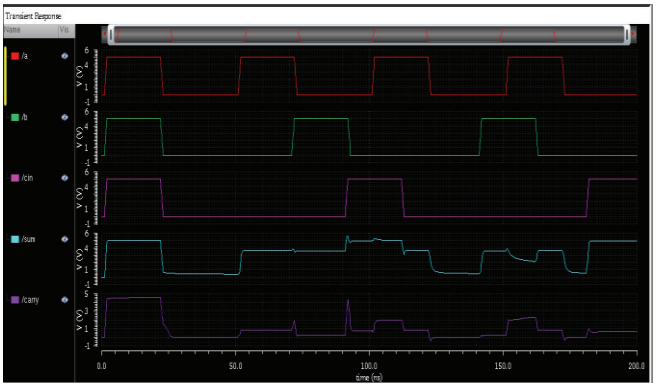

Fig. 16. Simulated output of 2T XNOR technique

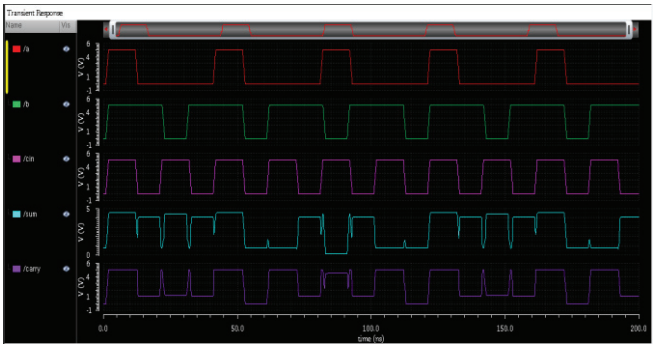

Fig. 17. Produced output of 2T XOR technique

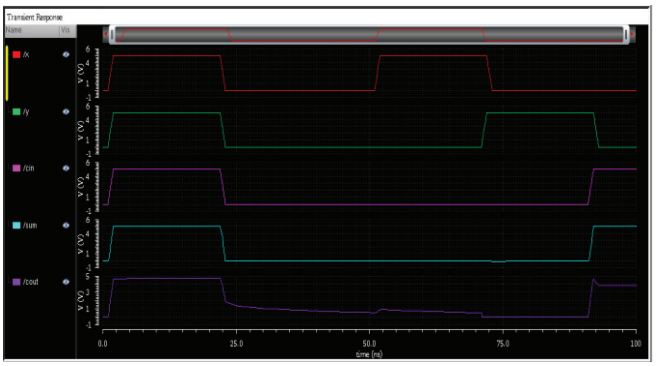

Fig. 18. Produced output of PASS TRANSISTORS technique

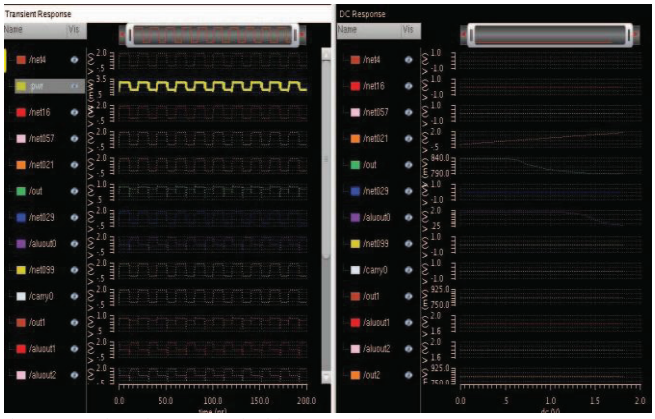

Fig. 19. Produced output of 4bit ALU for 2T XNOR, 2T XOR, PASS TRANSISTORS of full adder

TABLE IV. 4BIT ALU POWER CONSUMPTION

S.No	DESIGN	No. of Transistors	Input Delay (nS)	Power (nW) AVG.POWER=P(nW)*D(nS)
1	ALU with GDI Technique	60	1ns	37.533nW
2	ALU with 2T XNOR Technique	60	1ns	36.844nW
3	ALU with 2T XOR Technique	60	1ns	36.933nW
4	ALU with PASS .T Technique	60	1ns	37.268nW

V. CONCULSION

This work presents a 4-bit ALU designed by cadence Virtuoso 90nm technology for low area and power with 2T XNOR ,2T XOR, PASS TRANSISTORS of full adder and using GDI for multiplexer. Various methods of multiplexer and full adder are implemented and compared. Compared with previous paper, it reduced the power and area of ,30%. The 2x1 multiplexer and 4x1 multiplexer are designed using Gate Diffusion input Technique. Full adder based proposed technique are 37.533nW, but 2T XNOR technique consumes 36.844nW, for 2T XOR technique consumes 36.933nW and for PASS TRANSISTORS technique 37.268nW .As we can

observe pass transistor and XOR consume more than the XNOR technique. Using these techniques, full adder power leads to reduce, therefore he ALU design also tends to reduced. Power, delay and number of transistors are compared using GDI,PTL,2T XOR , 2T XNOR technique and PASS transistors.

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