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Visvesvaraya Technological University, Belgaum

Mini Project Report on

"LOW POWER AND AREA EFFICIENT ALU USING FULL ADDERS"

Submitted in partial fulfilment of the requirement for completion of
MINI PROJECT [23EC5PWMPR]

Submitted by

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CERTIFICATE

This is to certified that the Mini Project entitled **"LOW POWER AND AREA EFFICIENT ALU USIGN FULL ADDERS"** is a bonafide work carried out by **Sanjith B (1BM22EC220), Shreya P (1BM22EC233), Shreya Pandey (1BM22EC236) and Srilakshmi MR (1BM22EC257)** submitted in partial fulfilment of the requirement for completion of MINI PROJECT [23EC5PWMPR] of Bachelor of Engineering in Electronics and Communication during the academic year 2024-25. The Mini Project report has been approved as it satisfies the academic requirements.

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DECLARATION

We, **SANJITH B (1BM22EC220), SHREYA P (1BM22EC233), SHREYA PANDEY(1BM22EC236), and SRILAKSHMI MR (1BM22EC257),**
hereby declare that the Mini Project entitled "**LOW POWER AND AREA EFFICIENT ALU USING FULL ADDERS"** is a bonafide work and has been carried out by us under the guidance of **ASHWINI V, Assistant Professor**, Department of Electronics and Communication Engineering, BMS College of Engineering, Bengaluru submitted in partial fulfilment of the requirement for completion of MINI PROJECT [23EC5PWMPR] of Bachelor of Engineering in Electronics and Communication during the academic year 2024-25. The Mini Project report has been approved as it satisfies the academic requirements in Electronics and Communication engineering, Visvesvaraya Technological University, Belagavi, during the academic year 2024-25.

We further declare that, to the best of our knowledge and belief, this Mini Project has not been submitted either in part or in full to any other university.

Place: Bengaluru

Date:

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We heart fully thank our guide ASHWINI V for the guidance and constant encouragement throughout the course of this Mini Project without which this project would not be successful.

A number of personalities, in their own capacities have helped us in carrying out this Mini Project. We would like to take this opportunity to thank them all.

Last but not the least, we thank our friends and family for their encouragement and help in accomplishing the objective of the Mini Project work.

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ABSTRACT

This report explores the role of Very Large Scale Integration (VLSI) technology in advancing modern electronic systems, particularly focusing on the design of low-power and area-efficient Arithmetic Logic Units (ALUs). VLSI enables the integration of millions of transistors into a single microchip, driving innovations in devices like microprocessors, memory chips, and application-specific integrated circuits (ASICs). As electronic devices evolve, the need for high performance, reduced power consumption, and minimal area becomes more critical, especially in battery-operated and energy-efficient systems. Power consumption in VLSI circuits is primarily influenced by dynamic and static power, both of which have become key challenges in the design of digital circuits. Full adders, central to ALU functionality, are optimized for low power and area efficiency, impacting the overall performance of processors. This report investigates various strategies for designing low-power full adders, including novel circuit topologies and advanced logic synthesis techniques, highlighting the trade-offs and innovations that drive advancements in VLSI technology. The study underscores the importance of balancing power efficiency, speed, and reliability in the development of next-generation VLSI systems.

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List of abbreviations

1. IEEE- Institute of Electrical and Electronics Engineers
2. VLSI-Very Large Scale Integration
3. ASIC- Application Specific Integrated Circuits
4. ALU- Arithmetic Logic Unit
5. GDI- Gate Diffusion Input
6. MUX- Multiplexer

CHAPTER 1

Introduction:

VLSI (Very Large Scale Integration) refers to the process of integrating or embedding a large number of transistors, capacitors, resistors, and other electronic components onto a single microchip. This technology has revolutionized the field of electronics, enabling the creation of complex integrated circuits (ICs) that can perform a wide range of functions in a very small form factor. The primary goal of VLSI technology is to pack thousands to millions of transistors into a single chip to reduce size, cost, and power consumption while enhancing performance. VLSI has made significant advancements since its inception in the 1970s, facilitating the development of sophisticated devices such as microprocessors, memory chips, and application-specific integrated circuits (ASICs).

In the realm of Very Large Scale Integration (VLSI) design, the quest for enhanced performance, reduced power consumption, and minimized area has become paramount, especially as electronic devices become more sophisticated and ubiquitous. Among the critical components of digital systems, the Arithmetic Logic Unit (ALU) plays a central role in performing arithmetic and logical operations, thereby forming the backbone of processors and computational units. As technology scales down, designers are increasingly challenged to maintain a balance between high performance and low power consumption, particularly given the constraints imposed by battery-operated devices and the growing demand for energy efficiency in data centres. Power consumption in VLSI circuits is primarily categorized into dynamic and static components. Dynamic power, which is the energy consumed when the circuit is active, is predominantly influenced by the switching activity of transistors. In contrast, static power arises from leakage currents in transistors, which become more pronounced as technology nodes shrink. As a result, significant research has focused on developing low-power techniques that address both dynamic and static power consumption in digital circuits, particularly in ALUs, where power efficiency is crucial for overall system performance. At the heart of the ALU's functionality are the full adders, responsible for performing binary addition operations. Given their frequent utilization within ALUs, optimizing full adders for low power and area efficiency directly impacts the overall performance of the ALU. Various strategies have been developed to design low-power full adders, including but not limited to the use of novel circuit topologies, reduced swing voltage levels, and advanced logic synthesis techniques. These approaches aim to minimize switching activity, enhance robustness against process variations, and reduce the overall circuit area. This introduction sets the stage for a comprehensive exploration of low power and area-efficient ALUs, emphasizing the pivotal role of full adders. By delving into different types of low power full adders, including dynamic, static, and hybrid designs, we can better understand the trade-offs and innovations driving advancements in VLSI technology. Each approach not only addresses power efficiency but also considers the impact on performance metrics such as speed and reliability, thereby highlighting the multifaceted nature of modern VLSI design challenges.

CHAPTER 2

Literature survey:

1. **A Low Power and High Speed 8-bit ALU Design using 17T Full Adder~** 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN)

   In this paper proposed by Shubham Anand and Prof. S. Indu, this paper proposes a novel 17T full adder and its application in an efficient Arithmetic Logic Unit (ALU) design, aimed at reducing power consumption and minimizing delay. The proposed design significantly improves the power-delay product, enhancing the overall efficiency of digital processors. The ALU, which performs arithmetic and logical operations, benefits from increased speed and reduced power requirements, resulting in higher throughput. The 17T full adder uses multiplexing logic to generate Sum and Carry-Out signals with similar delay paths, achieving a signal propagation delay reduction of 83.8% to 89.9% compared to existing hybrid full adders (HFA-22T, HFA-20T, HFA-19T) and conventional 10T/11T adders. Additionally, power consumption is reduced by 71.5% to 74.3%. The proposed 8-bit ALU outperforms existing designs, showing a 52% improvement in power-delay product. Simulations and evaluations were performed using Cadence Virtuoso v15.0 in a 45 nm process. "GATE DIFFUSION TECHNIQUE is an recent useful method in the VLSI, it is used to reduce both power and area. It consists of G,P,N inputs and a output."

TABLE II. SIMULATION RESULTS (POWER IN e-6W, DELAY (units), AND PDP IN aJ) FOR DIFFERENT DESIGNS

Design	Power	Delay	PDP
FA-11T	16	64 ps	1024
HFA-22T	4.08	59.1 ps	241.1
*FA-17T	**1.16**	**9.52** ps	**11.04**
1-bit ALU [2]	4.47	20.33 ns	90.87
*1-bit ALU	**3.82**	**15.58** ns	**59.51**
8-bit ALU [2]	32.9	6.95 ns	228.65
*8-bit ALU	**26.30**	**4.18** ns	**109.93**

*Means proposed design

2. **Design of Low Area and Low Power Systolic Serial Parallel Multiplier using CNTFETs~ 2021 IEEE International Symposium on Smart Electronic Systems (iSES)**

   In this paper proposed by Dheeraj Kumar KB, Lakshmi Bhanuprakash Reddy, Vikramkumar Pudi and Srinivasu Bodapati we confer that This paper presents a CNTFET-based systolic serial-parallel multiplier, designed for 100% efficiency, operating with product terms 0, X, 2X, and 3X, where X is a serial input. The design incorporates modules such as 4×1 MUX, 2×1 MUX, OR gates, full adders, and D-Flipflops. To reduce area and power, combinational logic gates are designed using the Gate Diffusion Input (GDI) technique. A new 10-transistor D-Flipflop with a single clock load and a 10T full adder are proposed to further optimize area and power consumption. The proposed multiplier achieves a 41% area reduction and offers significant improvements over existing designs, including an 82.65% reduction in transistor count, a

95.96% decrease in power dissipation, a 98.12% reduction in delay, and a 99.92% reduction in power-delay product (PDP).

"In this paper, to achieve energy efficient multiplier design, we have utilized GDI based logic gates and proposed a new D flip-flop."

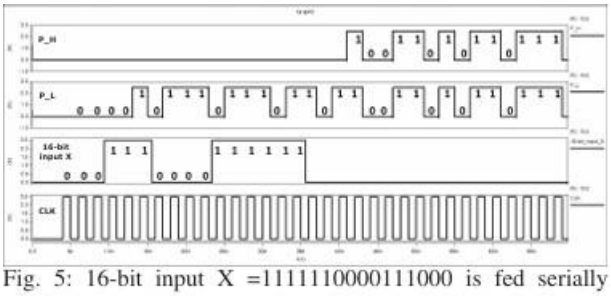


Fig. 5: 16-bit input X =1111110000111000 is fed serially starting with LSB first. Product obtained serially over P_L and P_H starting with LSB first.

3. Area Optimization of CMOS Full Adder Design using 3T XOR

In this paper oublished by Somashekhar Malipatil, Viaks Maheshwari and Marepally Bhanu Chandra, we confer that This paper proposes a low-power digital circuit design using the Gate Diffusion Input (GDI) technique, which minimizes area and power consumption. An XOR gate is designed with 3 transistors, and a CMOS full adder is implemented using two 3T XOR gates and one 2T MUX, totaling 8 transistors. Voltage scaling is applied by reducing the supply voltage. The proposed full adder achieves a power consumption of 4.604 μW and occupies an area of 144 μm².

"GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low power circuits, using reduced number of transistors. The dynamic power isexpressed as shown in equation"

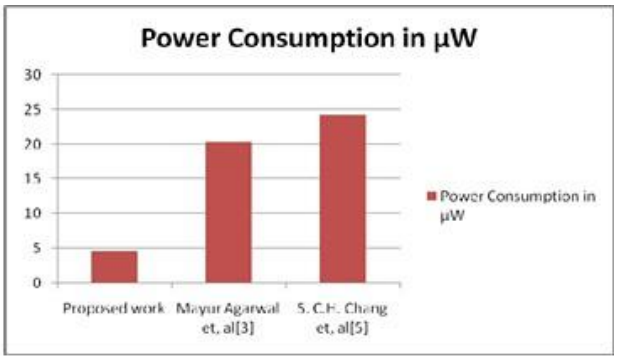


Fig. 12. Power consumption comparison with existed work.

4. Design of 8:1 Multiplexer using Gate Diffusion Input(GDI) Technique and Comparison of Delay Performance with Pass Transistor Logic

In this paper proposed by B. Sai kumar, Dr.S.Jayanthi, Dr.Rakhshgan, we confer that, his paper presents the design of an 8:1 multiplexer using the Gate Diffusion Input (GDI) technique, a pass transistor logic (PTL) approach, to address low power and energy efficiency in digital circuits. The design is implemented with basic GDI cells using the Tanner EDA tool and DSCH3. The GDI technique overcomes the limitations of PTL, offering improved performance. Simulation results show that the GDI-based multiplexer achieves a propagation delay of 0.04759 ns and power dissipation of 0.04007 W, compared to 0.06378 ns and 0.06191 W for PTL. The GDI technique demonstrates lower delay and power consumption than traditional PTL.

"In this investigation, it was found that the GDI approach dissipates power at a rate of 0.04007 w/s and delays at 0.04757 ns, while a pass transistor dissipates power at a rate of 0.06191 w/s and delays at 0.06378 ns.The GDI technique is better than existing pass transistor logic with reduction of delay performance and power consumption."

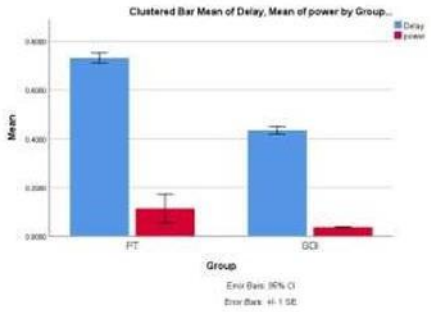


Fig. 6. The bar chart represents the comparison of average delay performance, average power consumption with GDI technique and pass transistor logic in terms of mean.

5. Design and Implementation of Full Adder Cicuit Based on VTM-Logic Gates~ 2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS) Phoenix, Arizona, USA, August 6-9, 2023

In this paper proposed by Frzad Mozafari, Majid Ahmadi and Arash Ahmadi, we confer that this paper explores the use of memristors in logic circuit design, building on a previously proposed Voltage-to-Memristance (VTM) architecture for memristive-based digital circuits. Using the VTM technique, the authors present the implementation of additional pure memristive logic gates, such as Exclusive-OR (XOR) and Exclusive-NOR (XNOR). To illustrate the effectiveness of this approach, a full adder design is presented. The paper also discusses the performance of the proposed technique in terms of power consumption and resource requirements.

"Adders are essential components of Computation-In-Memory (CIM) architecture, and variety of memristor-based adders have been proposed using two main approaches"

TABLE IV: Simulation results for proposed logic compared with adder circuits at 1.8 (v)

Adder circuits	Power supply (v)	Propagation Delay (ps)	Static power (pW)	Dynamic power (μW)	Count (#)
VTM (XOR, AND, OR)	1.8	173.4	68.6	3.01	20 Mem
VTM(NAND)	1.8	202.1	79.8	3.99	27 Mem
CMOS	1.8	251.7	374.0	5.542	28 Tr
CPL	1.8	188.0	1.383 (nW)	6.520	32+6 Tr
Hybrid	1.8	233.64	233.1	4.189	16 Tr

6. Low Power and Area Efficient Hybrid Adder for ALU operation~ 2023 IEEE International Symposium on Smart Electronic Systems (iSES)

In this paper proposed by Shilpa Sikdar and Trilochan Panigrahi, we are able to confer that, This study presents a low-power, area-efficient hybrid adder for arithmetic logic units (ALUs) in digital systems. It combines pass transistor logic (PTL), gate diffusion input (GDI) logic, and modified GDI (MGDI) logic to reduce power consumption and improve performance while minimizing transistor count. Evaluations were done using Cadence Virtuoso with a 45 nm process and a 1.2 V supply voltage. The proposed adder outperforms existing designs in terms of propagation delay (PD), average power (AP), and power- delay product (PDP). This work is valuable for designing efficient adders in portable, battery-powered devices.

"The formula for the average Power Pavg = Pdynamic + Pstatic"

TABLE III
PERFORMANCE OF FULL ADDER CELLS

Full Adder	TC	AP (uW)	PD (ps)	PDP (aJ)
CCMOS [5]	28	3.614	20.26	73.21
Parameshwara [10]	16	2.218	15.921	35.312
Hasan GDI FA [11]	18	3.124	21.41	66.884
Shoba [12]	22	2.021	16.17	32.679
Hussain [13]	18	1.92	14.47	27.782
Proposed FA	14	2.214	18.342	40.606

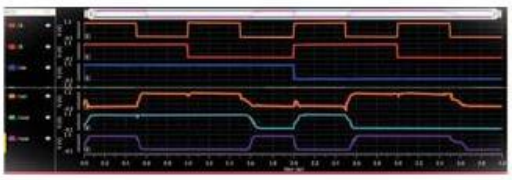


Fig. 4. Simulation result of proposed full adder

7. Low Power and Area Efficieny ALU With Different Type of Low Power in Full Adders ~ 2021 Asian Conference on Innovation in Technology (ASIANCON) Pune, India. Aug 28-29, 2021

In this paper proposed by K Aruna Manjusha, K Sahithya, B Naresh and D Subodh, we confer that this paper presents a design for a low-power, area-efficient Arithmetic Logic Unit (ALU) by employing various low-power full adder architectures. The full adders considered in the design are based on XNOR logic, pass transistor logic, and 2T XOR logic, which are analyzed for their impact on power consumption and area efficiency. The ALU performs both arithmetic operations, such as addition, subtraction, and two's complement, and logic operations like AND, OR, XOR, and XNOR. By optimizing the full adders, the overall power

consumption of the ALU is reduced significantly. Specifically, the power consumption can be reduced by up to 50% compared to traditional designs by using these low-power full adders. The simulation of the ALU design is conducted using Cadence Virtuoso with a 90nm technology node, and the results show improvements in both power efficiency and area compared to previous designs, including those using Gate Diffusion Input (GDI) techniques. The findings highlight the importance of optimizing the full adder circuit in reducing the power consumption of the ALU, thereby contributing to more energy-efficient digital systems.

“This work presents a 4-bit ALU designed by cadence Virtuoso 90nm technology for low area and power with 2T XNOR ,2T XOR, PASS TRANSISTORS of full adder and using GDI for multiplexer. Various methods of multiplexer and full adder are implemented and compared.”

TABLE IV. 4BIT ALU POWER CONSUMPTION

S.No	DESIGN	No. of Transistors	Input Delay (nS)	Power (nW) AVG.POWER=P(nW)*D(nS)
1	ALU with GDI Technique	60	1ns	37.533nW
2	ALU with 2T XNOR Technique	60	1ns	36.844nW
3	ALU with 2T XOR Technique	60	1ns	36.933nW
4	ALU with PASS .T Technique	60	1ns	37.268nW

CHAPTER 3:

Problem Analysis & Solution:

3.1 Problem Definition:

The paper addresses the challenge of designing a low-power, area-efficient Arithmetic Logic Unit (ALU), which is a key component in processors used for various digital systems like microprocessors and microcontrollers. The problem lies in reducing the power consumption and area of the ALU while maintaining performance, especially in the design of its full adder, which contributes significantly to both power and area consumption.

3.2 Proposed Solution:

The proposed solution is focused on designing a 1-bit-8 functional Arithmetic Logic Unit (ALU) that is both power-efficient and area-efficient. This ALU performs a variety of arithmetic and logical operations, and the design leverages a combination of basic gates and full adders to meet stringent power and area constraints. The design approach is based on CMOS (Complementary Metal-Oxide-Semiconductor) GDI technology, which is widely used for low-power, high-speed digital circuits. The implementation and analysis are carried out using Cadence Virtuoso for analog design and Cadence Genus for digital analysis.

Cadence Virtuoso and Cadence Genus:

Cadence Virtuoso is an analog and mixed-signal design platform. The required ALU circuit is built from transistor level. The components with different parameters or technologies (45nm) can be implemented, this helps analyzing and obtaining the most power and area efficient circuit.

Cadence Genus is a digital design tool that provides synthesis and optimization capabilities. In this context, it is used for synthesizing the digital logic (using full adders and other gates) and for generating power and area reports. These reports provide insights into the total power consumption and the area of the final ALU design, which are essential for verifying that the design meets the required power and area constraints with real time delay and constraints.

Power and Area Report:

Once the design is synthesized and optimized, Cadence Genus generates a **power and area report**. This report provides important metrics such as:

Total Power Consumption: The amount of power required to operate the ALU. This includes both dynamic power (due to switching activities) and static power (due to leakage currents).

Total Area: The total area occupied by the ALU design in silicon, which is important for ensuring that the design fits within the constraints of the target application or chip size. These reports help in verifying whether the design meets the power and area efficiency goals set out at the beginning of the project.

CHAPTER 4:

Methodology & Implementation

4.1 Block Diagram:

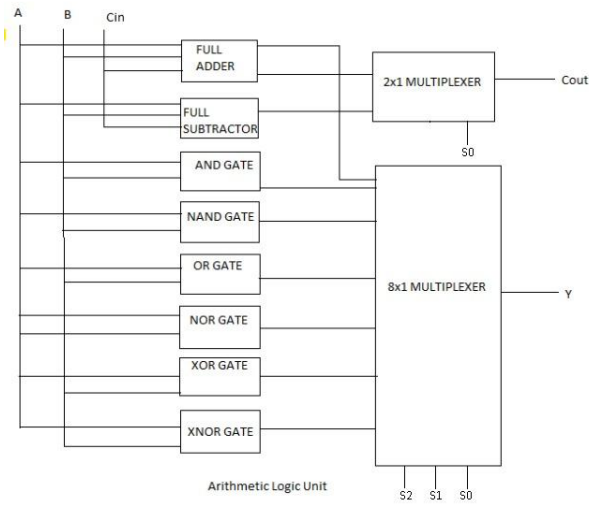


Fig (a): Arithmetic Logic Unit

Arithmetic Logic Unit (ALU) is a critical component of a computer's central processing unit (CPU) that performs arithmetic and logical operations. It acts as the computational engine within the CPU, processing data and carrying out calculations required by programs. The ALU is responsible for operations such as addition, subtraction, multiplication, division, and logical operations like AND, NAND, OR, NOR, XOR, XNOR, NOT.

4.1.1 Pictorial Representation

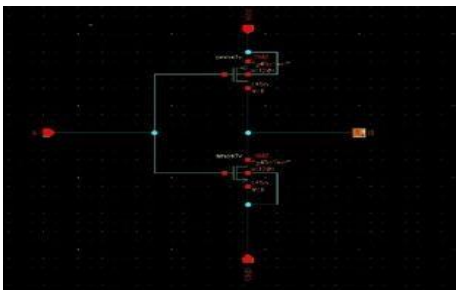
1. Inverter (NOT GATE):

   An **inverter**, also known as a **NOT gate**, is a fundamental logic gate in digital electronics that performs the operation of negation. It takes a single input and produces the opposite (or complement) of that input as its output.

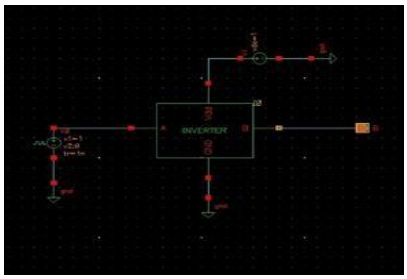
$$Y = \sim A$$

Input	Output
A	Y
0	1
1	0

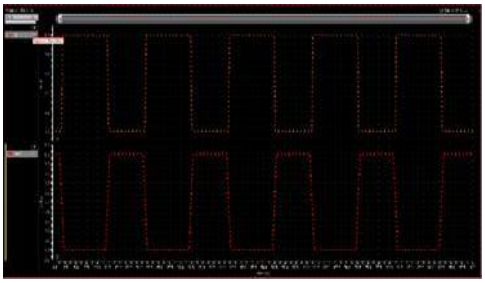
Truth Table



Circuit



Symbol



Output Waveform

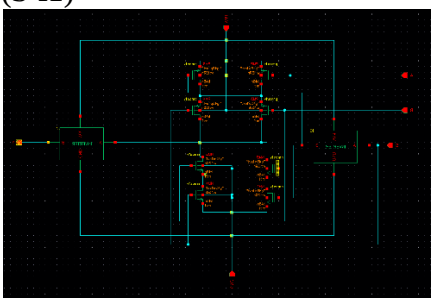
Fig(b): Inverter

2. 2x1 Multiplexer:
   A 2x1 multiplexer (MUX) is a digital device that selects one of two input signals and forwards the selected input to a single output, based on a control signal. The "2x1" indicates that there are two inputs (denoted as I0I_0I0 and I1I_1I1), one control signal (denoted as SSS), and one output.

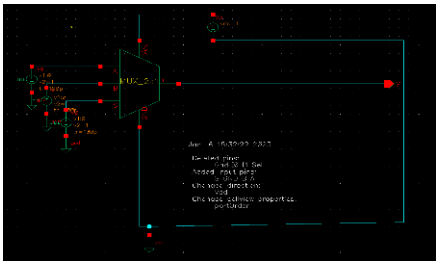
$$Y = (S' \cdot I0) + (S \cdot I1)$$

Select	Inputs		Output
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

Truth Table



Circuit



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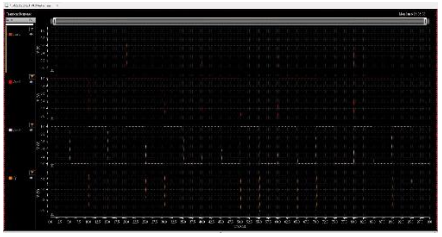


Output Waveform

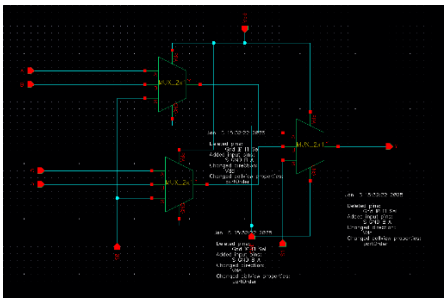
Fig(c): 2x1 Multiplexer

3. 4x1 Multiplexer:
   A 4x1 multiplexer (MUX) is a digital device that selects one of four input signals and forwards the selected input to a single output, based on two control signals. The "4x1" indicates that there are four inputs (denoted as I0,I1,I2,I3I_0, I_1, I_2, I_3I0,I1,I2,I3), two control signals (denoted as S0S_0S0 and S1S_1S1), and one output.

$$Y = (S1' \cdot S0' \cdot I0) + (S1' \cdot S0 \cdot I1) + (S1 \cdot S0' \cdot I2) + (S1 \cdot S0 \cdot I3)$$

INPUTS		Output
S_1	S_0	Y
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

Truth Table



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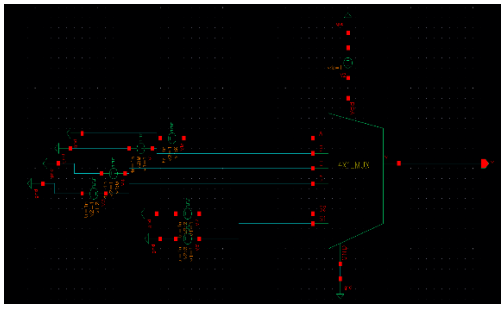

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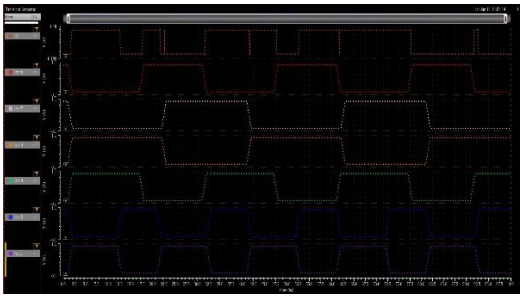


Output Waveform

Fig(d): 4x1 Multiplexer

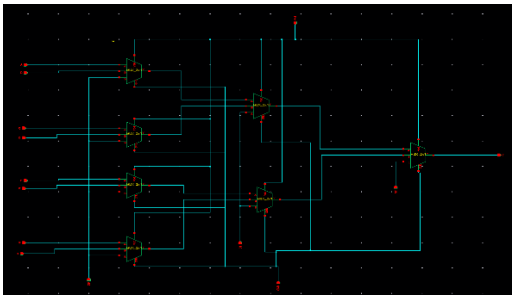
4. 8x1 Multiplexer:

An 8x1 multiplexer (MUX) is a digital device that selects one of eight input signals and forwards the selected input to a single output, based on three control signals. The "8x1" indicates that there are eight inputs (denoted as I0,I1,I2,I3,I4,I5,I6,I7I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7I0,I1,I2,I3,I4,I5,I6,I7), three control signals (denoted as S0,S1,S2S_0, S_1, S_2S0,S1,S2), and one output.

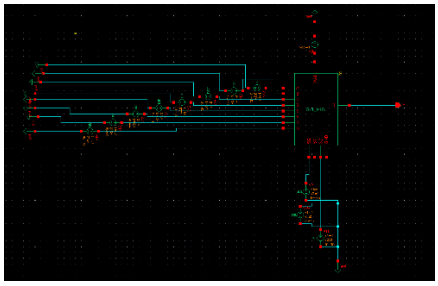
Y=(S2′·S1′·S0′·I0)+(S2′·S1′·S0·I1)+(S2′·S1·S0′·I2)+(S2′·S1·S0·I3)+(S2·S1′·S0′·I4)+(S2·S1′·S0·I5)+(S2·S1·S0′·I6)+(S2·S1·S0·I7)

INPUTS			Output
S_2	S_1	S_0	Y
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

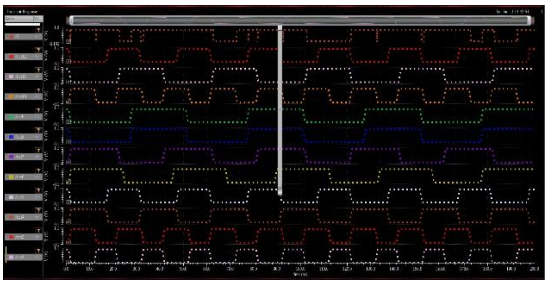
Truth Table



Circuit



Symbol



Output Waveform

Fig(e): 8x1 Multiplexer

5. FULL ADDER:
   A Full Adder is a digital circuit that adds three binary bits—two significant bits and a carry-in bit—and outputs a sum and a carry-out bit. The full adder is an essential building block in arithmetic circuits and is used to perform binary addition in systems like ALUs (Arithmetic Logic Units) and other computational devices.

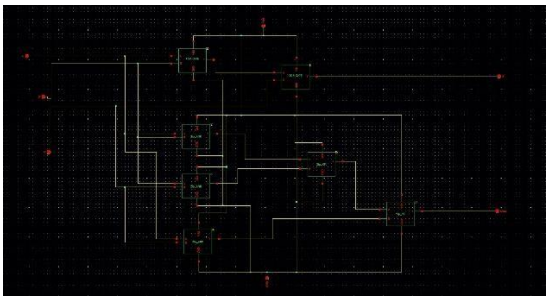
$$S=A \oplus B \oplus Cin$$

$$Cout=(A \cdot B)+(B \cdot Cin)+(A \cdot Cin)$$

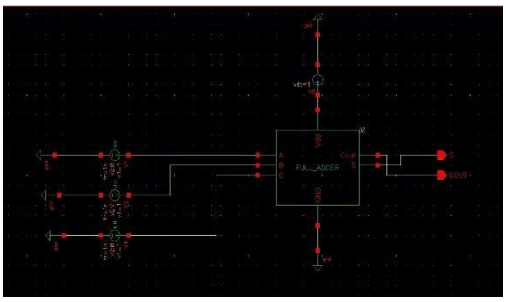
Full Adder

A	B	C	C Out	Sum
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Truth Table



Circuit



Symbol

Output Waveform

Fig(f): Full Adder

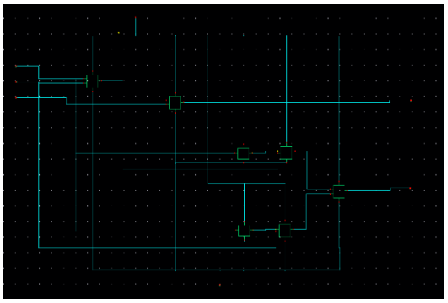
6. FULL SUBTRACTOR:
   A Full Subtractor is a digital circuit that subtracts one binary bit from another, considering a borrow-in bit from a previous lower significant stage. It outputs the difference (also called the "difference bit") and a borrow-out bit to the next higher significant stage. The full subtractor is essential for performing binary subtraction in systems like ALUs (Arithmetic Logic Units).

$$D=A \oplus B \oplus Bin$$

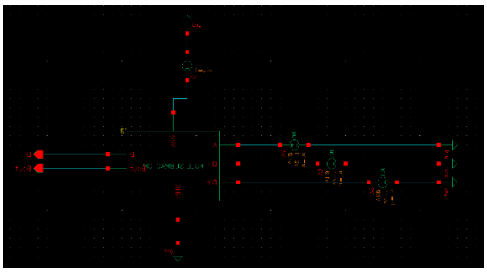
$$Bout= (A \cdot B)+(A \cdot Bin)+(B \cdot Bin)$$

Inputs			Outputs	
A	B	$Borrow_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

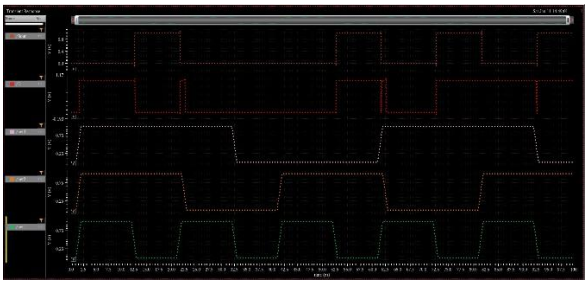
Truth Table



Circuit



Symbol



Output Waveform

Fig(g): Full Subtractor

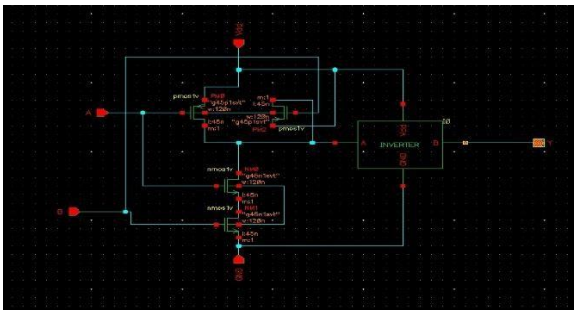
7. AND GATE:
   An AND gate is a basic digital logic gate that implements logical multiplication. It outputs a high signal (1) only when all of its inputs are high (1). If any of the inputs are low (0), the output will be low (0).

$$Y=A\cdot B$$

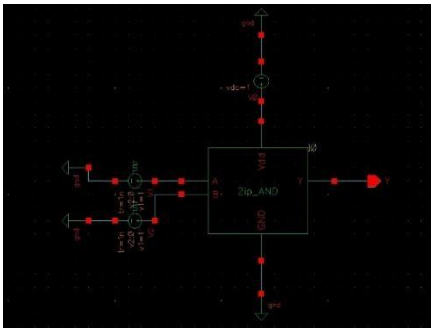
Truth Table

A (Input 1)	B (Input 2)	X = (A.B)
0	0	0
0	1	0
1	0	0
1	1	1

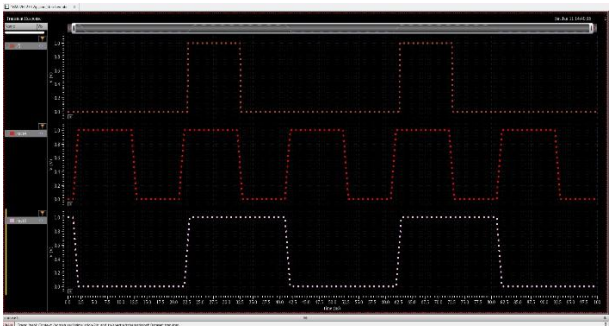
Truth Table



Circuit



Symbol



Output Waveform

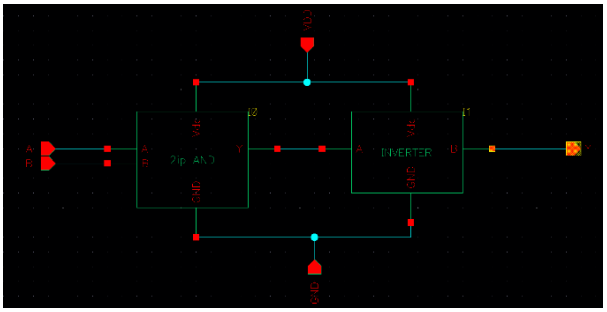
Fig(h): AND Gate

8. NAND GATE:
   A NAND gate (NOT-AND gate) is a digital logic gate that implements the negation of the AND operation. It produces an output of low (0) only when all of its inputs are high (1). In all other cases, the output is high (1). Essentially, a NAND gate is the complement of an AND gate
   .

$$Y=\sim(A\cdot B)$$

A	B	Output
0	0	1
1	0	1
0	1	1
1	1	0

Truth Table



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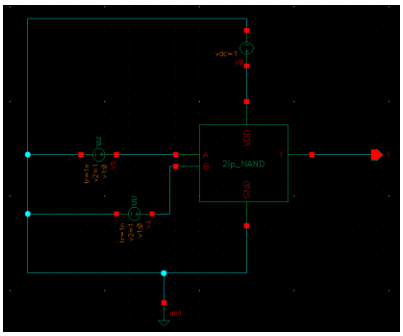
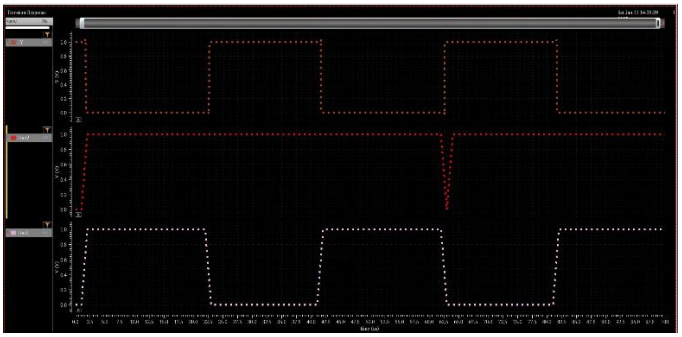


Symbol



Output Waveform

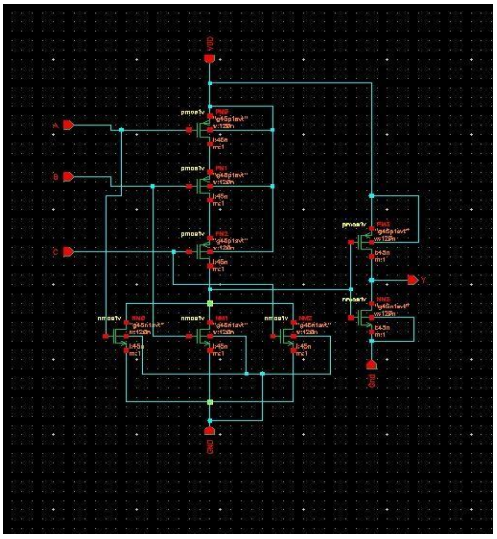
Fig(i): NAND Gate

9. OR GATE:
   An OR gate is a basic digital logic gate that implements logical addition. It outputs a high (1) signal if at least one of its inputs is high (1). The output is only low (0) when all of its inputs are low (0).

$$Y=A+B$$

INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	1

Truth Table



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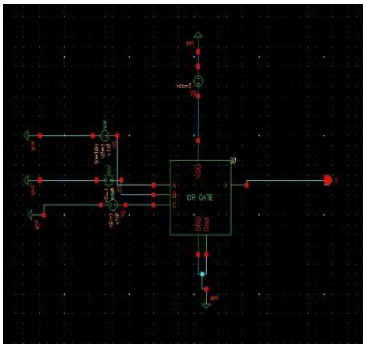
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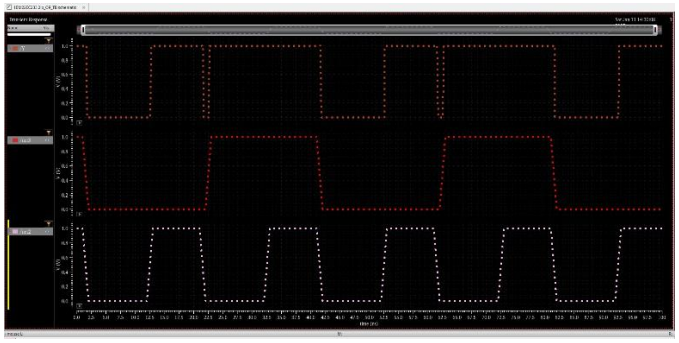

Output Waveform

Fig(j): OR Gate

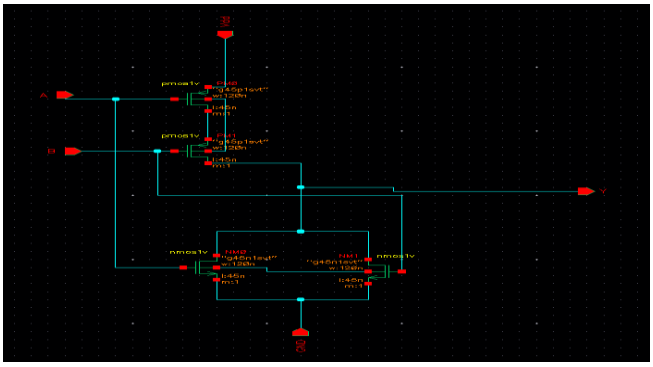
10. NOR GATE:

A NOR gate (NOT-OR gate) is a digital logic gate that implements the negation of the OR operation. It produces an output of high (1) only when all of its inputs are low (0). If any of the inputs are high (1), the output will be low (0). Essentially, a NOR gate is the complement of an OR gate.

$$Y=\sim (A+B)$$

INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

Truth Table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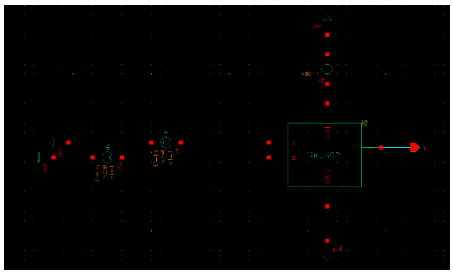
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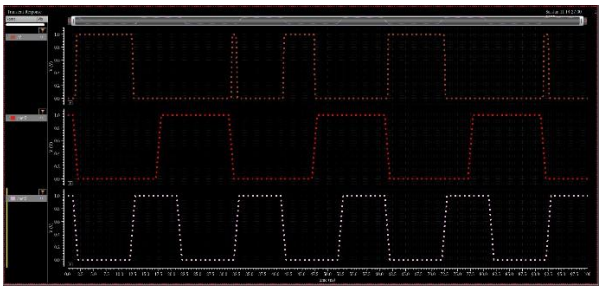

Output Waveform

Fig(k): NOR Gate

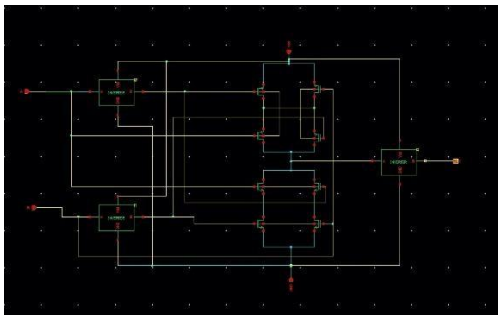
11. XOR GATE:

An XOR gate (Exclusive OR gate) is a digital logic gate that outputs high (1) only when the number of high (1) inputs is odd. For a two-input XOR gate, it produces an output of **1** if and only if exactly one of the inputs is **1**. If both inputs are the same (either both **0** or both **1**), the output will be **0**. The XOR gate is used for performing logical exclusive OR operations, which is crucial in applications like error detection, arithmetic operations, and cryptography.

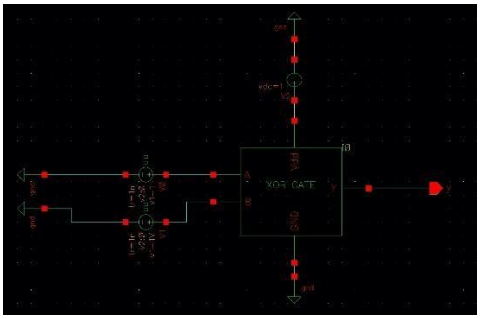
$$Y=A \oplus B$$

INPUT		OUTPUT
A	B	
0	0	0
1	0	1
0	1	1
1	1	0

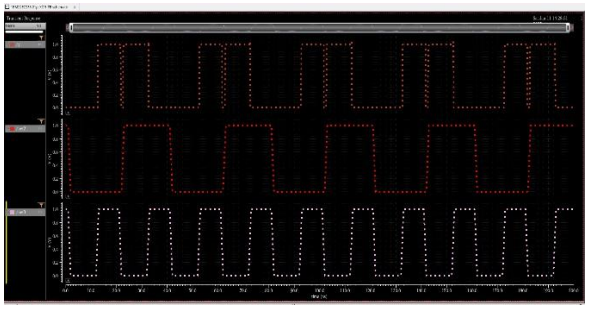
Truth Table



Circuit



Symbol



Output Waveform

Fig(l): XOR Gate

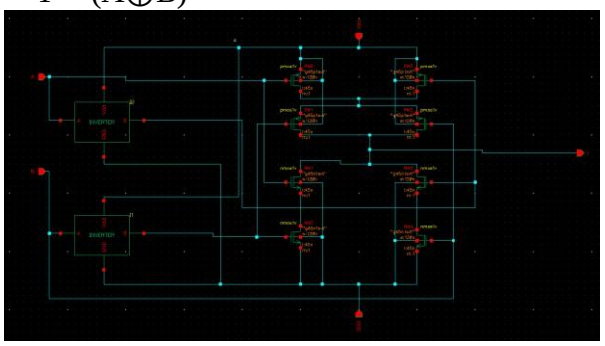
12. XNOR GATE:

An XNOR gate (Exclusive NOR gate) is a digital logic gate that is the complement (inverse) of the XOR gate. It produces an output of high (1) when the number of high (1) inputs is even. In other words, the output is **1** when both inputs are the same (either both **0** or both **1**), and it outputs **0** when the inputs are different. The XNOR gate is often referred to as an equality gate because it outputs **1** when the inputs are equal.

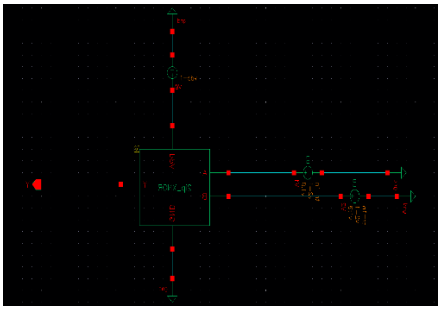
$$Y=\sim(A \oplus B)$$

INPUT		OUTPUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	1

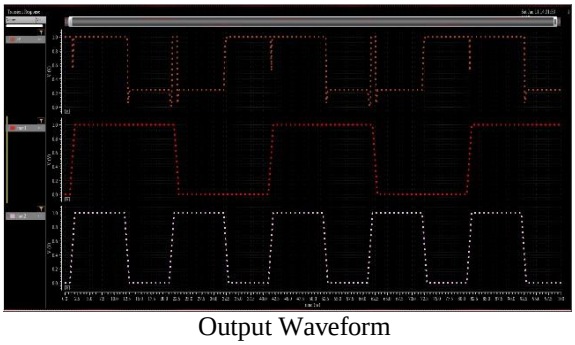
Truth Table



Circuit



Symbol

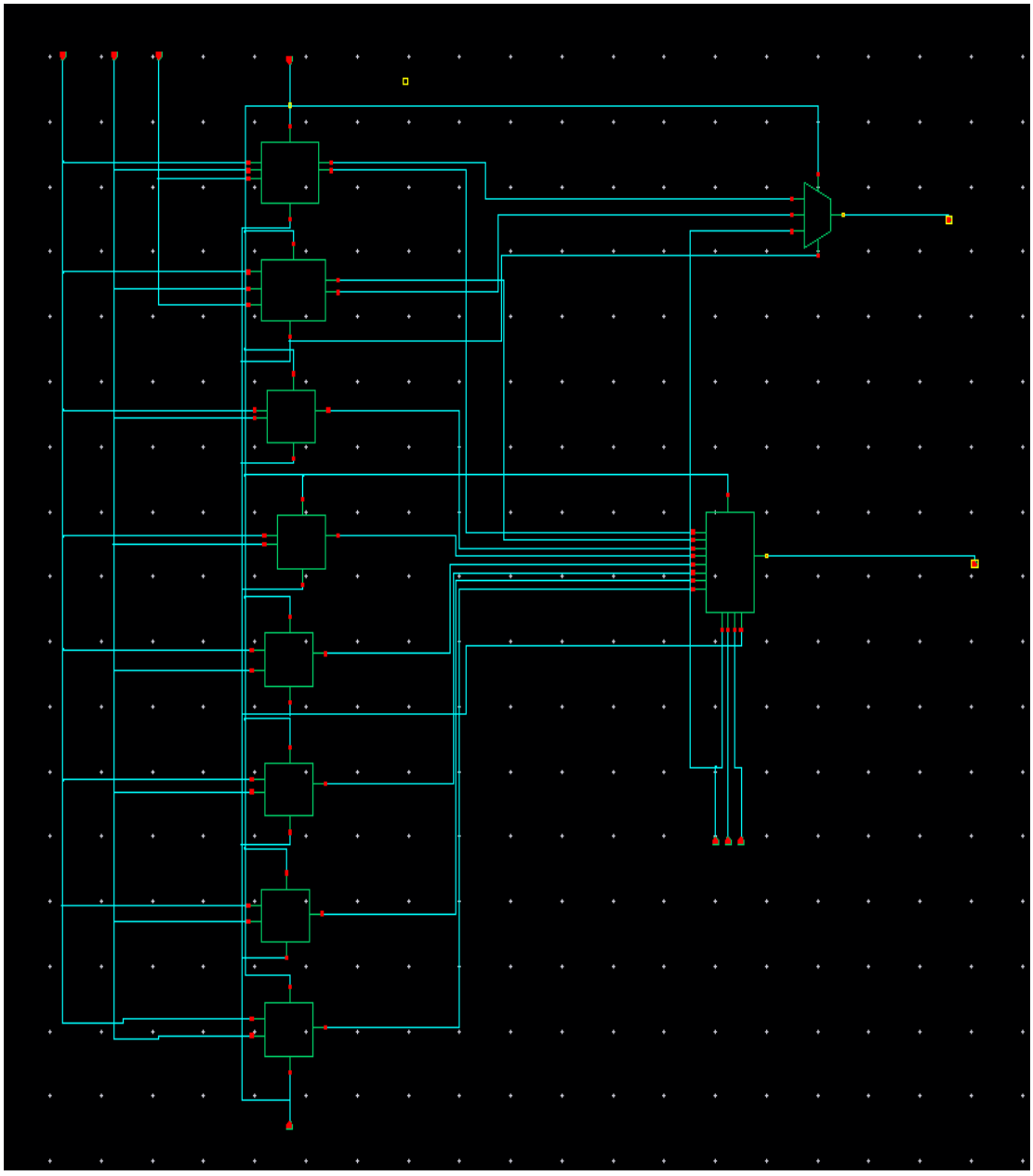


Output Waveform

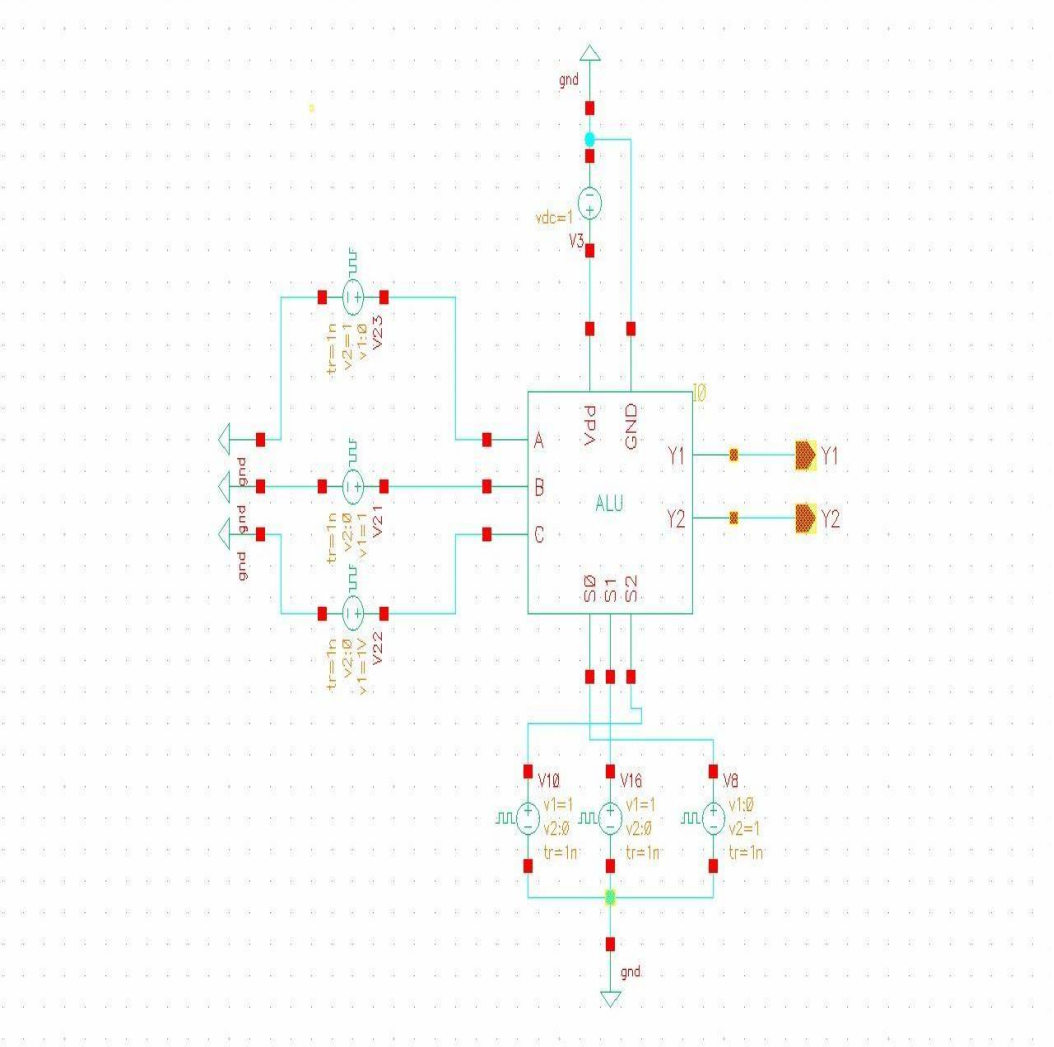
Fig(m): XNOR Gate

13. ARITHMETIC LOGIC UNIT (ALU):

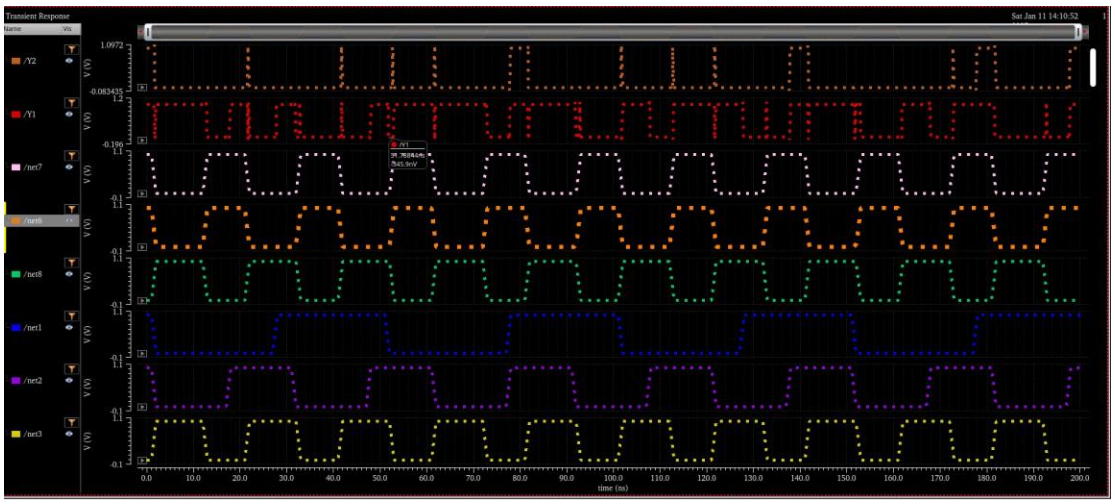
An Arithmetic Logic Unit (ALU) is a fundamental component of a computer's central processing unit (CPU) responsible for performing arithmetic and logic operations. The ALU performs operations such as addition, subtraction, multiplication, division, and logical operations (AND, OR, XOR, NOT). It is the core unit that handles the actual computation or decision-making required in a computing process. The ALU operates on binary numbers and is essential in executing instructions within a CPU, enabling the computer to perform tasks from simple calculations to more complex decision-making processes. Depending on the design, an ALU can support a variety of operations, which are determined by the instruction set architecture (ISA) of the processor.



Circuit



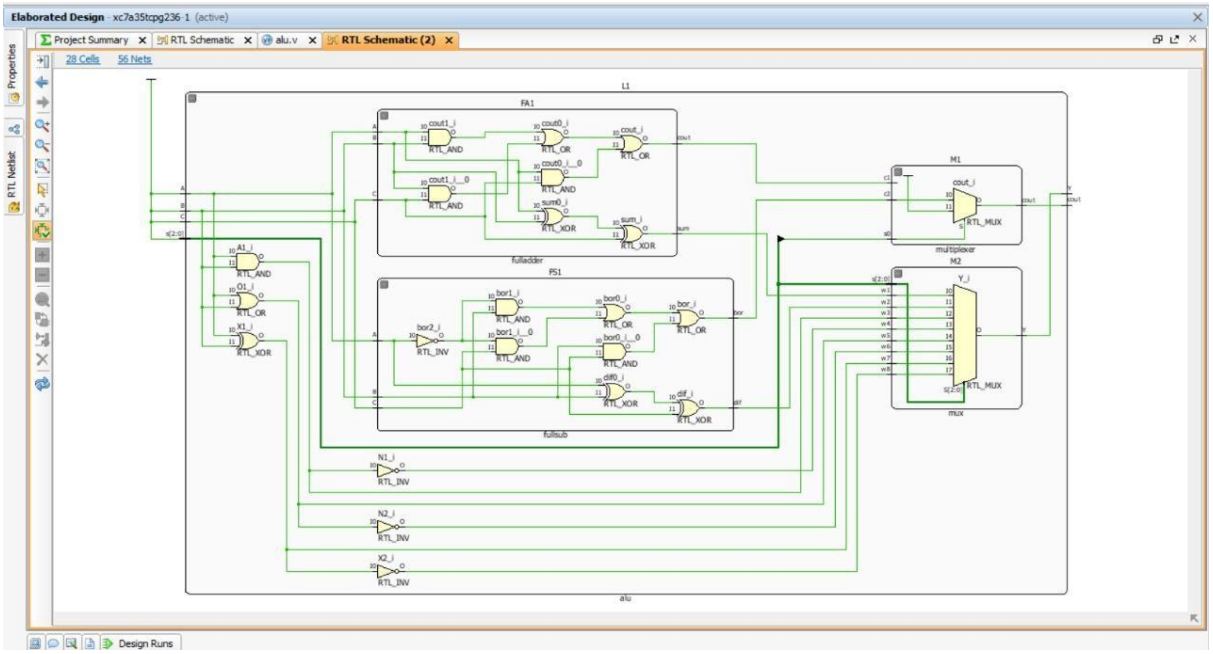
Symbol



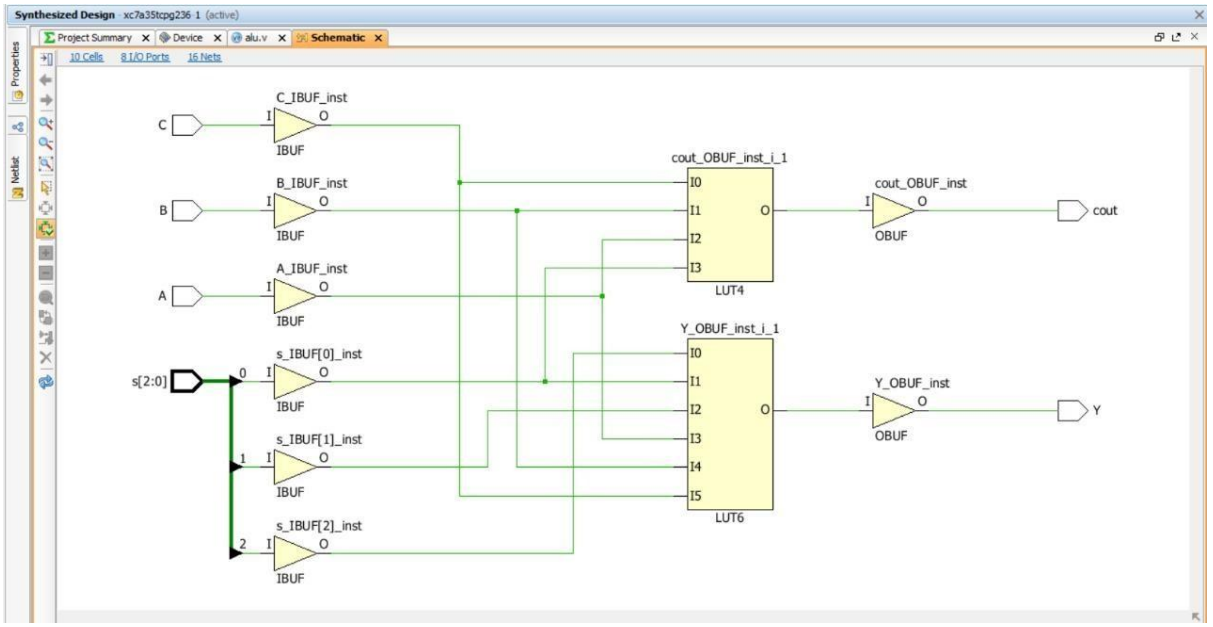
Output Waveform

Fig(n): ALU

4.1.2 Structure:



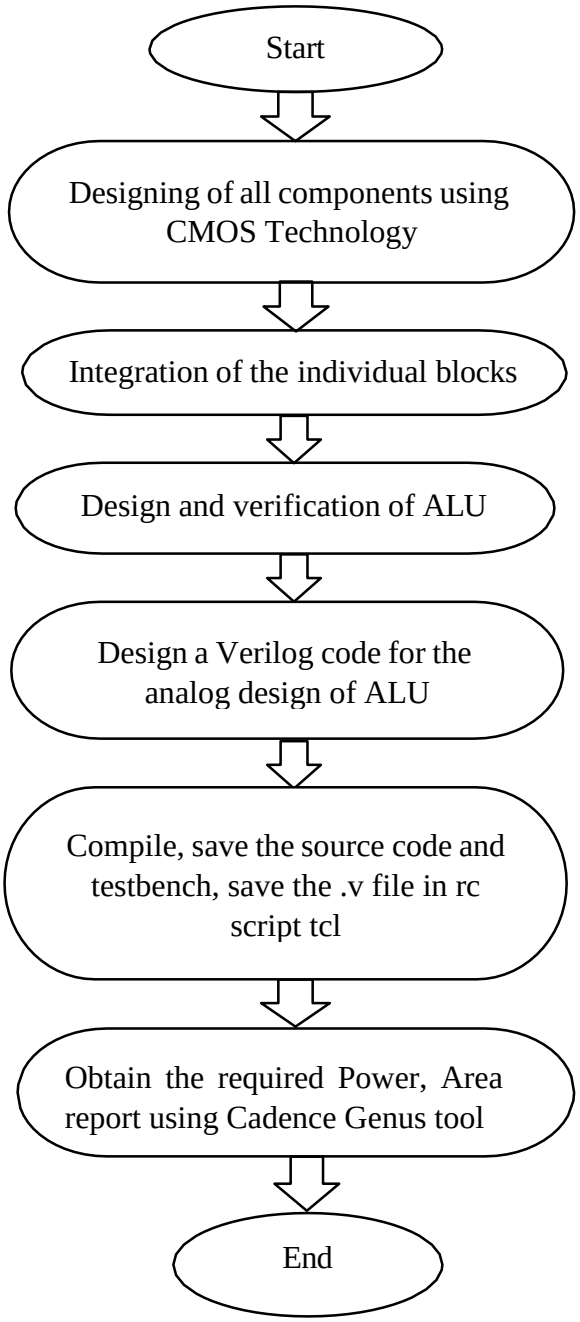
Fig(o): RTL Synthesis Diagram



Fig(p): Synthesis Diagram

This is the obtained RTL diagram and Synthesis diagram of our designed ALU.

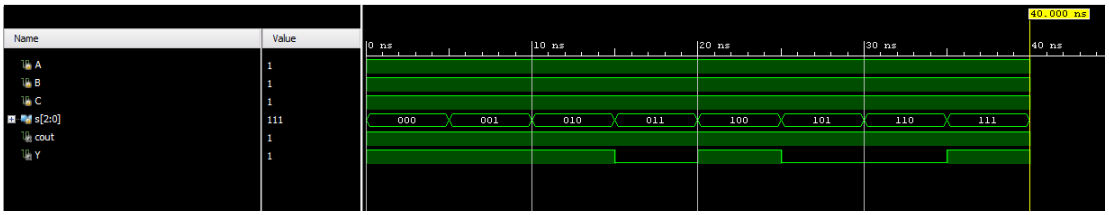
4.1.3 Flow Chart:



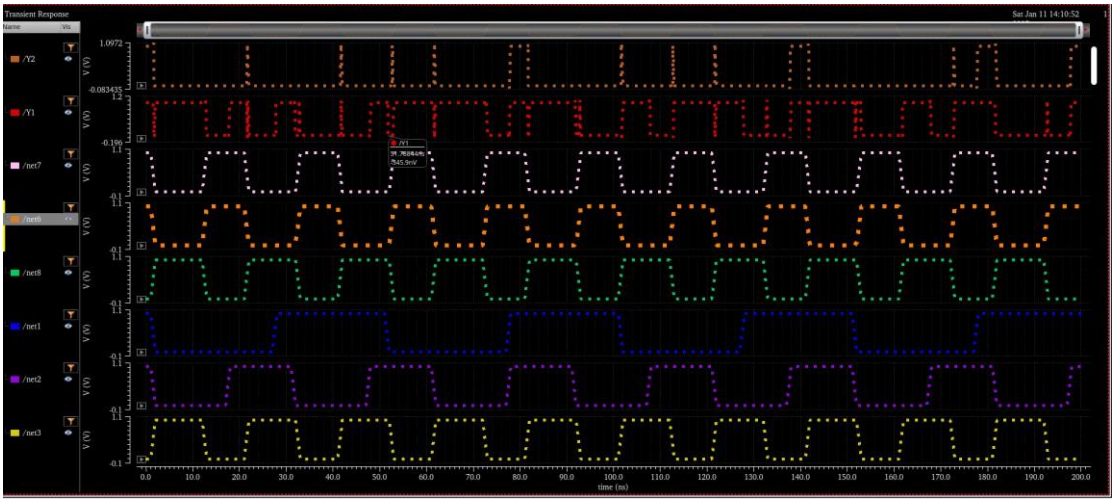
CHAPTER 5:

Results & Discussion:

A low-power and area-efficient 1-bit 8-functional ALU has been designed, capable of performing two arithmetic functions (Addition and Subtraction) and six logical functions (AND, NAND, OR, NOR, XOR, XNOR). The design was implemented using Cadence Virtuoso software (45nm CMOS technology) with the GDI technique to create the basic gates. These gates were then combined to build the Full Adder and Full Subtractor modules. Additionally, 8x1 and 4x1 multiplexers were designed using 2x1 multiplexers. Power, area, and timing analysis were performed using the Cadence Genus digital tool. A suitable code was written to convert the analogy design to a digital format, which was then verified and analysed, with the results presented below.



Fig(q): Output Waveform



Fig(r): Simulation Output

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.20793e-09	5.23610e-07	2.76445e-07	8.02263e-07	100.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.20793e-09	5.23610e-07	2.76445e-07	8.02263e-07	100.00%
Percentage	0.28%	65.27%	34.46%	100.00%	100.00%

Fig(s): Power Report

```
legacy_genus:/> report area
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jan 11 2025  01:22:54 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

Instance    Module    Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------------
alu                       20     36.594     0.000       36.594 <none> (D)
  FA1    fulladder         1      5.130     0.000        5.130 <none> (D)
  FS1    fullsub           3      6.498     0.000        6.498 <none> (D)
  M1     multiplexer       1      2.394     0.000        2.394 <none> (D)
  M2     mux              12     18.468     0.000       18.468 <none> (D)
  (D) = wireload is default in technology library
```

Fig(t): Area Report

```
legacy_genus:/> report timing
====================================================================
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  Generated on:           Jan 11 2025  01:23:05 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================

  Pin          Type       Fanout Load Slew Delay Arrival
                             (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------
A              in port          4  2.0    0    +0       0 R
FA1/A
  g63/A                                        +0       0
  g63/S        ADDFX1           1  0.2    8   +61      61 F
FA1/sum
M2/w1
  g170/B                                       +0      61
  g170/Y       OR2X1            1  0.3    6   +26      88 F
  g164/B1                                      +0      88
  g164/Y       OAI222XL         1  0.5   49   +23     111 R
  g163/B1                                      +0     111
  g163/Y       OAI221X1         1  0.0   28   +38     148 F
M2/Y
Y              interconnect                   28    +0     148 F
               out port                             +0     148 F
-------------------------------------------------------------
Timing slack :  UNCONSTRAINED
Start-point  : A
End-point    : Y
```

Fig(u): Timing Report

```
legacy_genus:/> report gates
===============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Jan 11 2025  01:23:13 pm
  Module:                 alu
  Technology library:     fast_vdd1v0 1.0
  Operating conditions:   PVT_1P1V_0C (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
===============================================================


  Gate    Instances   Area      Library
-----------------------------------------
ADDFX1            2  10.260    fast_vdd1v0
AND2X1            3   4.104    fast_vdd1v0
AOI32X1           1   2.394    fast_vdd1v0
INVX1             2   1.368    fast_vdd1v0
INVXL             3   2.052    fast_vdd1v0
MX2XL             1   2.394    fast_vdd1v0
NOR2BX1           1   1.368    fast_vdd1v0
NOR2XL            1   1.026    fast_vdd1v0
OAI211X1          1   1.710    fast_vdd1v0
OAI221X1          1   2.394    fast_vdd1v0
OAI222XL          1   2.736    fast_vdd1v0
OAI22XL           1   2.052    fast_vdd1v0
OR2X1             2   2.736    fast_vdd1v0
-----------------------------------------
total            20  36.594


     Type      Instances  Area  Area %
----------------------------------------
inverter               5  3.420    9.3
logic                 15 33.174   90.7
physical_cells         0  0.000    0.0
----------------------------------------
total                 20 36.594  100.0
```

Fig(v): Gate Report

CHAPTER 6:

Future Trends and Conclusion:

1.1 Conclusion:

The conclusion of this project demonstrates the successful design of a **Low Power and Area Efficient Arithmetic Logic Unit (ALU)** utilizing **Full Adders**. Through the application of advanced techniques such as **CMOS technology** and the **GDI (Gate Diffusion Input) technique**, we were able to significantly reduce both power consumption and physical area while maintaining the required functionality. The ALU was designed to perform multiple arithmetic and logical operations, including addition, subtraction, and logical functions such as AND, OR, XOR, and their respective inverses.By optimizing the design of the **Full Adders**, we achieved improved power efficiency, directly contributing to the overall low-power characteristics of the ALU. Additionally, the area-efficient design was ensured by utilizing compact and effective circuit configurations, which minimized the chip footprint without compromising on performance.The use of **Cadence Virtuoso** for the analog design and **Cadence Genus** for the digital tool integration enabled thorough analysis of power, area, and timing parameters, which confirmed the efficacy of the design in achieving both low power and reduced area metrics. Furthermore, the transition from analog to digital was successfully implemented, ensuring functional correctness and verification of the design.
In summary, this project highlights the practical application of efficient design methodologies to achieve an optimized, low-power, and area-efficient ALU, suitable for integration into energy-conscious electronic systems and devices.
We have reduced the amount of power consumption from 37.533Nw to 8.02263e-07 nW.

	Low Power And Area Efficient ALU Using Full Adders (PROJECT RESULTS)	Low Power and Area Efficiency ALU With Different Type of Low Power in Full Adders (REFERENCE PAPER RESULTS)
Power	**8.02263e-07nW**	**37.533nw**
Area	**36.594µm^2**	**30% reduced**
Timing	**148ps**	**-**
Gates	**20 Gates**	**-**

Tb (a): ALU Parameters Comparison

1.2 Future Trends:

In future work, the ALU can be further optimized using alternative techniques such as **pass transistors** and other advanced circuit design methods to further reduce power consumption and area. These approaches hold the potential for improving efficiency, particularly in minimizing the overhead associated with conventional transistor designs. Additionally, hardware implementation of the ALU is possible; however, it presents significant challenges due to the complexity and precision required in physical design and fabrication. Despite

these difficulties, such efforts could lead to even more optimized, real-world implementations of ALUs for various applications in low-power and high-performance systems.

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