
STM32
CubeMX

1. Description

1.1. Project

Project Name	2024_03_08-Manual-robot-code_FREERTOS3
Board Name	NUCLEO-F746ZG
Generated with:	STM32CubeMX 6.12.0
Date	07/15/2024

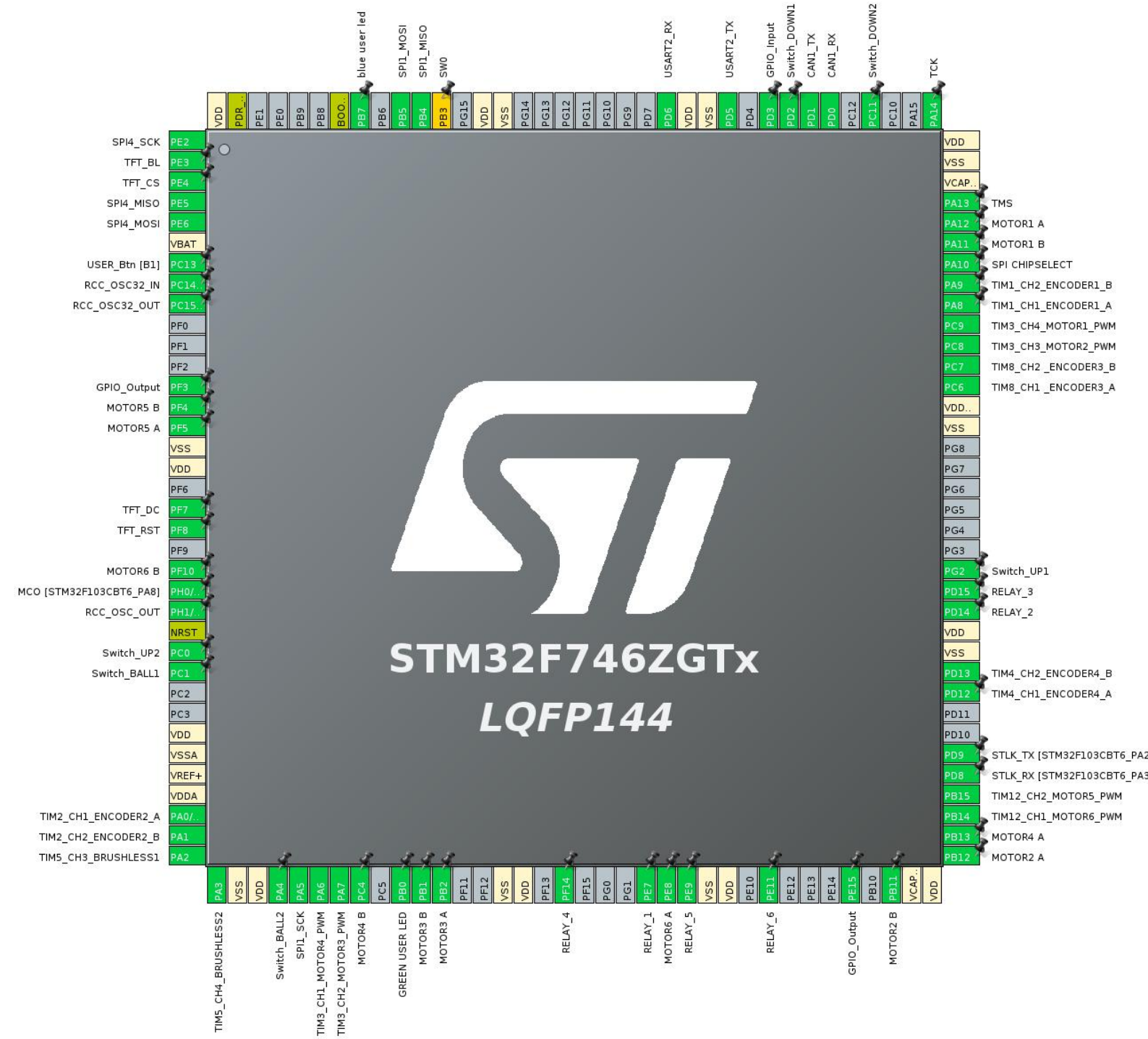
1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746ZGTx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
2	PE3 *	I/O	GPIO_Output	TFT_BL
3	PE4 *	I/O	GPIO_Output	TFT_CS
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	USER_Btn [B1]
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
13	PF3 *	I/O	GPIO_Output	
14	PF4 *	I/O	GPIO_Output	MOTOR5 B
15	PF5 *	I/O	GPIO_Output	MOTOR5 A
16	VSS	Power		
17	VDD	Power		
19	PF7 *	I/O	GPIO_Output	TFT_DC
20	PF8 *	I/O	GPIO_Output	TFT_RST
22	PF10 *	I/O	GPIO_Output	MOTOR6 B
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Input	Switch_UP2
27	PC1 *	I/O	GPIO_Input	Switch_BALL1
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM2_CH1	TIM2_CH1_ENCODER2_A
35	PA1	I/O	TIM2_CH2	TIM2_CH2_ENCODER2_B
36	PA2	I/O	TIM5_CH3	TIM5_CH3_BRUSHLESS1
37	PA3	I/O	TIM5_CH4	TIM5_CH4_BRUSHLESS2
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Input	Switch_BALL2
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	TIM3_CH1	TIM3_CH1_MOTOR4_PWM

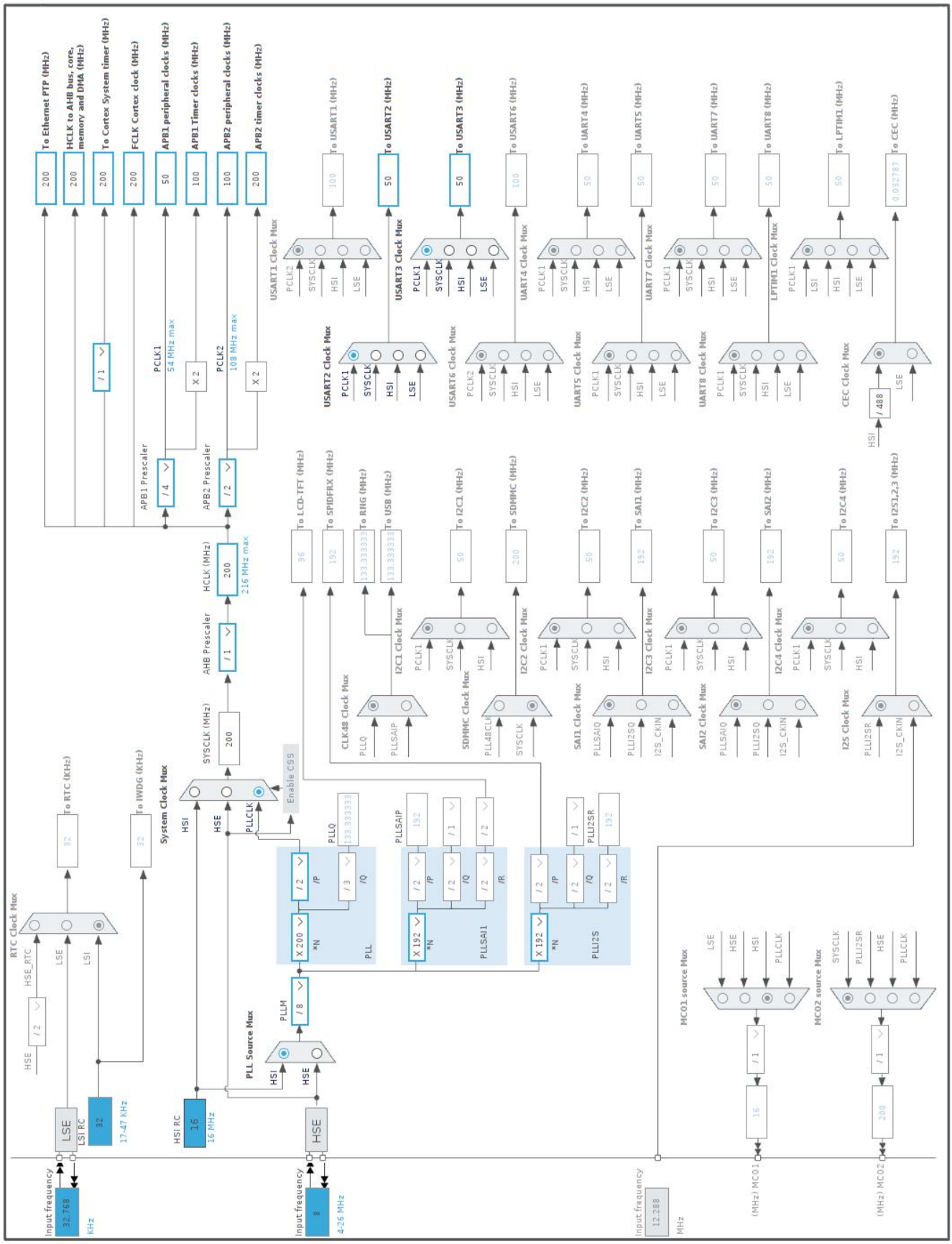
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PA7	I/O	TIM3_CH2	TIM3_CH2_MOTOR3_PWM
44	PC4 *	I/O	GPIO_Output	MOTOR4 B
46	PB0 *	I/O	GPIO_Output	GREEN USER LED
47	PB1 *	I/O	GPIO_Output	MOTOR3 B
48	PB2 *	I/O	GPIO_Output	MOTOR3 A
51	VSS	Power		
52	VDD	Power		
54	PF14 *	I/O	GPIO_Output	RELAY_4
58	PE7 *	I/O	GPIO_Output	RELAY_1
59	PE8 *	I/O	GPIO_Output	MOTOR6 A
60	PE9 *	I/O	GPIO_Output	RELAY_5
61	VSS	Power		
62	VDD	Power		
64	PE11 *	I/O	GPIO_Output	RELAY_6
68	PE15 *	I/O	GPIO_Output	
70	PB11 *	I/O	GPIO_Output	MOTOR2 B
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	MOTOR2 A
74	PB13 *	I/O	GPIO_Output	MOTOR4 A
75	PB14	I/O	TIM12_CH1	TIM12_CH1_MOTOR6_PWM
76	PB15	I/O	TIM12_CH2	TIM12_CH2_MOTOR5_PWM
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
81	PD12	I/O	TIM4_CH1	TIM4_CH1_ENCODER4_A
82	PD13	I/O	TIM4_CH2	TIM4_CH2_ENCODER4_B
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Output	RELAY_2
86	PD15 *	I/O	GPIO_Output	RELAY_3
87	PG2 *	I/O	GPIO_Input	Switch_UP1
94	VSS	Power		
95	VDDUSB	Power		
96	PC6	I/O	TIM8_CH1	TIM8_CH1 _ENCODER3_A
97	PC7	I/O	TIM8_CH2	TIM8_CH2 _ENCODER3_B
98	PC8	I/O	TIM3_CH3	TIM3_CH3_MOTOR2_PWM

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
99	PC9	I/O	TIM3_CH4	TIM3_CH4_MOTOR1_PWM
100	PA8	I/O	TIM1_CH1	TIM1_CH1_ENCODER1_A
101	PA9	I/O	TIM1_CH2	TIM1_CH2_ENCODER1_B
102	PA10 *	I/O	GPIO_Output	SPI CHIPSELECT
103	PA11 *	I/O	GPIO_Output	MOTOR1 B
104	PA12 *	I/O	GPIO_Output	MOTOR1 A
105	PA13	I/O	SYS_JTMS-SWDIO	TMS
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	TCK
112	PC11 *	I/O	GPIO_Input	Switch_DOWN2
114	PD0	I/O	CAN1_RX	
115	PD1	I/O	CAN1_TX	
116	PD2 *	I/O	GPIO_Input	Switch_DOWN1
117	PD3 *	I/O	GPIO_Input	
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	USART2_RX	
130	VSS	Power		
131	VDD	Power		
133	PB3 **	I/O	SYS_JTDO-SWO	SW0
134	PB4	I/O	SPI1_MISO	
135	PB5	I/O	SPI1_MOSI	
137	PB7 *	I/O	GPIO_Output	blue user led
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746ZGTx
Datasheet	DS10916_Rev4

1.2. Parameter Selection

Temperature	25
Vdd	3.3

1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

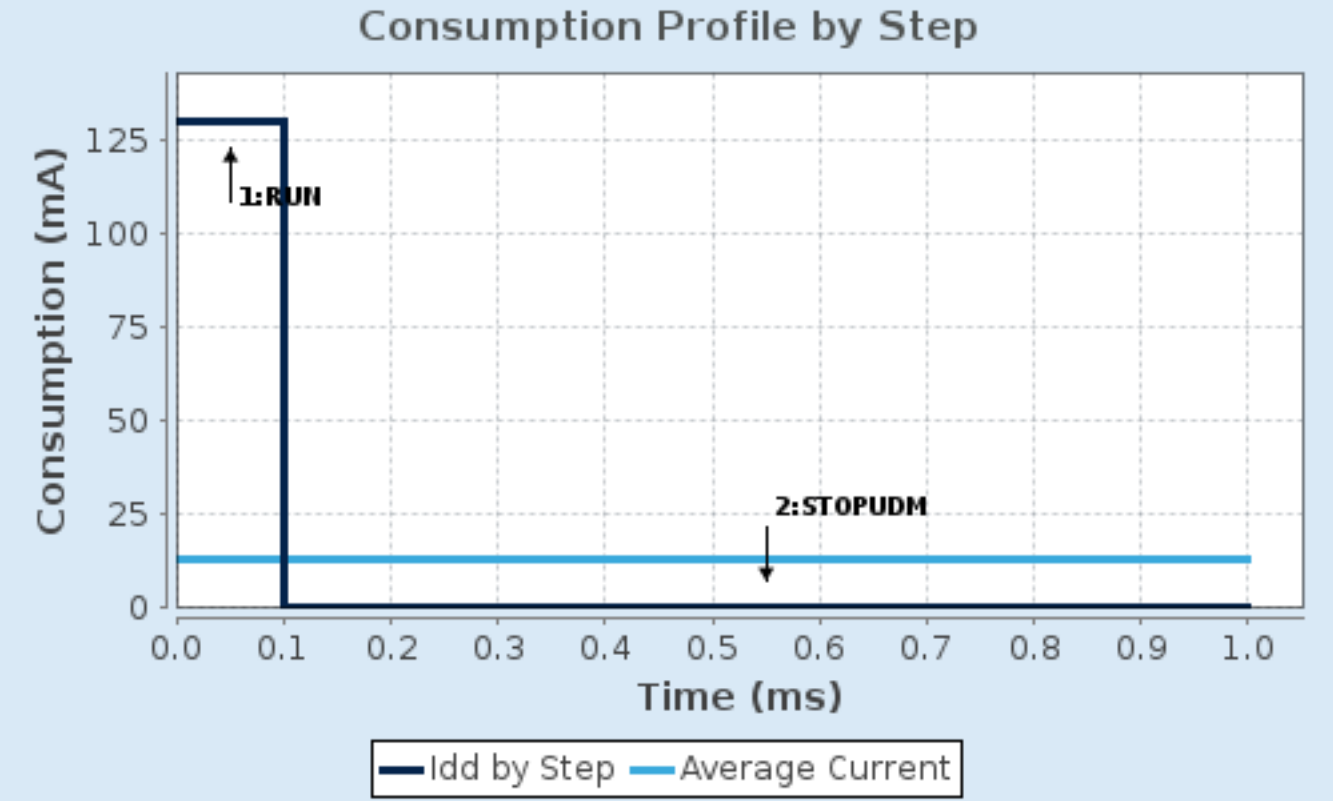
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ITCM/FLASH/REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	130 mA	100 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	87.84	104.99
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	13.09 mA
Battery Life	1 day, 23 hours	Average DMIPS	462.24005 DMIPS

1.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

2. Software Project

2.1. Project Settings

Name	Value
Project Name	2024_03_08-Manual-robot-code_FREERTOS3
Project Folder	/home/tutu/STM32CubeIDE/workspace_1.14.0/2024_03_08-Manual-robot-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F7 V1.17.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_TIM1_Init	TIM1
5	MX_TIM2_Init	TIM2
6	MX_TIM4_Init	TIM4
7	MX_TIM5_Init	TIM5
8	MX_TIM8_Init	TIM8
9	MX_TIM12_Init	TIM12
10	MX_USART3_UART_Init	USART3
11	MX_SPI1_Init	SPI1

Rank	Function Name	Peripheral Instance Name
12	MX_TIM3_Init	TIM3
13	MX_SPI4_Init	SPI4
14	MX_TIM10_Init	TIM10
15	MX_USART2_UART_Init	USART2
16	MX_CAN1_Init	CAN1

3. Peripherals and Middlewares Configuration

3.1. CAN1

mode: Activated

3.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**5 ***
Time Quantum	**100.0 ***
Time Quanta in Bit Segment 1	**6 Times ***
Time Quanta in Bit Segment 2	**3 Times ***
Time for one Bit	1000
Baud Rate	**1000000 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	**Enable ***
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

3.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

3.3. SPI1

Mode: Full-Duplex Master

3.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	**LSB First ***

Clock Parameters:

Prescaler (for Baud Rate)	**256 ***
Baud Rate	**390.625 KBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

3.4. SPI4

Mode: Full-Duplex Master

3.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**25.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled

NSS Signal Type	Software

3.5. SYS

Debug: Serial Wire

Timebase Source: TIM9

3.6. TIM1

Combined Channels: Encoder Mode

3.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.7. TIM2

Combined Channels: Encoder Mode

3.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.8. TIM3

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

3.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**427 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.9. TIM4

Combined Channels: Encoder Mode

3.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.10. TIM5

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

3.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**21600-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**100-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	**Low ***

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable

CH Polarity	**Low ***

3.11. TIM8

Combined Channels: Encoder Mode

3.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

3.12. TIM10

mode: Activated

3.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

3.13. TIM12

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1686 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**127 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.14. USART2

Mode: Asynchronous

3.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**460800 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.15. USART3

Mode: Asynchronous

3.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	**460800 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

3.16. FREERTOS

Interface: CMSIS_V1

3.16.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**256 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**20000 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

3.16.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled
uxTaskGetStackHighWaterMark2	Disabled

3.16.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

*** User modified value**

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE6	SPI4_MOSI	Alternate Function Push Pull	**Pull-up ***	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	TCK
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_CH1_ENCODER1_A
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_CH2_ENCODER1_B
TIM2	PA0/WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH1_ENCODER2_A
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH2_ENCODER2_B
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH1_MOTOR4_PW

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						M
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH2_MOTOR3_PWM
	PC8	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH3_MOTOR2_PWM
	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH4_MOTOR1_PWM
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM4_CH1_ENCODER4_A
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM4_CH2_ENCODER4_B
TIM5	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM5_CH3_BRUSHLESS1
	PA3	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM5_CH4_BRUSHLESS2
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM8_CH1_ENCODER3_A
	PC7	TIM8_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM8_CH2_ENCODER3_B
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM12_CH1_MOTOR6_PWM
	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM12_CH2_MOTOR5_PWM
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	**Pull-up ***	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
Single Mapped Signals	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SW0
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TFT_BL
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TFT_CS
	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	USER_Btn [B1]
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR5 B
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR5 A
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TFT_DC
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TFT_RST
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR6 B

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_UP2
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_BALL1
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_BALL2
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR4 B
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GREEN USER LED
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR3 B
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR3 A
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_4
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_1
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR6 A
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_5
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_6
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2 B
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR2 A
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR4 A
	PD14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_2
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RELAY_3
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_UP1
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI CHIPSELECT
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1 B
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR1 A
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_DOWN2
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Switch_DOWN1
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	blue user led

4.2. DMA configuration

DMA request	Stream	Direction	Priority
USART3_RX	DMA1_Stream1	Peripheral To Memory	**High ***
USART3_TX	DMA1_Stream3	Memory To Peripheral	**High ***
SPI4_RX	DMA2_Stream0	Peripheral To Memory	Low
SPI4_TX	DMA2_Stream1	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI4_TX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
CAN1 RX0 interrupts	true	5	0
TIM1 break interrupt and TIM9 global interrupt	true	15	0
USART2 global interrupt	true	5	0
USART3 global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 TX interrupts	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM14 global interrupt			
TIM8 capture compare interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		

4.3.2. NVIC Code generation

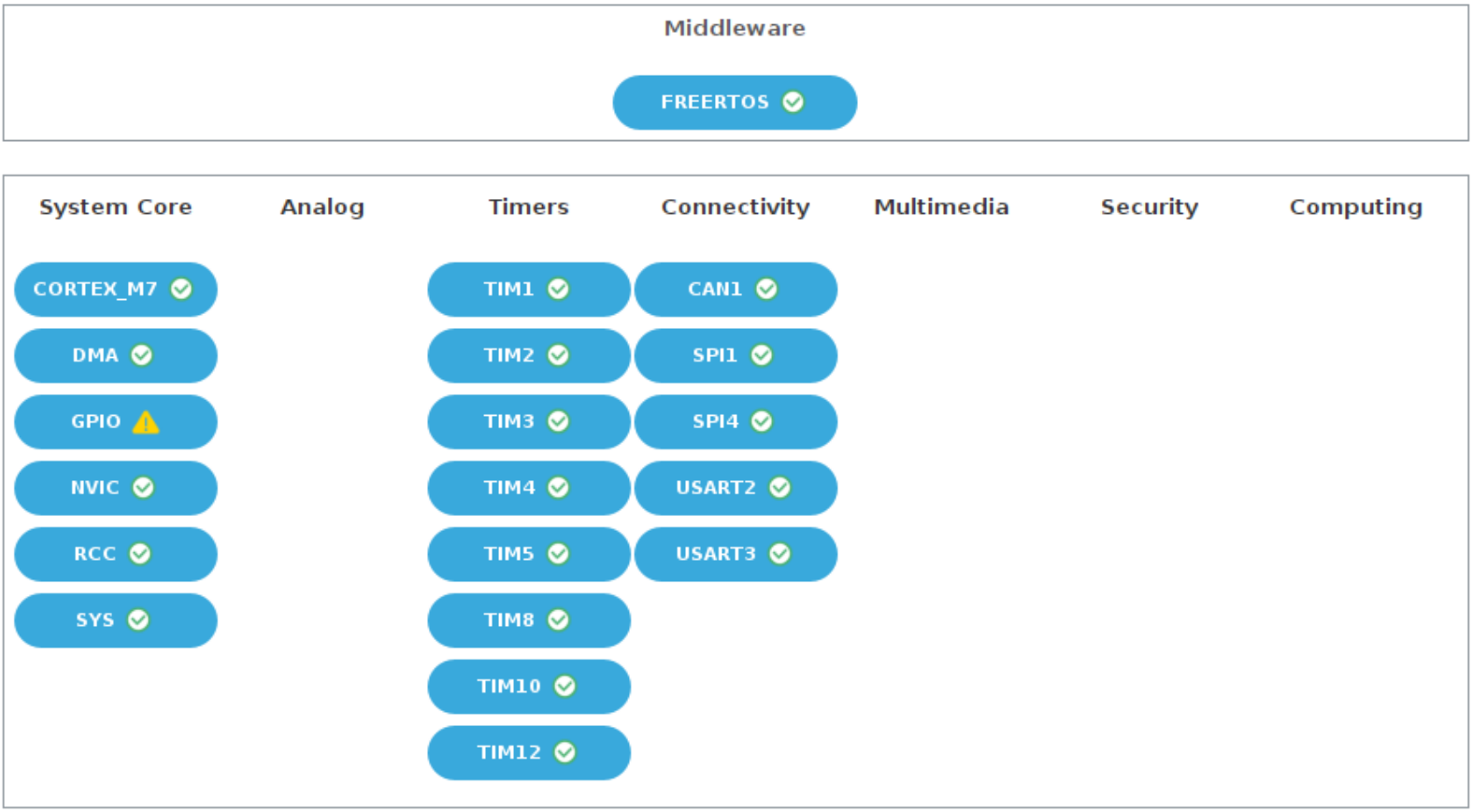
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
DMA1 stream1 global interrupt	false	true	true
DMA1 stream3 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
DMA1 stream6 global interrupt	false	true	true
CAN1 RX0 interrupts	false	true	true
TIM1 break interrupt and TIM9 global interrupt	false	true	true
USART2 global interrupt	false	true	true
USART3 global interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true
DMA2 stream1 global interrupt	false	true	true

*** User modified value**

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type	Link