Experiment Name: STUDY OF CHARACTERISTICS OF BIPOLAR JUNCTION TRANSISTOR (BJT).

Objectives: DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.

Biasing of BJT.

Small signal Analysis using BJT.

Theory:

Transistor has two p-n junctions (see figure below). One junction is called emitter junction and other is called collector junction. When transistor is used as an amplifier, it is operated in active mode. In active mode, emitter junction is forward biased and collector junction is reverse biased.

Emitter current is given by IE = InE + IpE we can also write IE = IC + IB = [(1 + B)/B]IC Where B = IC /IB is called common emitter current gain.

In good transistor IC>>IB i.e. B>>1. IC can also be expressed as IC = (alpha)IE . where B = B/(1+B) B. is called common base current gain. For good transistor,is close to unity.

Procedure:

2.1. Draw the circuit of Fig. 3 (Self Bias Circuit). By choosing Setup analysis, mark Bias Point Detail and Temperature. Set Temperature to 270 C.

2.2. Run the simulation and click on the Enable Bias Voltage Display and Enable Bias Current Display icons.

2.3. Fill up the following table

2.4. Change R1 to around 57K, so that VCE = 0.5 VCC.

2.5. Change temperature to 500 C and note the change in VCE.

2.6. Change transistor model (replace Q2N3904 with Q2N2222) and set temperature back to 270 C. Again, note the change in VCE.

2.7. Now, for circuit in Fig. 3, remove RE and short Emitter to ground (Fixed Bias Circuit). Repeat steps 2 to 6. R1 will needed to be set around 228K to achieve VCE = 0.5 VCC.

2.8. Comment on the stability of the biasing circuits (fixed and self) with change in temperature and device model (current gain, etc.).

Biasing of BJT:

In order to characterize the operation of a particular transistor, a complete set of characteristic equations is needed. Typically, these curves look like those in Figure. These curves show that in the active region of operation, the collector current is constant and depends on the base current.

Circuit Diagram:

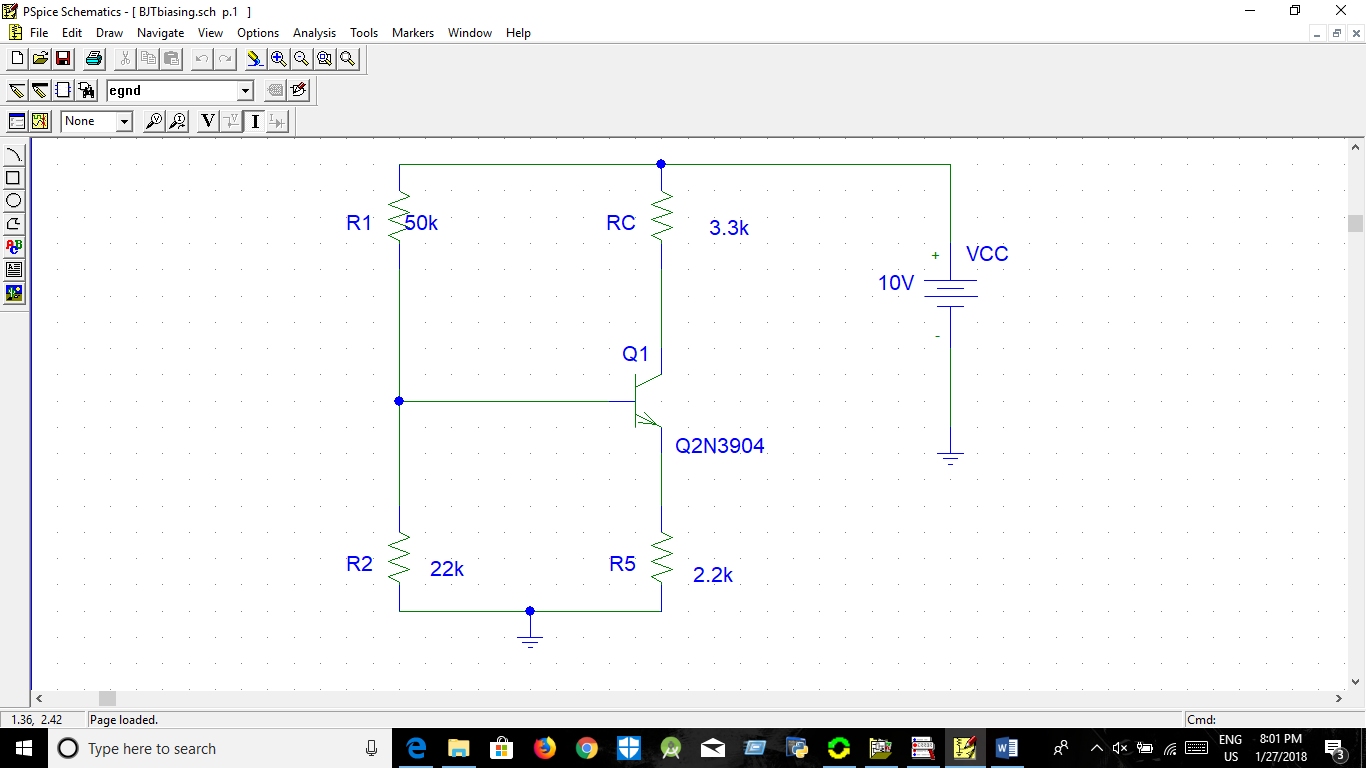


Fig.. Biasing of BJT

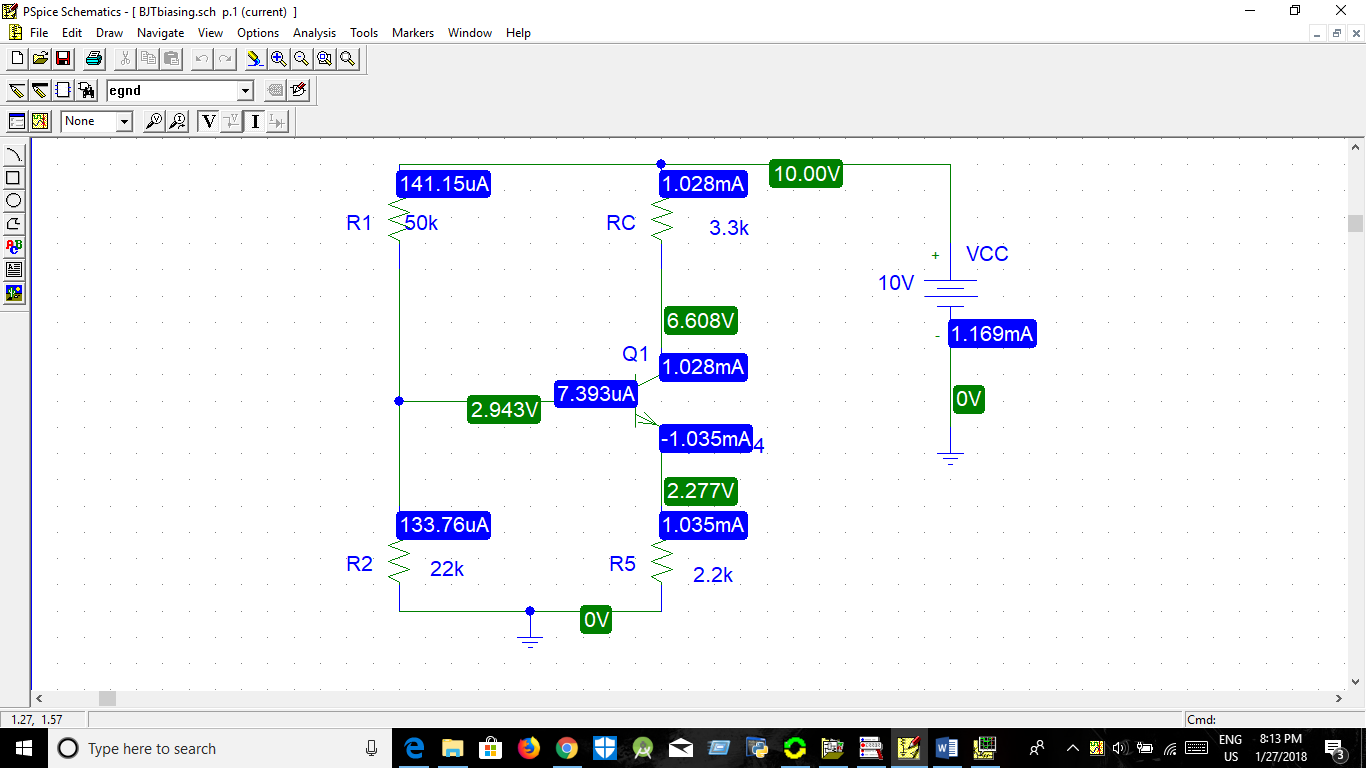


Fig. Biasing of BJT v & I

Graph:

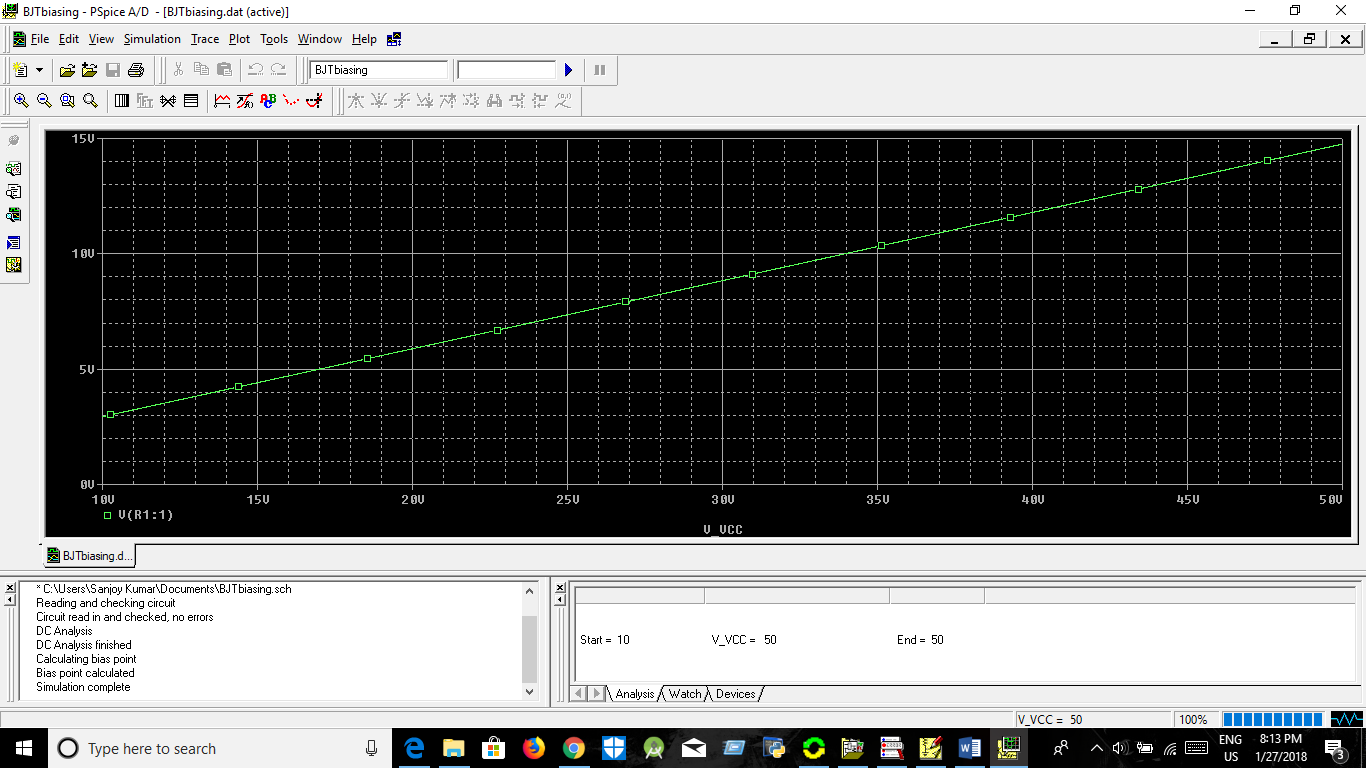


Fig:Graph of Biasing

Discussion:

1.The biasing of BJT is the In order to characterize the operation of a particular transistor

2.From this experiment use Q2N3904 transistor.

3.The graph have been shown in the figure

Submission By

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Dept of EEE.

Experiment Name: Small Signal Analysis of BJT

Objectives: : DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.

Biasing of BJT.

Small signal Analysis using BJT.

Theory:

Transistor has two p-n junctions (see figure below). One junction is called emitter junction and other is called collector junction. When transistor is used as an amplifier, it is operated in active mode. In active mode, emitter junction is forward biased and collector junction is reverse biased.

Emitter current is given by IE = InE + IpE we can also write IE = IC + IB = [(1 + B)/B]IC Where B = IC /IB is called common emitter current gain.

In good transistor IC>>IB i.e. B>>1. IC can also be expressed as IC = (alpha)IE . where B = B/(1+B) B. is called common base current gain. For good transistor,is close to unity.

Procedure:

3.1. Draw the circuit shown in Fig. 4 in PSpice schematics.

3.2. Here, VIN is variable frequency AC source (Having Part Name of VAC). Set its amplitude to 1 mV, keeping other parameters (e.g. Vdc) to zero value.

3.3. Select AC Sweep from Setup Analysis. Select sweep from 10 Hz to 10 MHz (or higher or lower, ensure that you observe both the cut-off frequencies) in Decade mode, with 20 Pts/decade.

3.4. Run the simulation.

3.5. Observe the voltage gain (AV=vo/vin) and phase shift between vo and vi at different frequencies. [For obtaining phase difference click on the Add trace icon, obtain the plotting of P(vo)-P(vin)].

3.6. Normalize the voltage gain AVN=AV/AVmax

3.7. Plot the voltage gain (in dB) vs. frequency (f) [AVdB=20log10(AVN)]

3.8. Determine the -3dB (cut-off) frequencies from the plot. Also note the phase difference between vo and vi at –3dB frequencies.

3.9. [Home work] At mid-band frequency, note the voltage gain (AV), current gain (AI), input resistance (Ri) and output resistance (Ro) of the configuration. For output resistance use the knowledge obtained from thevenin’s equivalence.

Circuit Diagram:

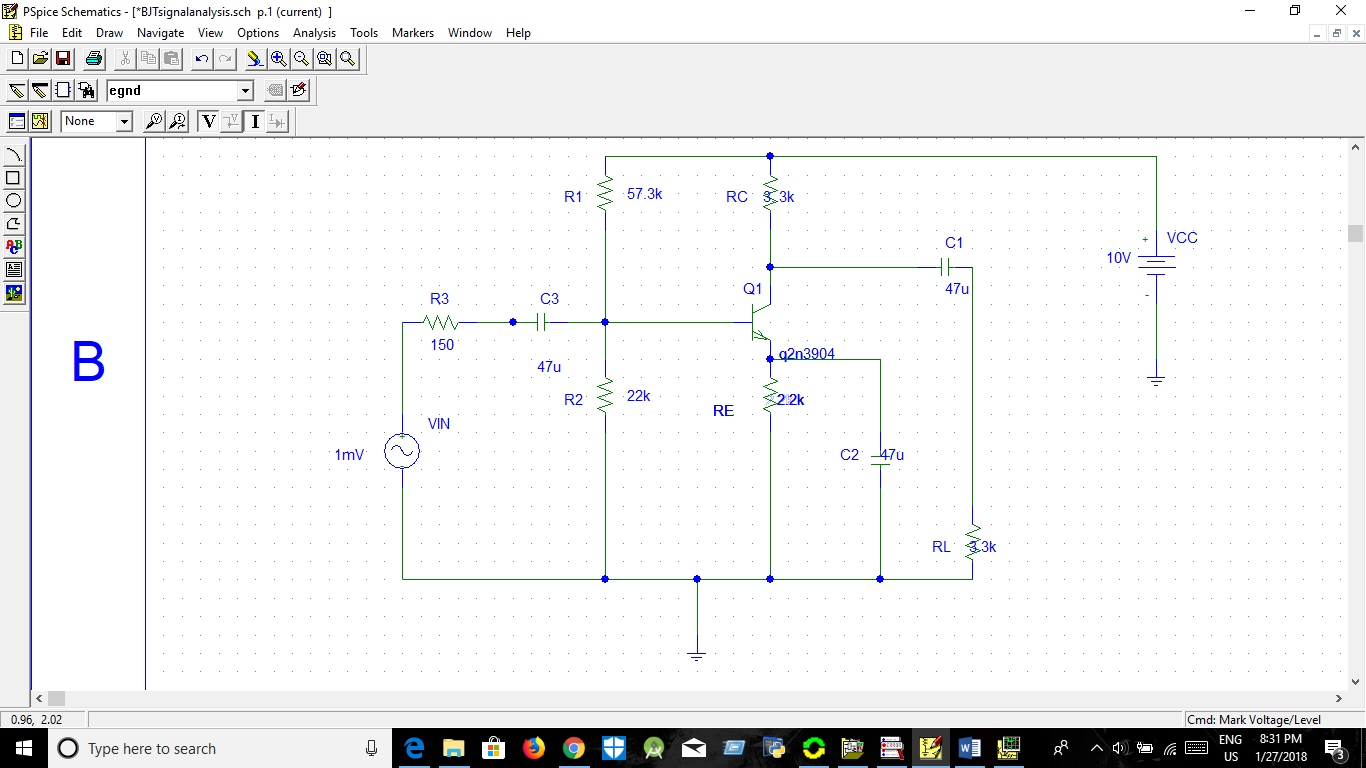


Fig.4. Circuit for Small signal analysis using BJT

Graph:

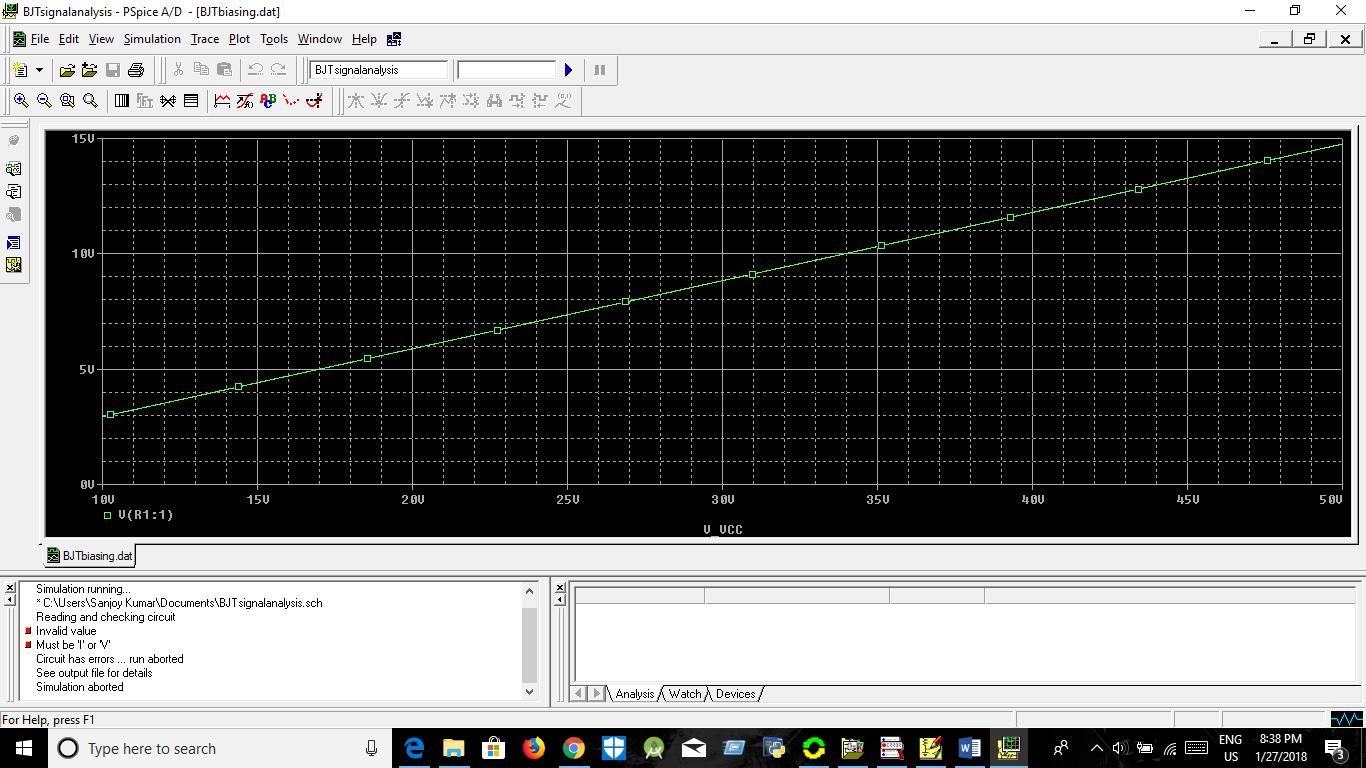


Fig : Graph of Small signal analysis using BJT

Name of the Experiment: STUDY OF CASCADED AND FEEDBACK AMPLIFIER CIRCUITS USING BJT

Objectives:

OBJECTIVE The objective of this experiment is to simulate and observe the characteristics of the following amplifier circuits using BJT’s  A two-stage cascaded amplifier. Feedback Amplifiers .

Voltage-series feedback amplifier.  Voltage-shunt feedback amplifier.

Current-series feedback amplifier.  Current-shunt feedback amplifier

Procedure:

1.1. Draw the circuit shown in Fig. 1 in PSpice schematics.

1.2. Here, Vin is variable frequency AC source (Having Part Name of VAC). Set its amplitude to 1 mV, keeping other parameters (e.g. Vdc) to zero value.

1.3. Select AC Sweep from Setup Analysis. Select sweep from 10 Hz to 1 MHz (or higher or lower, ensuring that you observe both the cut-off frequencies) in Decade mode, with 20 Pts/decade.

Page 5 of 8

1.4. Run the simulation.

1.5. Observe the voltage gain (AV=vo/vi) and phase shift between vo and vi at different frequencies.

1.6. Normalize the voltage gain AVN=AV/AVmax

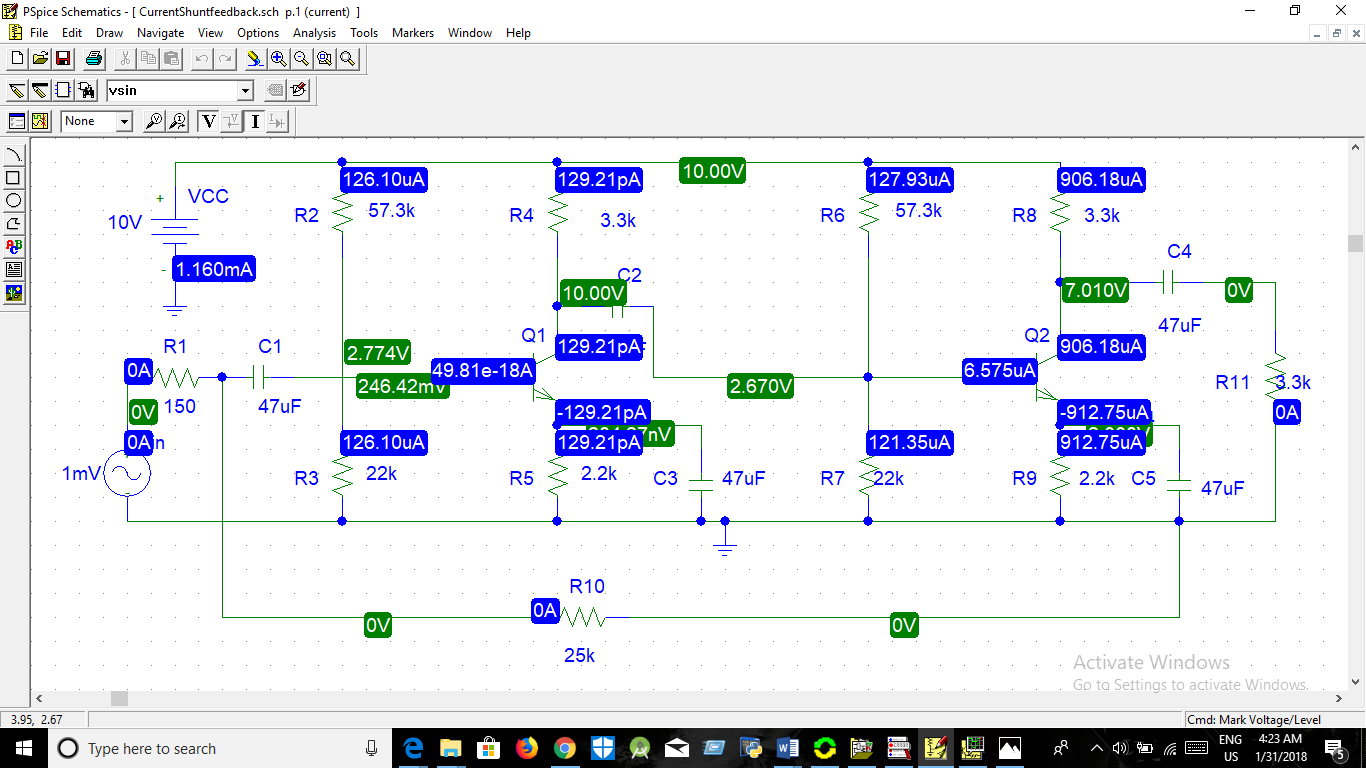
1.7. Plot the voltage gain (in dB) vs. frequency (f) [AVdB=20log10(AVN)]

1.8. Determine the -3dB (cut-off) frequencies from the plot. Also note the phase difference between vo and vi at –3dB frequencies. 1.9. At mid-band frequency, note the voltage gain (AV), current gain (AI), input resistance (Ri) and output resistance (Ro) of the configuration.

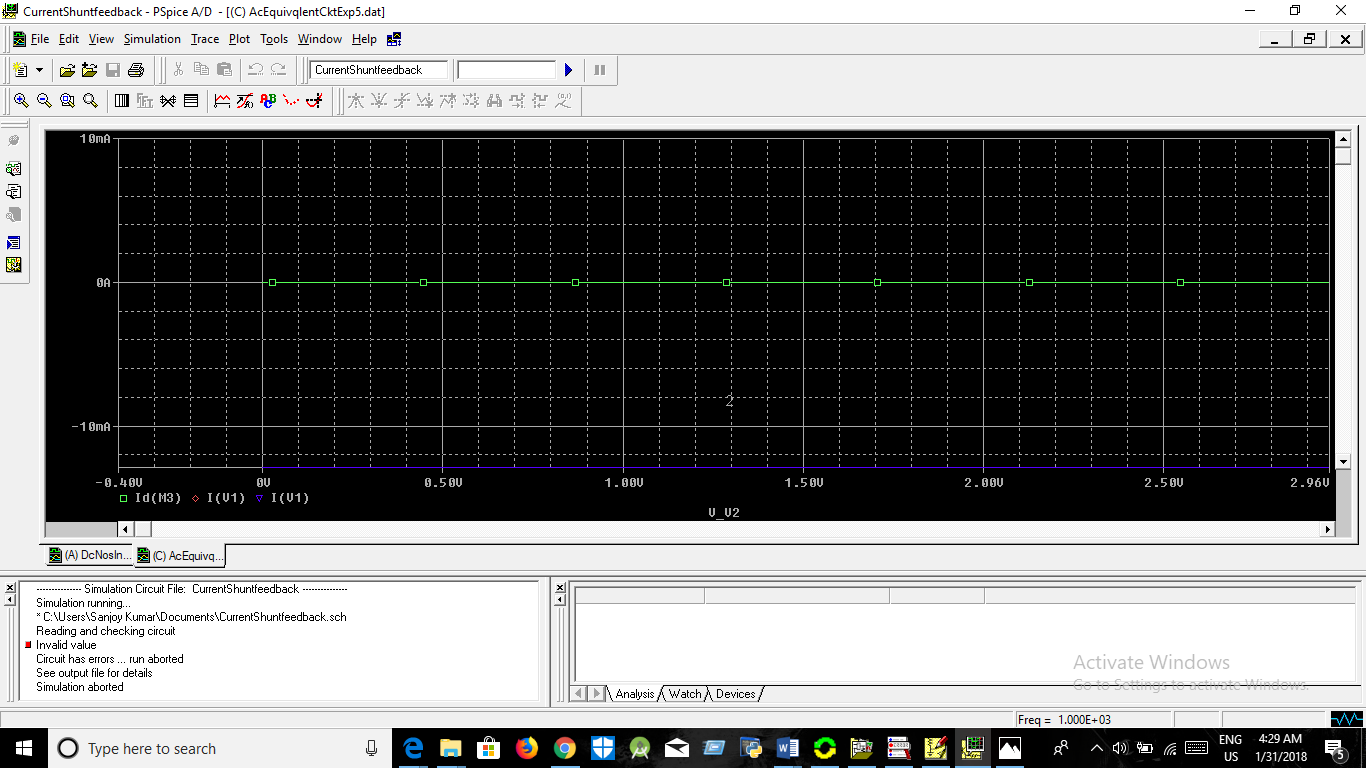
1.10. Find the h- parameters of the given CE configuration using the data taken in step 9.

1.11. Compare the results with that of Single-stage amplifier studied in previous simulation. Also compare the gain-bandwidth product (GB) of single-stage and cascaded amplifiers. (GB=BW\*AV, where BW=fHC-fLC & AV =vo/vi)

Circuit Diagram:



Graph:



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Experiment name: FEEDBACK AMPLIFIERS Voltage-Shunt Feedback

Objectives: Objectives: : DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.

Biasing of BJT.

Small signal Analysis using BJT.

Procedure:

Draw the circuit shown in Fig. 2 in PSpice schematics. Here, Vin is variable frequency AC source (Having Part Name of VAC). Set its amplitude to 1 mV, keeping other parameters (e.g. Vdc) to zero value. Select AC Sweep from Setup Analysis. Select sweep from 10 Hz to 1 MHz (or higher or lower, ensuring that you observe both the cut-off frequencies) in Decade mode, with 20 Pts/decade. Run the simulation. Observe the voltage gain (AV=vo/vi) at different frequencies. At mid-band frequency, note the voltage gain (AV), current gain (AI), input resistance (Ri) and output resistance (Ro) of the configuration. Compare the results with that of single stage amplifier (without feedback) studied in previous simulation. Hence, find the desensitivity (D) of the amplifier. Verify the values measured in step 6, with theoretical values obtained from without feedback single-stage amplifier’s preserved values modified using D.

Circuit Diagram:

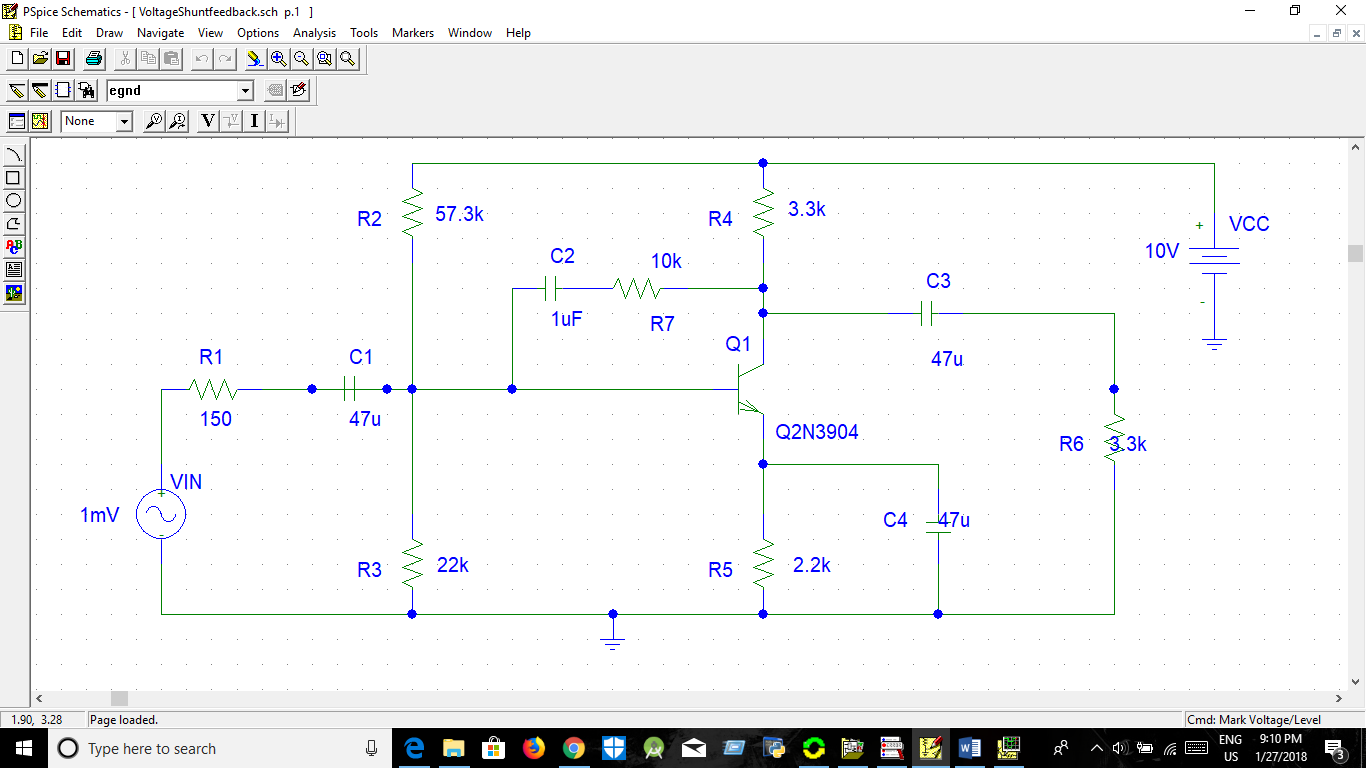
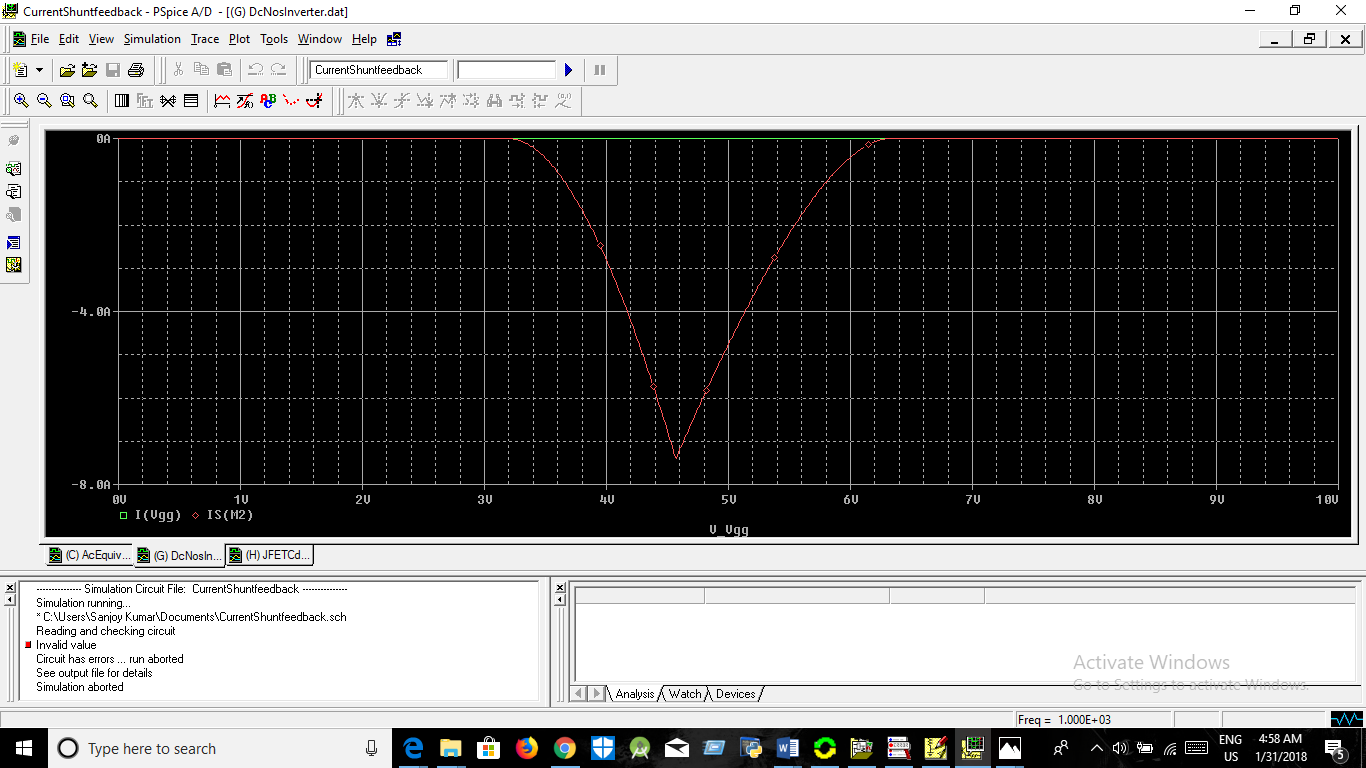


Fig.2. Voltage-series feedback amplifier

Circuit Graph:



Discussion:

1.Voltage series feedback amplifier depends on the common emitter and common base .

2.Its depends on the system on small signal.

3.the graph shown in the figure.

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Experiment name:Experiment on Current-Shunt Feedback.

Objectives: Objectives: Objectives: : DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.

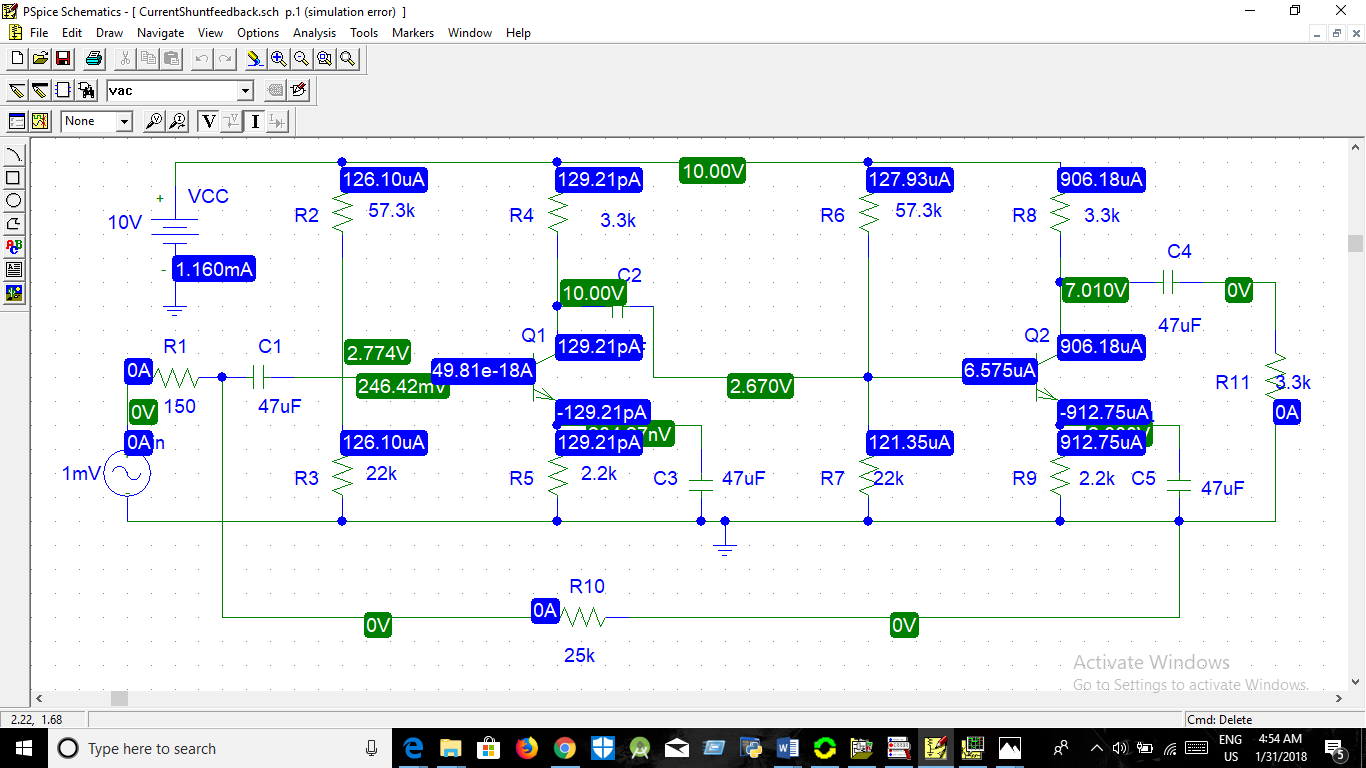
Biasing of BJT.

Small signal Analysis using BJT.

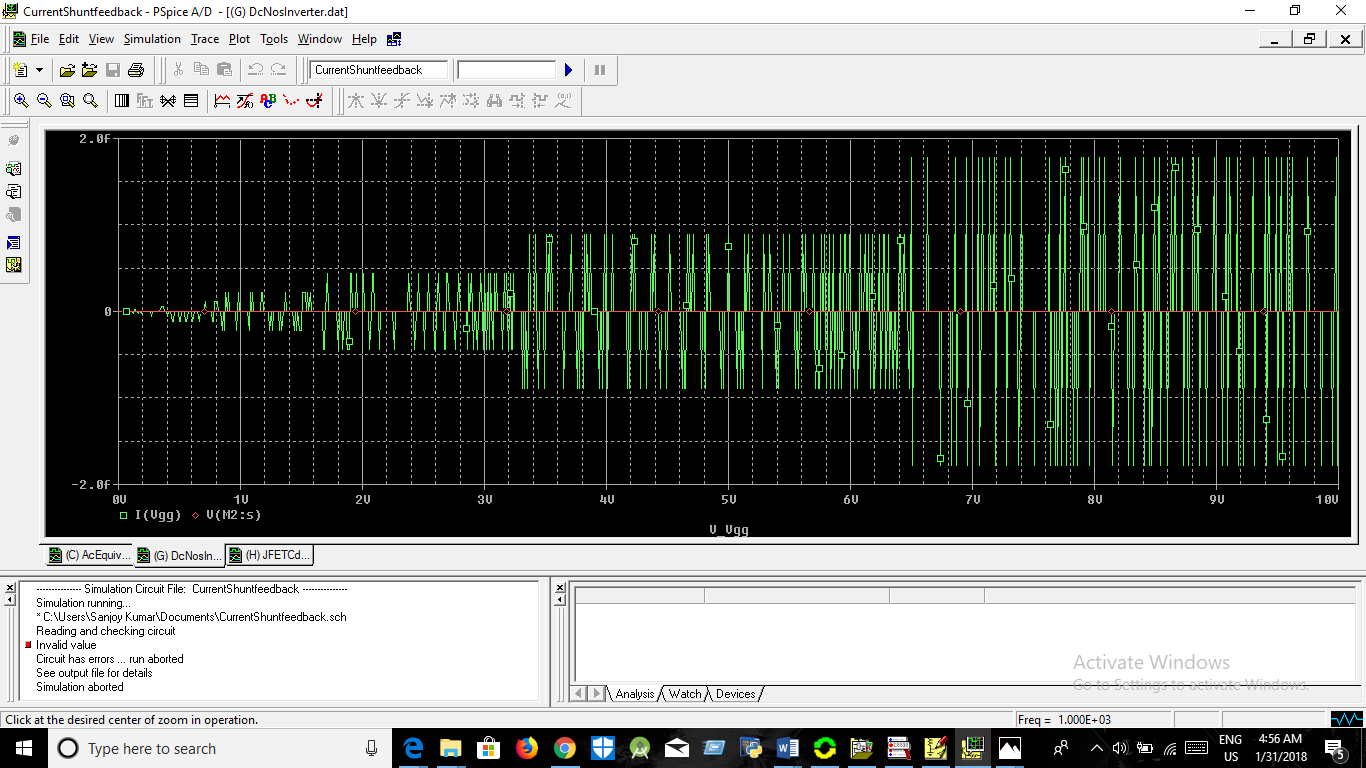
Procedure:

5.1. Draw the circuit shown in Fig. 2 in PSpice schematics. 5.2. Here, Vin is variable frequency AC source (Having Part Name of VAC). Set its amplitude to 1 mV, keeping other parameters (e.g. Vdc) to zero value. 5.3. Select AC Sweep from Setup Analysis. Select sweep from 10 Hz to 1 MHz (or higher or lower, ensuring that you observe both the cut-off frequencies) in Decade mode, with 20 Pts/decade. 5.4. Run the simulation. 5.5. Observe the voltage gain (AV=vo/vi) at different frequencies. 5.6. At mid-band frequency, note the voltage gain (AV), current gain (AI), input resistance (Ri) and output resistance (Ro) of the configuration. 5.7. Compare the results with that of single stage amplifier (without feedback) studied in previous simulation. Hence, find the desensitivity (D) of the amplifier. 5.8. Verify the values measured in step 6, with theoretical values obtained from without feedback single-stage amplifier’s preserved values modified using D

Circuit Diagram:



Graph diagram:



Discussion:

1.Current Shunt feedback amplifier depends on the common emitter and common base .

2.Its depends on the system on small signal.

3.the graph shown in the figure.

Submission By

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Experiment name: DC Characteristics of Complementary MOS (CMOS) Inverter

Objectives: Objectives: Objectives: Objectives: : DC characteristics of BJT in Common Emitter (CE) and Common Base (CB) configuration.

Biasing of BJT.

Small signal Analysis using BJT.

Procedure:

4.1. Draw the circuit shown in Fig. 3 in PSpice schematics. [Note that the MOSFETs selected for this inverter circuit has complementary, i.e. that have similar properties like rise time, fall time, etc. Also note that the p-MOSFET’s source is connected to positive terminal of DC source and n-MOSFET’s source connected to ground for proper operation of the circuit.]

Plot of Transfer Curve of CMOS Inverter 4.2. Set DC Sweep (linear) of Vgg from 0 to 10 volts in 0.01 volts steps. 4.3. Place a voltage marker across the load resistance. Run the simulation. 4.4. The transfer Curve will appear on the screen.

Circuit Diagram:

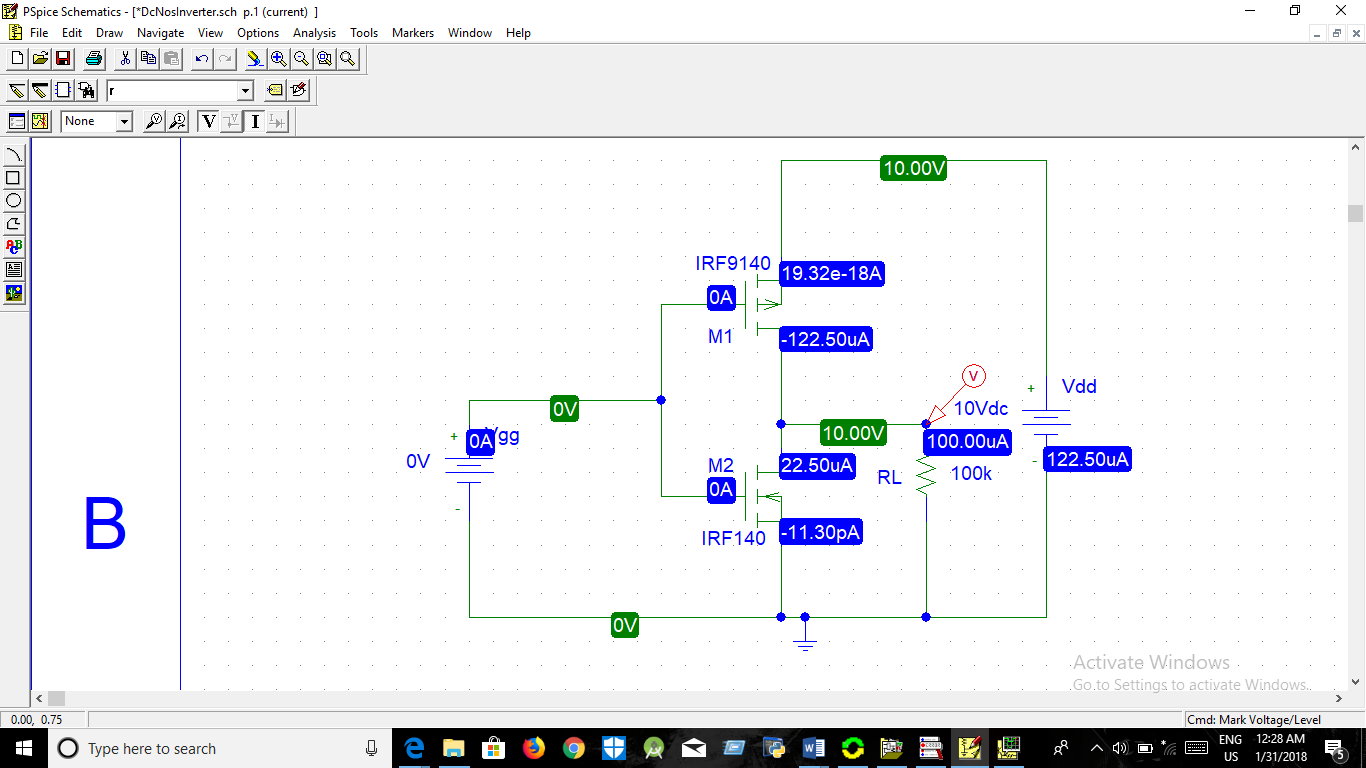


Fig.4. Circuit for DC analysis of CMOS Inverter

Graph Diagram:

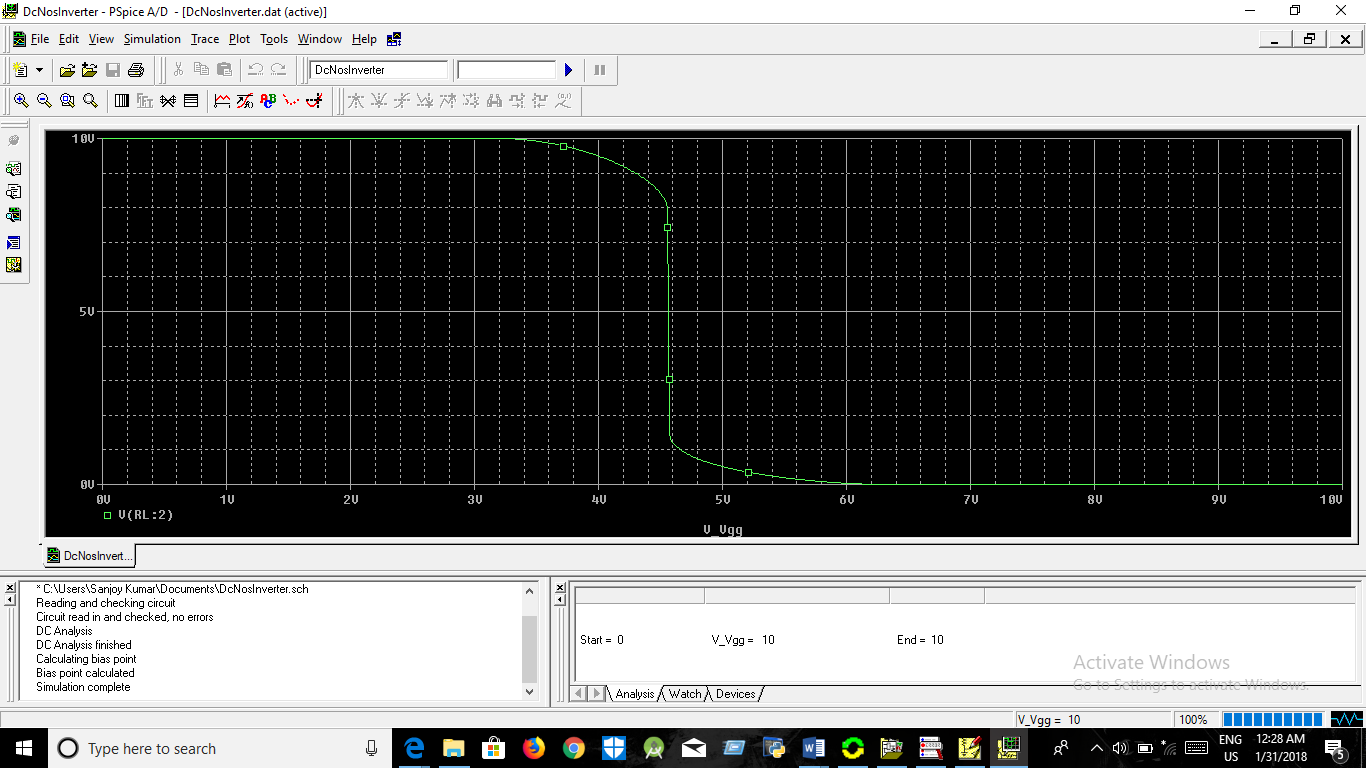


Fig:Graph of DC analysis of CMOS

Discussion:

1.MosFetamplifier depends on the common emitter and common base .

2.Its depends on the system on small signal of parts

3.the graph shown in the figure.

Submission By

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Dept of EEE.

Name of the Experiment: STUDY OF JFET SMALL SIGNAL AMPLIFIER.

OBJECTIVE The objective of this experiment is to simulate for studying the performance of the Common Source (CS) and Common Drain (CD) JFET small signal amplifiers

Theory:

The input impedance of the JFET is very high since the gate-to-channel junction is always reverse biased. FET’s are therefore useful in the design of high-input-impedance amplifiers. In this experiment we shall study two configurations of FET amplifiers: the common-source circuit, and the common-drain or source follower. In addition to its application in amplifier design, JFETs are very useful as voltage controlled resistances.

Procedure:

1.1. Draw the circuit shown in Fig. 2.

1.2. By choosing Setup analysis, mark Bias Point Detail and Transient.

1.3. Choose appropriate step and stop time.

1.4. Run the simulation and click on the Enable Bias Voltage Display and Enable Bias Current Display icons. Note IDSQ and VGSQ. Compare this with theoretical values.

1.5. Draw the small signal equivalent circuit [Homework]

1.6. Obtain the voltage gain for the circuit (v0/vs) from the display in probe.

1.7. Remove CS and calculate the voltage gain. Compare it with the result of step 6. What is the effect of CS on the gain?

1.8. Reconnect CS and connect a resistance of 100 k of in series with the source. Calculate the new voltage gain.

1.9. From step 6 and 8 calculate input resistance of the amplifier.

1.10. With CS connected, set the load resistance RL = 1M and calculate the voltage gain. Use the result of step 8 to calculate the output resistance.

Circuit Diagram:

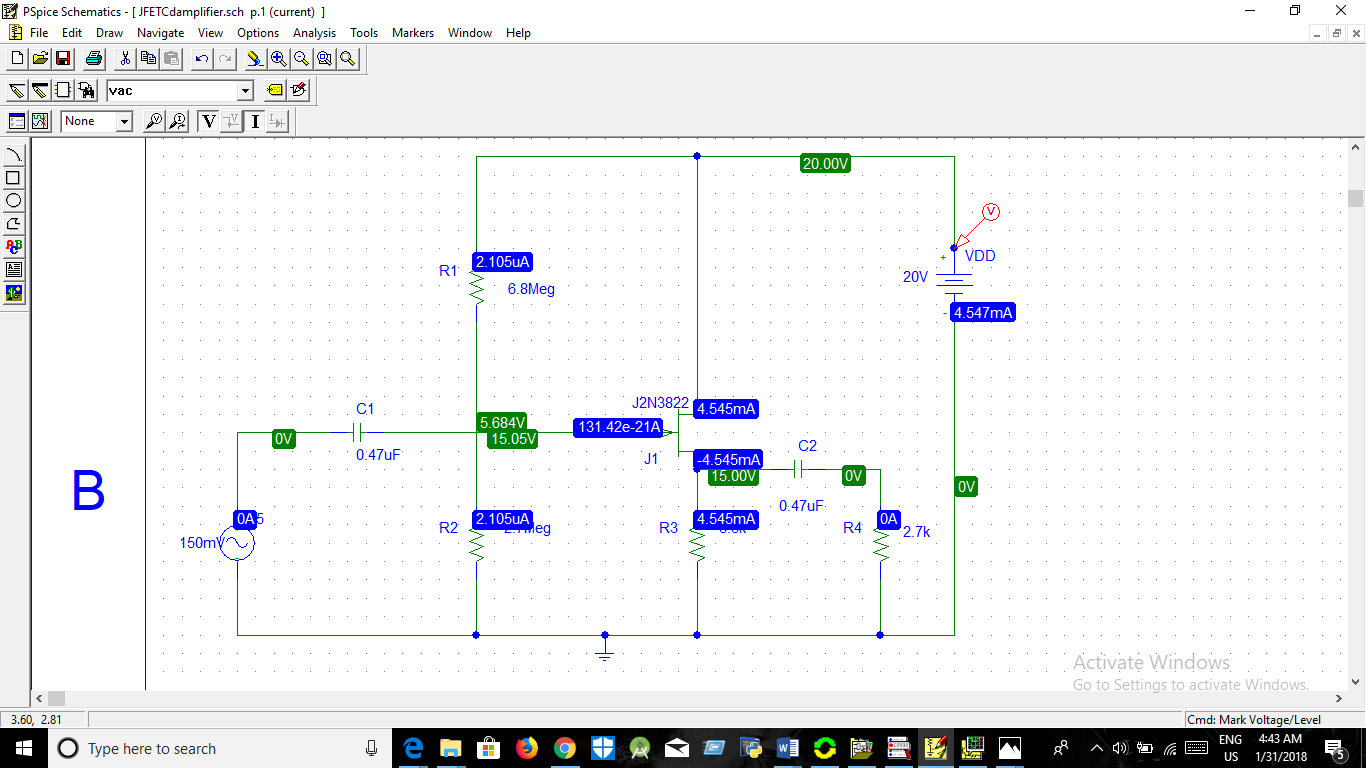
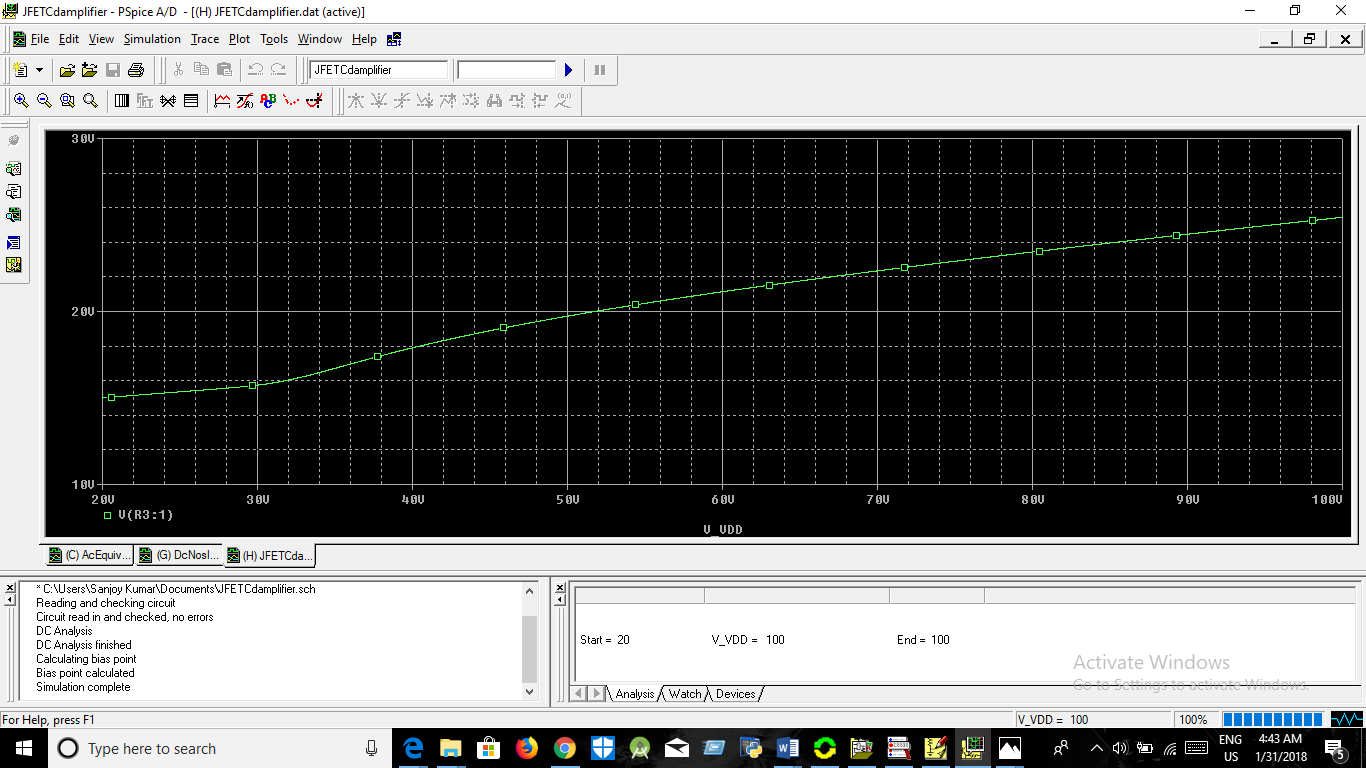


Fig.2. Circuit for Small signal analysis using JFET as CS Amplifier

Graph Diagram:



Name Of The Experiment: STUDY OF BIASING AND FREQUENCY RESPONSE OF AN INTEGRATED CIRCUIT MOS AMPLIFIER.

OBJECTIVE To familiarize with biasing of Integrated MOSFET and frequency response of a Current Source (CS) Amplifier.

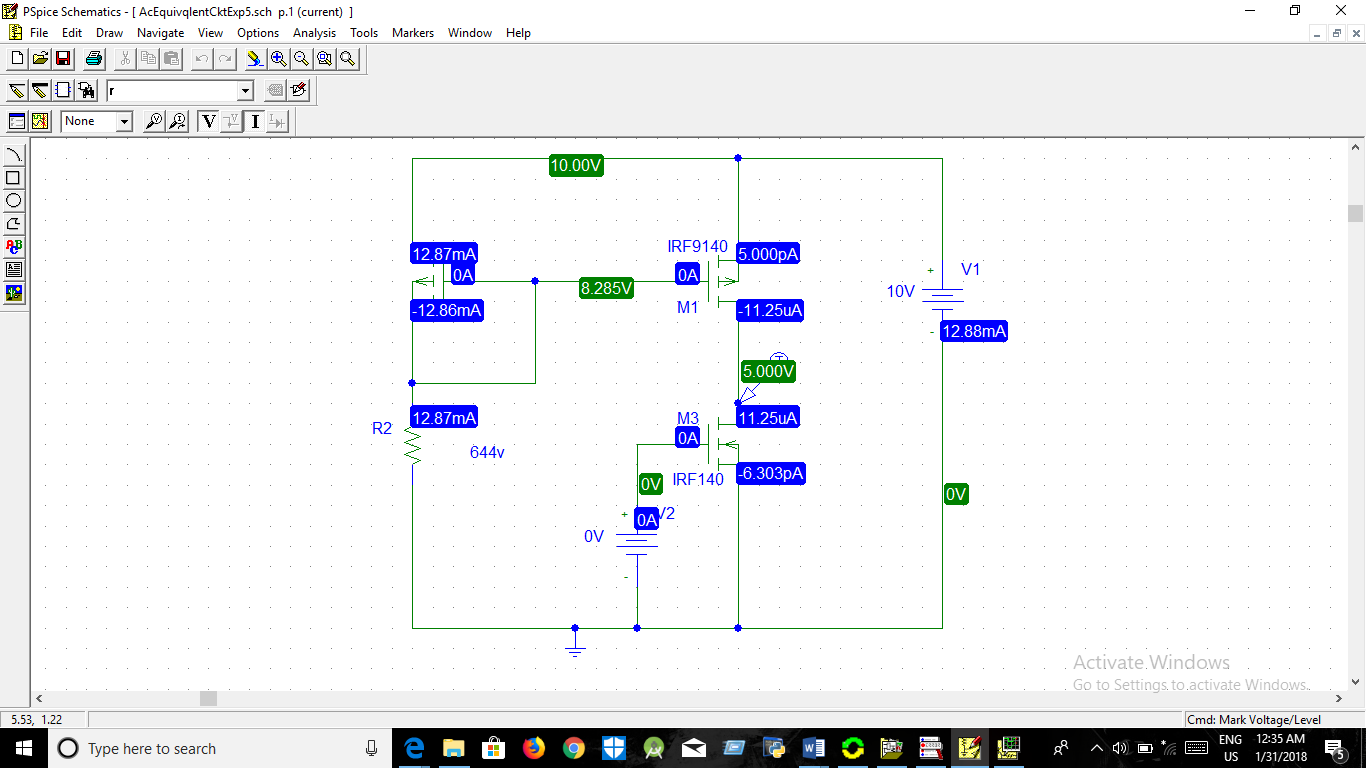
Procedure:

a) Draw the circuit in Fig. 6. Set value of Rbreak to 10kΩ. b) Note the value of VGS, VDS and ID for determining the value of early voltage, VA c) Replace the p-MOSFET (IRF9140) with n-MOSFET (IRF140). Following the steps in (b-d), find the value of early voltage for the n-MOSFET.d) Draw the circuit in Fig.7. Set value of Rbreak to 10kΩ.

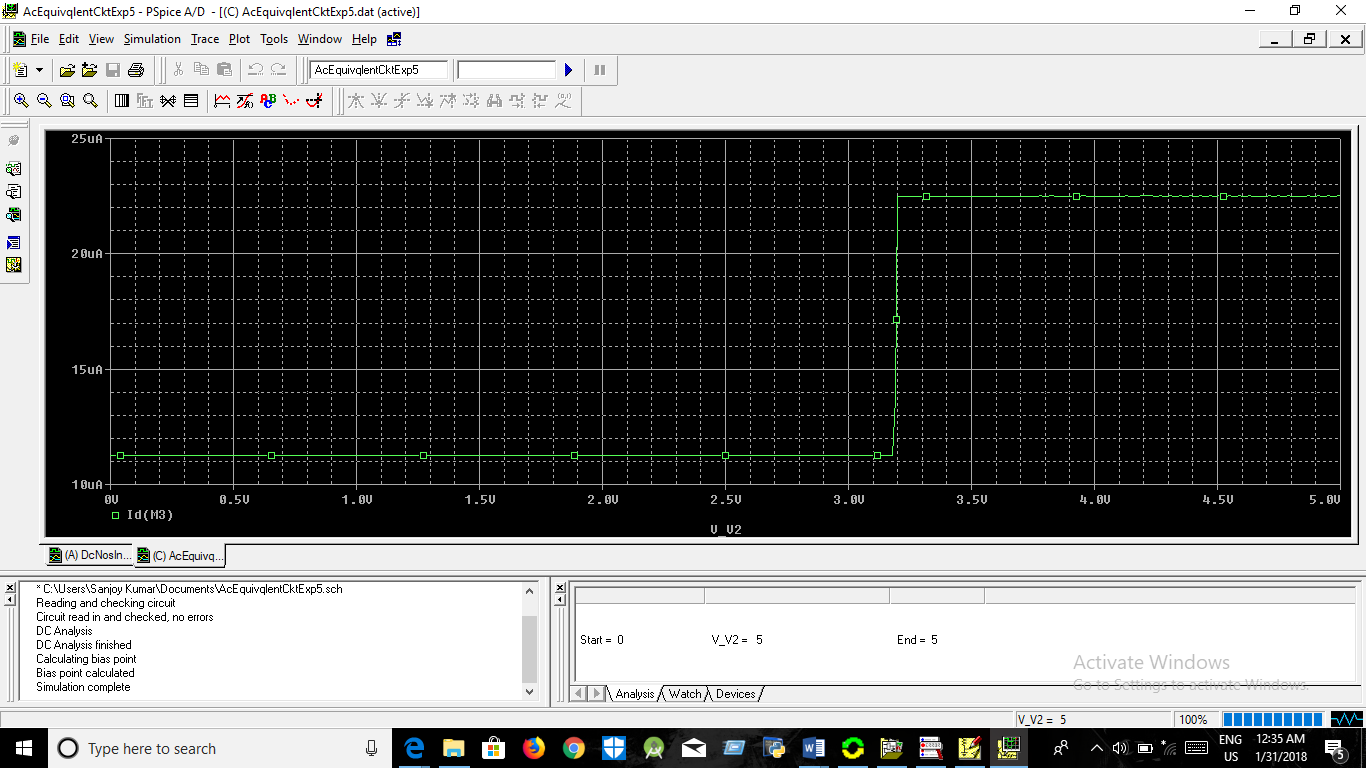
e) Vary the resistance R1 from 0.1 kΩ to 20 kΩ. [For varying R1, choose Rbreak from part list, then from DC sweep select Model Parameter as sweep variable type. Use RES as Model type, Rbreak as Model name and R as Param. Name. Vary R from 0.1 to 2 in steps of 0.1.] f) Determine the value of R1 ( = R x 10kΩ) for which the value of IR2 is 1mA. Replace Rbreak with a resistance having the determined value.

g) Note VDS3, VDS2, VGD2

Circuit Diagram:



Graph Diagram:



Discussion:

1.Mosfet b amplifier depends on the common emitter and common base .

2.Its depends on the system on small signalof the any electronic device.

3.the graph shown in the figure.

Submission By

Sanjoy Kumar

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Dept of EEE.

Experiment Name: A-C EQUIVALENT CIRCUIT

Objectives:

OBJECTIVE To familiarize with biasing of Integrated MOSFET and frequency response of a Current Source (CS) Amplifier.

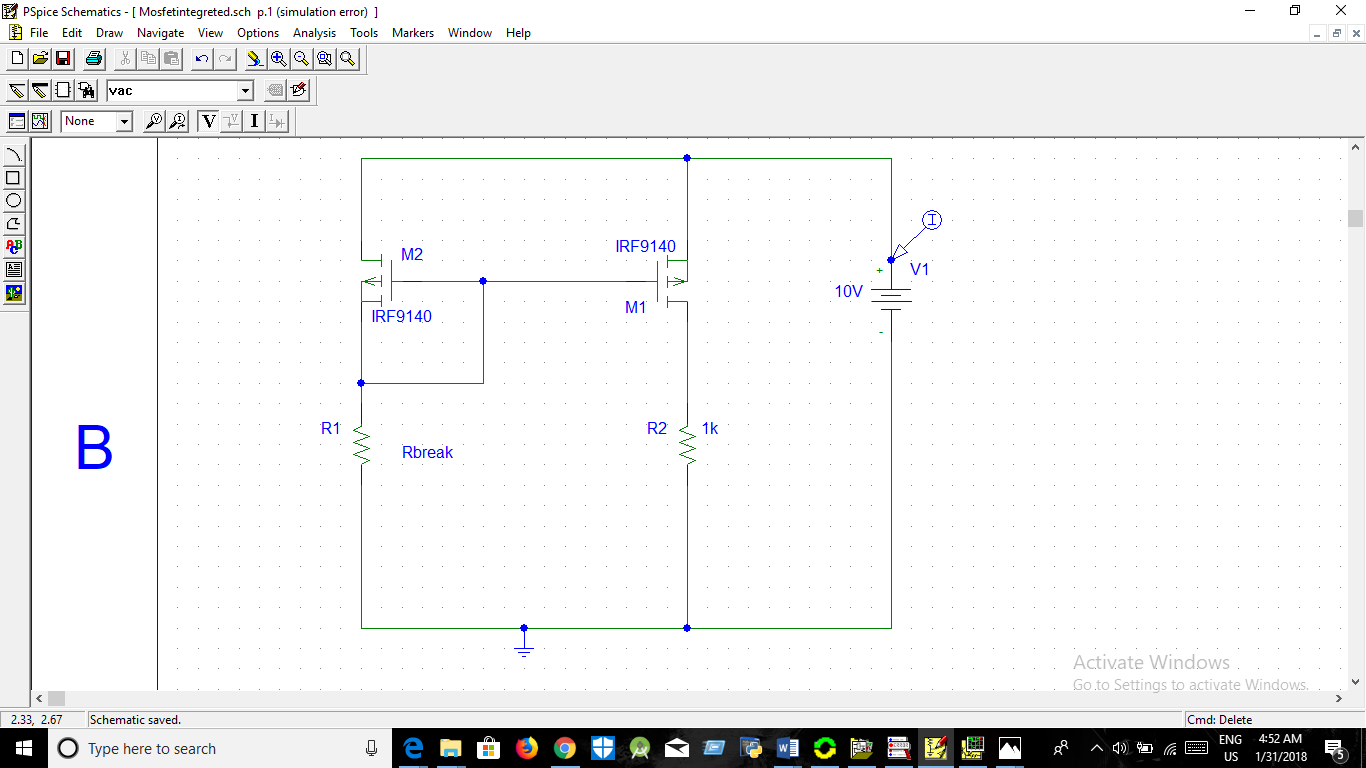
Procedure:

a) Draw the circuit in Fig. 6. Set value of Rbreak to 10kΩ. b) Note the value of VGS, VDS and ID for determining the value of early voltage, VA c) Replace the p-MOSFET (IRF9140) with n-MOSFET (IRF140). Following the steps in (b-d), find the value of early voltage for the n-MOSFET.d) Draw the circuit in Fig.7. Set value of Rbreak to 10kΩ.

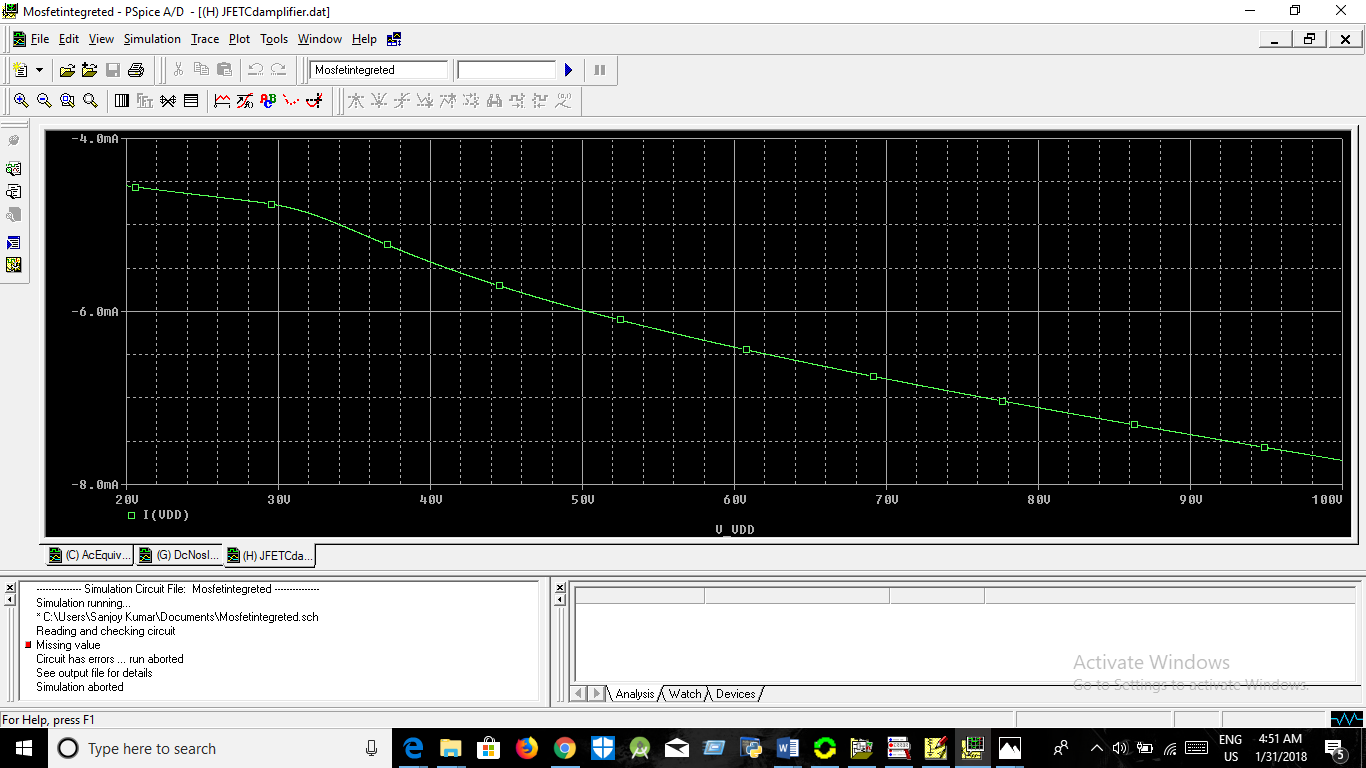
e) Vary the resistance R1 from 0.1 kΩ to 20 kΩ. [For varying R1, choose Rbreak from part list, then from DC sweep select Model Parameter as sweep variable type. Use RES as Model type, Rbreak as Model name and R as Param. Name. Vary R from 0.1 to 2 in steps of 0.1.] f) Determine the value of R1 ( = R x 10kΩ) for which the value of IR2 is 1mA. Replace Rbreak with a resistance having the determined value.

Circuit D

Circuit Diagram:



Graph Diagram:



Discussion:

1.Mosfet b amplifier depends on the common emitter and common base .

2.Its depends on the system on small signalof the any electronic device.

3.the graph shown in the figure.

Submission By

Sanjoy Kumar

ID:2015338532

Dept of EEE.

SYLHET ENGINEERING COLLEGE

Experiment Name: Simulation Lab Report.

Date Of Submission:1.02.2018

REMARK:

Submitted To Submitted By

Shahadat Hossain Parvez Sanjoy Kumar

Lecturer of EEE ID: 2015338532

Sylhet Engineering College Dept of EEE

Group:B

Name of the Simulation: 7a: Study of an R-C Phase Shift Oscillator Oscillator

OBJECTIVE OF 7a The objective of this module is to construct a C-R phase shift oscillator using Op-Amp. The theoretical frequency of oscillation is- 1 for C-R Oscillator 2 RC 6 6 for R-C Oscillator 2 RC f f    

OBJECTIVE OF 7b

The objective of this experiment is to study the operation of the Wien bridge oscillator

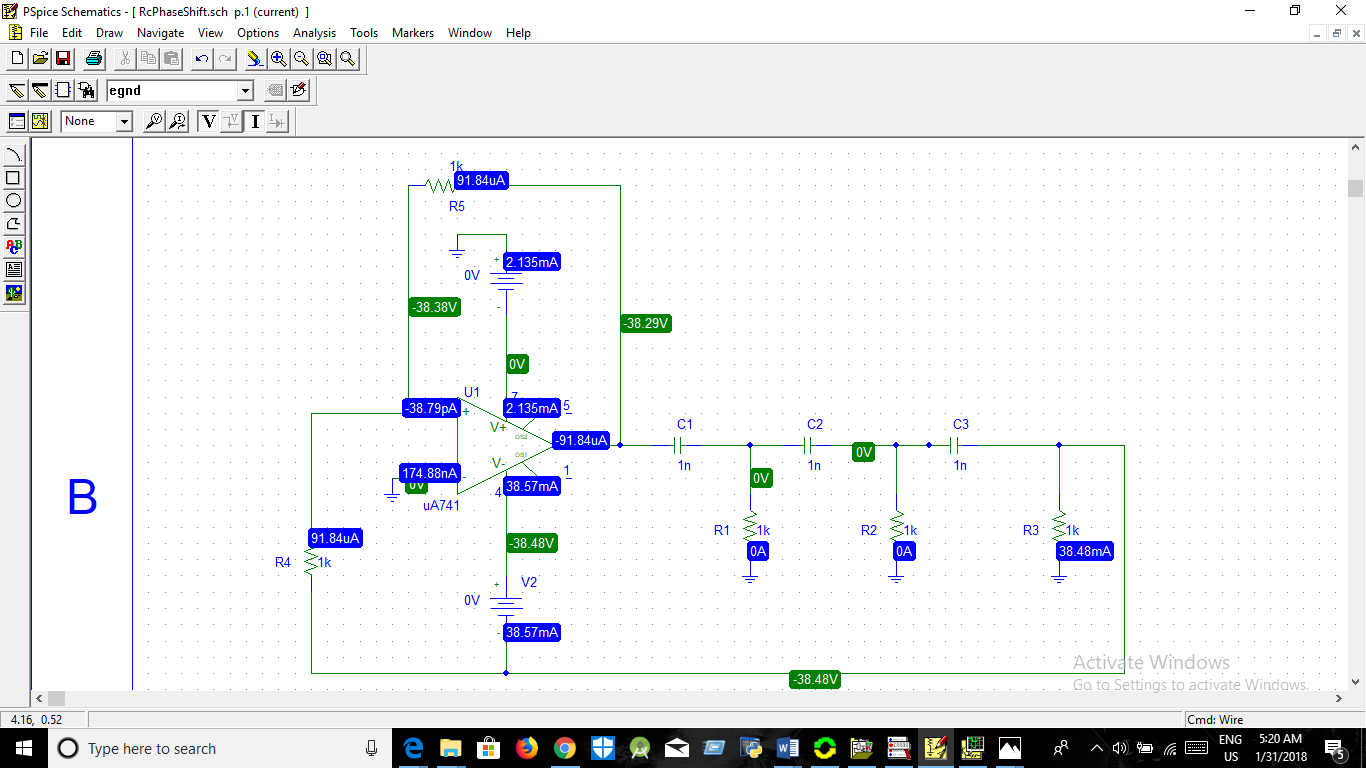
Theoretically the frequency of oscillation is given by

THEORY An oscillator circuit in which a several RC stages are used to make 1800 phase shift (condition for an oscillator) is called R-C or C-R Phase Shift Oscillator.

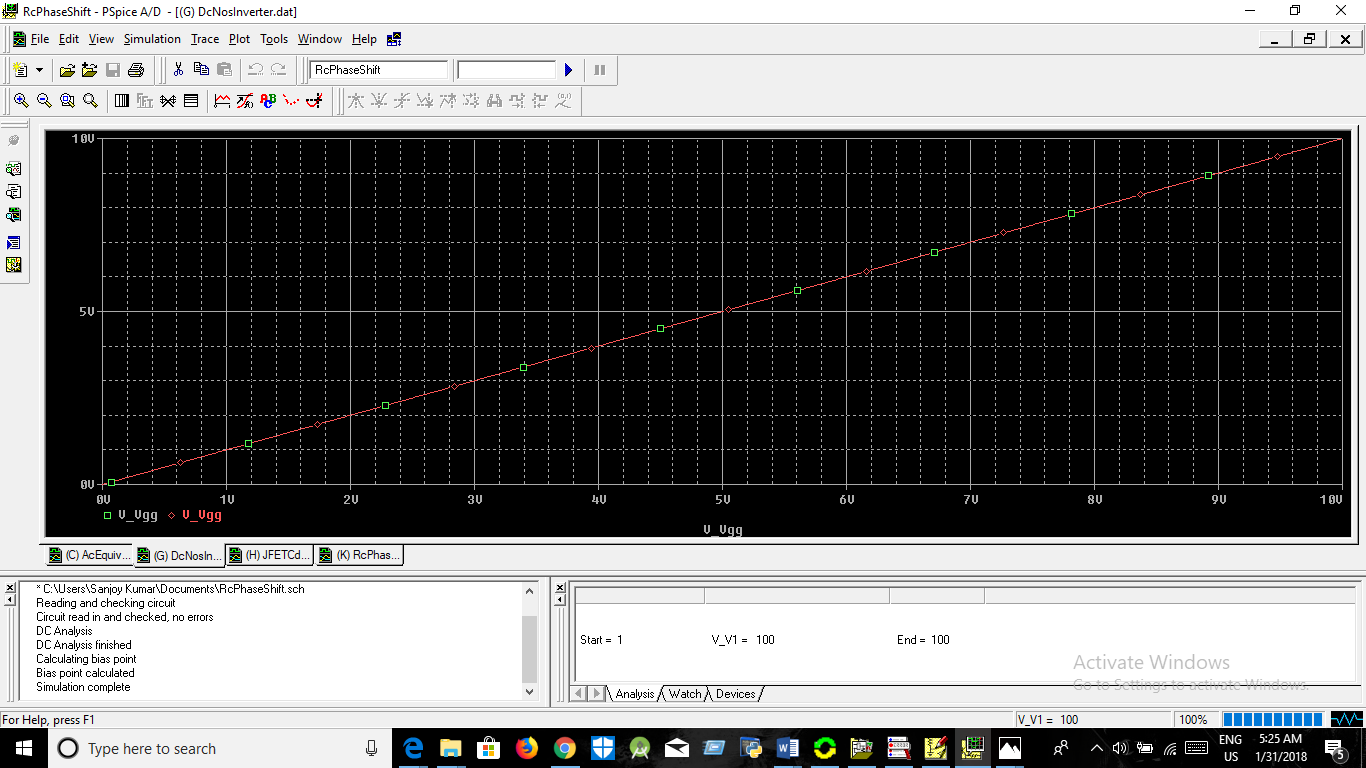
An oscillator circuit in which a balanced bridge is used as the feedback network is the Wien bridge oscillator. .The oscillation is maintained when R2/R1 ratio is approximately 2. Notice that if R2 is made appreciably greater than 2R1 a square wave oscillation is produced and if R2 is made less than 2R1 oscillation decays and ceases.

PROCEDURES 1) R-C Phase Shift Oscillator  Draw the circuit as shown in Fig.7a in PSpice schematics.  Select transient from Setup Analysis and set final time to 300ms

Circuit Diagram:



Graph Diagram:



Discussion:

1.Mosfet b amplifier depends on the Rc Phase shift ossicilotor .

2.Its depends on the system on small signalof the any electronic device.

3.the graph shown in the figure.

Submission By

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