Sankalpa Hota

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Education

University of California San Diego, CA GPA : 3.77/4.0
Master of Science in Electrical and Computer Engineering *Sept. 2025 – June 2027*
Coursework: VLSI Implementation for ML, Computer Architecture, VLSI Digital System Algorithms & Architectures

National Institute of Technology, Rourkela GPA : 3.93/4.0
Bachelor of Technology in Electrical Engineering , Minor in Computer Science *Aug. 2018 – May 2022*
Coursework: Processor Design, Microprocessors, Testing & Verification of VLSI Circuits, Digital Design

Technical Skills

Languages: SystemVerilog, Verilog, C++, UVM, C, TcL/Tk, Perl, Shell, MATLAB
Software: Vivado, Cadence Virtuoso, Innovus ,Genus , Design Compiler, Quartus Prime, Iverilog

Professional Experience

Semiconductor Engineer II, Micron Technology Apr 2024 – Aug 2025

- Led **RTL design and integration** of custom IP blocks for **Flash/Cache memory retention** and **PCIe Gen5 TLP and DLLP datapaths**, contributing to protocol correctness and timing closure.
- Designed and validated **control logic and datapaths** for **NAND, DDR, NVMe controller, and PCIe subsystems** on FPGA-based platforms, enabling **architectural bring up** and early silicon risk reduction.
- Drove debug and root-cause analysis across **RTL**, firmware, and hardware, analyzing **waveforms, protocol traces, logs, and scan dumps** via **JTAG and UART** to resolve functional, timing, and data integrity issues.
- Collaborated with firmware, NAND, and physical design teams to close **functional and system level issues** across memory and **high speed link layers**.
- Co-authored **3 US patents** on firmware hardware co-design architectures for **memory subsystems** and **physical link layers**, strengthening system reliability and performance.

Semiconductor Engineer I, Micron Technology Aug 2022 – Apr 2024

- Developed **RTL based validation infrastructure** for **microSD controllers** using **AMD Zynq 7000 FPGA**, including **bitstream generation**, **FPGA programming**, and FPGA level validation workflows.
- Designed and executed **stress driven verification scenarios** across **workload and cross environment conditions**, improving coverage of corner cases in **ARM** controllers for **NVMe 2.0**.
- Debugged **firmware, protocol, and link level issues** related to **data retention, recovery, and integrity** supporting functional and system closure.

Projects

Performance Enhanced Reconfigurable 2D Systolic Array with Integrated Controller Sept 2025 – Dec 2025

- Designed a **reconfigurable systolic array accelerator** for **low power CNN inference** on **FPGA platforms**.
- Achieved a **69.22%** reduction in convolution latency, **82.8%** memory size savings and **55%** fewer MAC operations compared to baseline designs using techniques like input data sieving, parallel accumulation, and pipelining
- Optimized execution using **Input Channel LUT filtering** and **MAC accumulation**, reducing clock cycles by **67%**.
- Reduced power and area via **clock gating**, **FIFO depth reduction**, and **datapath register optimization.**
- Synthesized and mapped the accelerator onto **Cyclone V FPGA**, meeting **timing**, **resource**, and **DSP utilization constraints** targets using Quartus Prime after verification using **UVM**.

Dual Core Machine Learning Accelerator for Transformer Attention Mechanism Sept 2025 – Ongoing

- Developed a **1-D vector processor** with **pipelined execution**, enabling **parallel computation** of attention weights.
- Engineered a **custom controller** with **clock gating**, reducing **dynamic power** in sparse data scenarios.
- Optimized **division latency** using **custom pipelined divider**, achieving **0.9ns clock period** with reduced latency.
- Developed an **accumulator shifter based parallel normalization technique**, improving **throughput** and reducing **memory accesses** during attention score computation.
- Conducted full **RTL to GDSII implementation**, including **synthesis**, **place & route (PnR)**, and **PPA analysis**.
- Integrated **asynchronous FIFOs** for **synchronization** between independently **clocked cores**.
- Accomplished significant **power savings** through **block wise & columnar clock gating**, reducing unnecessary **toggling**.

VLSI design for Near Memory Crypto Engine Sept 2025 – Ongoing

- Architected **near memory crypto engine** integrating **Advanced Encryption System (AES)** RTL using Verilog.
- Applied fully pipelined **datapaths** sustaining **PCIe Gen5 throughput** at **500 MHz** target frequency.
- Designed **nonce generation** and **replay mechanisms** ensuring correctness across encryption and decryption.
- Implemented **ready/valid flow control** and **arbitration logic** to avoid **structural hazards** across cipher pipelines.
- Optimized critical datapath stages balancing **pipeline depth, OoO**, **area**, and **power** while meeting **timing constraints**
- Ongoing work on **DRAM/SRAM architecture** with **near memory error correction** for data corruption handling.