

EXPERIMENT NO. - 6

TITLE: Interfacing Push Buttons.

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EXPERIMENT NO.-6

TITLE: Interfacing Push Buttons, LEDs, Relay & Buzzer to PIC Microcontroller
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MICROCONTROLLERS – LABORATORY MANUAL

AIM: To Interface Push buttons, LEDs, Relay and Buzzer to PIC Microcontroller. Write a program in Embedded C to interact with peripherals as follows.

- LED's start chasing from left to right and turn ON Relay & buzzer whenever Push button 1 is pressed.
- LED's start chasing from right to left and turn OFF Relay & buzzer whenever Push button 2 is pressed.

OBJECTIVE:

1. To understand the PORT Structure of PIC Microcontroller.
2. To study the SFRs to control the PORT Pins.
3. To interface common peripherals like pushbuttons, LEDs, relay.
4. To understand the use of MPLABX IDE and C18 Compiler.
5. To write a simple program in Embedded C.

THEORY:

Depending on the device selected, there are up to five general purpose I/O ports available on PIC18F Microcontroller devices. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

1. Some common Features of the I/O Ports

- Up to 70 bi-directional I/O pins
 - Some multiplexed with peripheral functions
- High drive capability
 - 25mA source/sink capability
- Direct, single cycle bit manipulation
- 4kV ESD protection diodes
 - Based on human body model
- After reset:
 - Digital I/O default to Input (Hi-Z)
 - Analog capable pins default to analog

2. SFR Associated with I/O Port

Each port has three registers for its operation and figure 1.1 and figure 1.2 shows the functioning of each registers:

TRIS register (Data Direction register): To select PORT pin as input or output. All port pins are input by default. Whenever a bit in the TRISx register is a 0, the corresponding bit in PORTx is an output. If the bit in

➤ **PORT register** (reads the levels on the pins of the device)

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- **LAT register (output latch):** The data latch (LAT register) is useful for read modify-write operations on the value that the I/O pins are driving.

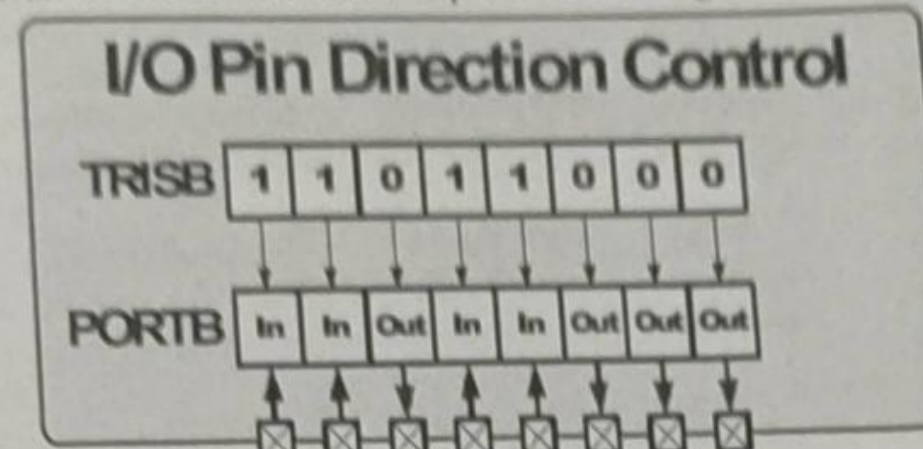


Figure 1.1 : TRISx Register

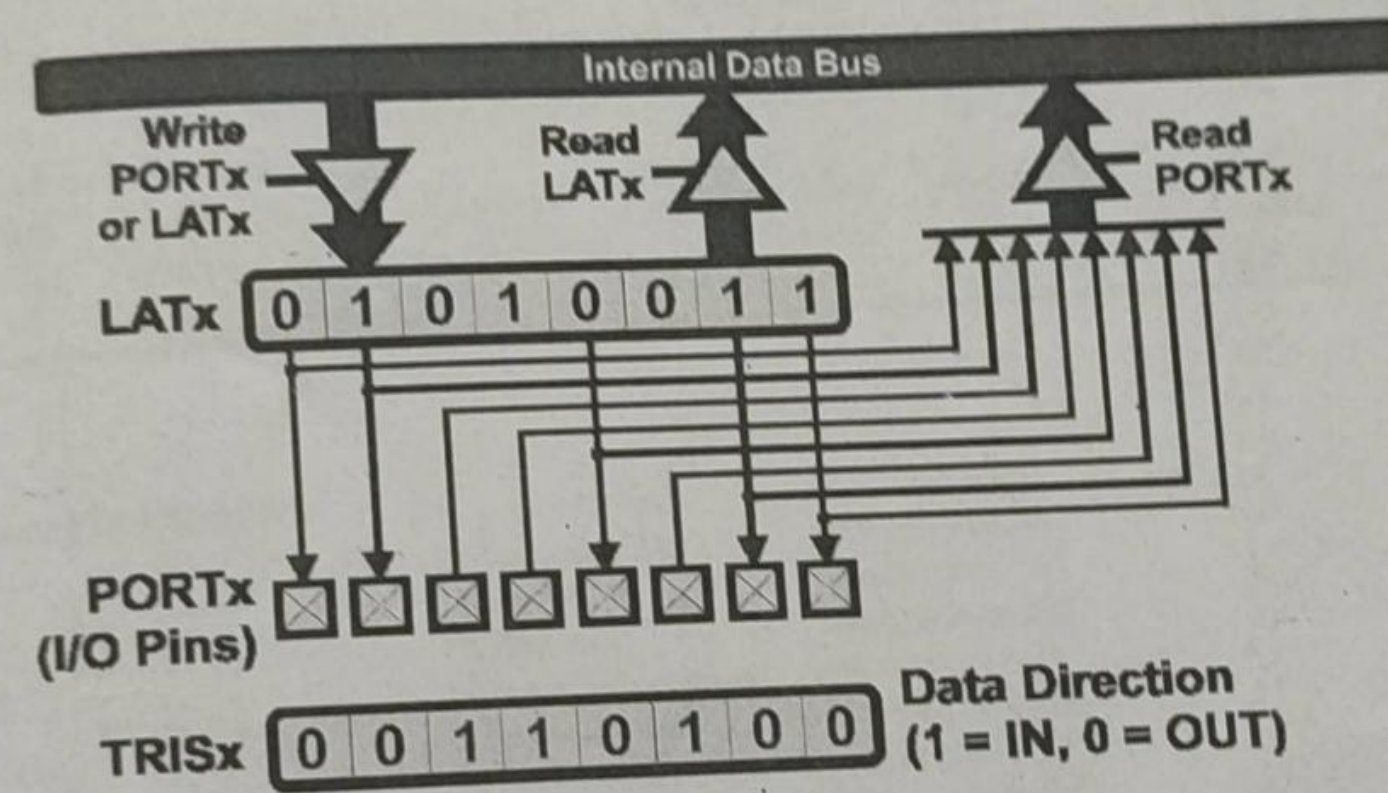


Figure 1.2 : SFRs associated with I/O Port

2.1 Register Map

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SFR	Description	Access	Reset Value	Address
PORTA: RA6 – RA0				
TRISA	PORTA Direction Register	Read/Write	0x7F	0xF92
PORTA	PORTA Read/Write Register	Read/Write	unknown	0xF80
LATA	PORTA Output Latch Register	Read/Write	unknown	0xF89
PORTB: RB7 – RB0				
TRISB	PORTB Direction Register	Read/Write	0xFF	0xF93
PORTB	PORTB Read/Write Register	Read/Write	unknown	0xF81
LATB	PORTB Output Latch Register	Read/Write	unknown	0xF8A
PORTC: RC7 – RC0				
TRISC	PORTC Direction Register	Read/Write	0xFF	0xF94
PORTC	PORTC Read/Write Register	Read/Write	unknown	0xF82
LATC	PORTC Output Latch Register	Read/Write	unknown	0xF8B
PORTD: RD7 – RD0				
TRISD	PORTD Direction Register	Read/Write	0xFF	0xF95
PORTD	PORTD Read/Write Register	Read/Write	unknown	0xF83
LATD	PORTD Output Latch Register	Read/Write	unknown	0xF8C
PORTD: RE2 – RE1				
TRISE	PORTD Direction Register	Read/Write	0x07	0xF96
PORTD	PORTD Read/Write Register	Read/Write	unknown	0xF84
LATE	PORTD Output Latch Register	Read/Write	unknown	0xF8D

2.2 Port Pin-Diagram

1	MCLR/Vpp/RE3	RB7/KBI3/PGD	40
2	RA0/AN0	RB6/KBI2/PGC	39
3	RA1/AN1	RB5/KBI1/PGM	38
4	RA2/AN2/Vref-ICVref	RB4/KBI0/AN11	37
5	RA3/AN3/Vref+	RB3/AN9/CCP2 ⁺	36
6	RA4/T0CKI/C1out	RB2/INT2/AN8	35
7	RA5/AN4/SS/HLVDin/C2out	RB1/INT1/AN10	34
8	RE0/RD/AN5	RB0/INT0/FLT0/AN12	33
9	RE1/WR/AN6	VDD	32
10	RE2/CS/AN7	VSS	31
11	VDD	RD7/PSP7/P1D	30
12	VSS	RD6/PSP6/P1C	29
13	OSC1/CLKI/RA7	RD5/PSP5/P1B	28
14	OSC2/CLKO/RA6	RD4/PSP4	27
15	RC0/T1OSO/T13CKI	RC7/RX/DT	26
16	RC1/T1OSI/CCP2 ⁺	RC6/TX/CK	25
17	RC2/CCP1/P1A	RC5/SDO	24
18	RC3/SCK/SCL	RC4/SDI/SDA	23
19	RD0/PSP0	RD3/PSP3	22
20	RD1/PSP1	RD2/PSP2	21

3. Generic I/O Port structure:

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All the ports of PIC18 are bidirectional and identical. They all have the following four components in their structure as shown in figure 1.3.

1. DATA LATCH
2. OUTPUT DRIVER
3. INPUT BUFFER
4. TRIS LATCH

The PIC18 Ports have both the latch and buffer. Therefore, when reading the ports there are two possibilities:

1. Reading the input pin
2. Reading the latch

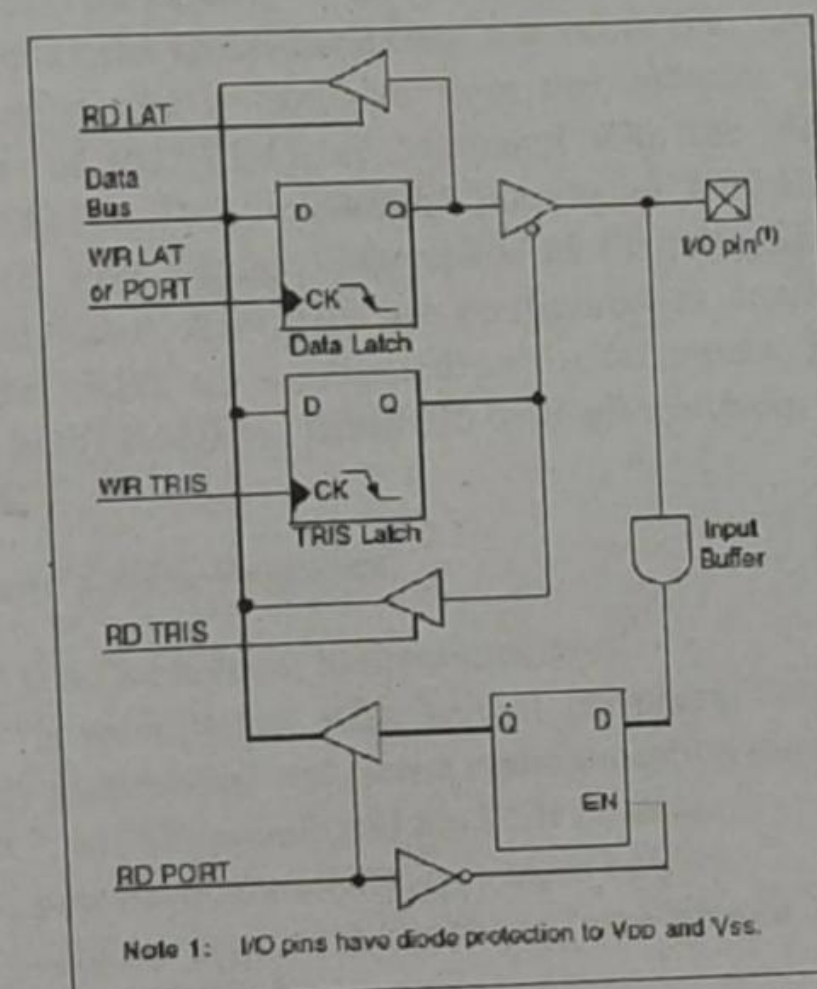


Figure 1.4: Generic I/O Port Operation

3.1 PORTA, TRISA and LATA Registers.

- PORTA is an 8-bit wide, bidirectional port.
- The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin.
- The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register.
- Several PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output.

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- The operation of pins RA5 and RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register.
- On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

3.2 PORTB, TRISB and LATB Registers

- PORTB is an 8-bit wide, bidirectional port.
- Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (INTCON2 register). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.
- Four of the PORTB pins (RB7:RB4) have an interrupt on change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt on change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit RBIF (INTCON register).
- On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs. By programming the configuration bit, PBADEN, RB4:RB0 will alternatively be configured as digital inputs on POR.

3.3 PORTC, TRISC and LATC Registers

- PORTC is an 8-bit wide, bidirectional port.
- PORTC is multiplexed with several peripheral functions. PORTC is primarily multiplexed with serial communication modules, including the EUSART, MSSP module and the USB module.
- PORTC pins have Schmitt Trigger input buffers.
- When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin.
- Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input.
- The user should refer to the corresponding peripheral section for the correct TRIS bit settings. The pin override value is not loaded into the TRIS register.
- This allows read-modify-write of the TRIS register, without concern due to peripheral overrides.
- In PIC18F2455/2550/4455/4550 devices, the RC3 pin is not implemented.
- On a Power-on Reset, these pins are configured as digital inputs.

3.4 PORTD, TRISD and LATD Registers

- PORTD is an 8-bit wide, bidirectional port.

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- All pins on PORTD are implemented with Schmitt Trigger input buffers.
- Three of the PORTD pins are multiplexed with outputs P1B, P1C and P1D of the enhanced CCP module.
- PORTD can also be configured as an 8-bit wide microprocessor port (Parallel Slave Port (PSP) or Streaming Parallel Port (SPP)). In this mode, the input buffers are TTL.
- On a Power-on Reset, these pins are configured as digital inputs.

3.5 PORTE, TRISE and LATE Registers

- For 40/44-pin devices, PORTE is a 4-bit wide port
- Three pins (RE0/RD/AN5, RE1/WR/AN6 and RE2/CS/AN7) are individually configurable as inputs or outputs.
- These pins have Schmitt Trigger input buffers. When selected as an analog input, these pins will read as '0's.
- The fourth pin of PORTE (MCLR/VPP/RE3) is an input only pin. Its operation is controlled by the MCLRE configuration bit. When selected as a port pin (MCLRE = 0), it functions as a digital input only pin; as such, it does not have TRIS or LAT bits associated with its operation. Otherwise, it functions as the device's Master Clear input. In either configuration, RE3 also functions as the programming voltage input during programming.
- For 28-pin devices, PORTE is only available when Master Clear functionality is disabled (MCLRE = 0). In these cases, PORTE is a single bit, input only port comprised of RE3 only.
- On a Power-on Reset, RE2:RE0 are configured as analog inputs. On a Power on Reset, RE3 is enabled as a digital input only if Master Clear functionality is disabled.

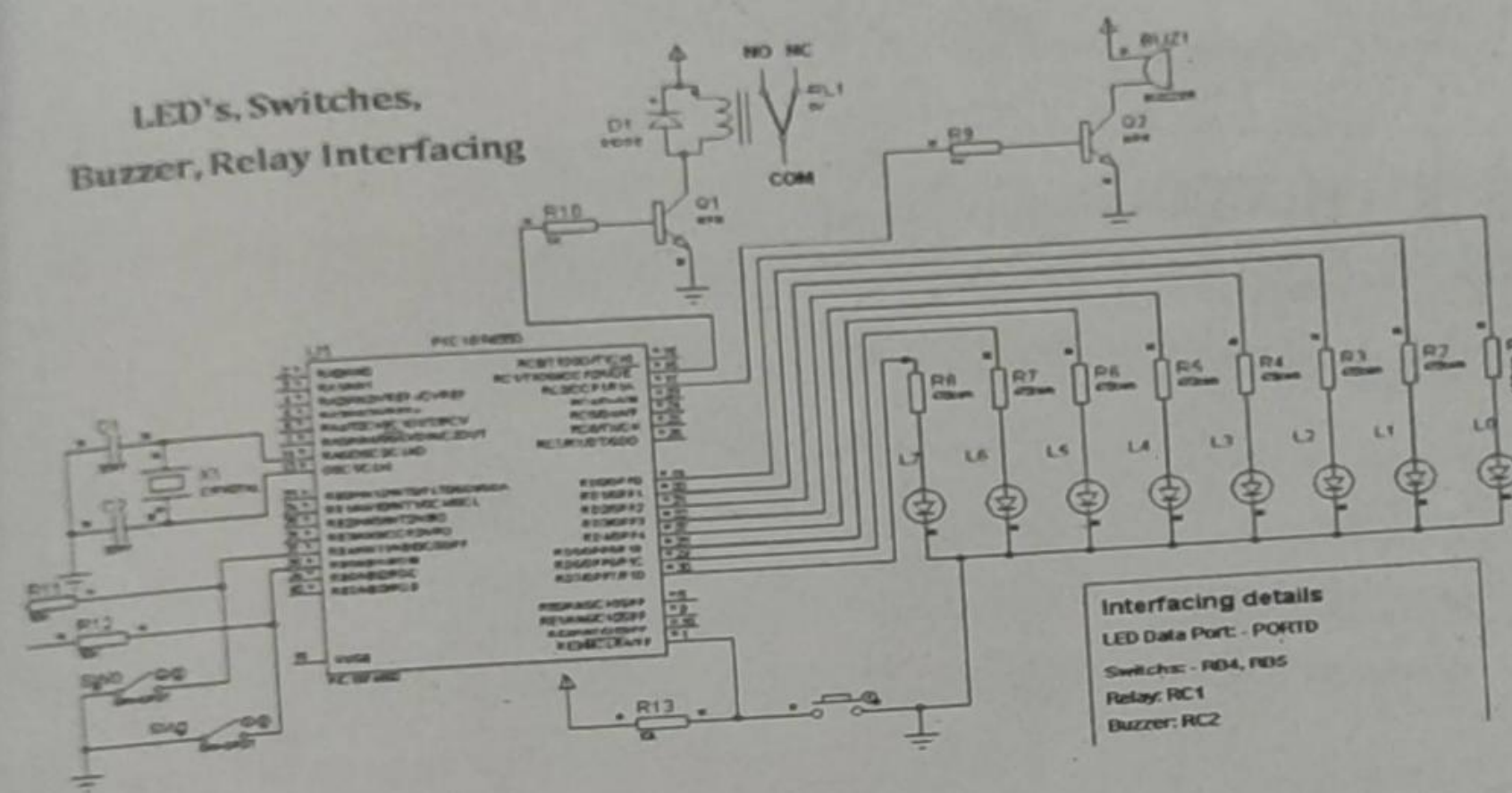
ALGORITHM

1. As LED connected to PORTD configure these pins as output by writing 0x00 to the appropriated TRES register.
2. As buttons are connected to RB.4 and RB.5 so configure these pins as input by writing 1 to the appropriated bits of TRES register.
3. Check the status of RB.4, if it is zero then move 1 bit of PORTB from right to left.
4. Else check the status of RB.5, if it is zero then move 1 bit of PORTB from left to right.
5. Repeat step 3 to 4

INTERFACING DIAGRAM:

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LED's, Switches, Buzzer, Relay Interfacing



CONCLUSION:
In this practical we have studied about to interface Push buttons, LED's, Relay and Buzzer to PIC microcontroller.

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