

# Schmitt Trigger in 28nm CMOS Technology

Sanket M Mantrashetti  
RV College of Engineering(Bangalore)

**Abstract-The Scope of the work is to design 2 Schmitt trigger using 28nm CMOS technology with relatively lower power consumption and low area. The proposed Schmitt triggers works for low voltage and has an intended use over high-speed applications. It is designed using 3 PMOS and 3 NMOS.**

**Keywords-PMOS NMOS CMOS highspped**

## 1.INTRODUCTION

Schmitt triggers made of CMOS have a wide application in both analog and digital technology. They are widely used to shape the signals. They convert irregular shaped signals to triangular or square pulse. Schmitt trigger are found useful to remove noise from signals and mechanical contact bounce in switches.

Lately aggressive scaling of CMOS to nanometer have found application in various fields. Schmitt trigger works on the principle of comparator, when the input is greater or lower than a chosen threshold the output switches. Schmitt trigger designed using OP-Amp and feedback resistors have high power losses and greater area consumption over the chip. While the CMOS technology benefits over both the drawbacks of conventional method.

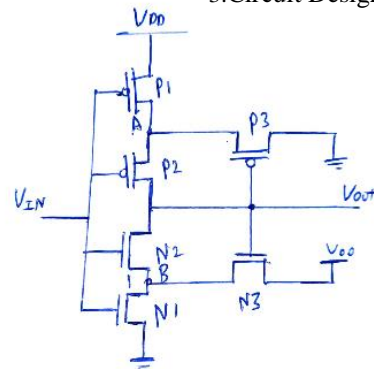
Schmitt trigger provides two switching thresholds one for positive-going and other for negative-going input signal, but the comparator gives only one switching threshold. This feature of Schmitt trigger is called hysteresis. Various Schmitt triggers are compared for noise margin and noise stable from the hysteresis curve.

## 2.Circuit Details

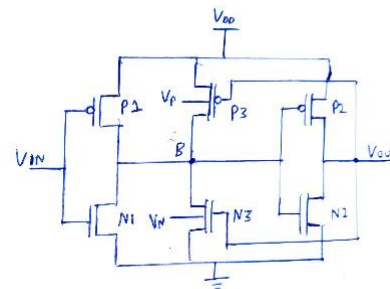
1. *Circuit 1* - Consider  $V_{out} = 0$  and  $V_{in} \leq V_{dd}$  at this state P3 is on and there is path to ground for Node A. When  $V_{in}$  changes from  $V_{dd}$  to 0 and  $V_{out}$  changes from 0 to  $V_{dd}$ , the output is compromised because current has a alternative path to ground through P3 till  $V_{out}$  raises such that P3 goes to off condition. So there is a slight variation in waveform from the ideal waveform when plotted for high frequency input voltage. Considering the other case When  $V_{out} = V_{dd}$  and  $V_{in} \geq V_{dd}$  at this stage N3 is on and there is path to  $V_{dd}$  for node B. . When  $V_{out}$  changes from  $V_{dd}$  to 0 and  $V_{in}$  changes from 0 to  $V_{dd}$ , the output is compromised because current has a alternative path to  $V_{dd}$  through N3 till  $V_{out}$  decreases such that N3 goes to off condition.

2. *Circuit 2* - Assuming  $V_{in}$  is low and  $V_{out}$  is low, So N1,N3 are in cutoff region and similarly P1,P3 are in saturation region. For  $V_{in}$  to change from low to high, N1 turns on slowly, the voltage at node B decrease, and  $V_{out}$  increase slowly. Since the voltage  $V_p$  can be changed, so this acts as threshold voltage for positive form of the output and similarly  $V_n$  acts as threshold voltage for negative part of the output. Circuit 2 dominates Circuit 1 for having 2 threshold voltages.

## 3.Circuit Design



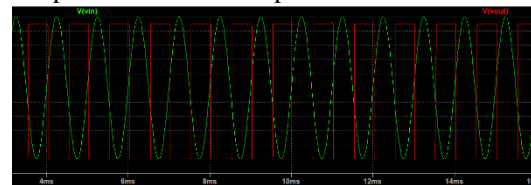
CIRCUIT 1



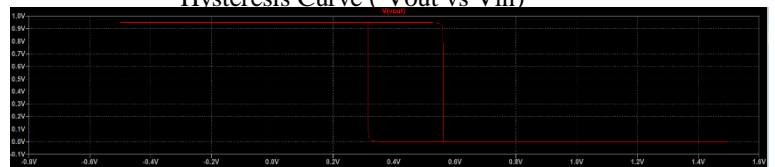
CIRCUIT 2

## 3.OUTPUT WAVEFORMS

Output waveform and input waveform vs time



Hysteresis Curve (  $V_{out}$  vs  $V_{in}$  )



Transistor Dimensions

Length = 28nm	Circuit 1	Circuit 2
	Width(nm)	Width(nm)
P1	560	560
P2	560	560
P3	728	280
N1	280	280
N2	280	280
N3	630	140

## 4.References

- <http://web.mit.edu/Magic/Public/papers/00260219.pdf>
- R. Sapawi, R. L. S. Chee, S. K. Sahari and N. Julai, "Performance of CMOS Schmitt Trigger," 2008 International Conference on Computer and Communication Engineering, 2008, pp. 1317-1320, doi: 10.1109/ICCCE.2008.4580818.
- W. Ibrahim, V. Beiu, M. Tache and F. Kharbash, "On Schmitt trigger and other inverters," 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), 2013, pp. 29-32, doi: 10.1109/ICECS.2013.6815337.
- <https://ieeexplore.ieee.org/document/87026>